NCV7424

Four Channel LIN Transceiver

NCV7424 is a four channel physical layer device using the Local Interconnect Network (LIN) protocol. It allows interfacing of four independent LIN physical buses and the LIN protocol controllers. The device is compliant to LIN 2.x Protocol Specification package and the SAE J2602 standard.

The NCV7424 LIN device is a member of the in-vehicle networking (IVN) transceiver family. The device is a monolithic solution incorporating 4 times the NCV7321-1 transceiver.

It is designed to work in a harsh automotive environment and is qualified following the TS16949 flow.

Features

- TSSOP16 Package. Pin-out Compatible with One Single LIN NCV7321 Transceiver (Pin Numbers 4 to 7, and 10 to 13)
- Compliant with LIN2.x, Backwards Compatible to Version 1.3 and J2602
- Transmission Rate 1 kbps to 20 kbps
- Indefinite Short-Circuit Protection on LIN towards Supply and Ground
- Bus Pins Protected Against Transients in an Automotive Environment
- Thermal Shutdown
- System ESD on LIN Pin Exceeding 10 kV, No Need for External ESD Protections
- Load Dump Protection (45 V)
- Integrated Slope Control Resulting into Excellent EME Performance also without any Capacitor on LIN Pin
- Excellent EMI Performance
- Remote Wake-up via LIN Bus on all Four Channels
- 3.3 V and 5 V Compatible Digital Inputs
- These are Pb-Free Devices

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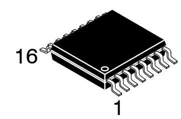
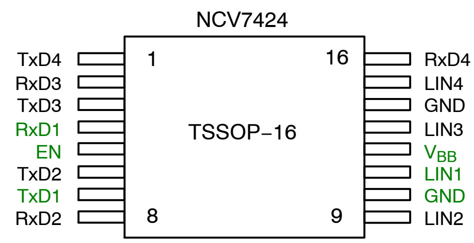
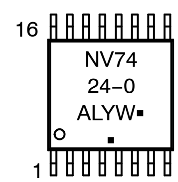


TSSOP−16
CASE 948F

PACKAGE PICTURE



MARKING DIAGRAM



NV7424−0	=	Specific Device Code
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 11 of this data sheet.

BLOCK DIAGRAM

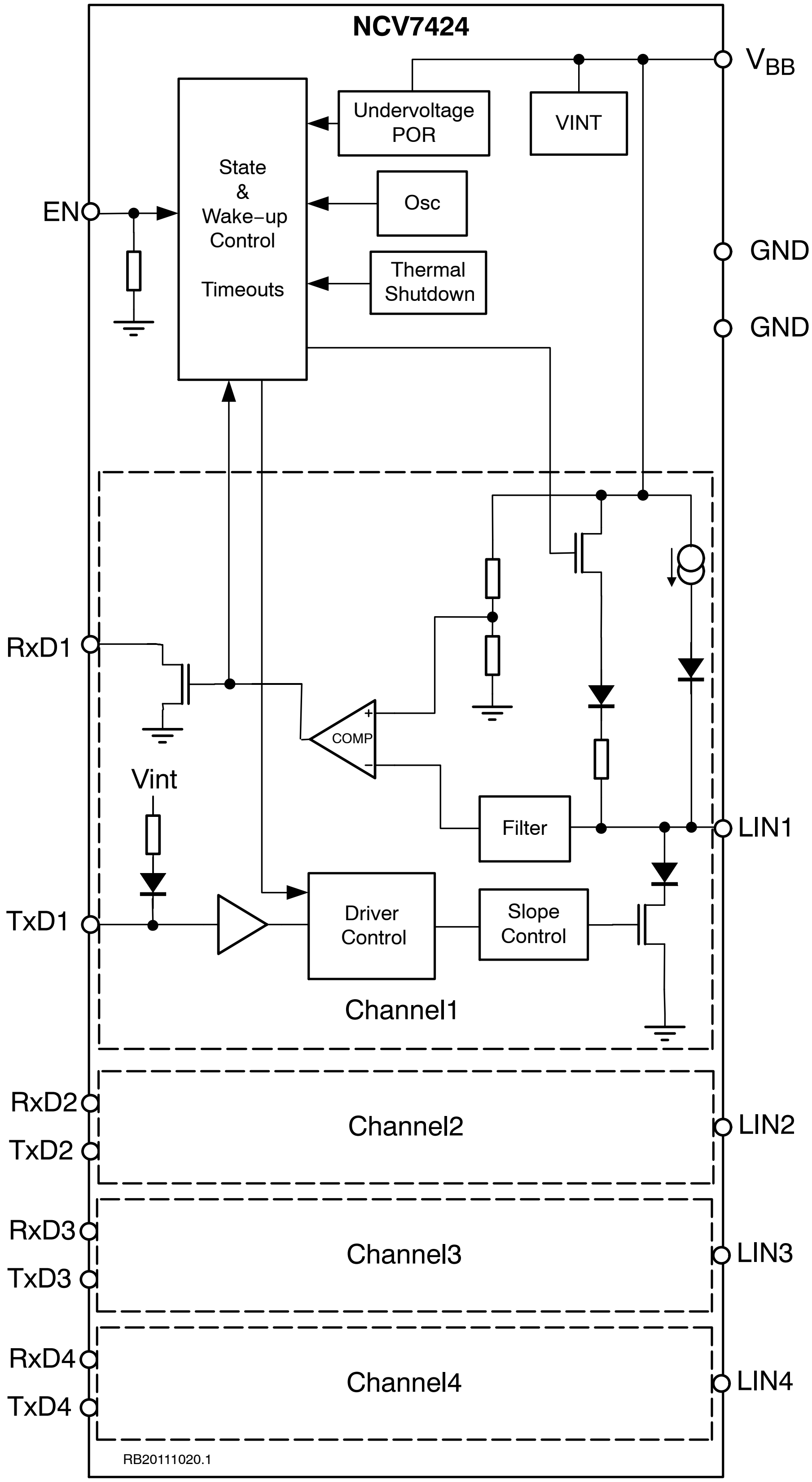


Figure 1. Block Diagram

Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Nominal Battery Operating Voltage (Note 1)	5	12	27	V
	Load Dump Protection			45	
I_{BB}_SLP	Supply Current in Sleep Mode, V_{BB} = 12 V, T_J < 85°C V_{LINx} = V_{BB}		10	30	μA
V_{LIN}	LIN Bus Voltage	−45		45	V
V_Dig_IO	Operating DC Voltage on Digital IO Pins (EN, RxD1-4, TxD1-4)	0		5.5	V
T_J	Junction Thermal Shutdown Temperature	150	165	185	°C
T_{amb}	Operating Ambient Temperature	−40		125	°C
V_{ESD}	Electrostatic Discharge Voltage (all pins) Human Body Model (Note 2) Conform to EIA−JESD22−A114−B	−4		4	kV
	Electrostatic Discharge Voltage (LIN) System Human Body Model (Note 3) Conform to EIC 61000−4−2	−10		10	kV

1. Below 5 V on V_{BB} in normal mode, the bus will either stay recessive or comply with the voltage level specifications and transition time specifications as required by SAE J2602. It is ensured by the battery monitoring circuit. Above 27 V on V_{BB}, LIN communication is operational (LIN pin toggling) but parameters cannot be guaranteed. For higher battery voltage operation above 27 V, LIN pull-up resistor must be selected large enough to avoid clamping of LIN pin by voltage drop over external pull-up resistor and LIN pin min current limitation.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test−house.

Table 2. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD4	Transmit Data Input, Low for Dominant State; Pull-up to internal supply guaranteed above pin input threshold
2	RxD3	Receive Data Output; Low in Dominant State
3	TxD3	Transmit Data Input, Low for Dominant State; Pull-up to internal supply guaranteed above pin input threshold
4	RxD1	Receive Data Output; Low in Dominant State
5	EN	Enable Input, Transceiver in Normal Operation Mode when High, Pull-down Resistor to GND
6	TxD2	Transmit Data Input, Low for Dominant State; Pull-up to internal supply guaranteed above pin input threshold
7	TxD1	Transmit Data Input, Low for Dominant State; Pull-up to internal supply guaranteed above pin input threshold
8	RxD2	Receive Data Output; Low in Dominant State
9	LIN2	LIN Bus Output/Input
10	GND	Ground
11	LIN1	LIN Bus Output/Input
12	V_{BB}	Battery Supply Input
13	LIN3	LIN Bus Output/Input
14	GND	Ground
15	LIN4	LIN Bus Output/Input
16	RxD4	Receive Data Output; Low in Dominant State

TYPICAL APPLICATION

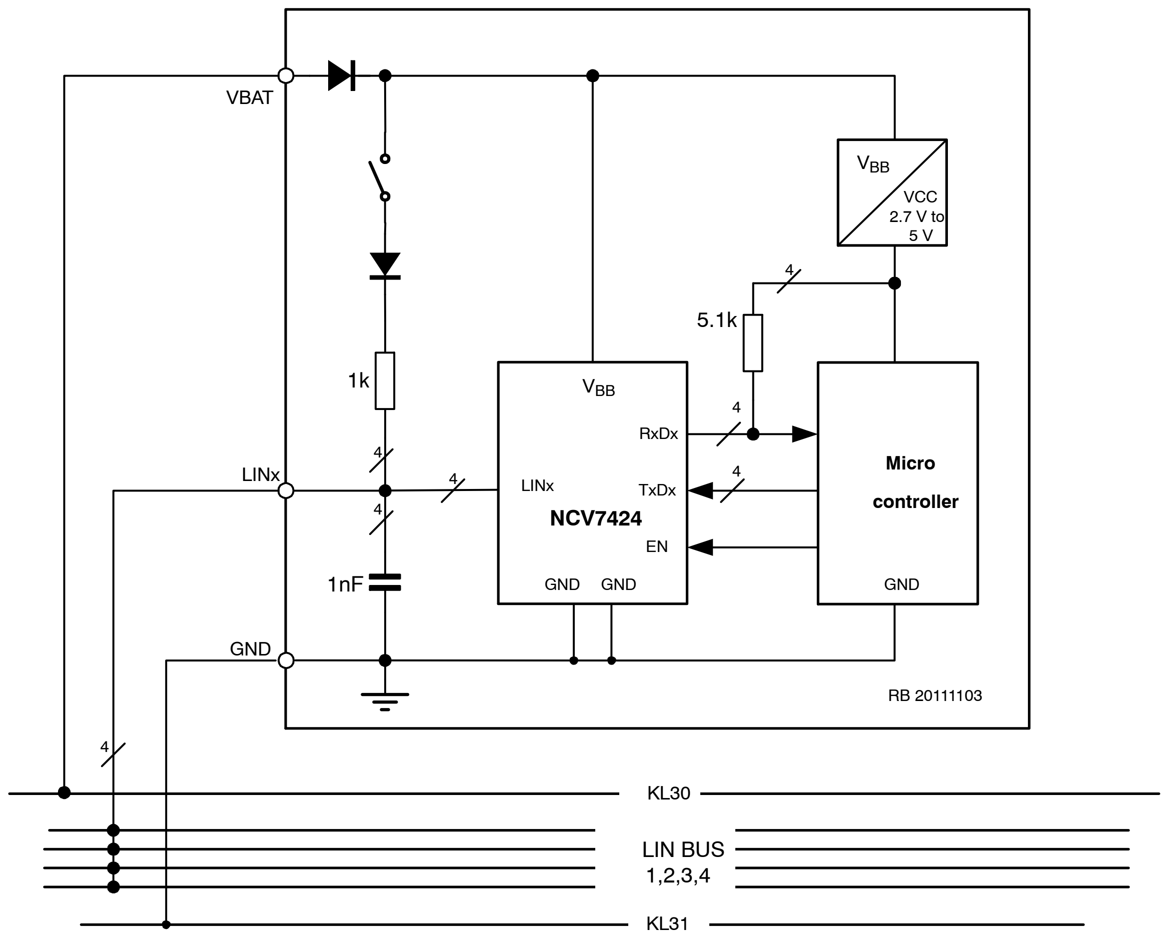


Figure 2. Application Diagram, Four LIN Master Nodes

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Voltage on Pin V_{BB}	−0.3		45	V
V_{LINx}	LINx Bus Voltage (LIN1-4)	−45		45	V
V_Dig_IO	DC Input Voltage on Pins (EN, RxD1-4, TxD1-4)	−0.3		6	V
T_J	Maximum Junction Temperature	−40		150	°C
V_{ESD}	HBM (All Pins) (Note 4) Conform to EIA−JESD22−A114−B	−4		4	kV
	CDM (All Pins) According to ESD STM 5.3.1−1999	−750		750	V
	HBM (LINx and V_{BB}) (Note 4)	−8		8	kV
	System HBM (LINx and V_{BB}) (Note 5) Conform to EIC 61000−4−2	−10		10	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
5. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test−house.

Table 4. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, JESD51-3 1S0P PCB	Free air	128	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, JESD51-7 2S2P PCB	Free air	72	K/W

FUNCTIONAL DESCRIPTION

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications. The domain is class-A multiplex buses with a single master node and a set of slave nodes.

The NCV7424 contains four independent LIN transmitters, LIN receivers plus common battery monitoring, power-on-reset (POR) circuits and thermal shutdown (TSD). The used LIN transmitter is optimized for the maximum specified transmission speed of 20 kbps with excellent EMC performance due to reduced slew rate of the LIN outputs.

The junction temperature is monitored via a thermal shutdown circuit that switches the LIN transmitters off when temperature exceeds the TSD trigger level.

The NCV7424 has four operating states (unpowered mode, standby mode, normal mode and sleep mode) that are determined by the supply voltage V_{BB}, input signals EN and activity on the LIN bus. The operating states and principal transitions between them are depicted in Figure 3.

OPERATING STATES

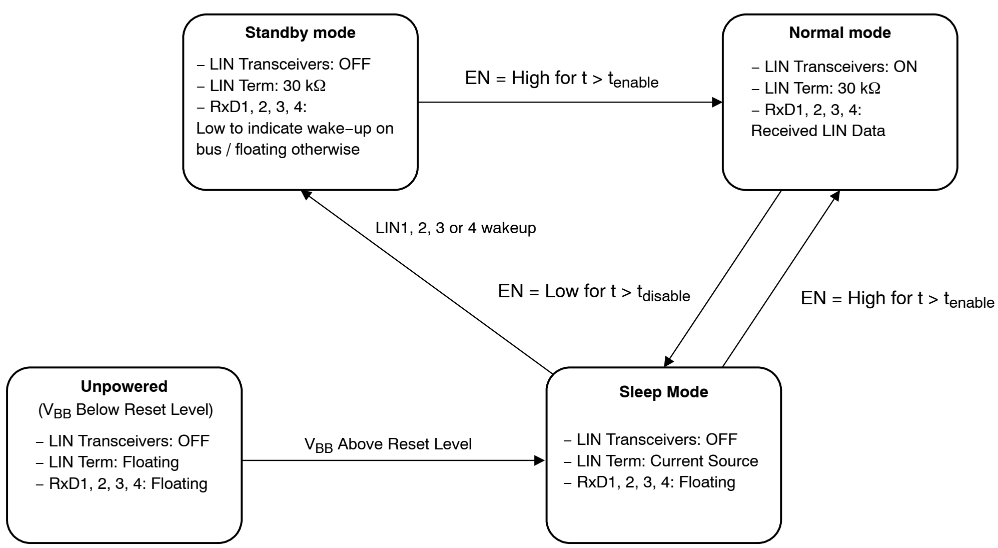


Figure 3. State Diagram

Unpowered Mode

As long as V_{BB} remains below its power-on-reset level, the chip is kept in a safe unpowered state. LIN transmitters are inactive, LINx pins are left floating. Pins RxDx remain floating.

The unpowered state will be entered from any other state when V_{BB} falls below its power-on-reset level.

Standby Mode

Standby mode is a low-power mode, where the LIN transceivers remain inactive. A 30 kΩ resistor in series with a reverse-protection diode is internally connected between individual LIN pins and pin V_{BB}. Standby mode is entered after a wake-up event is recognized while the chip was in the sleep mode, the RxD1,2,3 or 4 pin is pulled low depending on which of the respective pins LIN1,2,3 or 4 the valid LIN wake-up occurred. While staying in standby mode, wake-up signaling by RxDx pins on each LIN channel is fully functional. This is also in case if wake event(s) started in sleep mode but actual transition from sleep to standby was caused by preceding wake-up event on other LIN channel.

Normal Mode

In normal mode, the full functionality of the LIN transceivers is available. Data are sent to the LINx bus according to the state of TxDx inputs and RxDx pins reflect the logical symbol received on the LINx bus – high-impedant for recessive and Low level for dominant.

A 30 kΩ resistor in series with a reverse-protection diode is internally connected between LIN and V_{BB} pins.

To avoid that, due to a failure of the application (e.g. software error, a short to ground,…), the LIN bus is permanently driven dominant and thus blocking all subsequent communication, the signal on each TxDx pin passes through an independent timer per LIN channel, which releases the bus in case TxDx remains

Low for longer than $t_{TxD\_timeout}$. The transmission can continue once the TxDx returns to High logical level. This is independent on each channel, means permanent dominant on one channel is not blocking the other channels from communication.

In case the junction temperature increases above the thermal shutdown threshold, e.g. due to a short of the LIN wiring to the battery and high ambient temperature, all four transmitters are disabled and LIN buses are kept in recessive state independently of TxDx inputs. RxDx pins are kept Low during thermal shutdown.

Once the junction temperature decreases below the thermal shutdown release level, the transmission is enabled again. RxD pins are released from asserted thermal shutdown low level immediately when chip is below thermal shutdown threshold.

As required by SAE J2602, the transceiver behaves safely below its operating range – it either continues to transmit correctly (according to its specification) or remains silent (transmits a recessive state regardless of the TxDx signal). A battery monitoring circuit in NCV7424 deactivates the transmitter in normal mode if the V_{BB} level drops below MONL_VBB. Transmission is enabled again when V_{BB} reaches MONH_VBB. The internal logic remains in normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power-on-reset levels are overlapping, it is ensured by the implementation that the monitoring level never falls below the power-on-reset level.

Normal mode can be entered from either standby or sleep mode when EN Pin is High for longer than t_{enable}. When the transition is made from standby mode, RxDx is put high-impedant immediately after EN becomes High (before the expiration of t_{enable} filtering time). Transmission on each LINx channel is only possible for particular TxDx pin starting from High to Low level (if TxDx pin is Low when entering Normal mode, transmission is not enabled).

Sleep Mode

Sleep mode provides extremely low current consumption. The LIN transceiver is inactive and the battery consumption is minimized. Only a weak pull-up current source is internally connected between LIN and V_{BB} pins, in order to minimize current consumption even in case of LIN short to GND.

Sleep mode can be entered:

- After the voltage level at V_{BB} pin rises above its power-on-reset level. RxDx pins are set high-impedant after start-up
- From normal mode by assigning a Low logical level to pin EN for longer than $t_{disable}$. The sleep mode can be entered even if a permanent short occurs on the LINx Pin.

If a wake-up event occurs during the transition between normal and sleep mode (during the $t_{disable}$ filtering time), it will be regarded as a valid wake-up and the chip will enter standby mode with the appropriate setting of pins RxDx.

LIN Wake−up

Remote (or LIN) wake-up can be recognized on all LINx pins on NCV7424 when LINx bus is externally driven dominant for longer than t_{LIN_wake} and a rising edge on LIN occurs afterwards – see Figure 4. Wake-up events can be exclusively detected in sleep mode or during the transition from normal mode to sleep mode. Due to timing tolerances, valid wake-up events beginning shortly before normal-to-sleep mode transition can be also sometimes regarded as valid wake−ups.

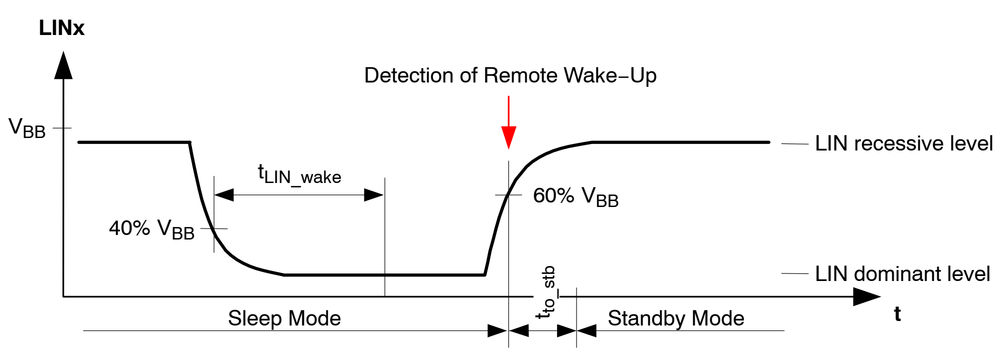


Figure 4. LIN Bus Wake−up Detection

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pins 10, 14. These pins are electrically connected inside of the package). Positive currents flow into the IC.

Table 5. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CURRENT CONSUMPTION						
I_{BB}_ON_rec	V_{BB} Consumption	Normal Mode; LIN Recessive V_{LINx} = V_{BB}		2.3	4.7	mA
I_{BB}_ON_dom	V_{BB} Consumption	Normal Mode; LIN Dominant TxDx = Low		16.5	28	mA
I_{BB}_STB	V_{BB} Consumption	Standby Mode V_{LINx} = V_{BB}		0.22	0.45	mA
I_{BB}_SLP	V_{BB} Consumption	Sleep Mode V_{LINx} = V_{BB}		11	35	μA
I_{BB}_SLP_18V	V_{BB} Consumption	Sleep Mode, V_{BB} < 18 V V_{LINx} = V_{BB}		10	33	μA
I_{BB}_SLP_12V	V_{BB} Consumption	Sleep Mode, V_{BB} = 12 V, T_J < 85°C V_{LINx} = V_{BB}		9	30	μA
POR AND V_{BB} MONITOR						
PORH_V_{BB}	Power−on Reset High Level on V_{BB}	V_{BB} Rising	2	3.3	4.5	V
PORL_V_{BB}	Power−on Reset Low Level on V_{BB}	V_{BB} Falling	1.7	2.9	4	V
MONH_V_{BB}	Battery Monitoring High Level	V_{BB} Rising		4.1	4.5	V
MONL_V_{BB}	Battery Monitoring Low Level	V_{BB} Falling	3	4		V
LIN TRANSMITTERs						
VLINx_dom_LoSup	LINx Dominant Output Voltage	TxDx = Low; V_{BB} = 7.3 V		1	1.2	V
VLINx_dom_HiSup	LINx Dominant Output Voltage	TxDx = Low; V_{BB} = 18 V		1.4	2.0	V
VLINx_REC	LIN Recessive Output Voltage	TxDx = High; I_{LIN} = 10 μA (Note 6)	V_{BB} − 1.5		V_{BB}	V
ILINx_lim	Short Circuit Current Limitation	V_{LINx} = V_{BB} = 18 V; TxDx = Low	70	140	200	mA
$RLINx_{slave}$	Internal Pull−up Resistance		20	33	47	kΩ
LIN RECEIVERs						
VLINx_bus_dom	Bus Voltage for Dominant State				0.4	V_{BB}
VLINx_bus_rec	Bus Voltage for Recessive State		0.6			V_{BB}
VLINx_rec_dom	Receiver Threshold	LIN Bus Recessive − Dominant	0.4	0.45	0.6	V_{BB}
VLINx_rec_rec	Receiver Threshold	LIN Bus Dominant − Recessive	0.4	0.55	0.6	V_{BB}

6. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 5. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN RECEIVERs						
VLINx_rec_cnt	Receiver Centre Voltage	(VLINx_rec_dom + VLINx_rec_rec) / 2	0.475	0.5	0.525	V_{BB}
VLINx_rec_hys	Receiver Hysteresis	(VLINx_rec_rec − VLINx_rec_dom)	0.05	0.1	0.175	V_{BB}
ILINx_off_dom	LIN Output Current, Bus externally driven to dominant state	Normal Mode, Driver Off; V_{BB} = 12 V; TxDx = High; V_{LINx} = 0 V	−1	−0.37	−0.2	mA
ILINx_off_dom_slp	LIN Output Current, Bus externally driven to dominant state	Sleep Mode, Driver Off; V_{BB} = 12 V; TxDx = High; V_{LINx} = 0 V	−20	−8	−2	μA
ILINx_off_rec	LIN Output Current, Bus in Recessive State	Driver Off; V_{BB} < 18 V; V_{BB} < V_{LINx} < 18 V			2	μA
ILINx_no_GND	Communication not Affected	V_{BB} = GND = 12 V; 0 < V_{LINx} < 18 V	−1		1	mA
ILINx_no_V_{BB}	LIN Bus Remains Operational	V_{BB} = GND = 0 V; 0 < V_{LINx} < 18 V		0	5	μA
C_{LINx}	Capacitance on LINx pin	Not tested in production, guaranteed by design		20	30	pF
PIN EN						
Vil_EN	Low Level Input Voltage		−0.3		0.8	V
Vih_EN	High Level Input Voltage		2.0		5.5	V
Rpd_EN	Pull−down Resistance to Ground		150	350	650	kΩ
PIN RxDx						
Iol_RxDx	Low Level Output Current	V_{RxD} = 0.4 V, Normal Mode, V_{LINx} = 0 V	1.5	4.3		mA
Ioh_RxDx	High Level Output Current	V_{RxD} = 5 V, Normal Mode, V_{LINx} = V_{BB}	−5	0	5	μA
PIN TxDx						
Vil_TxDx	Low Level Input Voltage		−0.3		0.8	V
Vih_TxDx	High Level Input Voltage		2.0		5.5	V
Rpd_TxDx	Pull−up on TxDx Pins		60	100	150	kΩ
THERMAL SHUTDOWN						
T_{JSD}	Thermal Shutdown Junction Temperature	Temperature Rising	150	165	185	°C
T_{JSD_HYST}	Thermal Shutdown Hysteresis			5		°C

6. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 6. AC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	$TH_{REC(max)}$ = 0.744 x V_{BB} $TH_{DOM(max)}$ = 0.581 x V_{BB} t_{BIT} = 50 μs V(V_{BB}) = 7 V to 18 V	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	$TH_{REC(min)}$ = 0.422 x V_{BB} $TH_{DOM(min)}$ = 0.284 x V_{BB} t_{BIT} = 50 μs V(V_{BB}) = 7.6 V to 18 V	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	$TH_{REC(max)}$ = 0.778 x V_{BB} $TH_{DOM(max)}$ = 0.616 x V_{BB} t_{BIT} = 96 μs V(V_{BB}) = 7 V to 18 V	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	$TH_{REC(min)}$ = 0.389 x V_{BB} $TH_{DOM(min)}$ = 0.251 x V_{BB} t_{BIT} = 96 μs V(V_{BB}) = 7.6 V to 18 V	0.5		0.590	
D1e	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	$TH_{REC(max)}$ = 0.744 x V_{BB} $TH_{DOM(max)}$ = 0.581 x V_{BB} t_{BIT} = 50 μs V(V_{BB}) = 5 V to 40 V, (Notes 7 and 8)	0.39		0.5	
D2e	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	$TH_{REC(min)}$ = 0.422 x V_{BB} $TH_{DOM(min)}$ = 0.284 x V_{BB} t_{BIT} = 50 μs V(V_{BB}) = 5 V to 40 V, (Notes 7 and 8)	0.5		0.59	
D3e	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	$TH_{REC(max)}$ = 0.778 x V_{BB} $TH_{DOM(max)}$ = 0.616 x V_{BB} t_{BIT} = 96 μs V(V_{BB}) = 5 V to 40 V, (Notes 7 and 8)	0.41		0.5	
D4e	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	$TH_{REC(min)}$ = 0.389 x V_{BB} $TH_{DOM(min)}$ = 0.251 x V_{BB} t_{BIT} = 96 μs V(V_{BB}) = 5 V to 40 V, (Notes 7 and 8)	0.5		0.6	
$t_{tx\_prop\_down\_x}$	Propagation Delay of TxDx to LINx. TxD High to Low		1.3	4.2	10	μs
$t_{tx\_prop\_up\_x}$	Propagation Delay of TxDx to LINx. TxD Low to High		1.3	4.6	10	μs
$t_{tx\_sym\_x}$	Propagation Delay Symmetry	$t_{trx\_prop\_down\_x} - t_{trx\_prop\_up\_x}$	−2.5	−0.4	2.5	μs
t_{fall}	LINx Falling Edge	Normal Mode; V_{BB} = 12 V		9	22.5	μs
t_{rise}	LINx Rising Edge	Normal Mode; V_{BB} = 12 V		10	22.5	μs
t_{sym}	LINx Slope Symmetry	Normal Mode; V_{BB} = 12 V	−4	0	4	μs
LIN RECEIVERs						
$t_{rec\_prop\_down\_x}$	Propagation Delay of LINx to RxDx Receiver Falling Edge		0.1	1.6	6	μs
$t_{rec\_prop\_up\_x}$	Propagation Delay of LINx to RxDx Receiver Rising Edge		0.1	1.35	6	μs
$t_{rec\_sym\_x}$	Propagation Delay Symmetry	$t_{rec\_prop\_down\_x} - t_{rec\_prop\_up\_x}$	−2	0.25	2	μs

7. The external pull-up resistor for duty cycles on V(V_{BB}) = 40 V is 1 kΩ
8. Not tested in production Extended battery range (5 V; 40 V) is tested on limited sample base only

Table 6. AC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MODE TRANSITIONS AND TIMEOUTS						
t_{LINx_wake}	Duration of LINx Dominant for Detection of Wake−up via LINx bus	Sleep Mode	30	90	150	μs
t_{to_stb}	Delay from LIN Bus Dominant to Recessive Edge to Entering of Standby Mode after Valid LIN Wake−up	See Figure 4	2	2.8	18.5	μs
t_{enable}	Duration of High Level on EN Pin for Transition to Normal Mode		2	18	47	μs
$t_{disable}$	Duration of Low Level on EN Pin for Transition to Sleep Mode		2	7.5	18.5	μs
$t_{TxD\_timeout}$	TxD Dominant Timeout	Normal Mode, TxD = Low, Guarantees Baudrate as Low as 1 kbps	15	28	50	ms

7. The external pull-up resistor for duty cycles on V(V_{BB}) = 40 V is 1 kΩ
8. Not tested in production Extended battery range (5 V; 40 V) is tested on limited sample base only

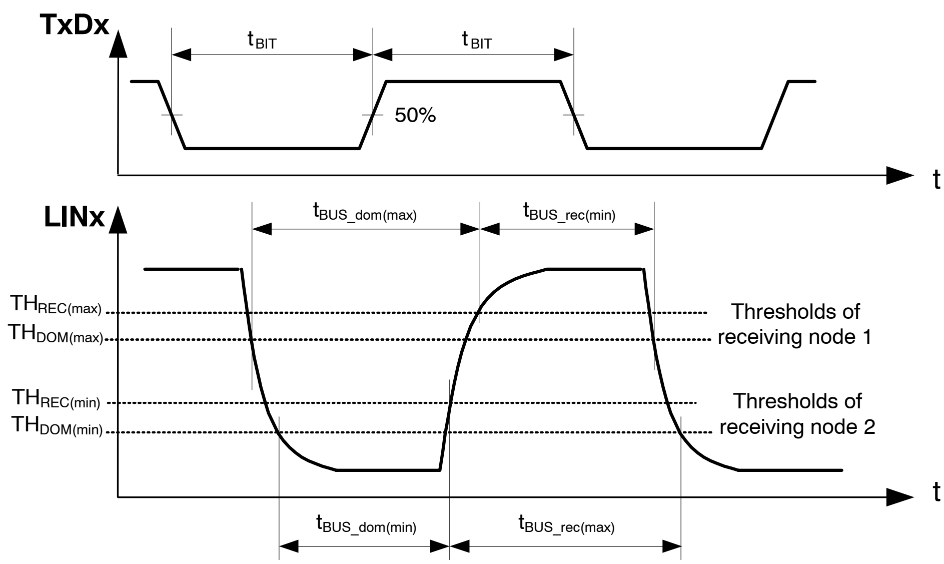


Figure 5. LINx Bus Transmitter Duty Cycle

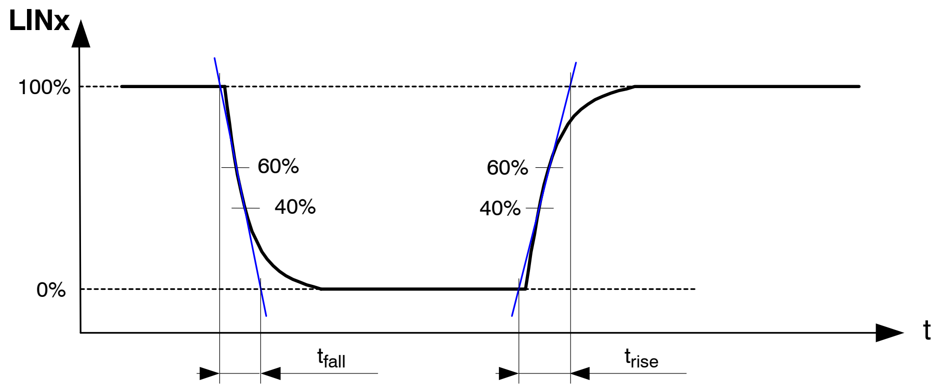


Figure 6. LINx Bus Transmitter Rising and Falling Times

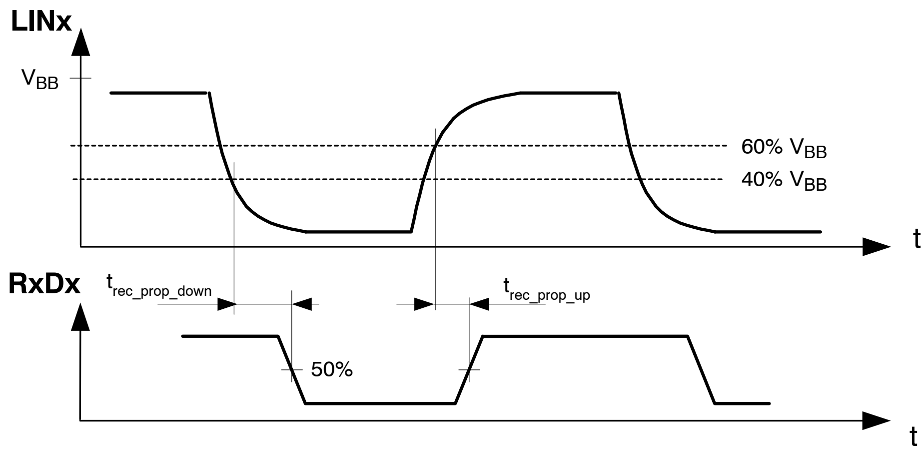


Figure 7. LINx Bus Receiver Timing

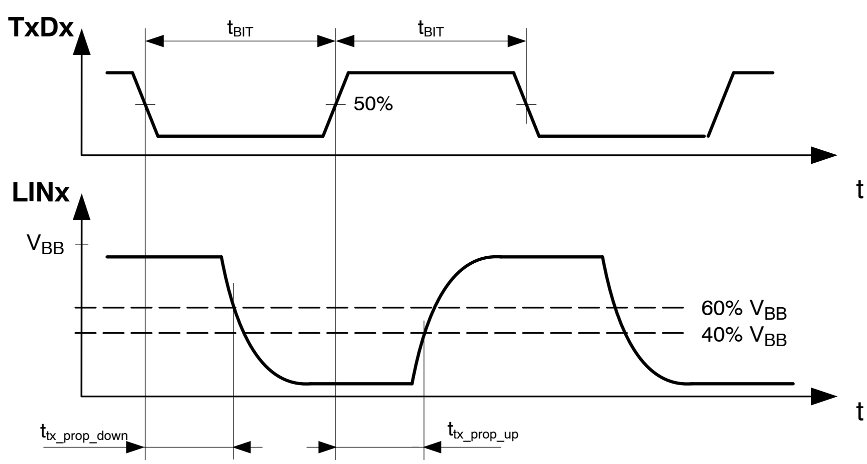


Figure 8. LINx Transmitter Timing

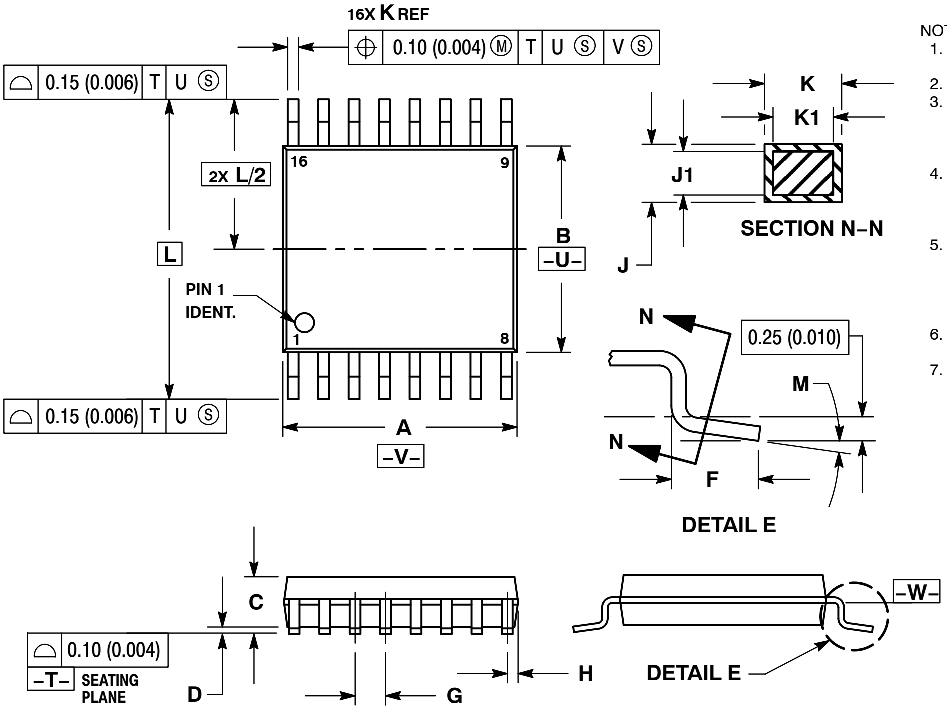
ORDERING INFORMATION

Part Number	Description	Temperature Range	Package	Shipping†
NCV7424DB0R2G	Quad LIN Transceiver	−40°C to +125°C	TSSOP16 GREEN (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

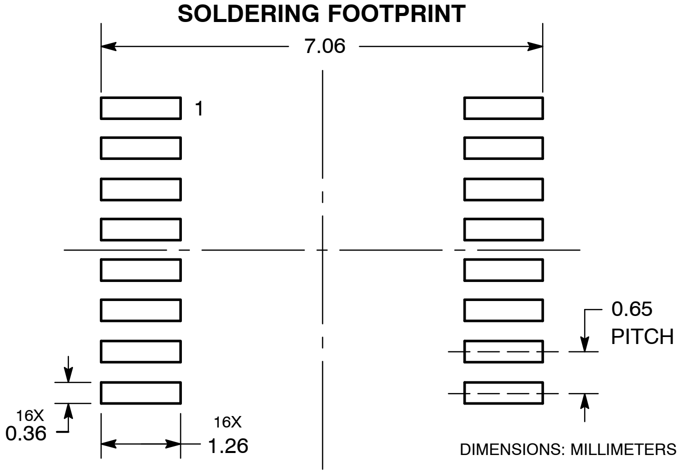
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



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