Panasonic

AN32181B

http://www.semicon.panasonic.co.jp/en/

12 x 12 Dots Matrix LED Driver IC

FEATURES

- 12 × 12 LED Matrix Driver
  (Total LED that can be driven = 144)
- LED Selectable Maximum Current
- LED Melody Mode Function
- LED Open/Short Detection
- LED Ghost Image Prevention Function
- SPI Interface
- I²C interface
  (Standard Mode, Fast Mode and Fast Mode Plus)
  (4 Slave address selectable)
- 28 pin Plastic Quad Flat Non-leaded Package
  (QFN Type)

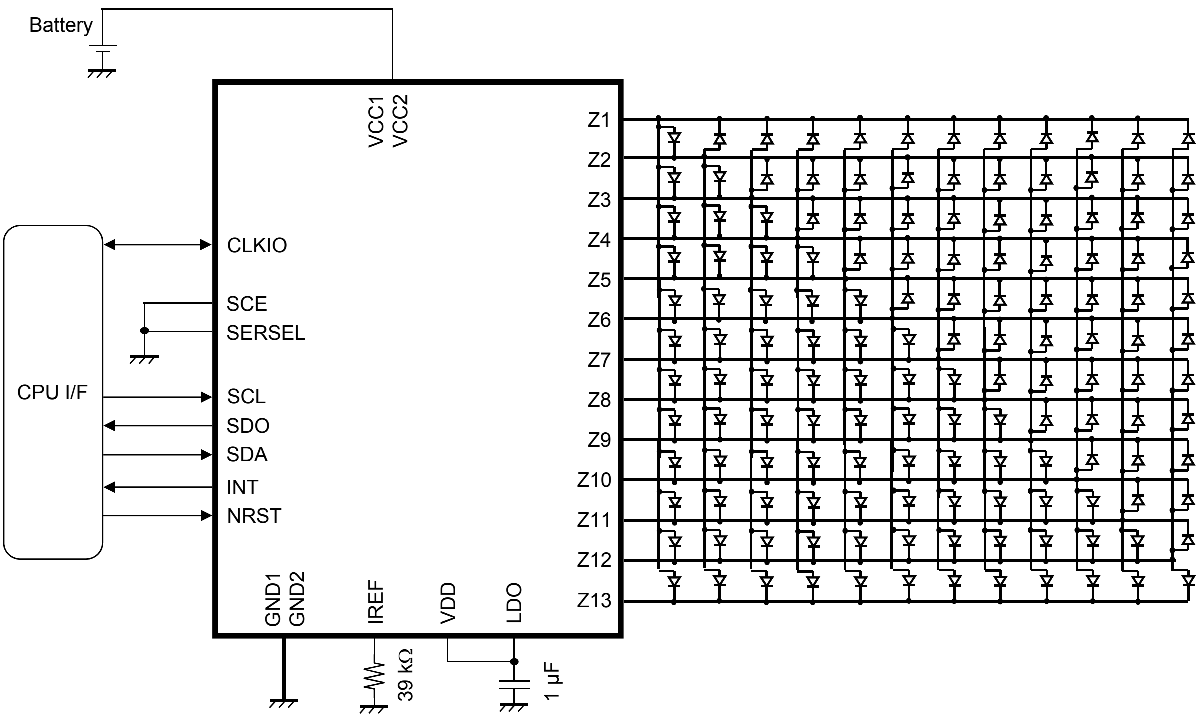
DESCRIPTION

AN32181B is a 144 Dots Matrix LED Driver.
It can drive up to 48 RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
AN32181B-VB	Matrix LED Driver	28 pin QFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VCC_{MAX}	6.0	V	*1
	VDD_{MAX}	6.0	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	V_{SERSEL}, V_{SCL}, V_{SDA}, V_{SCE}, V_{CLKIO}, V_{NRST}	– 0.3 to 6.0	V	—
Output Voltage Range	V_{INT}, V_{CLKIO}, V_{SDO}, V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}, V_{Z8}, V_{Z9}, V_{Z10}, V_{Z11}, V_{Z12}, V_{Z13}	– 0.3 to 6.0	V	—
	V_{LDO}	– 0.3 to 4.0	V	—
ESD	HBM	2.0	kV	—

Note: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

VCC_{MAX} is voltage for VCC1 and VCC2. VCC1 = VCC2.

VDD_{MAX} is voltage for VDD.

Do not apply external currents or voltages to any pin not specifically mentioned.

*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for operating ambient temperature, operating junction temperature and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

Package	θ_{j-a}	P_D (Ta = 25 °C)	P_D (Ta = 85 °C)
28 pin Plastic Quad Flat Non-leaded package (QFN Type)	175.5 °C / W	0.569 W	0.228 W

Note: For the actual usage, please refer to the P_D-Ta characteristics diagram in the Package Standards, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage range	V_{CC}	3.1	3.6	5.5	V	*1
	V_{DD}	1.70	1.85	5.50	V	*1
Input Voltage Range	V_{SCL}, V_{SDA}, V_{SCE}, V_{CLKIO}	– 0.3	—	V_{DD} + 0.3	V	*2
	V_{SERSEL}, V_{NRST}	– 0.3	—	V_{CC} + 0.3	V	*2
Output Voltage Range	V_{INT}, V_{CLKIO}, V_{SDO}	– 0.3	—	V_{DD} + 0.3	V	*2
	V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}, V_{Z8}, V_{Z9}, V_{Z10}, V_{Z11}, V_{Z12}, V_{Z13}	– 0.3	—	V_{CC} + 0.3	V	*2
	V_{LDO}	– 0.3	—	3.5	V	—

Note: *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND1 and GND2.
GND1 = GND2.
V_{CC} is voltage for VCC1 and VCC2. VCC1 = VCC2.
V_{DD} is voltage for VDD.
Do not apply external currents or voltages to any pin not specifically mentioned.
*2: (V_{CC} + 0.3) V must not exceed 6.0 V. (V_{DD} + 0.3) V must not exceed 6.0 V.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits Min	Limits Typ	Limits Max	Unit	Note
Circuit Current							
Circuit Current (1) OFF Mode	I_{CC1}	V_{NRST} = 0 V	—	0	1	μA	—
Circuit Current (2) OFF Mode	I_{CC2}	V_{NRST} = High	—	240	500	μA	—
Internal Oscillator							
Oscillation Frequency	F_{DC1}	—	1.92	2.40	2.88	MHz	—
SCAN Switch							
Switch On Resistance	R_{SCAN}	$I_{Z1\ to\ Z12}$ = – 20 mA	—	1.0	2.5	Ω	—
Constant Voltage Source (LDO)							
Output voltage (1)	V_{L1}	I_{LDO} = – 10 μA	2.75	2.85	2.95	V	—
Output voltage (2)	V_{L2}	I_{LDO} = – 15 mA	2.75	2.85	2.95	V	—
CLKIO							
High Level Input Voltage Range	V_{IH1}	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Input Voltage Range	V_{IL1}	Low Level Acknowledged Voltage (At External CLK Input Mode)	– 0.3	—	0.3 × V_{DD}	V	—
High Level Output Voltage	V_{OH1}	I_{CLKIO} = – 1 mA (At Internal CLK Output Mode)	0.8 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Output Voltage	V_{OL1}	I_{CLKIO} = 1 mA (At Internal CLK Output Mode)	– 0.3	—	0.2 × V_{DD}	V	—
High Level input Current	I_{IH1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{CLKIO} = 5.5 V	– 1	0	1	μA	—
Low Level input Current	I_{IL1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{CLKIO} = 0 V	– 1	0	1	μA	—

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits Min	Limits Typ	Limits Max	Unit	Note
Constant Current Source (Matrix LED)							
Output Current (1)	I_{MX1}	LED Current Setting = 19.85 mA IMAX = [01010] $V_{Z1\ to\ Z13}$ = 1 V	18.85	19.85	20.85	mA	*1
IMAX Current Step	I_{MXSTEP}	Constant Current Mode LED current setting = 22 mA, IMAX = [01011] $V_{Z1\ to\ Z13}$ = 1 V, ILED1 = $I_{Z1\ to\ Z13}$ LED current setting = 19.85 mA, IMAX = [01010] $V_{Z1\ to\ Z13}$ = 1 V, ILED2 = $I_{Z1\ to\ Z13}$ IMXSTEP = ILED1 – ILED2	0.0	2.0	3.5	mA	—
OFF Mode Leak Current (1)	I_{MXOFF1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V OFF Mode $V_{Z1\ to\ Z13}$ = 5.5 V	– 1	—	1	μA	—
OFF Mode Leak Current (2)	I_{MXOFF2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V OFF Mode $V_{Z1\ to\ Z13}$ = 0 V	– 1	—	1	μA	—
Channel Difference	I_{MXCH}	LED Current Setting = 19.85 mA IMAX = [01010] Difference of Z1 to 13 current from the average current value	– 5	—	5	%	—
Voltage at which LED driver can keep constant current value							
LED Driver Voltage	V_{LD}	LED Current Setting = 19.85 mA IMAX = [01010] Voltage at which LED Current change within ± 5 % compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note: * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits Min	Limits Typ	Limits Max	Unit	Note
SERSEL							
High Level Input Voltage Range	V_{IH2}	High Level Acknowledged Voltage	0.7 × V_{CC}	—	V_{CC} + 0.3	V	—
Low Level Input Voltage Range	V_{IL2}	Low Level Acknowledged Voltage	– 0.3	—	0.3 × V_{CC}	V	—
High Level Input Current	I_{IH2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SERSEL} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SERSEL} = 0 V	– 1	0	1	µA	—
NRST							
High Level Input Voltage Range	V_{IH3}	High Level Acknowledged Voltage	1.5	—	V_{CC} + 0.3	V	—
Low Level Input Voltage Range	V_{IL3}	Low Level Acknowledged Voltage	– 0.3	—	0.6	V	—
High Level Input Current	I_{IH3}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{NRST} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL3}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{NRST} = 0 V	– 1	0	1	µA	—
INT							
ON Resistance	R_{INTON}	I_{INT} = 5 mA	—	10	50	Ω	—
SDO							
High Level Output Voltage	V_{OH3}	I_{SDO} = – 3 mA	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Output Voltage	V_{OL3}	I_{SDO} = 3 mA	0	—	0.3 × VDD	V	—
SCE							
High-level input voltage range	V_{IH4}	High Level Acknowledged Voltage	V_{DD} × 0.7	—	V_{DD} + 0.5	V	—
Low-level input voltage range	V_{IL4}	Low Level Acknowledged Voltage	– 0.5	—	V_{DD} × 0.3	V	—
High-level input current	I_{IH4}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SCE} = 5.5 V	– 1	0	1	µA	—
Low-level input current	I_{IL4}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SCE} = 0 V	– 1	0	1	µA	—

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits Min	Limits Typ	Limits Max	Unit	Note
I²C bus (Internal I/O stage characteristics) (SCL, SDA)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	– 0.5	—	0.3 × V_{DD}	V	*2
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × V_{DD}	—	V_{DDmax} + 0.5	V	*2 *3
Low-level output voltage 1	V_{OL1}	V_{DD} > 2 V I_{SDA}, I_{SCL} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	V_{DD} < 2 V I_{SDA}, I_{SCL} = 3 mA	0	—	0.2 × V_{DD}	V	—
Low-level output current	I_{OL}	V_{SDA} = 0.4 V	20	—	—	mA	—
Input current each I/O pin	I_i	V_{CC} = 5.5 V , V_{DD} = 5.5 V V_{SDA}, V_{SCL} = 0.1 × V_{DDmax} to 0.9 × V_{DDmax}	– 10	0	10	μA	*3
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz	—

Note: *2 : The input threshold voltage of I²C bus (Vth) is linked to V_{DD} (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not V_{DD}, the threshold voltage (Vth) is fixed to ((V_{DD} / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILmax}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (V_{DD}).

*3 : V_{DDmax} refers to the maximum operating supply voltage of V_{DD}.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which Constant current circuit, and Matrix SW turn off.	—	150	—	°C	*4 *5
Constant Voltage Source (LDO)							
Ripple rejection ratio (1)	PSL11	V_{CC} = 3.6 V + 0.3 V[p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20 log(acV$_{LDO}$ / 0.3)	—	– 50	—	dB	*5
Ripple rejection ratio (2)	PSL12	V_{CC} = 3.6 V + 0.3 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20 log(acV$_{LDO}$ / 0.3)	—	– 40	—	dB	*5
Short-circuit protection current	I_{PT1}	V_{LDO} = 0 V	—	40	—	mA	*5
I²C bus (Internal I/O stage characteristics)							
Hysteresis of Schmitt trigger input (1)	V_{hys1}	V_{DD} > 2 V, Hysteresis of SDA, SCL	0.05 × V_{DD}	—	—	V	*6 *7
Hysteresis of Schmitt trigger input (2)	V_{hys2}	V_{DD} < 2 V, Hysteresis of SDA, SCL	0.1 × V_{DD}	—	—	V	*6 *7
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	Bus capacitance: 10 pF to 550 pF $I_P \leq$ 20 mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*6 *7
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	—	0	—	50	ns	*6 *7
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*6 *7

Note: *4 : Constant current circuit, and Matrix SW turn off and IS reset when TSD operates.
*5 : Typical Design Value
*6 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 11. All values referred to V_{IHmin} and V_{ILmax} level.
*7 : These are values checked by design but not production tested.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

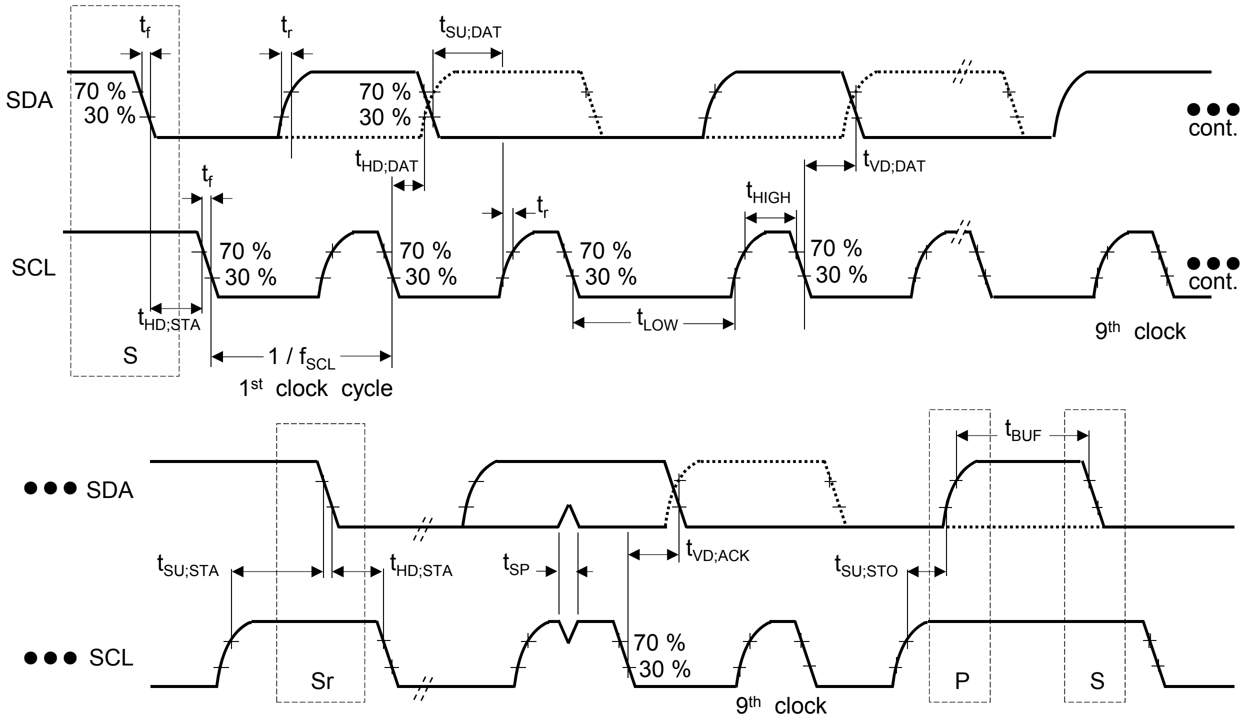
Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	μs	*6 *7
Low period of the SCL clock	t_{LOW}	—	0.5	—	—	μs	*6 *7
High period of the SCL clock	t_{HIGH}	—	0.26	—	—	μs	*6 *7
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.26	—	—	μs	*6 *7
Data hold time	$t_{HD:DAT}$	—	0	—	—	μs	*6 *7
Data set-up time	$t_{SU:DAT}$	—	50	—	—	ns	*6 *7
Rise time of both SDA and SCL signals	t_r	—	—	—	120	ns	*6 *7
Fall time of both SDA and SCL signals	t_f	—	—	—	120	ns	*6 *7
Set-up time of STOP condition	$t_{SU:STO}$	—	0.26	—	—	μs	*6 *7
Bus free time between STOP and START condition	t_{BUF}	—	0.5	—	—	μs	*6 *7
Capacitive load for each bus line	C_b	—	—	—	550	pF	*6 *7
Data valid time	$t_{VD:DAT}$	—	—	—	0.45	μs	*6 *7
Data valid acknowledge	$t_{VD:ACK}$	—	—	—	0.45	μs	*6 *7
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × V_{DD}	—	—	V	*6 *7
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × V_{DD}	—	—	V	*6 *7

Note: *6 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 11. All values referred to V_{IHmin} and V_{ILmax} level.
*7 : These are values checked by design but not production tested.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned



V_{VILMAX} = 0.3 × V_{DD}

V_{VIHMIN} = 0.7 × V_{DD}

S : START condition

Sr : Repeat START condition

P : STOP condition

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ELECTRICAL CHARACTERISTICS (continued)

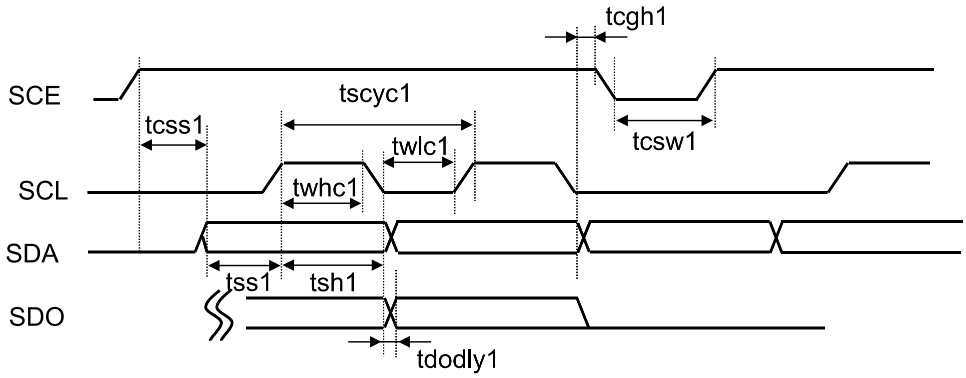
V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI interface characteristics (V_{DD} = 1.85 V ± 3 %) Reception timing							
SCL cycle period	tscyc1	—	—	200	—	ns	*5
SCL cycle period High period	twhc1	—	—	100	—	ns	*5
SCL cycle period Low period	twlc1	—	—	100	—	ns	*5
Serial data setup time	tss1	—	—	142	—	ns	*5
Serial data hold time	tsh1	—	—	142	—	ns	*5
Transceiving interval	tcsw1	—	—	100	—	ns	*5
Chip enable setup time	tcss1	—	—	5	—	ns	*5
Chip enable hold time	tcgh1	—	—	5	—	ns	*5
SPI interface characteristics (V_{DD} = 1.85 V ± 3 %) Transmission timing							
SCL cycle period	tscyc1	—	—	200	—	ns	*5
SCL cycle period High period	twhc1	—	—	100	—	ns	*5
SCL cycle period Low period	twlc1	—	—	100	—	ns	*5
Serial data setup time	tss1	—	—	142	—	ns	*5
Serial data hold time	tsh1	—	—	142	—	ns	*5
Transceiving interval	tcsw1	—	—	100	—	ns	*5
Chip enable setup time	tcss1	—	—	5	—	ns	*5
Chip enable hold time	tcgh1	—	—	5	—	ns	*5
DC delay time	tdodly1	Read mode only	—	30	—	ns	*5

Note: *5 : Typical Design Value

Interface timing chart



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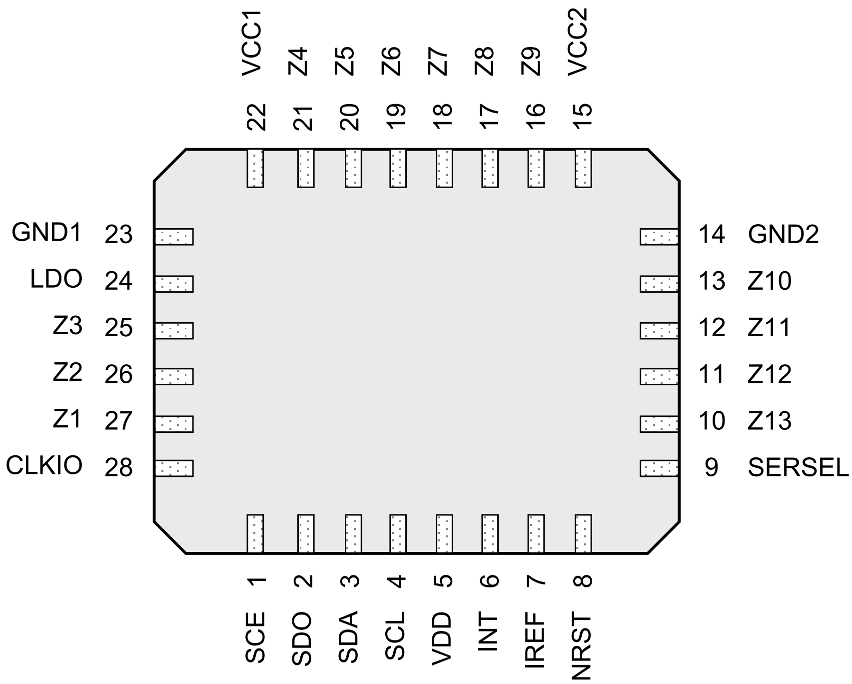
PIN CONFIGURATION

Top View



PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
1	SCE	Input	Chip enable signal for SPI interface.	SERSEL = High Then GND or V_{CC}
			Slave address selection pin for I²C interface.	SERSEL = Low Then GND or V_{CC} or SCL or SDA
2	SDO	Output	Data output pin for SPI interface	Open
3	SDA	Input/Output	Data input / output pin for SPI or I²C interface	(Required pin)
4	SCL	Input	Clock input pin for SPI or I²C interface	(Required pin)
5	VDD	Power Supply	Power supply for SPI or I²C interface	(Required pin)
6	INT (*1)	Output	Interruption signal output pin / Open drain	Open
7	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
8	NRST	Input	Reset input pin	(Required pin)
9	SERSEL	Input	Serial Interface selection pin / SPI or I²C interface	(Required pin)
10	Z13	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open

Note: *1 : INT pin must be pulled up to V_{DD} when it is in use.

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PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description	Pin processing at unused
11	Z12	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	Z11	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
13	Z10	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
14 23	GND2 GND1	Ground	Ground pin	(Required pin)
15 22	VCC2 VCC1	Power Supply	Power supply for matrix driver, Internal reference circuit	Battery or External power supply
16	Z9	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
17	Z8	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
18	Z7	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
19	Z6	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
20	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
21	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
24	LDO	Output	LDO output pin	(Required pin)
25	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
26	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
27	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
28	CLKIO	Input/Output	Reference clock input/output, LED control input pin	Open

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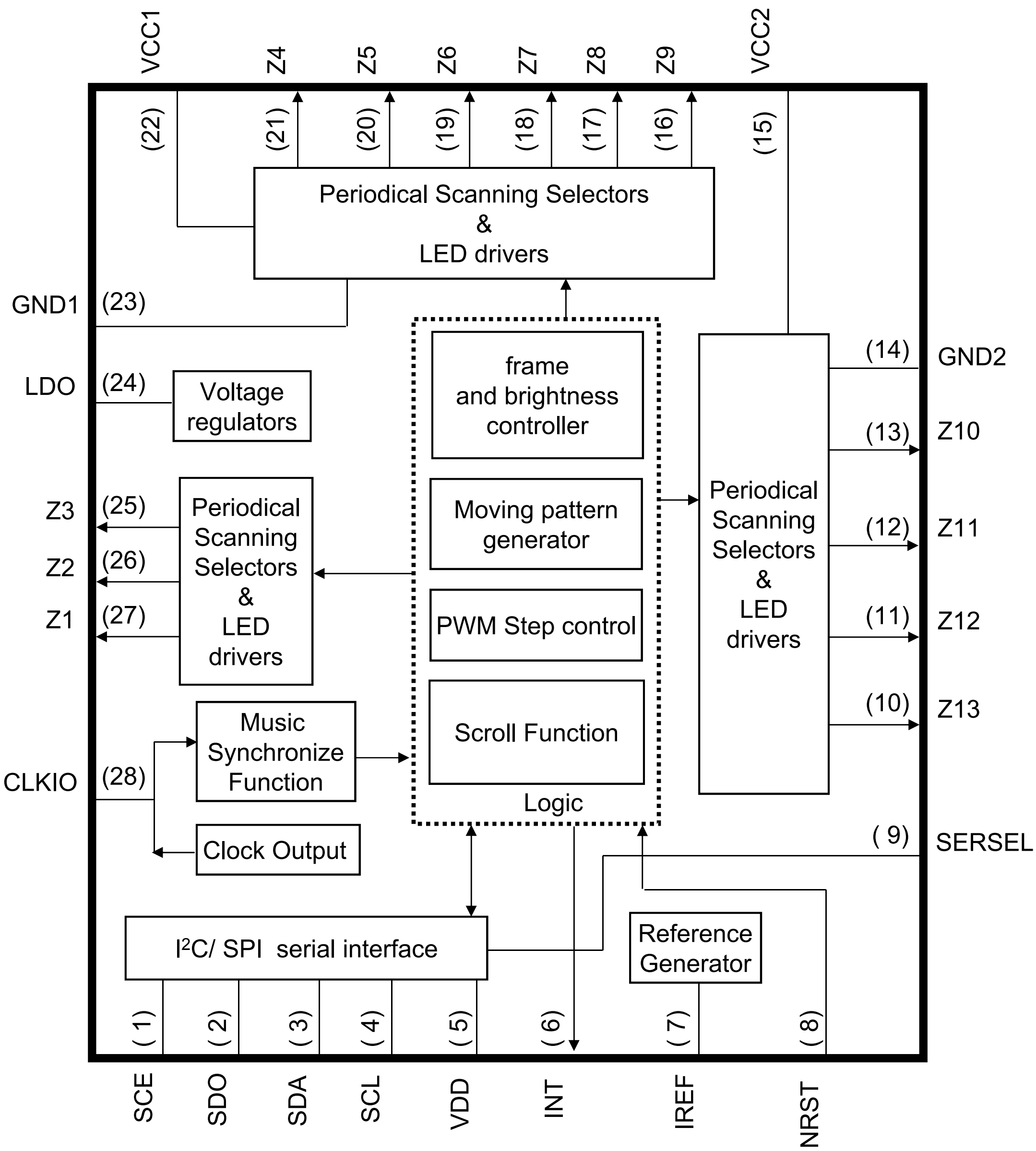
FUNCTIONAL BLOCK DIAGRAM

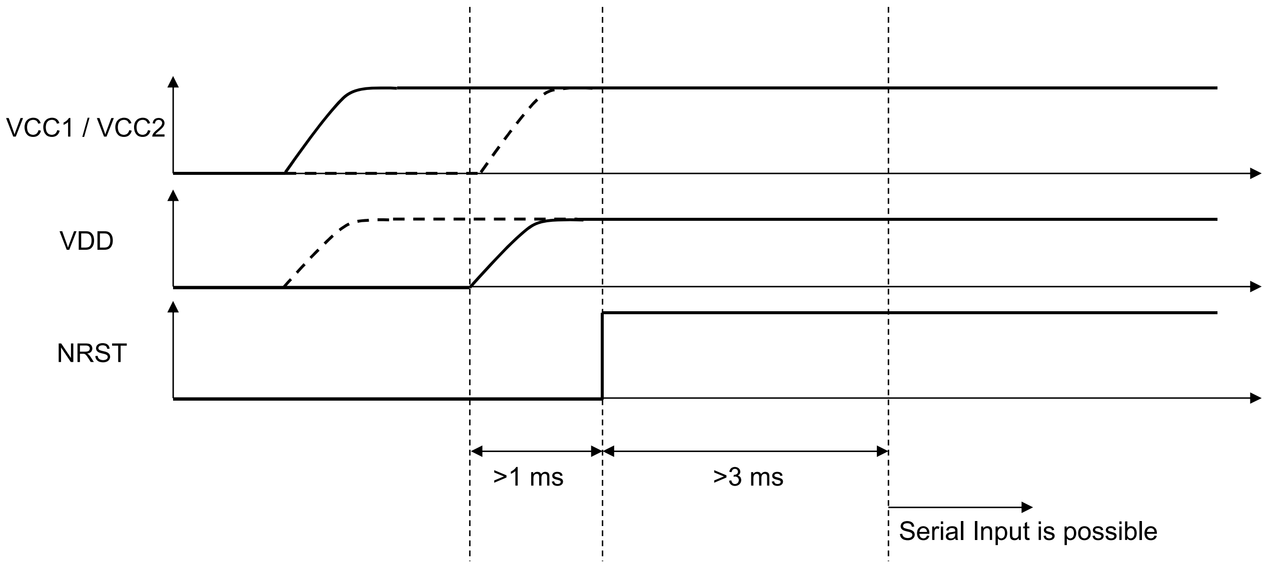


Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

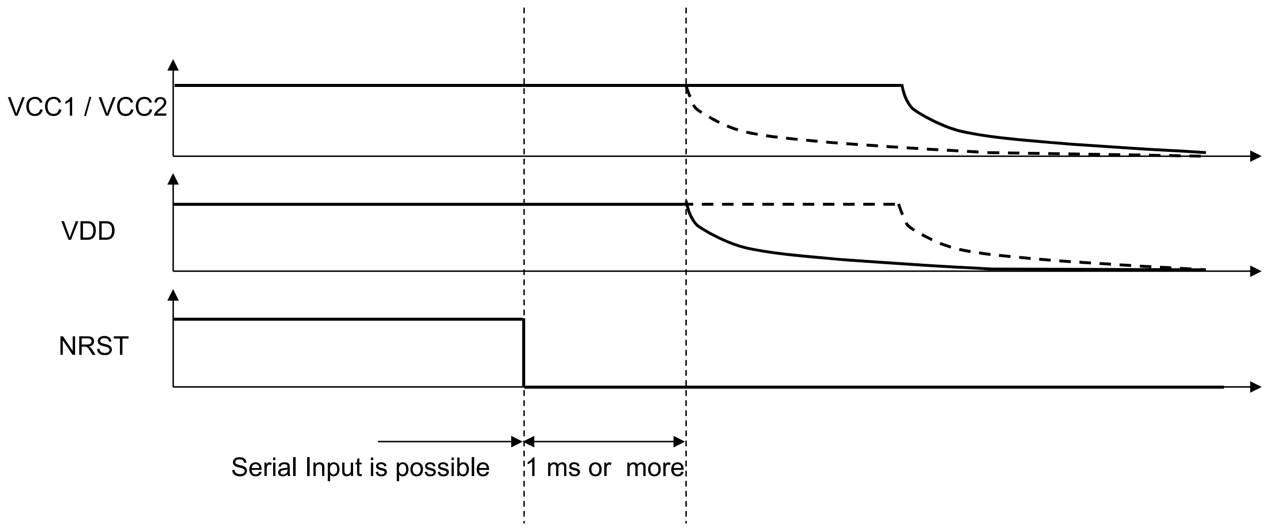
1. Power Supply Sequence

Power ON



Note: For the Startup Timing of VCC1 / VCC2 and VDD, it is possible to be changed.

Power OFF



Note: For the Shut down Timing of VCC1 / VCC2 and VDD, it is possible to be changed.

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OPERATION (continued)

2. Register Map

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
00h	RST	00h	R/W	--	--	--	--	--	RAM2RST	RAM1RST	SRST
01h	reserved	--	--	--	--	--	--	--	--	--	--
02h	reserved	--	--	--	--	--	--	--	--	--	--
03h	CLKCTL	78h	R/W	IMAX[4:0]					OSCEN	CLKOUT	EXTCLK
04h	MTXON	00h	R/W	--	--	--	--	ZPDEN	MTXMODE[1:0]		MTXON
05h	FRMSEL	00h	R/W	--	--	--	--	--	--	--	FRMSEL
06h	MTXON1	00h	R/W	A8ON	A7ON	A6ON	A5ON	A4ON	A3ON	A2ON	A1ON
07h	MTXON2	00h	R/W	B4ON	B3ON	B2ON	B1ON	A12ON	A11ON	A10ON	A9ON
08h	MTXON3	00h	R/W	B12ON	B11ON	B10ON	B9ON	B8ON	B7ON	B6ON	B5ON
09h	MTXON4	00h	R/W	C8ON	C7ON	C6ON	C5ON	C4ON	C3ON	C2ON	C1ON
0Ah	MTXON5	00h	R/W	D4ON	D3ON	D2ON	D1ON	C12ON	C11ON	C10ON	C9ON
0Bh	MTXON6	00h	R/W	D12ON	D11ON	D10ON	D9ON	D8ON	D7ON	D6ON	D5ON
0Ch	MTXON7	00h	R/W	E8ON	E7ON	E6ON	E5ON	E4ON	E3ON	E2ON	E1ON
0Dh	MTXON8	00h	R/W	F4ON	F3ON	F2ON	F1ON	E12ON	E11ON	E10ON	E9ON
0Eh	MTXON9	00h	R/W	F12ON	F11ON	F10ON	F9ON	F8ON	F7ON	F6ON	F5ON
0Fh	MTXON10	00h	R/W	G8ON	G7ON	G6ON	G5ON	G4ON	G3ON	G2ON	G1ON
10h	MTXON11	00h	R/W	H4ON	H3ON	H2ON	H1ON	G12ON	G11ON	G10ON	G9ON
11h	MTXON12	00h	R/W	H12ON	H11ON	H10ON	H9ON	H8ON	H7ON	H6ON	H5ON
12h	MTXON13	00h	R/W	I8ON	I7ON	I6ON	I5ON	I4ON	I3ON	I2ON	I1ON
13h	MTXON14	00h	R/W	J4ON	J3ON	J2ON	J1ON	I12ON	I11ON	I10ON	I9ON
14h	MTXON15	00h	R/W	J12ON	J11ON	J10ON	J9ON	J8ON	J7ON	J6ON	J5ON
15h	MTXON16	00h	R/W	K8ON	K7ON	K6ON	K5ON	K4ON	K3ON	K2ON	K1ON
16h	MTXON17	00h	R/W	L4ON	L3ON	L2ON	L1ON	K12ON	K11ON	K10ON	K9ON
17h	MTXON18	00h	R/W	L12ON	L11ON	L10ON	L9ON	L8ON	L7ON	L6ON	L5ON
18h	THOLD	00h	R/W	THOLD[7:0]							
19h	MELODY	00h	R/W	--	MLDCOM[2:0]			GRP4	GRP3	GRP2	GRP1
1Ah	INTREG	00h	R/W	--	--	--	--	TSTEND	OPEN	SHORT	FRMINT
1Bh	INTMSK	0Fh	R/W	--	--	--	--	TSTMSK	OPMSK	SHMSK	FRMMSK
1Ch	DETECT	00h	W	--	--	--	--	--	--	--	DETECT
1Dh	LEDON	00h	R/W	FADTIM	LED7ON	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1ON

Note: "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
1Eh	PWM1CTL	00h	R/W	--	PWM1EN	LED1DT[5:0]					
1Fh	PWM2CTL	00h	R/W	--	PWM2EN	LED2DT[5:0]					
20h	PWM3CTL	00h	R/W	--	PWM3EN	LED3DT[5:0]					
21h	PWM4CTL	00h	R/W	--	PWM4EN	LED4DT[5:0]					
22h	PWM5CTL	00h	R/W	--	PWM5EN	LED5DT[5:0]					
23h	PWM6CTL	00h	R/W	--	PWM6EN	LED6DT[5:0]					
24h	PWM7CTL	00h	R/W	--	PWM7EN	LED7DT[5:0]					
25h	LED0	00h	R/W	SDTH[1:0]		SDTL[1:0]		BRT0[3:0]			
26h	LED1	00h	R/W	--	SDT1[2:0]			BRT1[3:0]			
27h	LED2	00h	R/W	--	SDT2[2:0]			BRT2[3:0]			
28h	LED3	00h	R/W	--	SDT3[2:0]			BRT3[3:0]			
29h	LED4	00h	R/W	--	SDT4[2:0]			BRT4[3:0]			
2Ah	LED5	00h	R/W	--	SDT5[2:0]			BRT5[3:0]			
2Bh	LED6	00h	R/W	--	SDT6[2:0]			BRT6[3:0]			
2Ch	LED7	00h	R/W	--	SDT7[2:0]			BRT7[3:0]			
2Dh	LEDSEL1	00h	R/W	--	A2SEL[2:0]			--	A1SEL[2:0]		
2Eh	LEDSEL2	00h	R/W	--	A4SEL[2:0]			--	A3SEL[2:0]		
2Fh	LEDSEL3	00h	R/W	--	A6SEL[2:0]			--	A5SEL[2:0]		
30h	LEDSEL4	00h	R/W	--	A8SEL[2:0]			--	A7SEL[2:0]		
31h	LEDSEL5	00h	R/W	--	A10SEL[2:0]			--	A9SEL[2:0]		
32h	LEDSEL6	00h	R/W	--	A12SEL[2:0]			--	A11SEL[2:0]		
33h	LEDSEL7	00h	R/W	--	B2SEL[2:0]			--	B1SEL[2:0]		
34h	LEDSEL8	00h	R/W	--	B4SEL[2:0]			--	B3SEL[2:0]		
35h	LEDSEL9	00h	R/W	--	B6SEL[2:0]			--	B5SEL[2:0]		
36h	LEDSEL10	00h	R/W	--	B8SEL[2:0]			--	B7SEL[2:0]		
37h	LEDSEL11	00h	R/W	--	B10SEL[2:0]			--	B9SEL[2:0]		
38h	LEDSEL12	00h	R/W	--	B12SEL[2:0]			--	B11SEL[2:0]		
39h	LEDSEL13	00h	R/W	--	C2SEL[2:0]			--	C1SEL[2:0]		
3Ah	LEDSEL14	00h	R/W	--	C4SEL[2:0]			--	C3SEL[2:0]		
3Bh	LEDSEL15	00h	R/W	--	C6SEL[2:0]			--	C5SEL[2:0]		
3Ch	LEDSEL16	00h	R/W	--	C8SEL[2:0]			--	C7SEL[2:0]		
3Dh	LEDSEL17	00h	R/W	--	C10SEL[2:0]			--	C9SEL[2:0]		
3Eh	LEDSEL18	00h	R/W	--	C12SEL[2:0]			--	C11SEL[2:0]		
3Fh	LEDSEL19	00h	R/W	--	D2SEL[2:0]			--	D1SEL[2:0]		

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

Established : 2012-02-07
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OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
40h	LEDSEL20	00h	R/W	--	D4SEL[2:0]			--	D3SEL[2:0]		
41h	LEDSEL21	00h	R/W	--	D6SEL[2:0]			--	D5SEL[2:0]		
42h	LEDSEL22	00h	R/W	--	D8SEL[2:0]			--	D7SEL[2:0]		
43h	LEDSEL23	00h	R/W	--	D10SEL[2:0]			--	D9SEL[2:0]		
44h	LEDSEL24	00h	R/W	--	D12SEL[2:0]			--	D11SEL[2:0]		
45h	LEDSEL25	00h	R/W	--	E2SEL[2:0]			--	E1SEL[2:0]		
46h	LEDSEL26	00h	R/W	--	E4SEL[2:0]			--	E3SEL[2:0]		
47h	LEDSEL27	00h	R/W	--	E6SEL[2:0]			--	E5SEL[2:0]		
48h	LEDSEL28	00h	R/W	--	E8SEL[2:0]			--	E7SEL[2:0]		
49h	LEDSEL29	00h	R/W	--	E10SEL[2:0]			--	E9SEL[2:0]		
4Ah	LEDSEL30	00h	R/W	--	E12SEL[2:0]			--	E11SEL[2:0]		
4Bh	LEDSEL31	00h	R/W	--	F2SEL[2:0]			--	F1SEL[2:0]		
4Ch	LEDSEL32	00h	R/W	--	F4SEL[2:0]			--	F3SEL[2:0]		
4Dh	LEDSEL33	00h	R/W	--	F6SEL[2:0]			--	F5SEL[2:0]		
4Eh	LEDSEL34	00h	R/W	--	F8SEL[2:0]			--	F7SEL[2:0]		
4Fh	LEDSEL35	00h	R/W	--	F10SEL[2:0]			--	F9SEL[2:0]		
50h	LEDSEL36	00h	R/W	--	F12SEL[2:0]			--	F11SEL[2:0]		
51h	LEDSEL37	00h	R/W	--	G2SEL[2:0]			--	G1SEL[2:0]		
52h	LEDSEL38	00h	R/W	--	G4SEL[2:0]			--	G3SEL[2:0]		
53h	LEDSEL39	00h	R/W	--	G6SEL[2:0]			--	G5SEL[2:0]		
54h	LEDSEL40	00h	R/W	--	G8SEL[2:0]			--	G7SEL[2:0]		
55h	LEDSEL41	00h	R/W	--	G10SEL[2:0]			--	G9SEL[2:0]		
56h	LEDSEL42	00h	R/W	--	G12SEL[2:0]			--	G11SEL[2:0]		
57h	LEDSEL43	00h	R/W	--	H2SEL[2:0]			--	H1SEL[2:0]		
58h	LEDSEL44	00h	R/W	--	H4SEL[2:0]			--	H3SEL[2:0]		
59h	LEDSEL45	00h	R/W	--	H6SEL[2:0]			--	H5SEL[2:0]		
5Ah	LEDSEL46	00h	R/W	--	H8SEL[2:0]			--	H7SEL[2:0]		
5Bh	LEDSEL47	00h	R/W	--	H10SEL[2:0]			--	H9SEL[2:0]		
5Ch	LEDSEL48	00h	R/W	--	H12SEL[2:0]			--	H11SEL[2:0]		
5Dh	LEDSEL49	00h	R/W	--	I2SEL[2:0]			--	I1SEL[2:0]		
5Eh	LEDSEL50	00h	R/W	--	I4SEL[2:0]			--	I3SEL[2:0]		
5Fh	LEDSEL51	00h	R/W	--	I6SEL[2:0]			--	I5SEL[2:0]		

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

Established : 2012-02-07
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OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0
60h	LEDSEL52	00h	R/W	--	I8SEL[2:0]			--	I7SEL[2:0]		
61h	LEDSEL53	00h	R/W	--	I10SEL[2:0]			--	I9SEL[2:0]		
62h	LEDSEL54	00h	R/W	--	I12SEL[2:0]			--	I11SEL[2:0]		
63h	LEDSEL55	00h	R/W	--	J2SEL[2:0]			--	J1SEL[2:0]		
64h	LEDSEL56	00h	R/W	--	J4SEL[2:0]			--	J3SEL[2:0]		
65h	LEDSEL57	00h	R/W	--	J6SEL[2:0]			--	J5SEL[2:0]		
66h	LEDSEL58	00h	R/W	--	J8SEL[2:0]			--	J7SEL[2:0]		
67h	LEDSEL59	00h	R/W	--	J10SEL[2:0]			--	J9SEL[2:0]		
68h	LEDSEL60	00h	R/W	--	J12SEL[2:0]			--	J11SEL[2:0]		
69h	LEDSEL61	00h	R/W	--	K2SEL[2:0]			--	K1SEL[2:0]		
6Ah	LEDSEL62	00h	R/W	--	K4SEL[2:0]			--	K3SEL[2:0]		
6Bh	LEDSEL63	00h	R/W	--	K6SEL[2:0]			--	K5SEL[2:0]		
6Ch	LEDSEL64	00h	R/W	--	K8SEL[2:0]			--	K7SEL[2:0]		
6Dh	LEDSEL65	00h	R/W	--	K10SEL[2:0]			--	K9SEL[2:0]		
6Eh	LEDSEL66	00h	R/W	--	K12SEL[2:0]			--	K11SEL[2:0]		
6Fh	LEDSEL67	00h	R/W	--	L2SEL[2:0]			--	L1SEL[2:0]		
70h	LEDSEL68	00h	R/W	--	L4SEL[2:0]			--	L3SEL[2:0]		
71h	LEDSEL69	00h	R/W	--	L6SEL[2:0]			--	L5SEL[2:0]		
72h	LEDSEL70	00h	R/W	--	L8SEL[2:0]			--	L7SEL[2:0]		
73h	LEDSEL71	00h	R/W	--	L10SEL[2:0]			--	L9SEL[2:0]		
74h	LEDSEL72	00h	R/W	--	L12SEL[2:0]			--	L11SEL[2:0]		
75h	SCROLL1	00h	R/W	--	E_STOP	D_STOP	C_STOP	B_STOP	A_STOP	UP	LEFT
76h	SCROLL2	00h	R/W	--	--	--	--	--	SCLTIME[2:0]		
77h	XCONST1	00h	R/W	X8CONST	X7CONST	X6CONST	X5CONST	X4CONST	X3CONST	X2CONST	X1CONST
78h	XCONST2	00h	R/W	--	--	--	X13 CONST	X12 CONST	X11 CONST	X10 CONST	X9 CONST
79h	YMSK1	00h	R/W	Y8MSK	Y7MSK	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
7Ah	YMSK2	00h	R/W	--	--	--	YMSKVAL	Y12MSK	Y11MSK	Y10MSK	Y9MSK
7Bh	reserved	--	--	--	--	--	--	--	--	--	--
7Ch	reserved	--	--	--	--	--	--	--	--	--	--
7Dh	reserved	--	--	--	--	--	--	--	--	--	--
7Eh	SCANSET	0Bh	R/W	--	--	--	--	SCANSET[3:0]			
7Fh	reserved	--	--	--	--	--	--	--	--	--	--

Note) "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

3. Register map Detailed Explanation

Register Name		RST							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00h	W	--	--	--	--	--	RAM2RST	RAM1RST	SRST
Default	00h	0	0	0	0	0	0	0	0

D2 : RAM2RST Frame 2 reset control
[0] : No operation (default)
[1] : Frame 2 data is cleared

D1 : RAM1RST Frame 1 reset control
[0] : No operation (default)
[1] : Frame1 data is reset

D0 : SRST Soft reset control
[0] : No operation (default)
[1] : System reset

• This register will auto-return to [0] when written with [1] logic value.

Established : 2012-02-07
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		CLKCTL							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
03h	R/W	IMAX[4:0]					OSCEN	CLKOUT	EXTCLK
Default	78h	0	1	1	1	1	0	0	0

D7 : IMAX Maximum current selection
[0] : 30 mA (default)
[1] : 60 mA

D6-3 : IMAX Maximum current setup selection
[0000] : 0 mA / 0 mA
[0001] : 2 mA / 4 mA
....
[1110] : 28 mA / 56 mA
[1111] : 30 mA (Default) / 60 mA

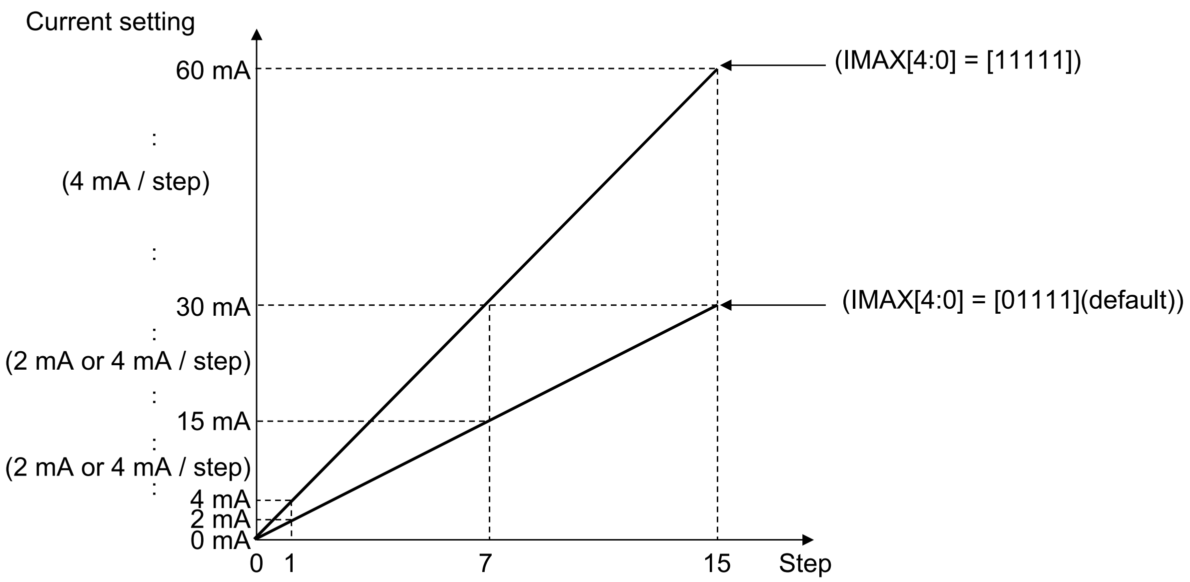
D2 : OSCEN Internal oscillator ON / OFF control
[0] : Internal oscillator OFF (default)
[1] : Internal oscillator ON

• Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = [1]) even if this bit is [0].

D1 : CLKOUT Internal clock output enable
[0] : Internal clock is not output from CLKIO (default)
[1] : Internal clock is output from CLKIO

D0 : EXTCLK Internal / external clock select
[0] : 2.4 MHz Internal clock is used in operation (default)
[1] : External clock is used in operation

• Please do not set MTXMODE = [10] (Melody Mode), EXTCLK = [1] and CLKOUT = [1] at the same time.
In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.



OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MTXON							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
04h	R/W	--	--	--	--	ZPDEN	MTXMODE[1:0]		MTXON
Default	00h	0	0	0	0	0	0	0	0

D3 : ZPDEN Ghost image prevention function enable
[0] : Turn off ghost image prevention (default)
[1] : Turn on ghost image prevention

D2-1 : MTXMODE Matrix mode of operation select
[00] : Display Matrix frame 1 character (default)
[01] : Display Matrix frame 2 character
[10] : Melody Mode
[11] : Scroll Mode

D0 : MTXON Matrix ON / OFF setting
[0] : OFF (default)
[1] : ON

- Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method. Please refer to Page.59 for details.
- Please refer to Page.60 for details especially when this IC is used for RGB driver.

Register Name		FRMSEL							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
05h	R/W	--	--	--	--	--	--	--	FRMSEL
Default	00h	0	0	0	0	0	0	0	0

D0 : FRMSEL

(1) Normal Modes :
[0] : Matrix Frame 1 is selected for character write (default).
[1] : Matrix Frame 2 is selected for character write.

(2) Melody Mode :
[0] : Matrix Frame 1 is selected for character write (default).
[1] : Matrix Frame 2 is selected for melody enable for each LED.

- During scroll mode, FRMSEL need not be set. Frame to be written is automatically selected whichever is free.

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MTXON1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
06h	W	A8ON	A7ON	A6ON	A5ON	A4ON	A3ON	A2ON	A1ON
Default	00h	0	0	0	0	0	0	0	0

D7 : A8ON

(1) Normal Mode : LED A8 of Matrix ON / OFF control
[0] : OFF (default)
[1] : ON

(2) Melody Mode & FRMSEL = [1] : LED A8 of Matrix Melody Mode ON / OFF control
[0] : LED A8 Melody Mode OFF (default)
[1] : LED A8 Melody Mode ON

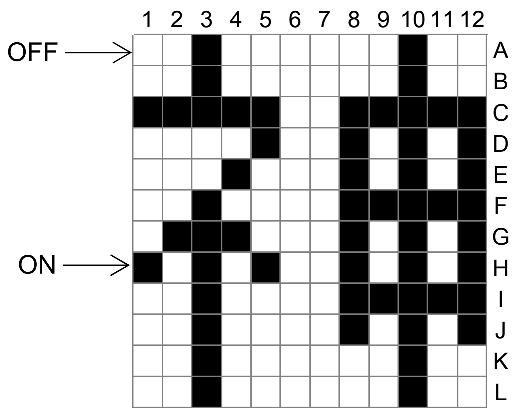
...

D0 : A1ON

(1) Normal Mode : LED A1 of Matrix ON / OFF control
[0] : OFF (default)
[1] : ON

(2) Melody Mode & FRMSEL = [1] : LED A1 of Matrix Melody Mode ON / OFF control
[0] : LED A1 Melody Mode OFF (default)
[1] : LED A1 Melody Mode ON

- The definition for register addresses 07h to 17h is the same as address 06h.
- Collectively, these register addresses are used to create frame character (*see figure*).
- If FRMSEL = [0], the data written to these group of registers will be for Matrix frame 1 character.
- If FRMSEL = [1], the data written to these group of registers will be for Matrix frame 2 character.
- During Melody Mode, the data written on these group of registers when FRMSEL = [1] will be designated as melody enable for each LED in matrix. The character to be display is determined by the data written when FRMSEL = [0].



OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		THOLD							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18h	R/W	THOLD[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7 : THOLD[7] Threshold 8 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6 : THOLD[6] Threshold 7 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5 : THOLD[5] Threshold 6 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4 : THOLD[4] Threshold 5 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3 : THOLD[3] Threshold 4 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2 : THOLD[2] Threshold 3 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1 : THOLD[1] Threshold 2 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0 : THOLD[0] Threshold 1 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set [0], threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic [1] value at the same time.
- If 2 bits are set to [1] at the same time, system will only recognize the first [1] bit threshold that is set.

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MELODY							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
19h	R/W	--	MLDCOM[2:0]			GRP4	GRP3	GRP2	GRP1
Default	00h	0	0	0	0	0	0	0	0

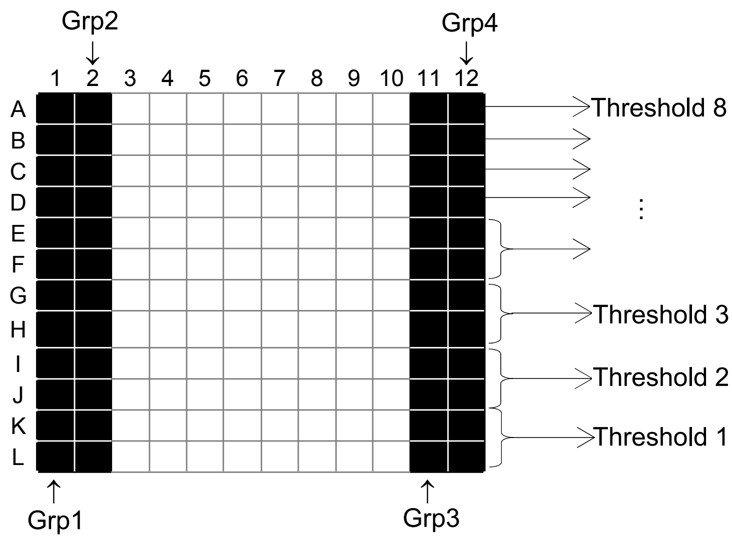
D6-4 : MLDCOM Brightness compensation in melody mode
[000] : No Compensation (default)
[001] : PWM duty + 12.5 %
[010] : PWM duty + 25.0 %
[011] : PWM duty + 37.5 %
[100] : PWM duty + 50.0 %
[101] : PWM duty + 62.5 %
[110] : PWM duty + 75.0 %
[111] : PWM duty + 87.5 %

D3 : GRP4 Group 4 LED melody control
[0] : Normal operation (default)
[1] : During melody mode, Group 4 LEDs are synchronized to external source as bar meter.

D2 : GRP3 Group 3 LED melody control
[0] : Normal operation (default)
[1] : During melody mode, Group 3 LEDs are synchronized to external source as bar meter.

D1 : GRP2 Group 2 LED melody control
[0] : Normal operation (default)
[1] : During melody mode, Group 2 LEDs are synchronized to external source as bar meter.

D0 : GRP1 Group 1 LED melody control
[0] : Normal operation (default)
[1] : During melody mode, Group 1 LEDs are synchronized to external source as bar meter.



• During Bar Meter Mode, auto threshold detection should be used.
This IC does not support Bar Meter Mode with fixed threshold setting.

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		INTREG							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Ah	R/W	--	--	--	--	TSTEND	OPEN	SHORT	FRMINT
Default	00h	0	0	0	0	0	0	0	0

D3 : TSTEND Indicates the LED test finish
[0] : Normal operation (default)
[1] : LED detection finished

D2 : OPEN Indicates open circuit is detected
[0] : Normal operation (default)
[1] : Open circuit detected

D1 : SHORT Indicates short circuit is detected
[0] : Normal operation (default)
[1] : Short circuit detected

D0 : FRMINT Indicate end of scroll of one frame
[0] : Normal operation (default)
[1] : End of frame.

- Any bit in this register will cause INT pin to go "Low".
- To clear interrupt, write [0] to corresponding bit.
- Writing [1] to these bits will be ignored.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		INTMSK							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Bh	R/W	--	--	--	--	TSTMSK	OPMSK	SHMSK	FRMMSK
Default	0Fh	0	0	0	0	1	1	1	1

D3 : TSTMSK TSTEND interrupt mask register
[0] : Interrupt is not masked.
[1] : Interrupt is masked. (default).

D2 : OPMSK Open error interrupt mask register
[0] : Interrupt is not masked.
[1] : Interrupt is masked. (default).

D1 : SHMSK Shorted error interrupt mask register
[0] : Interrupt is not masked.
[1] : Interrupt is masked. (default).

D0 : FRMMSK Frame interrupt mask register
[0] : Interrupt is not masked.
[1] : Interrupt is masked. (default).

Register Name		DETECT							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Ch	W	--	--	--	--	--	--	--	DETECT
Default	00h	0	0	0	0	0	0	0	0

D0 : DETECT Open/short detection enable
[0] : detection is OFF (default)
[1] : detection is ON

• Enabling this register will also enable the matrix operation. Don't set MTXON and DETECT both to [1] at same time.

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		LEDON							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Dh	R/W	FADTIM	LED7ON	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1ON
Default	00h	0	0	0	0	0	0	0	0

D7 : FADTIM Fade Out control
[0] : Fade Out step delay is same as Fade In step delay (default).
[1] : Fade Out step delay is 2× of Fade In step delay.

D6 : LED7ON LED Driver No. 7 ON / OFF control
[0] : OFF (default)
[1] : ON

D5 : LED6ON LED Driver No. 6 ON / OFF control
[0] : OFF (default)
[1] : ON

D4 : LED5ON LED Driver No. 5 ON / OFF control
[0] : OFF (default)
[1] : ON

D3 : LED4ON LED Driver No. 4 ON / OFF control
[0] : OFF (default)
[1] : ON

D2 : LED3ON LED Driver No. 3 ON / OFF control
[0] : OFF (default)
[1] : ON

D1 : LED2ON LED Driver No. 2 ON / OFF control
[0] : OFF (default)
[1] : ON

D0 : LED1ON LED Driver No. 1 ON / OFF control
[0] : OFF (default)
[1] : ON

- There are 7 LED drivers to control each of the 144 Matrix LED.
- These LED drivers are enabled through this register.
- Each LED can select their drivers through register addresses 2Dh to 74h.

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		PWM1CTL							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Eh	R/W	--	PWM1EN	LED1DT[5:0]					
Default	00h	0	0	0	0	0	0	0	0

D6 : PWM1EN LED Driver No. 1 PWM mode enable
[0] : PWM mode disabled (default)
[1] : PWM mode enabled

D5-0 : LED1DT LED Driver No. 1 PWM duty control
[00_0000] 0 %
[00_0001] 1.56 % (1 / 64)
[00_0010] 3.13 % (2 / 64)
[00_0011] 4.69 % (3 / 64)
....
[11_1100] 95.3 % (61 / 64)
[11_1110] 96.9 % (62 / 64)
[11_1111] 98.4 % (63 / 64)

• The definition for register addresses 1Fh to 24h is the same as address 1Eh.

Established : 2012-02-07
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		LED0							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
25h	R/W	SDTH[1:0]		SDTL[1:0]		BRT0[3:0]			
Default	00h	0	0	0	0	0	0	0	0

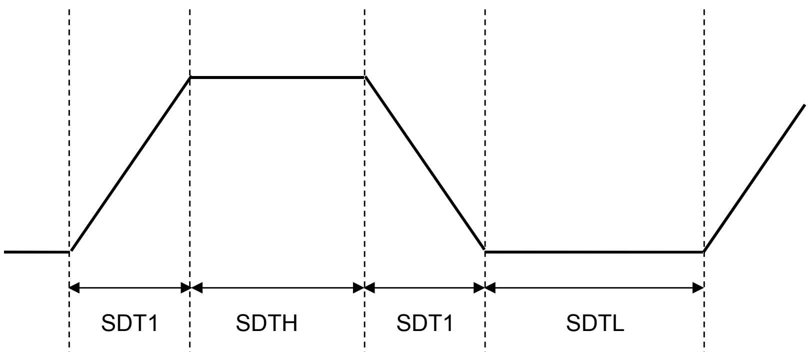
D7-6 : SDTH LED firefly maximum duty time extent
[00] : SDT(1 to 7) × 1 (default)
[01] : SDT(1 to 7) × 0.25
[10] : SDT(1 to 7) × 0.5
[11] : SDT(1 to 7) × 2

D5-4 : SDTL LED firefly minimum duty time extent
[00] : SDT(1 to 7) × 1 (default)
[01] : SDT(1 to 7) × 0.25
[10] : SDT(1 to 7) × 0.5
[11] : SDT(1 to 7) × 2

- These settings are valid for LED drivers No. 1 to 7 during LED firefly operation.
- Time SDT(1 to 7) of LED Drivers No. 1 to 7 are controlled through registers 26h to 2Ch.

D3-0 : BRT0 LED brightness setup when LED driver select is [000].
[0000] : Repeat Duty operation 1× for each column scan (default)
[0001] : Repeat Duty operation 2× for each column scan
[0010] : Repeat Duty operation 3× for each column scan
[0011] : Repeat Duty operation 4× for each column scan
....
[1110] : Repeat Duty operation 15× for each column scan
[1111] : Repeat Duty operation 16× for each column scan

- LED driver select is set through register 2Dh to 74h.



OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		LED1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
26h	R/W	--	SDT1[2:0]			BRT1[3:0]			
Default	00h	0	0	0	0	0	0	0	0

D6-4 : SDT1

(1) Firefly Operation (PWM*EN = [0]) LED Driver No. 1 rise / fall time extent.

[000] : Constant current mode (default)
[001] : 0.33 s (416.67 ns × 12,336 × 64 × 1)
[010] : 0.66 s (416.67 ns × 12,336 × 64 × 2)
[011] : 1.32 s (416.67 ns × 12,336 × 64 × 4)
[100] : 1.98 s (416.67 ns × 12,336 × 64 × 6)
[101] : 2.64 s (416.67 ns × 12,336 × 64 × 8)
[110] : 3.30 s (416.67 ns × 12,336 × 64 × 10)
[111] : 3.96 s (416.67 ns × 12,336 × 64 × 12)

(2) PWM Fade-in / out Operation (PWM*EN = [1]) LED Driver No. 1 one step time delay.

[000] : Instantaneous change (default)
[001] : 10.28 ms (416.67 ns × 12,336 × 2)
[010] : 20.56 ms (416.67 ns × 12,336 × 4)
[011] : 41.12 ms (416.67 ns × 12,336 × 8)
[100] : 61.68 ms (416.67 ns × 12,336 × 12)
[101] : 82.24 ms (416.67 ns × 12,336 × 16)
[110] : 102.8 ms (416.67 ns × 12,336 × 20)
[111] : 124.0 ms (416.67 ns × 12,336 × 24)

- If register 1Dh[7] FADTIM = [0], Fade Out step delay is same as Fade In step delay.
- If register 1Dh[7] FADTIM = [1], Fade Out step delay is 2× of Fade In step delay.

D3-0 : BRT1 LED Driver No. 1 brightness setup

[0000] : Repeat Duty operation 1× for each column scan (default)
[0001] : Repeat Duty operation 2× for each column scan
[0010] : Repeat Duty operation 3× for each column scan
[0011] : Repeat Duty operation 4× for each column scan
....
[1110] : Repeat Duty operation 15× for each column scan
[1111] : Repeat Duty operation 16× for each column scan

- The definition for register addresses 27h to 2Ch are the same as register 26h.

Established : 2012-02-07
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		LEDSEL1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2Dh	R/W	--	A2SEL[2:0]			--	A1SEL[2:0]		
Default	00h	0	0	0	0	0	0	0	0

D6-4 : A2SEL

(1) DETECT = [0] LED A2 driver select
[000] : Constant current mode (default)
[001] : LED Driver No. 1
[010] : LED Driver No. 2
[011] : LED Driver No. 3
[100] : LED Driver No. 4
[101] : LED Driver No. 5
[110] : LED Driver No. 6
[111] : LED Driver No. 7

(2) DETECT = [1] LED Open / Short detection control and status.
[000] : LED A2 Open / Short Detection is disabled (default)
[100] : LED A2 Open / Short Detection is enabled
[101] : LED A2 Open circuit detected
[110] : LED A2 Short circuit detected

D2-0 : A1SEL

(1) DETECT = [0] LED A1 driver select
[000] : Constant current mode (default)
[001] : LED Driver No. 1
[010] : LED Driver No. 2
[011] : LED Driver No. 3
[100] : LED Driver No. 4
[101] : LED Driver No. 5
[110] : LED Driver No. 6
[111] : LED Driver No. 7

(2) DETECT = [1] LED Open/Short detection control and status.
[000] : LED A1 Open / Short Detection is disabled (default)
[100] : LED A1 Open / Short Detection is enabled
[101] : LED A1 Open circuit detected
[110] : LED A1 Short circuit detected

- The definition for register addresses 2Eh to 74h are the same as register 2Dh.
- If constant current mode is selected, the brightness setting is controlled at register 25h
- During Open / Short Detection Mode (DETECT = [1]), the 2 LSB of the 3bit select register is the Open / Short detection status; e.g. A1SEL = [101] and A1SEL = [110] corresponds to the current state of open circuit and short circuit detection of LED A1 respectively. These bits are active High. If both bits are High at the same time, it will be ignored; e.g. A1SEL = [111].

Established : 2012-02-07
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		SCROLL1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
75h	R/W	--	E_STOP	D_STOP	C_STOP	B_STOP	A_STOP	UP	LEFT
Default	00h	0	0	0	0	0	0	0	0

D6 : E_STOP Row E LED scroll ON / OFF control
[0] : Row E LEDs during Scroll mode will scroll. (default)
[1] : Row E LEDs during Scroll mode are stationary.

D5 : D_STOP Row D LED scroll ON / OFF control
[0] : Row D LEDs during Scroll mode will scroll. (default)
[1] : Row D LEDs during Scroll mode are stationary.

D4 : C_STOP Row C LED scroll ON / OFF control
[0] : Row C LEDs during Scroll mode will scroll. (default)
[1] : Row C LEDs during Scroll mode are stationary.

D3 : B_STOP Row B LED scroll ON / OFF control
[0] : Row B LEDs during Scroll mode will scroll. (default)
[1] : Row B LEDs during Scroll mode are stationary.

D2 : A_STOP Row A LED scroll ON / OFF control
[0] : Row A LEDs during Scroll mode will scroll. (default)
[1] : Row A LEDs during Scroll mode are stationary.

D1 : UP Matrix scroll direction control 1
[0] : Scroll stop (default)
[1] : Matrix scroll up.

D0 : LEFT Matrix scroll direction control 2
[0] : Scroll stop (default)
[1] : Matrix scroll left.

- Note that scroll stop control, 75h[6:2], are not applicable if scroll direction is UP.
- During scroll mode (MTXMODE = [11]), all LEDs are in constant current mode.
- If both UP and LEFT direction is set, LEFT will have higher priority.

Register Name		SCROLL2							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
76h	R/W	--	--	--	--	--	SCLTIME[2:0]		
Default	00h	0	0	0	0	0	0	0	0

D2-0 : SCLTIME Scroll Time select
[000] : 0.025 s (default)
[001] : 0.050 s
[010] : 0.075 s
[011] : 0.100 s
[100] : 0.125 s
[101] : 0.150 s
[110] : 0.175 s
[111] : 0.200 s

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		XCONST1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
77h	R/W	X8CONST	X7CONST	X6CONST	X5CONST	X4CONST	X3CONST	X2CONST	X1CONST
Default	00h	0	0	0	0	0	0	0	0

D7 : X8CONST Z8 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z8 is fixed as constant current mode.

D6 : X7CONST Z7 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z7 is fixed as constant current mode.

D5 : X6CONST Z6 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z6 is fixed as constant current mode.

D4 : X5CONST Z5 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z5 is fixed as constant current mode.

D3 : X4CONST Z4 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z4 is fixed as constant current mode.

D2 : X3CONST Z3 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z3 is fixed as constant current mode.

D1 : X2CONST Z2 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z2 is fixed as constant current mode.

D0 : X1CONST Z1 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z1 is fixed as constant current mode.

• Please refer to Page.40 for details.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		XCONST2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
78h	R/W	--	--	--	X13CONST	X12CONST	X11CONST	X10CONST	X9CONST
Default	00h	0	0	0	0	0	0	0	0

D4 : X13CONST Z13 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z13 is fixed as constant current mode.

D3 : X12CONST Z12 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z12 is fixed as constant current mode.

D2 : X11CONST Z11 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z11 is fixed as constant current mode.

D1 : X10CONST Z10 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z10 is fixed as constant current mode.

D0 : X9CONST Z9 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z9 is fixed as constant current mode.

• Please refer to Page.40 for details.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		YMSK1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
79h	R/W	Y8MSK	Y7MSK	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
Default	00h	0	0	0	0	0	0	0	0

D7 : Y8MSK Internal control signal Y8CNT mask ON / OFF control.
[0] : Normal operation (default)
[1] : Y8CNT is mask to YMSKVAL logic value.

D6 : Y7MSK Internal control signal Y7CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y7CNT is mask to YMSKVAL logic value.

D5 : Y6MSK Internal control signal Y6CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y6CNT is mask to YMSKVAL logic value.

D4 : Y5MSK Internal control signal Y5CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y5CNT is mask to YMSKVAL logic value.

D3 : Y4MSK Internal control signal Y4CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y4CNT is mask to YMSKVAL logic value.

D2 : Y3MSK Internal control signal Y3CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y3CNT is mask to YMSKVAL logic value.

D1 : Y2MSK Internal control signal Y2CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y2CNT is mask to YMSKVAL logic value.

D0 : Y1MSK Internal control signal Y1CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y1CNT is mask to YMSKVAL logic value.

• Please refer to Page.48 for Internal control signal Y*CNT.

Established : 2012-02-07
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		YMSK2							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7Ah	R/W	--	--	--	YMSKVAL	Y12MSK	Y11MSK	Y10MSK	Y9MSK
Default	00h	0	0	0	0	0	0	0	0

D4 : YMSKVAL Y*MSK mask value control
[0] : Mask to Logic Low (default) Switch between VCC1 / VCC2 and Z* turns on.
[1] : Mask to Logic High Switch between VCC1 / VCC2 and Z* turns off.

D3 : Y12MSK Internal control signal Y12CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y12CNT is mask to YMSKVAL logic value.

D2 : Y11MSK Internal control signal Y11CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y11CNT is mask to YMSKVAL logic value.

D1 : Y10MSK Internal control signal Y10CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y10CNT is mask to YMSKVAL logic value.

D0 : Y9MSK Internal control signal Y9CNT mask ON / OFF control.
[0] : Normal matrix operation (default)
[1] : Y9CNT is mask to YMSKVAL logic value.

• XCONST* registers has higher priority than YMSK* meaning X constant mode has higher priority than Y mask to logic Low or High mode.
• Please refer to Page.48 for Internal control signal Y*CNT.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		SCANSET							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7Eh	R/W	--	--	--	--	SCANSET[3:0]			
Default	0Bh	0	0	0	0	1	0	1	1

D3-0 : SCANSET Column scan number control

[0000] : Scan the first column.
[0001] : Scan the first 2 column.
[0011] : Scan the first 3 column.
....

[1010] : Scan the first 11 column.
[1011] : Scan All columns (default).

- All other values will scan all column.
- This setting has no effect during Scroll Mode or DETECT = [1]. All columns will be scan in these modes.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

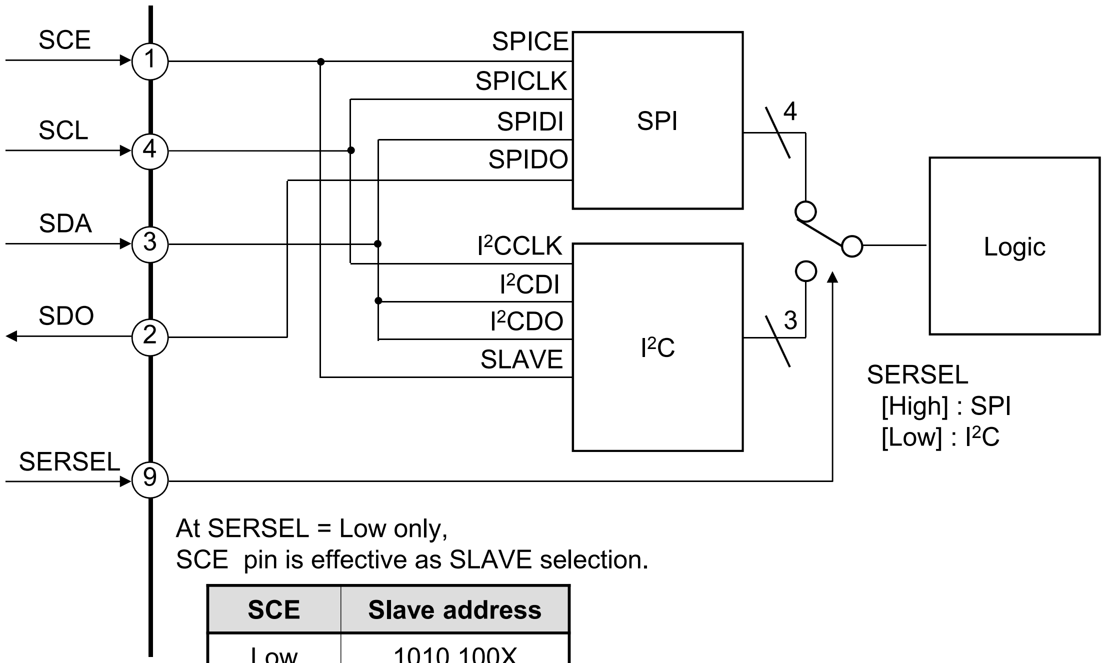
4. Operation Mode priority

MTXON	X*CONST	PWM*EN	SDT*	Operation Mode
0	x	x	x	OFF
1	1	x	x	Z* constant current mode
1	0	1	x	PWM mode
1	0	0	Not 000	Firefly mode
1	0	0	000	Constant current mode

• * for X*CONST = 1 to 13, PWM*EN and SDT* = 1 to 7

OPERATION (continued)

5. Interface Configuration



At SERSEL = Low only,
SCE pin is effective as SLAVE selection.

SCE	Slave address
Low	1010 100X
High	1010 101X
SCL	1010 110X
SDA	1010 111X

	SPI (SERSEL = High)	I^2C (SERSEL = Low)
SCE	in (Chip Enable)	in (Slave address selection)
SCL	in	in
SDA	in	in / out
SDO	out	Not use

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

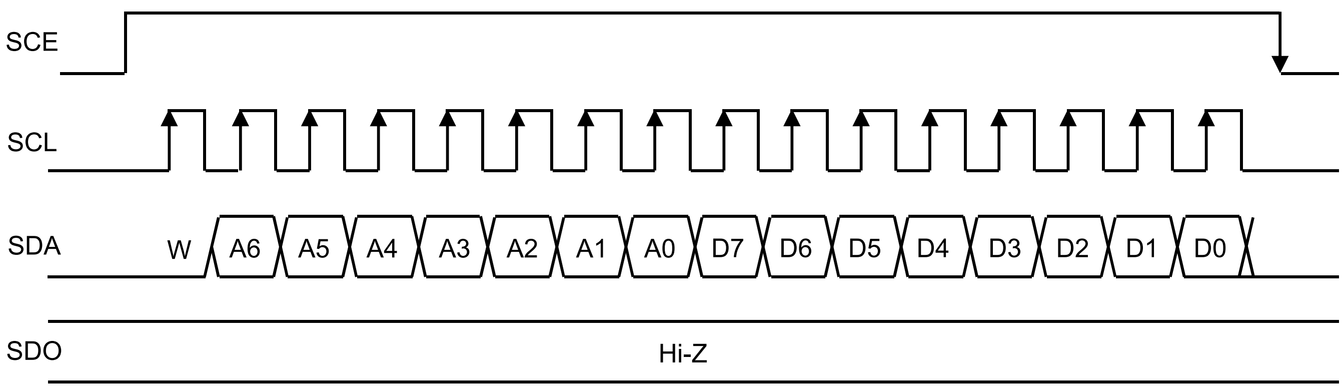
6. SPI Bus Interface

The interface with microcomputer consists of 16-bit serial register (8-bit of command, 8-bit of address), address decoder, and transmission register (8-bit).
Serial interface consists of 4 pins of serial clock pin (SCL), serial data input pin (SDA), serial data output pin (SDO), and chip enable input pin (SCE). When SPI interface is used, SERSEL pin should be fixed to High-level.

6.1 Write operation

In the case of MSB first, Write is recognized by SDA = Low at the 1st clock of SCL.
Data is taken into internal shift register at the rising edge of SCL.
(The frequency of SCL can be used up to 10 MHz.)
In High period of SCE, reception of data becomes enable. (active High)
In the case of MSB first, data is transmitted in order of control register address (8-bit) and control command (8-bit).

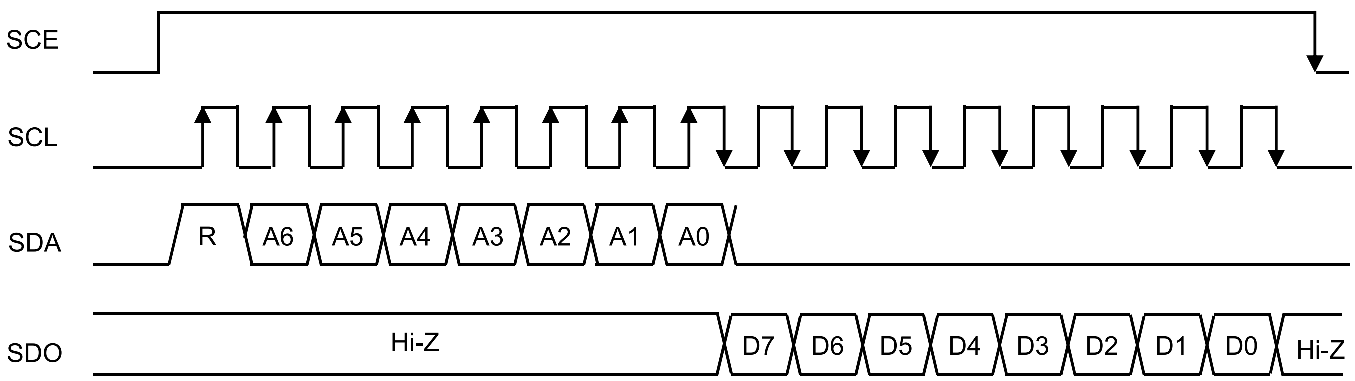
Writing access timing



6.2 Transmission operation

In the case of MSB first, Read is recognized by SDA = High at the 1st clock of SCL.
Data is taken into internal shift register at the rising edge of SCL.
(The frequency of SCL can be used up to 10 MHz.)
In High period of SCE, reception of data becomes enable. (active High)
In the case of MSB first, data is transmitted in order of control register address (8-bit) and control command (8-bit).
It is not possible to read RAM.

Read access timing



Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

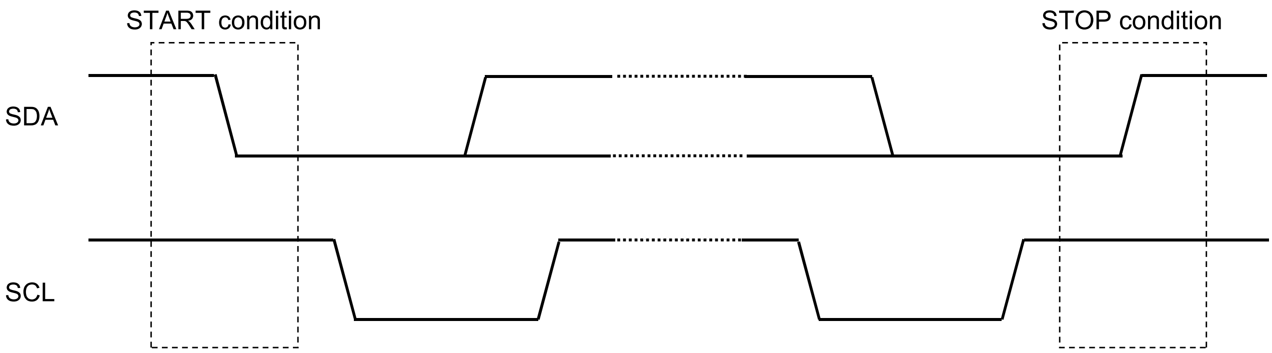
7. I²C Bus Interface

7.1 Basic Rules

- This IC, I²C-bus, is designed to correspond to the Standard-mode (100 kbps), Fast-mode (400 kbps) and Fast-mode plus (1000 kbps) devices in the version 03 of NXP's specification. However, it does not correspond to the HS-mode (to 3.4 Mbps).
- This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device.
- The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

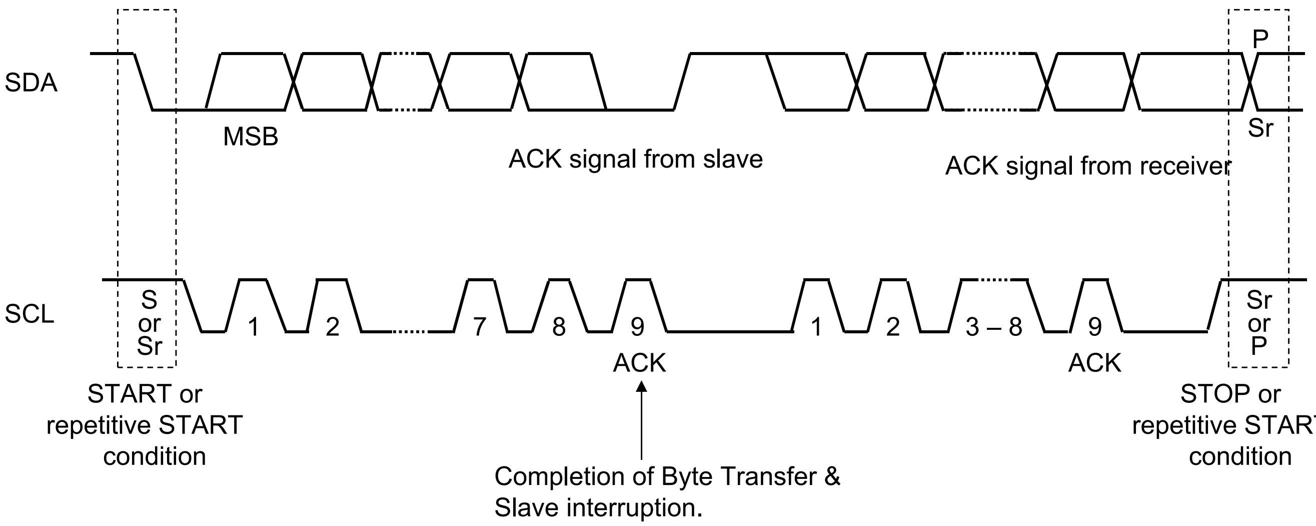
7.2 START and STOP conditions

When SDA signal changes from "High" to "Low" while SCL is "High" will trigger START condition. Whereas, STOP condition will be triggered when SDA signal changes from "Low" to "High" while SCL is "High". START condition and STOP condition are always formed by the master. After the START condition occurs, the bus becomes busy state. After STOP condition occurs, the bus becomes free again.



7.3 Data Transfer

Length of each byte output to SDA line is always 8 bits. There is no limitation in the number of bytes that can be transmitted at 1 time. Many bytes can be sent. The acknowledge bit is necessary for each byte. Data is sequentially transmitted from most significant bit (MSB).



OPERATION (continued)

7. I²C Bus Interface (continued)

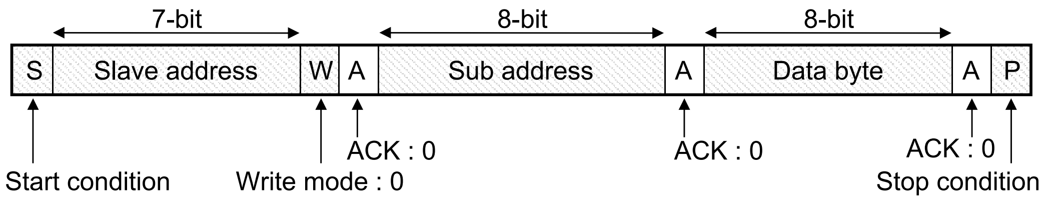
7.4 I²C Interface - Data Format

In this IC, 4 different Slave address can be changed by selecting SCE ("Low" or "High" or "SCL" or "SDA"). The slave addresses of this IC are as follow:

SCE	Slave address
Low	1010 100X
High	1010 101X
SCL	1010 110X
SDA	1010 111X

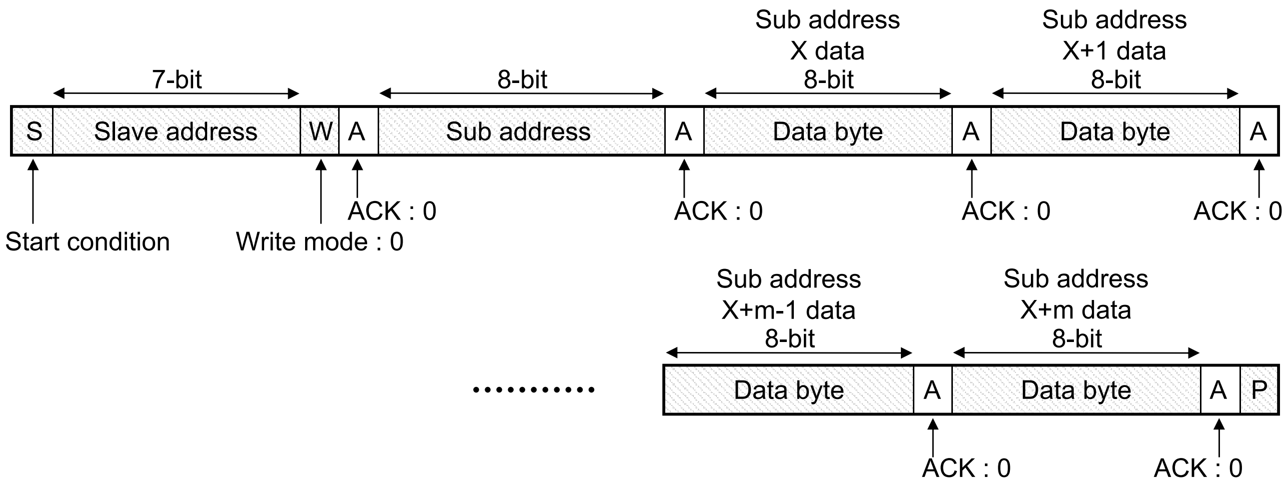
Write mode

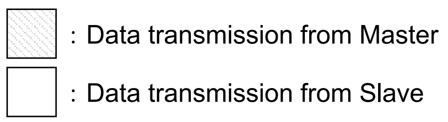
Sub address is not incremented automatically.
The next data byte is written in the same Sub address by transmitting data byte continuously.



Write mode (Auto increment mode)

Data byte can be written in Sub address by transmitting data byte continuously.
Sub address is incremented automatically.





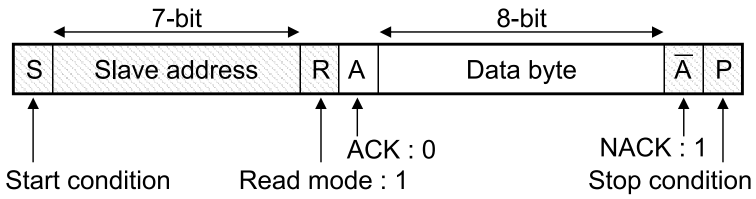
OPERATION (continued)

7. I²C Bus Interface (continued)

7.4 I²C Interface - Data Format (continued)

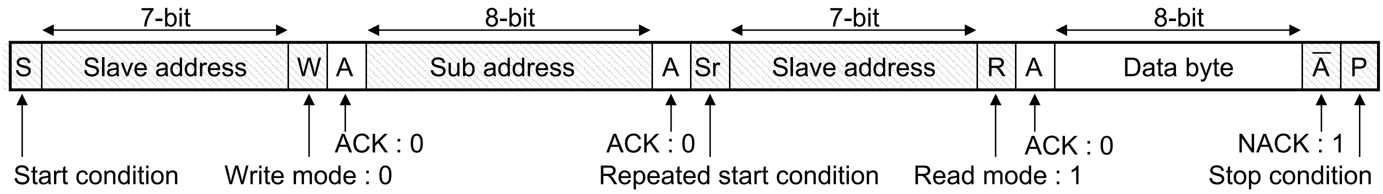
Read mode (in case Sub address is not specified)

When Sub address 8 bit is not specified and data is read, this IC allows to read the value of adjacent Sub address specified in the last Write mode.
The next data byte reads the same Sub address by transmitting data byte continuously.



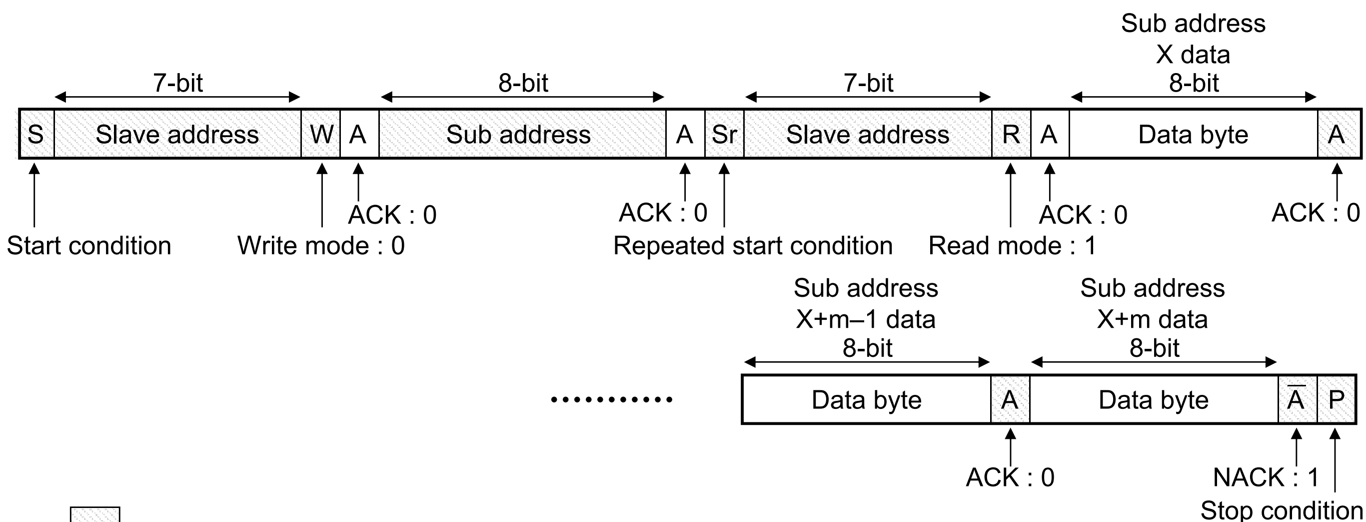
Read mode (in case Sub address is specified)

Sub address is not incremented automatically.
The next data byte reads the same Sub address by transmitting data byte continuously.



Read mode (Auto increment mode)

It is possible to read data byte in continuous Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

Established : 2012-02-07
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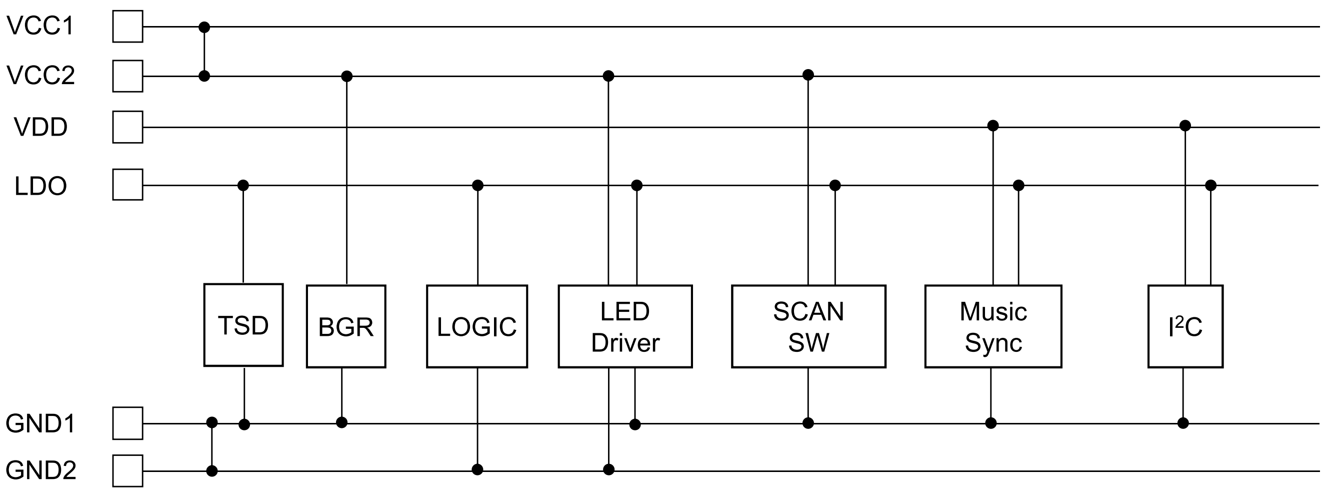
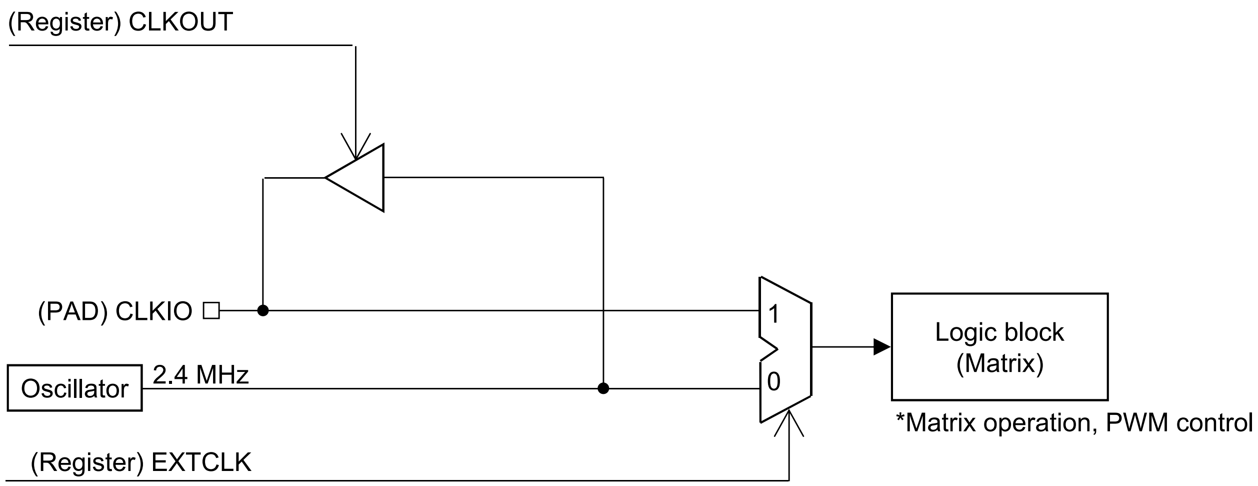
OPERATION (continued)

8. Signal distribution diagram

8.1 Distribution diagram of power supply



8.2 Distribution diagram of control / clock system



Established : 2012-02-07
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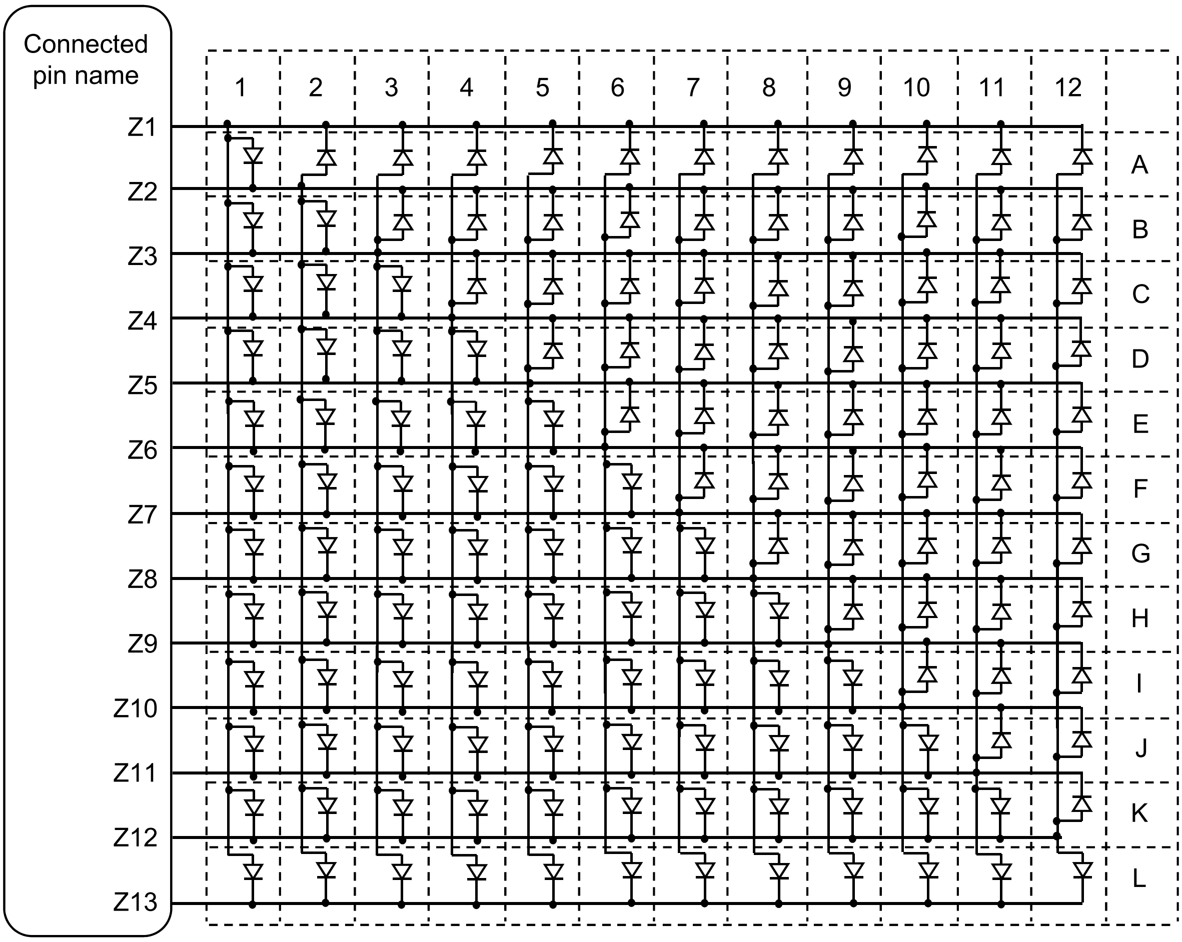
OPERATION (continued)

9. Block Configuration of Matrix LED

9.1 Matrix LED descriptions, Matrix LED's numbers

LED matrix driver circuit individually drives LED of 12 × 12 matrix. In total, the IC can drive and light up 144 LED. In this specification, LED's number controlled by each pin corresponds as follows.
The internal logic circuit is operated by using an internal clock or the external clock input to the terminal CLKIO.



Established : 2012-02-07
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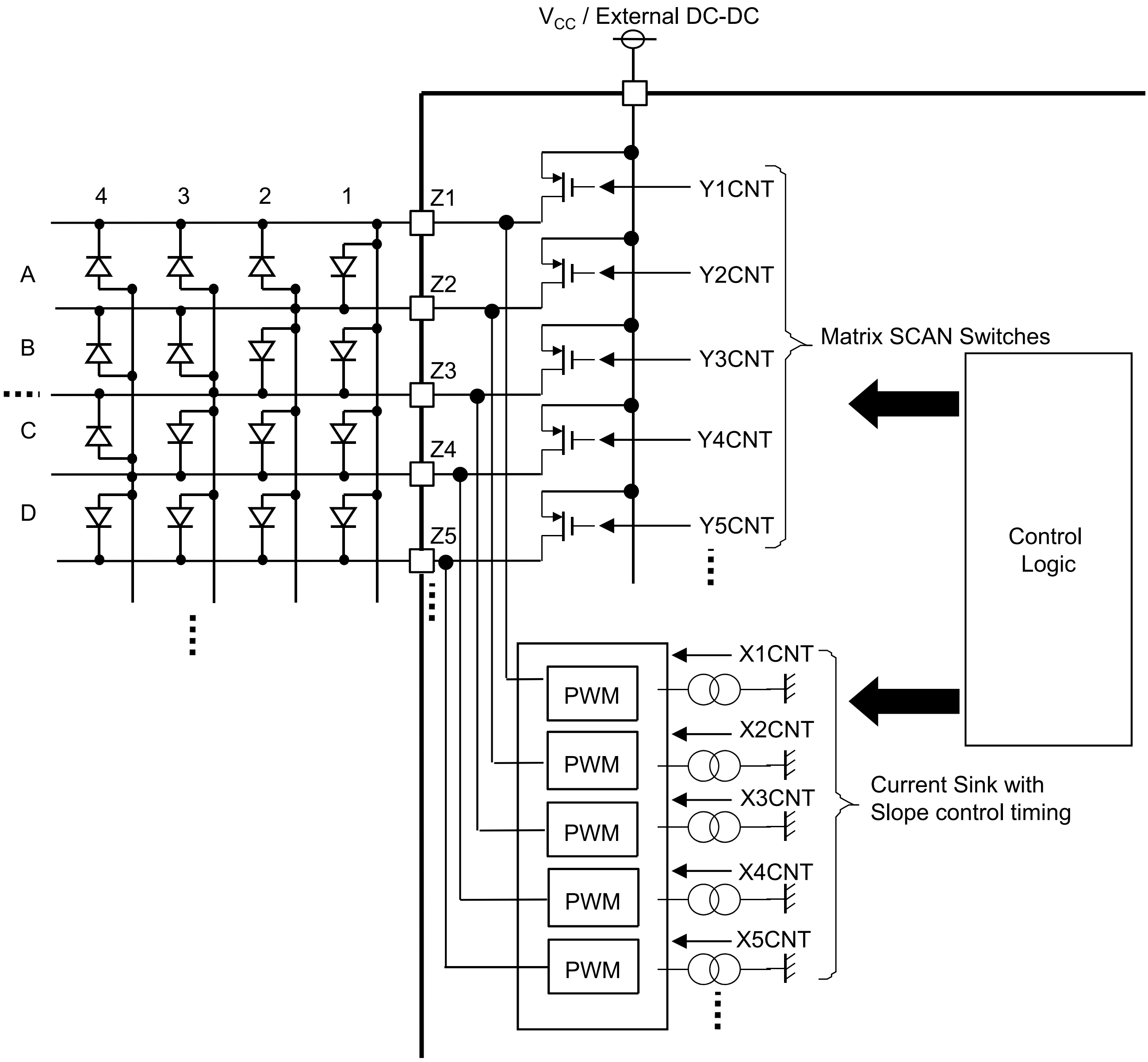
OPERATION (continued)

9. Block Configuration of Matrix LED (continued)

9.2 Driver Configuration

- Actual driver configuration is shown in the following figure.
- The anodes and cathode of each LED are connected to different Z* pin as shown in figure below.
- Z13 pin consists of only Current Sink and Slope control timing driver. Thus, LED anode are not to be connected to Z13 pin.
- Please do not remove any of the LED inside the matrix if it is not used. If LED are to be removed, it is advice to remove the entire row (e.g: all LED in row A) instead of removing only 1 LED. If only one LED in the row is removed instead of the whole row, user needs to avoid using LED whose reverse breakdown voltage is lower than the operating VCC level.
- Internal control logic according to user register settings is used to control Y1CNT to Y12CNT(PMOS ON / Off Scan Switches) as well as X1CNT to X13CNT (Current sink value as well as PWM / Slope timing for lighting effects)

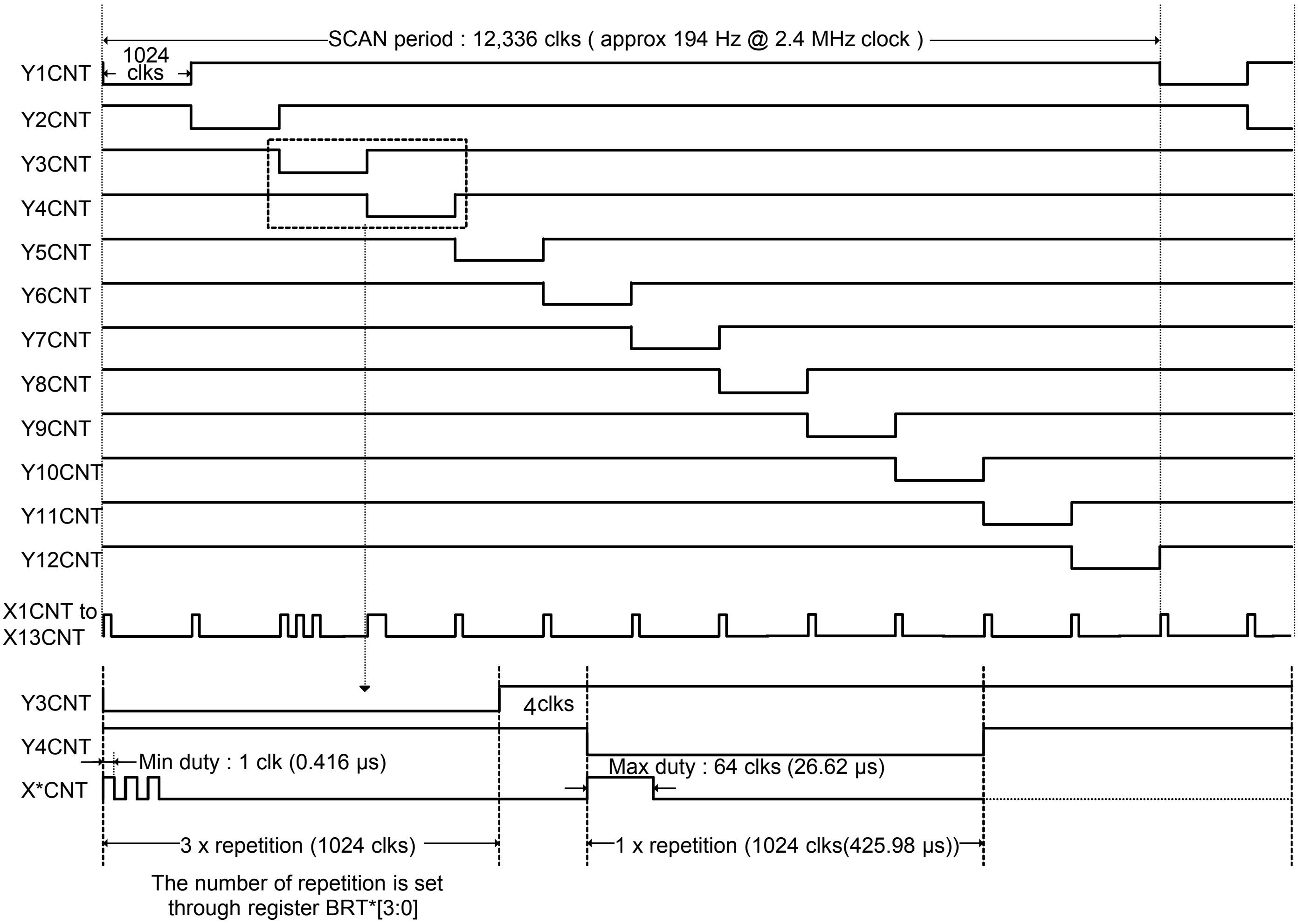


OPERATION (continued)

9. Block Configuration of Matrix LED (continued)

9.3 Timing Chart when in operation

- The figure below shows a timing chart when in operation.
- Timing can be controlled according to the external clock frequency input to CLKIO pin.
- In default condition, it is controlled by internal 2.4 MHz clock.
- Y1 to 12CNT are scan timing which is turned on one at a time. The ON period of each pin is constant 1024 clks (425.98 μs) and includes the interval of 4 clks (1.664 μs).
- 144 LED (12 × 12 matrix) are controlled by X1 to 13CNT according to below figure.
- When Y*CNT = High, X*CNT = Low, the actual waveform of Z* is set to Hi-Z.



Duty can be set using register LED*DT [5:0] from registers 1Eh to 24h. The number of repetition can be set through register BRT*[3:0] from register 26h to 2Ch. Brightness can be increased by the duty and the number of repetition.

Established : 2012-02-07
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OPERATION (continued)

10. LED Driver Block Function

Functions Table for LED Driver

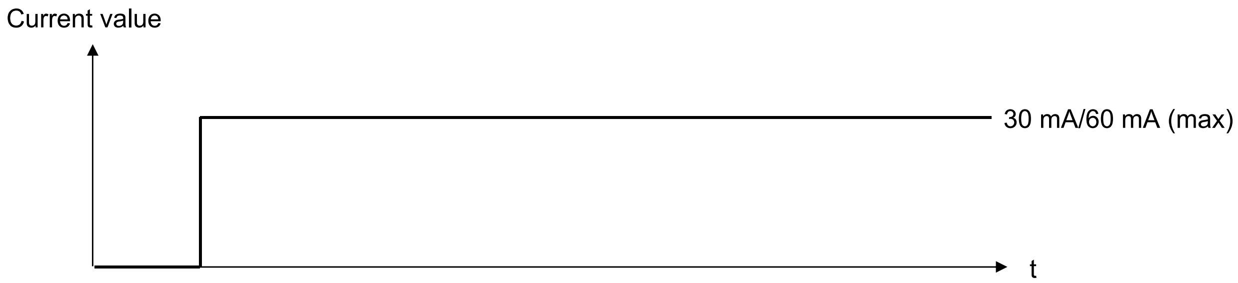
No.	Features	Setting Range
1	Constant current mode	IMAX Setting : 30 mA / 60 mA (max) IMAX Current Step : 2 mA / 4 mA (max) step
2	PWM mode and Fade-in/out mode	IMAX Setting : 30 mA / 60 mA (max) IMAX Current Step : 2 mA / 4 mA (max) step Adjustable detention Time for each step : (10.28 ms to 124 ms / step)
3	Firefly mode	Fixed Current at 100% Duty IMAX Setting : 30 mA / 60 mA (max) IMAX Current Step : 2 mA / 4 mA (max) step Adjustable detention Time for each step : (0.33 s to 3.96 s / step)
4	Melody mode	IMAX Setting : 30 mA / 60 mA (max) IMAX Current Step : 2 mA / 4 mA (max) step Each LED can synchronize with Music Input from CLKIO pin
5	Bar Meter Mode	IMAX Setting : 30 mA / 60 mA (max) IMAX Current Step : 2 mA / 4 mA (max) step Group LED can synchronize with Music Input from CLKIO pin Bar Meter Mode has more priority than Melody mode.
6	Scroll mode	IMAX Setting : 30 mA / 60 mA (max) IMAX Current Step : 2 mA / 4 mA (max) step Adjustable scroll time : (0.025 s to 0.2 s)

10.1 Constant Current Mode

Maximum current setting value can be set up as 30 mA or 60 mA using register IMAX[4:0] (register 03h).
Different current level can be set through the same register. (refer to page 22 for register 03h explanation).

Example:

If user sets register IMAX[4:0] (03h) = 01111 , current setting is setup as 30 mA max
If user sets register IMAX[4:0] (03h) = 01010 , current setting is setup as 20 mA max
If user sets register IMAX[4:0] (03h) = 11111 , current setting is setup as 60 mA max
If user sets register IMAX[4:0] (03h) = 11010 , current setting is setup as 40 mA max



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OPERATION (continued)

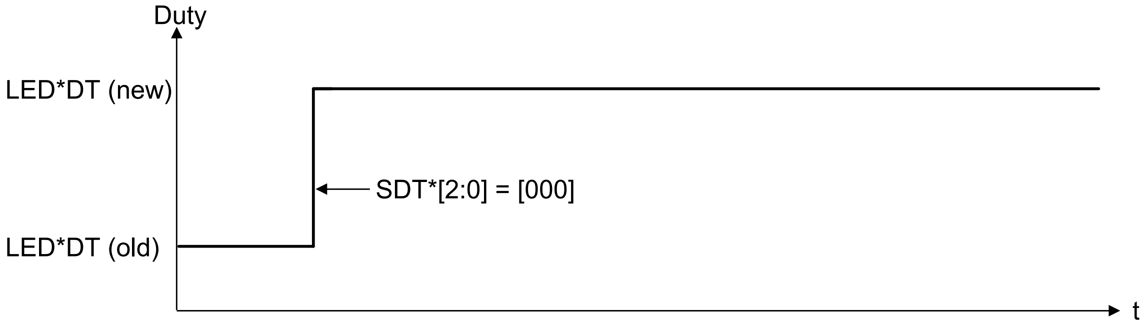
10. LED Driver Block Function (continued)

10.2 PWM Mode and Fade-in/out Mode

This operation is characterized by PWM signal having variable duty depending on register LED*DT [5:0] (registers 1Eh to 24h). However, any changes in duty is not instantaneous, but rather it will step to the new duty at time determined by register SDT*[2:0].

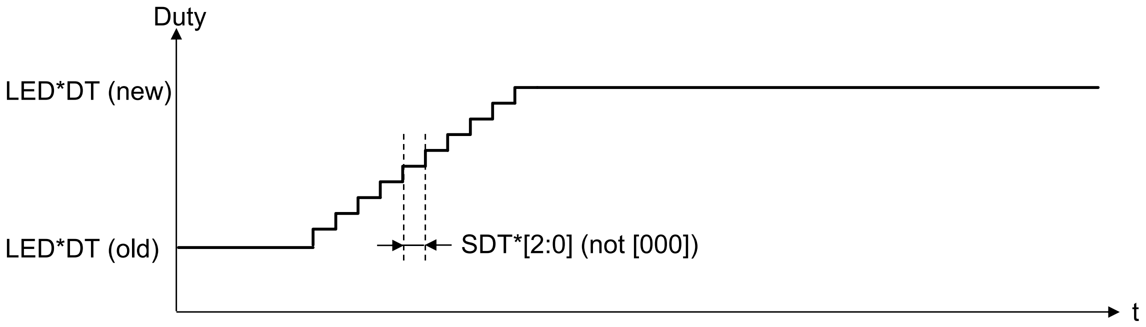
Example:

Case 1 : LED*DT (new) > LED*DT (old) (PWM Mode without Fade in/out control)



In Case 1, PWM duty has been changed from low to high duty. But the register SDT*[2:0] setting is [000] meaning there is no Fade in/out control. Therefore, PWM duty changes instantaneously. Users can see that LED becomes brighter instantaneously after PWM duty has been changed.

Case 2 : LED*DT (new) > LED*DT (old) (PWM Mode with Fade in control)



In Case 2, PWM duty has also been changed from low to high duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 2. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade in control. Users can see that LED becomes brighter slowly according to the timing set in register SDT*[2:0].

Established : 2012-02-07
Revised : 2014-09-01

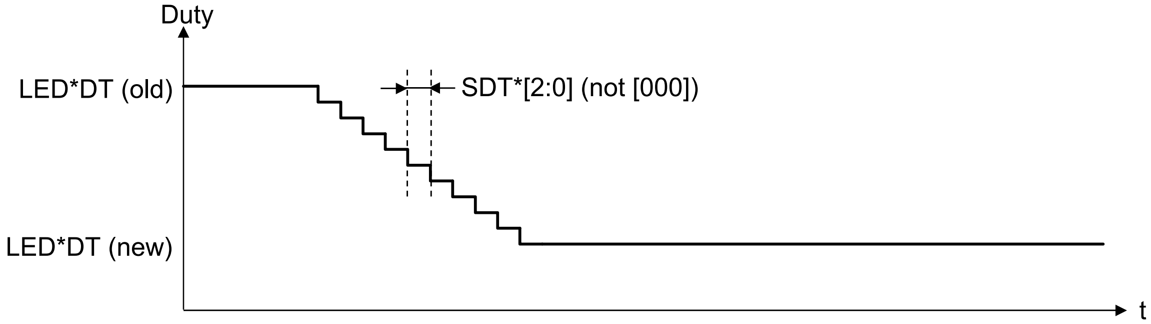
OPERATION (continued)

10. LED Driver Block Function (continued)

10.2 PWM Mode and Fade-in/out Mode (continued)

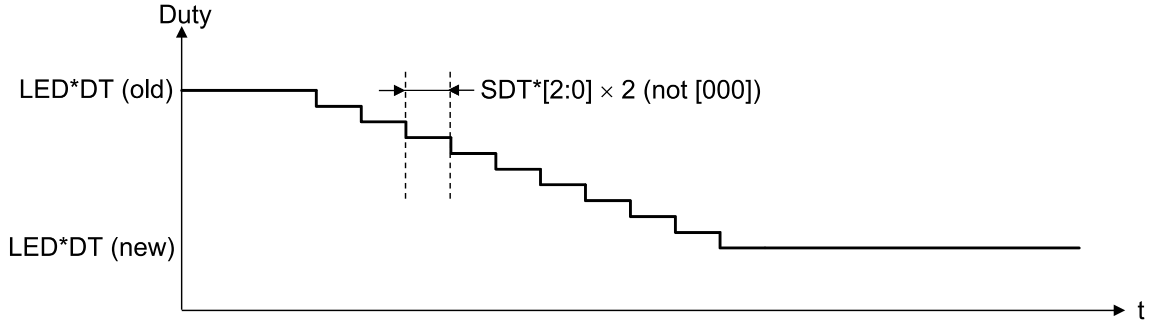
Example) (continued)

Case 3 : LED*DT (new) < LED*DT (old), FADTIM = [0] (PWM Mode with Fade out control)



In Case 3, PWM duty has been changed from high to low duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 3. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade out control. Users can see that LED becomes dimmer slowly according to the timing set in register SDT*[2:0].

Case 4 : LED*DT (new) < LED*DT (old), FADTIM = [1] (PWM Mode with Fade out control)



In Case 4, PWM duty has also been changed from high to low duty. Unlike in case 3, the register FADTIM is not [0]. Again, the register SDT*[2:0] setting is also not [000] in case 4. PWM duty has changed according to the register SDT*[2:0] setting. Users can see that LED becomes dimmer slowly. It is slower than Case3 as FADTIM register is high (2 times slower than Case 3 Fade out control).

LED*DT is set through register 1Eh to 24h. FADTIM is set through register 1Dh. SDT * [2:0] is set through register 26h to 2Ch.

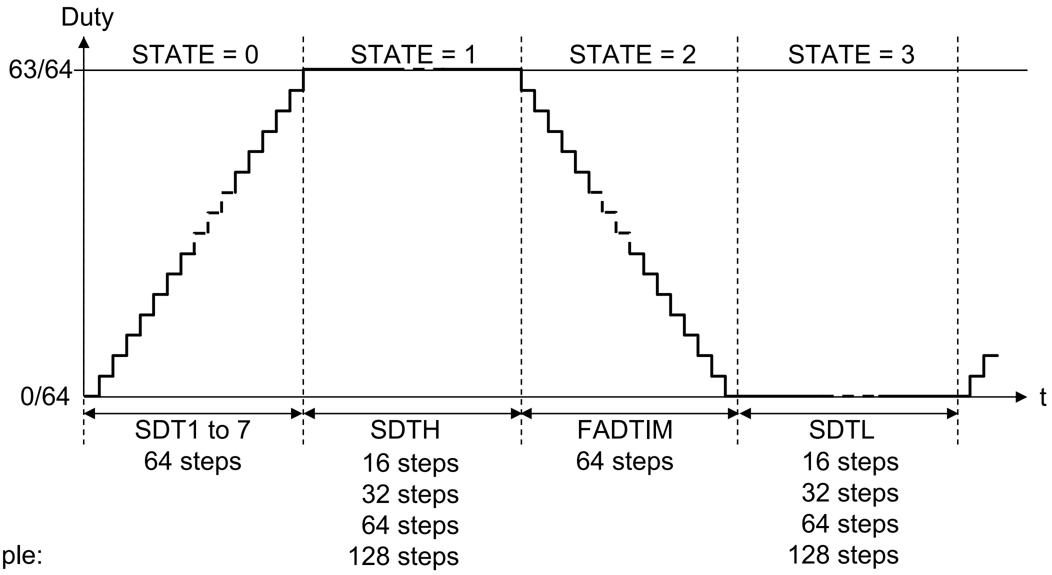
Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

10. LED Driver Block Function (continued)

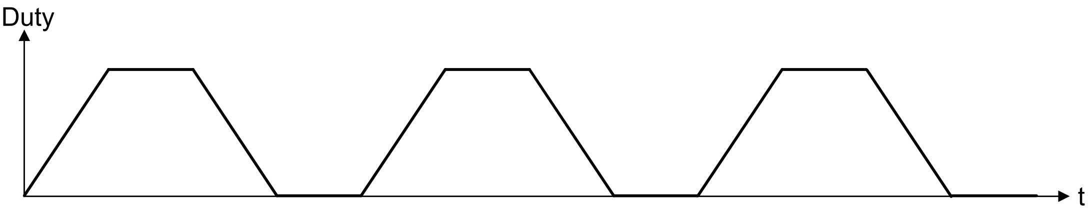
10.3 Firefly control

This operation is characterized by PWM signal cycling from minimum to maximum duty and vice versa with auto repeat function at time step determined by register SDT*[2:0]. Unlike PWM Fade in/out mode, firefly is auto repetition of the sequence and thus creating LED blinking function effect.

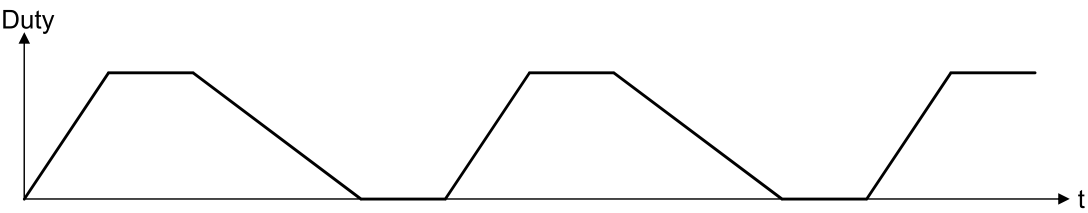


Example:

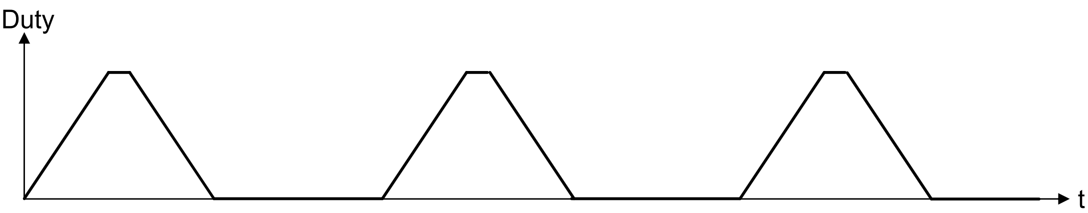
Example 1 : SDTH = [00] (SDT × 1), SDTL = [00] (SDT × 1), FADTIM = [0] (SDT × 1)



Example 2 : SDTH = [00] (SDT × 1), SDTL = [00] (SDT × 1), FADTIM = [1] (SDT × 2)



Example 3 : SDTH = [01] (SDT × 0.25), SDTL = [11] (SDT × 2), FADTIM = [0] (SDT × 1)



The SDTH[1:0], FADTIM and SDTL[1:0] setting is true for all PWM drivers. SDT*[2:0] registers are set individually for each driver. FADTIM is set through register 1Dh. SDTH[1:0] and SDTL[1:0] is set through register 25h. SDT*[2:0] is set through register 26h to 2Ch. The combinations of SDTH, SDTL and FADTIM are possible.

Established : 2012-02-07
Revised : 2014-09-01

OPERATION (continued)

10. LED Driver Block Function (continued)

10.4 Melody Mode explanation

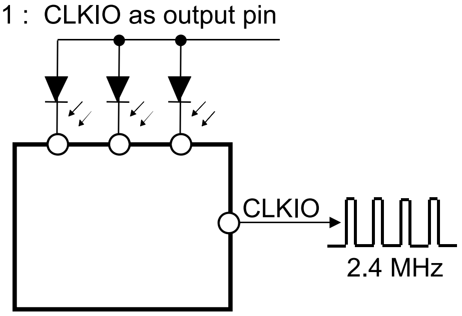
Melody mode is to synchronize LED to external music signal. Melody mode can be set through register MTXMODE[1:0] from register 04h. Each of the 144 LED matrix can be individually enabled for external music synchronization through register data (address 06h to 17h when register 05h is 01h).

External Music Signal can be injected from CLKIO pin. CLKIO pin serve as both input and output. CLKIO pin can output internal oscillator frequency by using CLKOUT register (register 03h).

CLKIO pin can be used as input for external signal by using EXTCLK register (register 03h). Internal clock frequency is typically 2.4 MHz. When IC is operating in I^{2}C mode, it is advisable to use external clock frequency from 1.2 MHz to 4.8 MHz . When IC is operating in SPI mode, it is advisable to use external clock frequency from 2 MHz to 4.8 MHz .

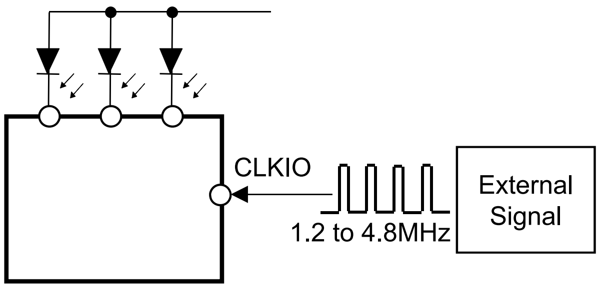
Please do not set MTXMODE = [10] (Melody Mode), EXTCLK = [1] and CLKOUT = [1] at the same time.
In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Case 1 : CLKIO as output pin



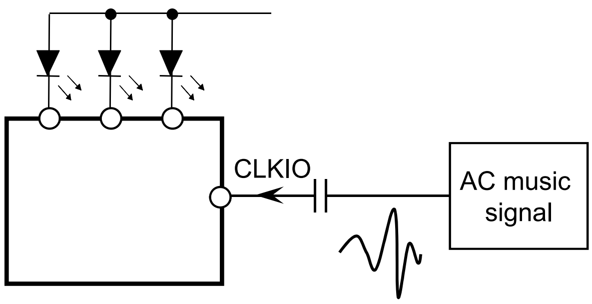
CLKIO output internal frequency by using CLKOUT register

Case 2 : CLKIO as input for external clock



CLKIO uses as external input by using EXTCLK register

Case 3 : CLKIO as input for music signal during melody mode



CLKIO uses as music input when melody mode is enabled by register MTXMODE [1:0].

Note : If input CLKIO voltage is higher than VDD, there will be back flow current to VDD. Its current value can be calculated as below.

$$I_{BackFlow} = \frac{(V_{CLKIO} - 0.7\ V - V_{DD})}{393\ k\Omega}$$

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OPERATION (continued)

10. LED Driver Block Function (continued)

10.4 Melody Mode explanation (continued)

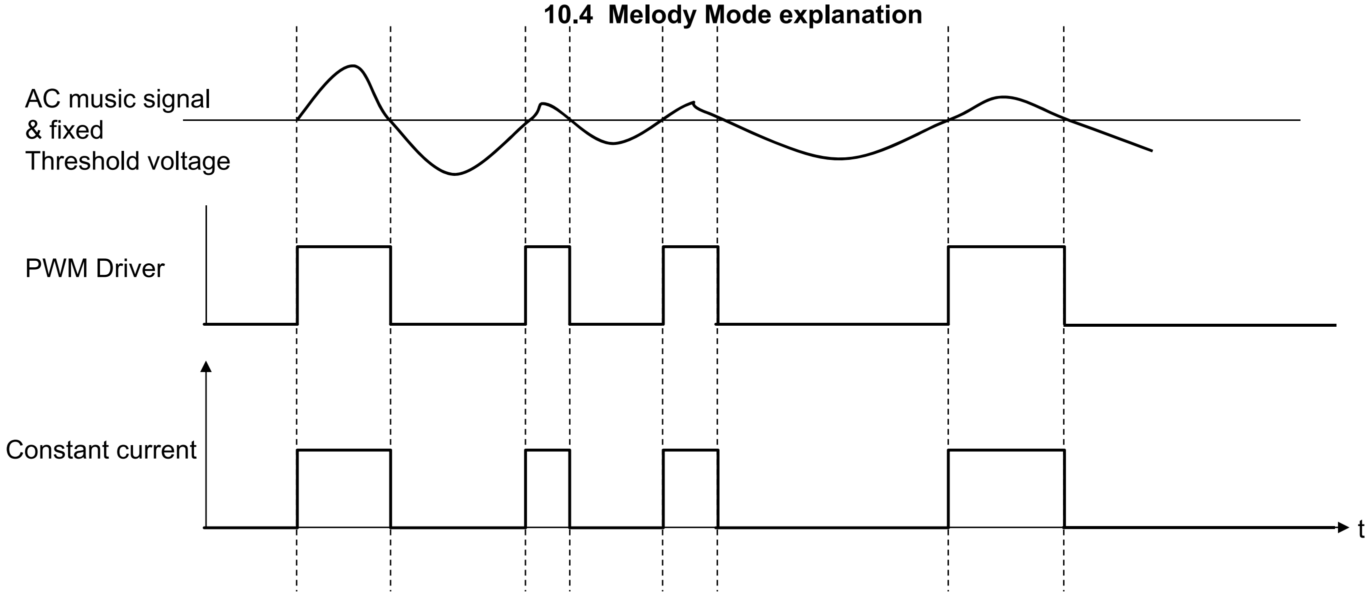
AC music signal input from CLKIO pin will be compared with internal threshold setting. Based on the comparison of music signal and threshold voltage, PWM driver control will change and control the LED ON / OFF. Therefore, LED light on / off control will synchronize with music tempo while LED brightness will synchronize with music loudness.
There are two threshold mode, one is auto threshold and the other is fixed threshold mode.

There are 8 threshold voltage levels in this IC as defined in the register 18h (THOLD[7:0]). Auto threshold mode means that the 8 threshold voltages will be scanned automatically from the lowest to highest threshold voltages at a fixed frequency higher than audio frequency. Input music signal will be compared with these scanning threshold voltages to control PWM Driver in order to have music synchronization effects. This mode allows user to easily use music synchronize function without having the trouble of manually setting the detection threshold. When melody mode is enabled, auto threshold mode will be the default mode.

Fixed threshold mode means that the threshold voltage is fixed at one threshold level. It can be set using register 18h (THOLD[7:0]). Input music signal will be compared with this fixed threshold voltage set by the user. During fixed threshold mode, do not set more than 1 register bit to logic "High" value at the same time. If user set more register bits to logic "High" after setting 1 register bit to “High”, system will only recognise the first "High" bit threshold that is set. In this mode, user can have the flexibility to configure different threshold voltage levels to achieve the desired LED music synchronizing visual effect according to the system music input level.

It is also advised that AC music signal peak to peak voltage to be at least 0.35 V and not more than 2.8 V.

10.4 Melody Mode explanation



Example of Fixed threshold mode

Brightness Compensation in Melody Mode

Additional brightness compensation in melody mode can be achieved by increasing or decreasing the turning on period of LED. Using brightness compensation register MLDCOM[2:0] (register 19h), LED turning on period can be controlled and LED can become brighter or dimmer.

This additional brightness compensation will be effective only in auto threshold mode. If fixed threshold mode is used, this register will not be able to control LED brightness.

Established : 2012-02-07
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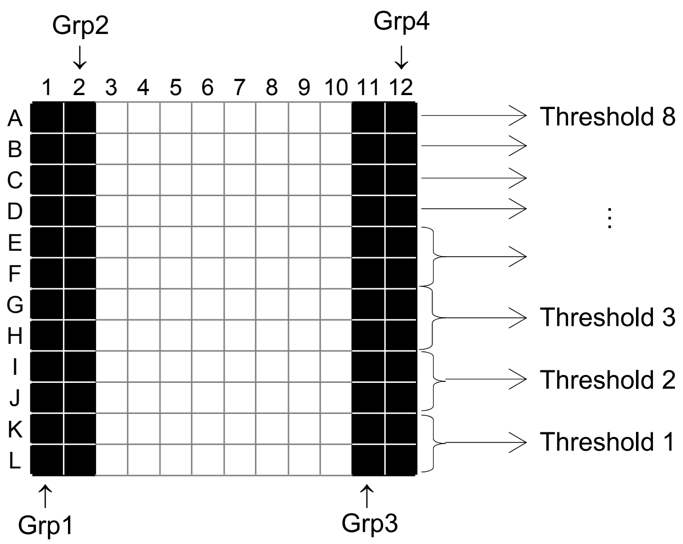
OPERATION (continued)

10. LED Driver Block Function (continued)

10.5 Bar Meter Mode explanation

Bar Meter Mode operation is another method of external melody mode wherein a group of LEDs are used instead of individual LED. Bar Meter Mode has higher priority than individual LED melody mode.



Given the above diagram, column 1 = group 1, column 2 = group 2, column B = group 3 and column C = group 4. Each group can be enabled through register GRP1 to 4 (address 19h). Each LED in the group must be enabled through Frame1 data register (address 06h to 17h, FRMSEL = 0).

The LED in the all groups will be synchronized to threshold signals Threshold 1 to 8 as follows:

Threshold Signal	Bar Meter Mode Group LED ON
Threshold 1	Row's K, L
Threshold 2	Row's I, J, K, L
Threshold 3	Row's G, H, I, J, K, L
Threshold 4	Row's E, F, G, H, I, J, K, L
Threshold 5	Row's D, E, F, G, H, I, J, K, L
Threshold 6	Row's C, D, E, F, G, H, I, J, K, L
Threshold 7	Row's B, C, D, E, F, G, H, I, J, K, L
Threshold 8	Row's A, B, C, D, E, F, G, H, I, J, K, L

All other LEDs not in Bar Meter Mode can operate in individual external melody mode.
During Bar Meter Mode, auto threshold detection should be used. This IC does not support Bar Meter Mode with fixed threshold setting. It is also recommended not to use other modes together with Bar Meter Mode for LED in group 1 to 4 (i.e. Grp1 to 4)

OPERATION (continued)

10. LED Driver Block Function (continued)

10.6 Scroll Mode explanation

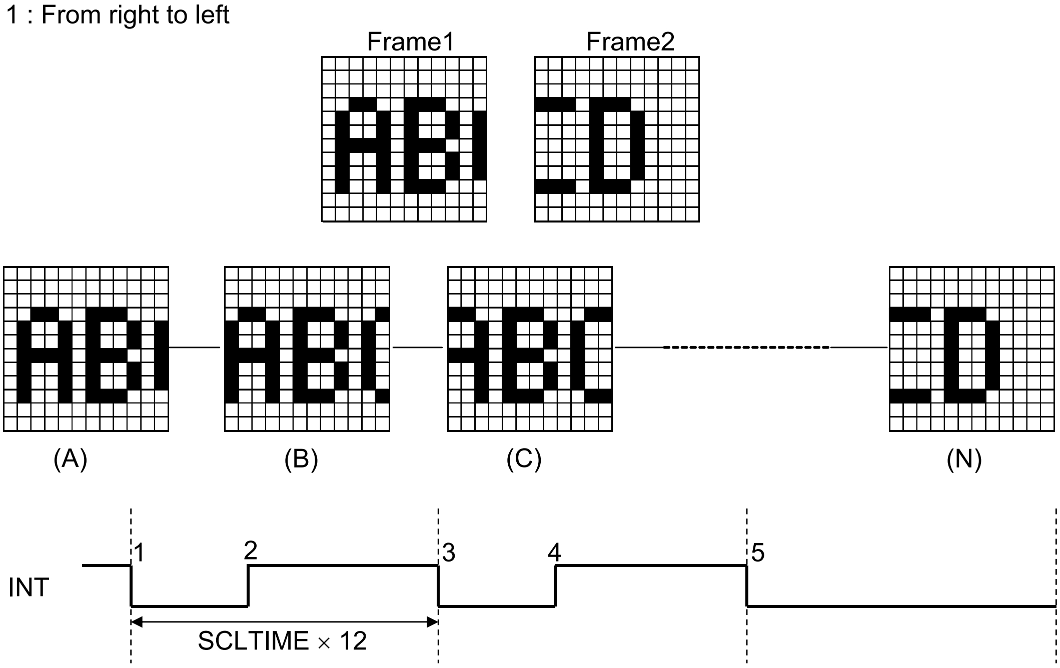
Scroll Mode can be set through MTXMODE [1:0] register (register 04h). The specified character can be scrolled for display from right to left or bottom to up using register LEFT or UP (register 75h).If both LEFT and UP registers are set [1], LEFT will have higher priority. Interrupt signal will be generated every time a full frame has been shifted and it will reflect at interrupt (INT) pin. Interrupt register (register 1Bh) should be unmasked. INT pin is an open drain connection and needs to be pulled up to VDD level.

The scroll time (SCLTIME) can be controlled by the setting of 76h register. The scroll time means the time that the display changes the (A) state to the (B) state, (B) to (C) state and so on (the display shifts one column) in the following figure (ex. LEFT scroll setting). In this IC, there are 12 columns in matrix display. Therefore, it needs 12 x SCLTIME timing to shift all the columns from Frame1 to Frame2 or vice versa. The initial default setting of scroll time is 0.025 s.

The below example shows how Frame1 and Frame2 data is scroll LEFT. First, User has to write data into Frame1 and Frame2. At the start of scroll operation, Frame1 is displayed (A). Interrupt will generate and INT pin will go low (at 1). User can write another data to Frame1 at that time. The data has to be written within 12 x SCLTIME timing (12 x 0.025sec for default) during the frame shifting. Once user finishes writing the data into Frame1, interrupt will clear and INT pin will go high (at 2). Scroll function will operate at the same timing of writing. For scrolling LEFT, the displayed data is shifted one position left and the right-most column is shifted with Frame2 column. This continues until the full Frame2 data is shifted in (N). Interrupt will generate again after Frame2 data is shifted in and INT pin will go low (at 3). User can now write another data to Frame2. The scrolling function will continue to display the new data from the Frame1. Once user finishes writing the data into Frame2, interrupt will clear and INT pin will go high again (at 4). During this writing, the display will continue shifting until new data of Frame 1 is shifted in. After all the new data of Frame1 is shifted in, interrupt will generate and INT pin will go low (at 5). If user does not write any data, INT will still low and scrolling function will repeat between the data of Frame1 and Frame 2 until Matrix and scroll mode is turned OFF. The same operation is also true for Scroll UP. The difference is that the displayed data is shifted one position up and the 1st row of Frame 2 is shifted at the bottom of the display.

Example:

Example 1 : From right to left



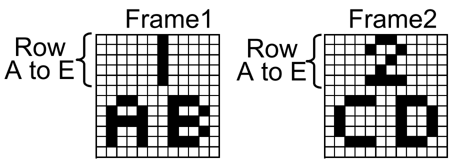
OPERATION (continued)

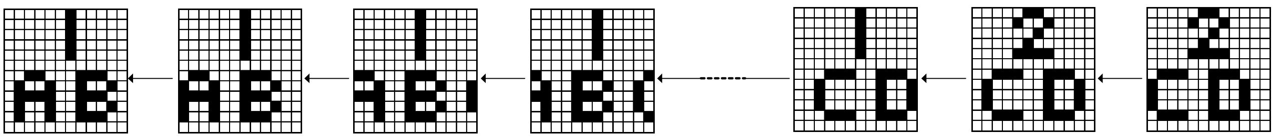
10. LED Driver Block Function (continued)

10.6 Scroll Mode explanation (continued)

Example: (continued)

Example 2 : Stop function





Scroll lower rows but Row A to E are stationary

After full frame 2 is shifted, Row A to E is updated

The stop function allows row A to E to be stationary during scroll mode (can be set using register 75h).
The shifting of stop row is done in one bulk at the end of each full frame. Row A to E stop function has individual controls hence combination of rows to stop is possible. Stop function is only valid if the direction selected is scroll LEFT. It has no effect if scroll direction is UP.

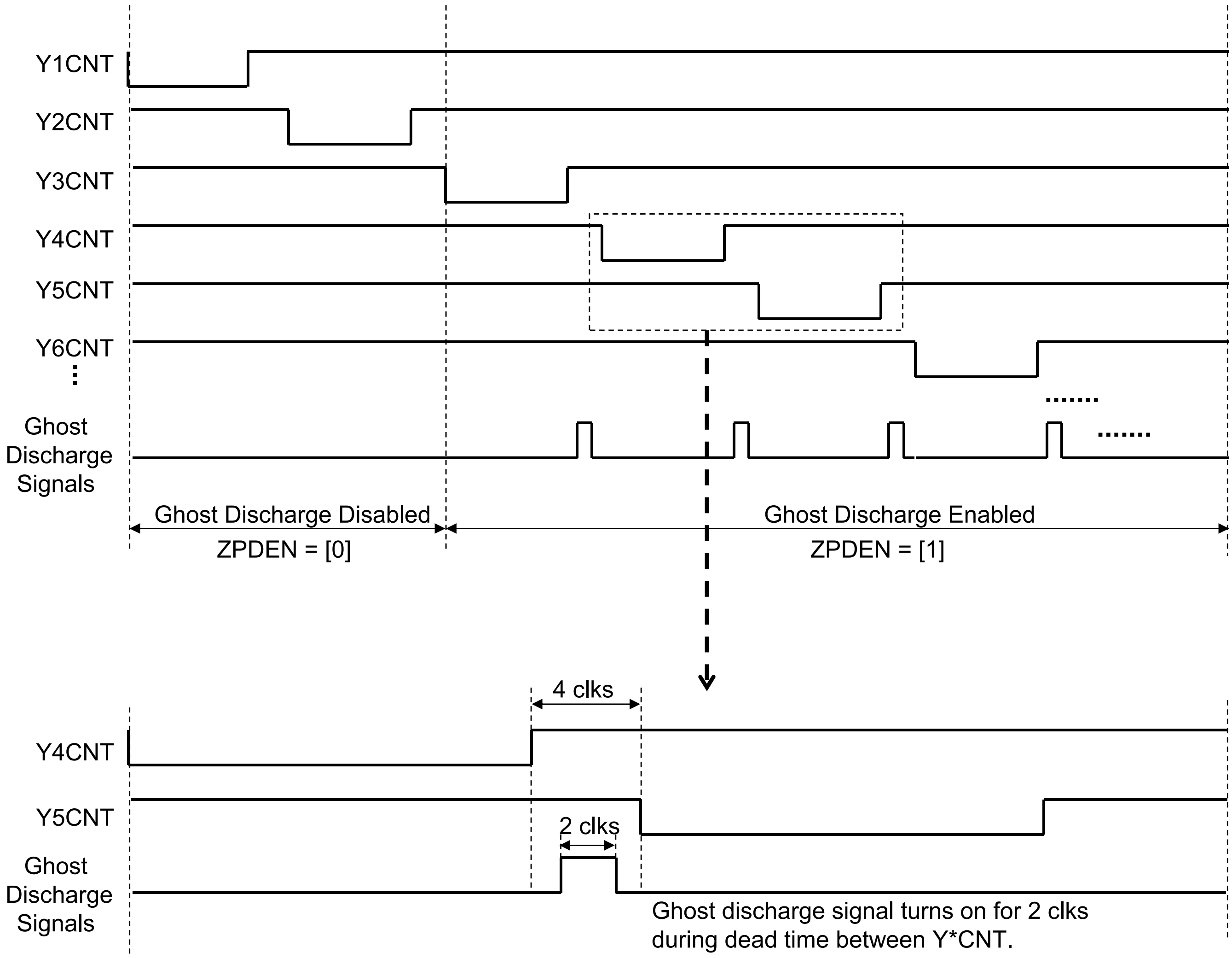
If stop register settings (register 75h) is changed during scroll operation, it will only take effect once the full frame has been shifted in. This prevents the character from mis-aligning. The same behavior is also true for direction registers UP and LEFT (register 75h).

OPERATION (continued)

11. Ghost Image Prevention Function

Ghost images sometimes appear during LED matrix mode operation. Very dim light can appear in some LED even during OFF condition. This is called Ghost Image. In this IC, Ghost Image Prevention Function is included to prevent Ghost Image. Ghost Image Prevention Function can be enabled through register ZPDEN (register 04h).

• Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method.



During normal operation, ghost discharge signal will be always low. When ghost image prevention function is enabled through register 04h, ghost discharge signal will turn on for 2 clks cycle during 4 clks dead time between each YCNT. During on period of 2 clks cycle, output Z* pin will be forced to half of V_{CC}.

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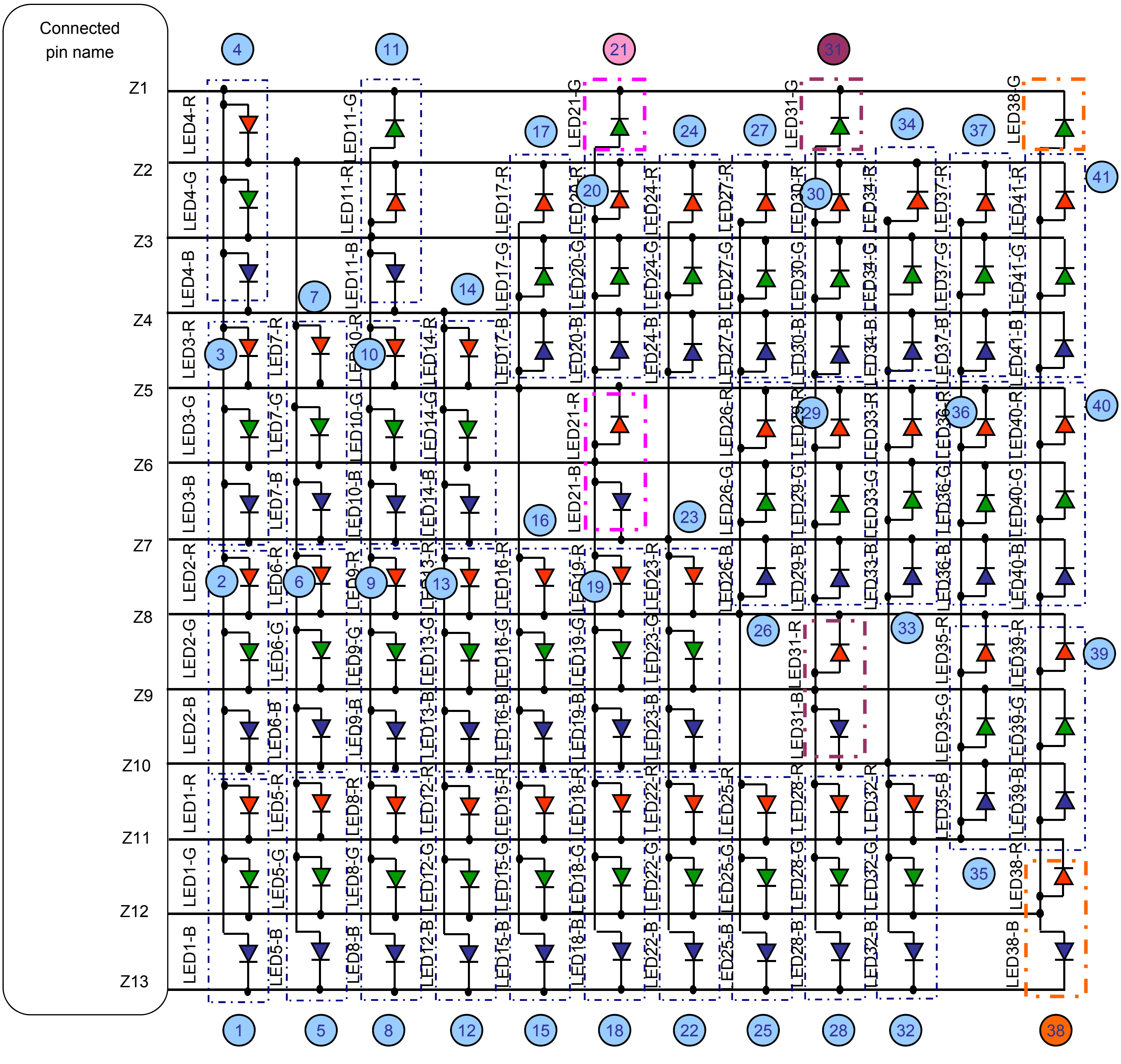
OPERATION (continued)

11. Ghost Image Prevention Function (continued)

To minimize ghost image, it is recommended to use LED with same forward voltage drop in LED panel. If user wants to use LED with different forward voltage drop in LED panel (e.g. RGB LED in LED panel), it is recommended that all the cathodes of LED connected to the same pin must have same forward voltage drop. (i.e. same color LED sharing the same cathode). A recommended RGB LED connection to minimize ghost image is shown in diagram below.



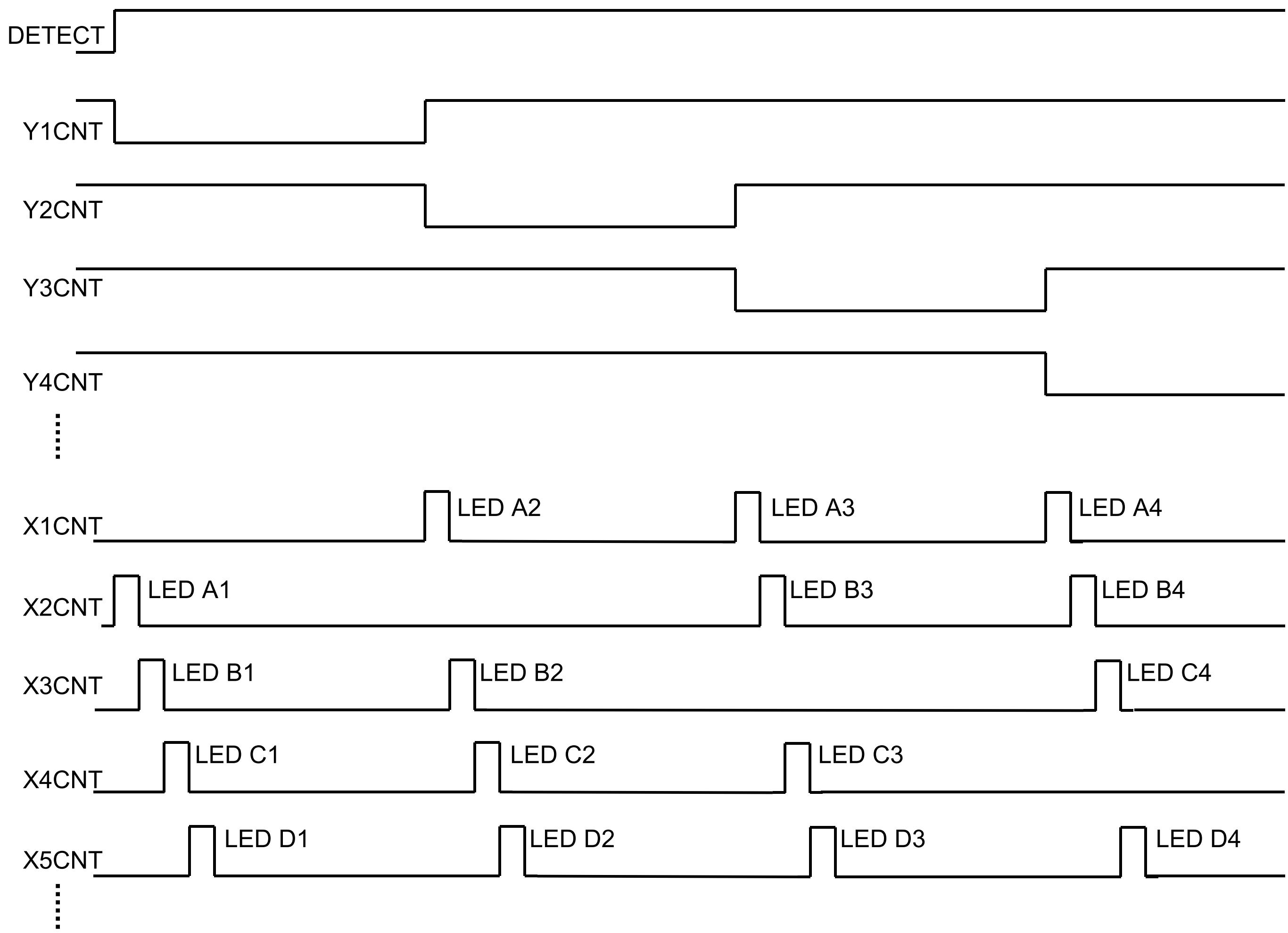
Example of RGB LED connection

OPERATION (continued)

12. Open / Short Detection Function

In this IC, Open or short condition of LED can be detected. This detection test is recommended to be used before IC is used for actual application.

Example)



Open/Short detection can be enabled through register DETECT (register 1Ch). First, set the LED current using register IMAX[4:0] (register 03h). (e.g. IMAX[4:0] = 10 mA [00101], It is recommended to use 10 mA for this test.). Second, select LED to test for open/short detection through register 2Dh to 74h. Lastly, enable open/short detection by register DETECT (register 1Ch).

When DETECT register is enabled (High), Y*CNT will scan for one time (from Y1CNT to Y12CNT). During Y*CNT turns on, all the X*CNT except the corresponding X*CNT will be scanned. (e.g. when Y1CNT turns on, X2 to X13CNT will scan but X1CNT will be low.) As shown above, individual LED is checked for open or short condition during the scan.

During X*CNT scan, output Z* terminal pins voltages will be compared with two reference voltages to determined whether LED is open or short. Open or short condition of LED can be read back by register 2Dh to 74h.

There are some procedures for this test as well as system limitations to this open / short detection function.

OPERATION (continued)

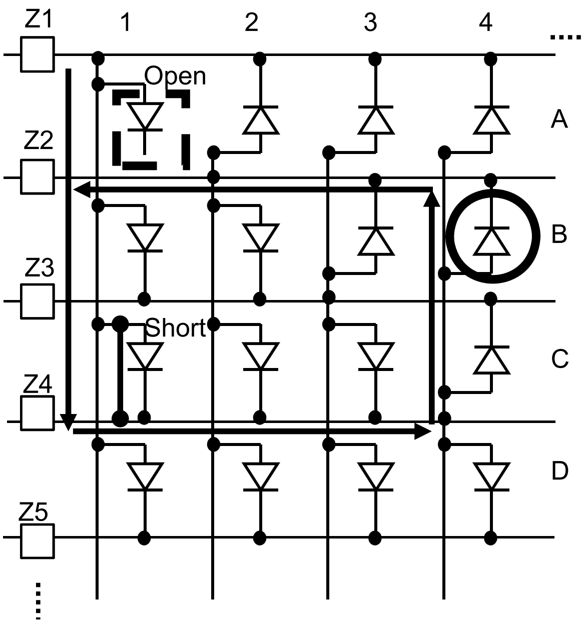
12. Open / Short Detection Function (continued)

System limitation to open / short detection function

Condition 1 : (Short + Open condition : System only detect short condition)

When there are both short and open condition in the system, the system will only detect short condition. Open condition will not be reflected.

Example)



In the figure on the left, A1 LED is open and C1 LED is short. System will only detect as C1 LED is shorted.

The current flow from Z1 to Z2 through shorted path (C1 LED) and B4 LED (LED in circle) instead of flowing through A1 LED during open / short check for A1 LED (as indicated in the arrow lines). Therefore, A1 LED will reflect as normal.

During open/short check for C1 LED, system will detect that C1 LED is shorted.

Therefore, if there is any short LED condition in the column, open condition in the same column cannot be detected.

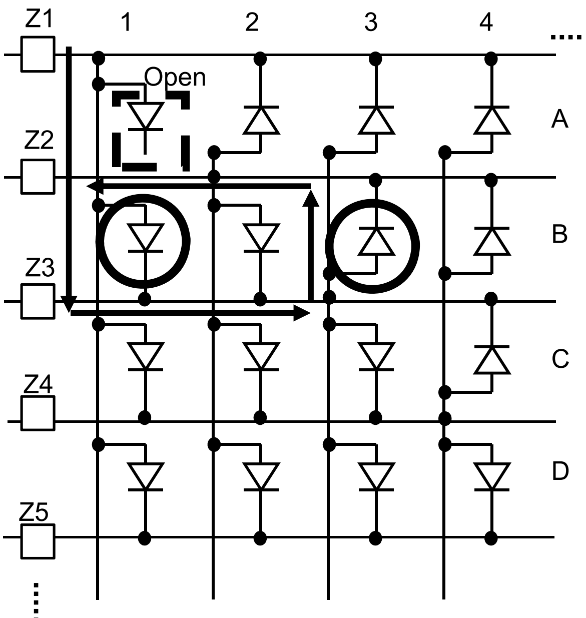
*Action Items :

It is recommended to run open / short detection for minimum two times when short condition is detected. Users should solve the short LED condition after first run before checking for open LED another time.

Condition 2 : (Open condition : System cannot detect open LED as $V_{CC} > 2 \times$ LED VF Drop)

If V_{CC} is higher than 2 × LED VF drop during open/short testing, system cannot detect open condition.

Example:



In the figure on the left, A1 LED is open. But the system cannot detect A1 LED open condition if V_{CC} is higher than two times of LED VF drop (forward voltage drop of LED).

When V_{CC} is higher than two times of LED VF drop, the current can flow from Z1 to Z2 through B1 LED and B3 LED (LED in circles) instead of flowing through A1 LED during open/short check for A1 LED (as indicated in the arrow lines). Therefore, A1 LED will reflect as normal.

*Action Items :

It is recommended to use V_{CC} less than two times of LED VF drop. Typical V_{CC}, 3.6 V is recommended to use for this IC during open/short detection testing.

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OPERATION (continued)

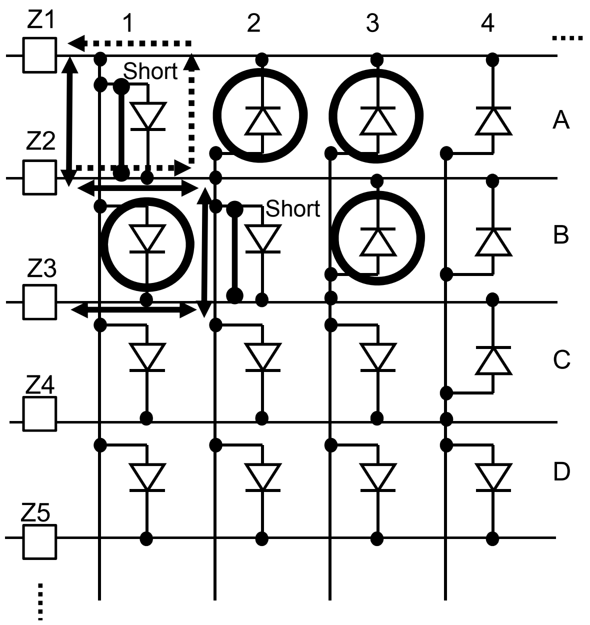
12. Open / Short Detection Function (continued)

System limitation to open / short detection function (continued)

Condition 3 : (Any of non cross-plex LED is shorted, cross-plex LED will also reflect as shorted)

When there is short condition in any of non cross-plex LED in the system, the system will also detect cross-plex LED as short condition even though it is not shorted. Moreover, system will detect additional short LED during some condition. Refer to below example for such case.

Example:



In the figure on the left, only A1 and B2 LED are shorted. But system will reflect that both A1, A2, A3, B1, B2 and B3 LED are shorted.

The current flow from Z2 to Z1 through shorted path (A1 LED as shown in dotted arrow lines) instead of flowing through A2 LED during open/short check for A2 LED. Therefore, A2 LED will reflect as short condition even though they are not shorted. (B3 LED will reflect as short condition in the same manner as A2 due to B2 LED is shorted.)

A3 LED will reflect as short condition due to A1 and B2 LED are shorted. The current will flow from Z3 to Z1 through shorted path (A1 and B2 LEDs as shown in arrow lines) instead of flowing through A3 LED during open/short check for A3. Therefore, A3 LED will reflect as short even through it is not shorted.

B1 LED will reflect as short condition due to A1 and B2 LED are shorted. The current will flow from Z1 to Z3 through shorted path (A1 and B2 LEDs as shown in arrow lines) instead of flowing through B1 LED during open/short check for B1. Therefore, B1 LED will reflect as short even through it is not shorted.

*Action Items :

It is recommended that Users should check all individual short LED after the system reflect more than one short condition.

Note:

In this IC, the minimum LED driver voltage to keep constant current value is 0.4 V and the worst case for scan switch impedance is 2 Ω. It is advised to calculate necessary V_{CC} voltage with the type of LED to be used using the following equation:

$$V_{CC} - 2 \times IOUT - VFLED > 0.4\ V$$

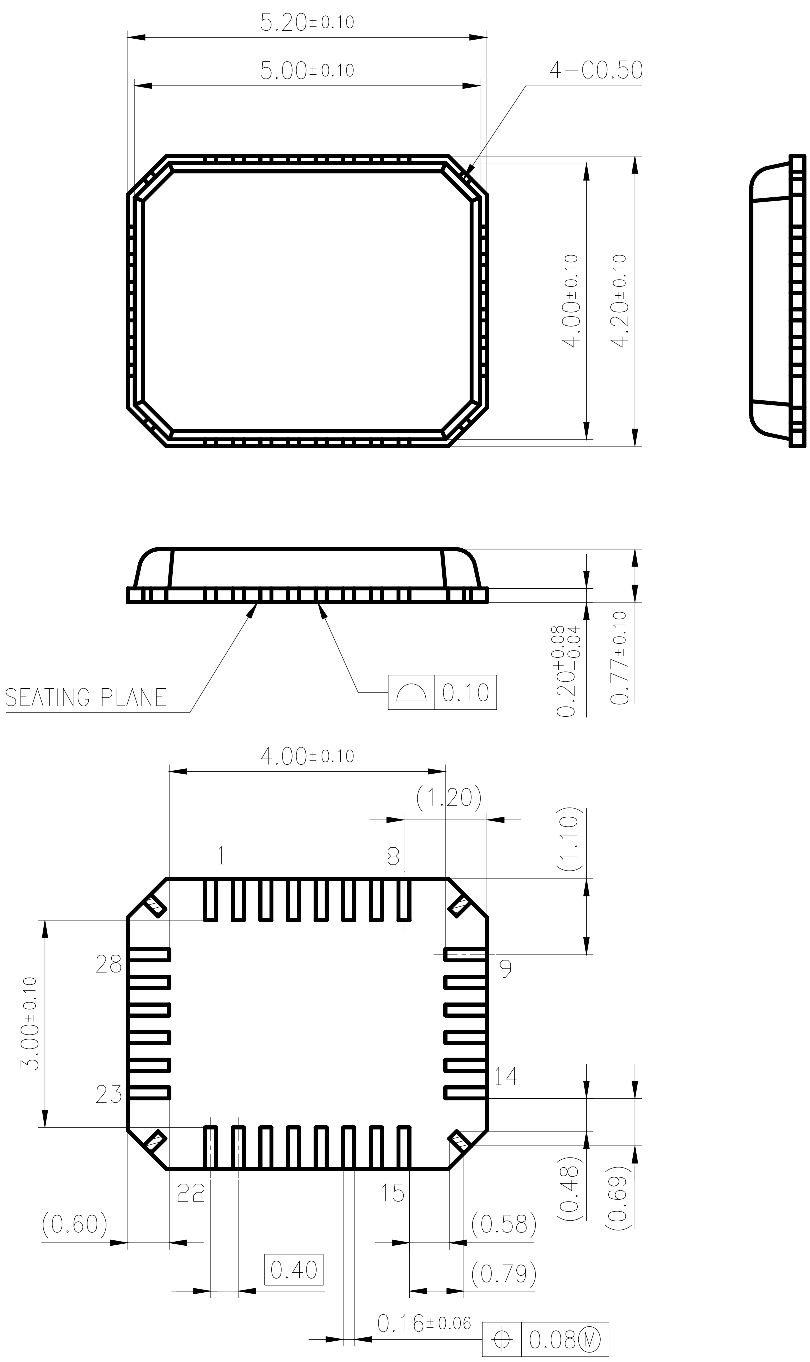
During open/short detection test, any voltage less than 0.15 V will be detected as open condition and any voltage larger than V_{CC} – 0.3 V will be detected as short condition. Therefore, LED current has to be set such that Z pin terminal voltages are within 0.15 V to V_{CC} – 0.3 V. For example, LED current is set at 10 mA (IMAX = 00101) which is the recommended value to use for this test.

As mentioned in system limitation condition two, it is recommended to use typical V_{CC} (3.6 V). With the forward voltage of LED (VFLED) to be used, LED current (IOUT) can be calculated. E.g. if VFLED is 3.15 V and V_{CC} is 3.6 V, using above equation, LED current (IOUT) has to be less than 25 mA.

PACKAGE INFORMATION (Reference Data)

Package Code : *QFN028-P-0405C

Unit:mm



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

Established : 2012-02-07
Revised : 2014-09-01

IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.

Established : 2012-02-07
Revised : 2014-09-01

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(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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Как с нами связаться

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