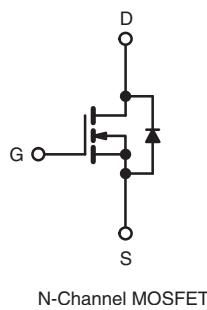
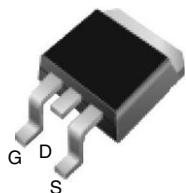


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V 1.2
Q_g (Max.) (nC)	42
Q_{gs} (nC)	10
Q_{gd} (nC)	20
Configuration	Single

D²PAK (TO-263)


RoHS*
COMPLIANT
HALOGEN
FREE
Available

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Forward

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHFBC40AS-GE3	SiHFBC40ASTRL-GE3 ^a	SiHFBC40ASTRR-GE3 ^a
Lead (Pb)-free	IRFBC40ASPbF	IRFBC40ASTRLPbF ^a	IRFBC40ASTRRPbF ^a
	SiHFBC40AS-E3	SiHFBC40ASTL-E3 ^a	SiHFBC40ASTR-E3 ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^e	I_D	6.2	A
		3.9	
Pulsed Drain Current ^{a, e}	I_{DM}	25	
Linear Derating Factor		1.0	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	570	mJ
Repetitive Avalanche Current ^a	I_{AR}	6.2	A
Repetitive Avalanche Energy ^a	E_{AR}	13	mJ
Maximum Power Dissipation	P_D	125	W
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	6.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 29.6$ mH, $R_g = 25$ Ω , $I_{AS} = 6.2$ A (see fig. 12).
- $I_{SD} \leq 6.2$ A, $dI/dt \leq 88$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- Uses IRFBC40A, SiHFBC40A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

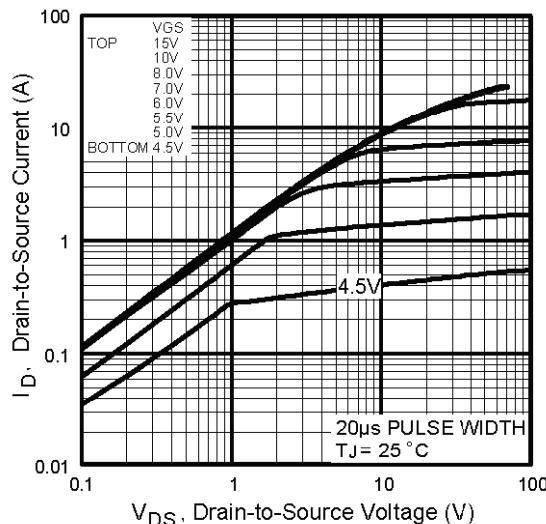
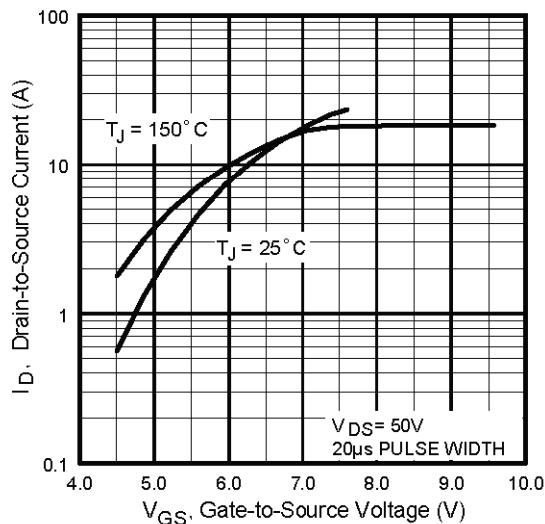
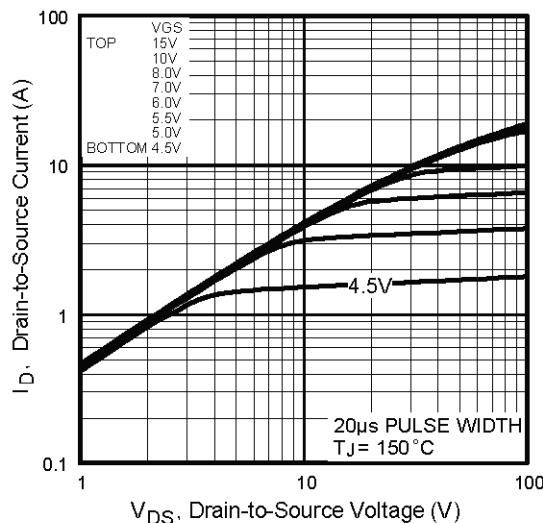
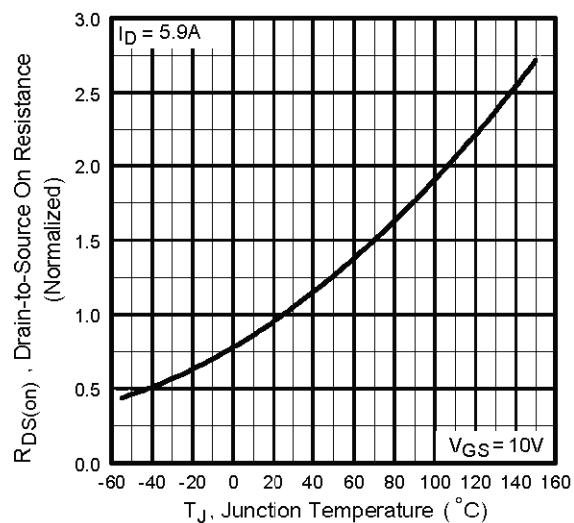
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	0.66	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V	
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{bss}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	25	μA	
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.7 A ^b	-	-	1.2	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3.7 A		3.4	-	-	S	
Dynamic								
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1036	-	pF	
Output Capacitance	C _{oss}			-	136	-		
Reverse Transfer Capacitance	C _{rss}			-	7.0	-		
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	1487	-	pF	
			V _{DS} = 480 V, f = 1.0 MHz	-	36	-		
Output Capacitance Effective	C _{oss eff.}		V _{DS} = 0 V to 480 V ^c	-	48	-		
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 6.2 A, V _{DS} = 480 V, see fig. 6 and 13 ^b	-	-	42	nC	
Gate-Source Charge	Q _{gs}			-	-	10		
Gate-Drain Charge	Q _{gd}			-	-	20		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 6.2 A, R _g = 9.1 Ω, R _D = 47 Ω, see fig. 10 ^b		-	13	-	ns	
Rise Time	t _r			-	23	-		
Turn-Off Delay Time	t _{d(off)}			-	31	-		
Fall Time	t _f			-	18	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.2	A	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	25		
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 6.2 A, V _{GS} = 0 V ^b		-	-	1.5	V	
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 6.2 A, dI/dt = 100 A/μs ^b		-	431	647	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.8	2.8	μC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}.
- d. Uses IRHFBC40A/SiHFBC40A data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

IRFBC40AS, SiHFBC40AS

Vishay Siliconix

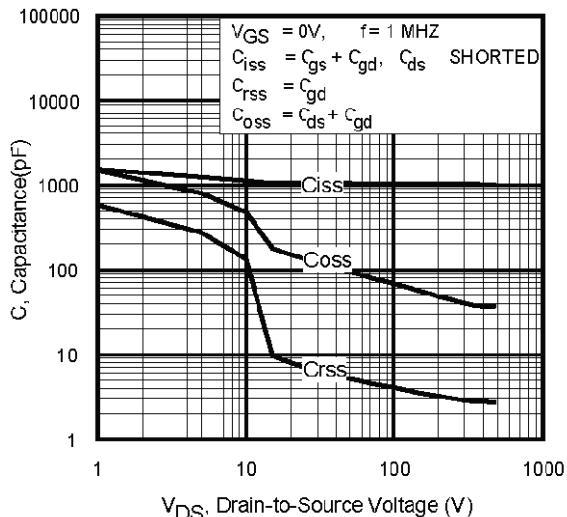


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

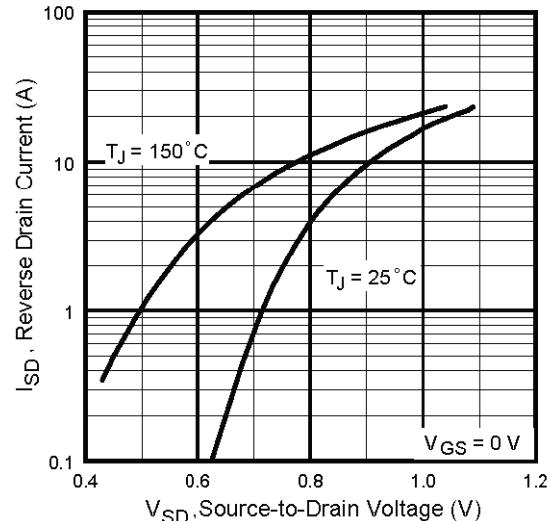


Fig. 7 - Typical Source-Drain Diode Forward Voltage

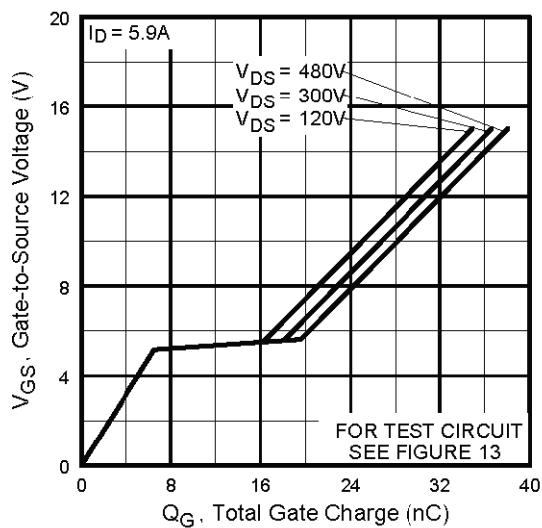


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

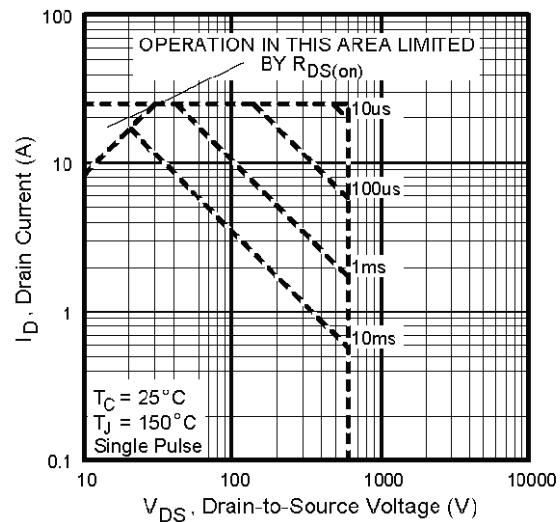


Fig. 8 - Maximum Safe Operating Area

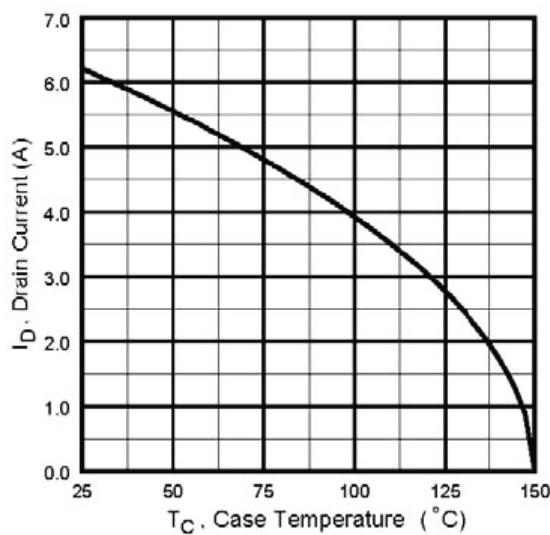


Fig. 9 - Maximum Drain Current vs. Case Temperature

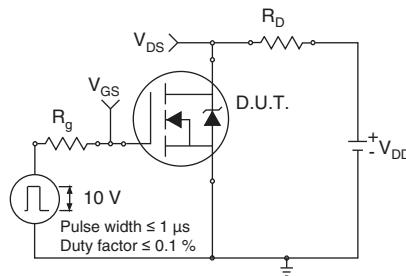


Fig. 10a - Switching Time Test Circuit

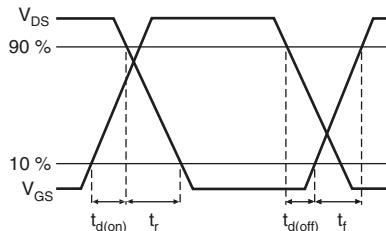


Fig. 10b - Switching Time Waveforms

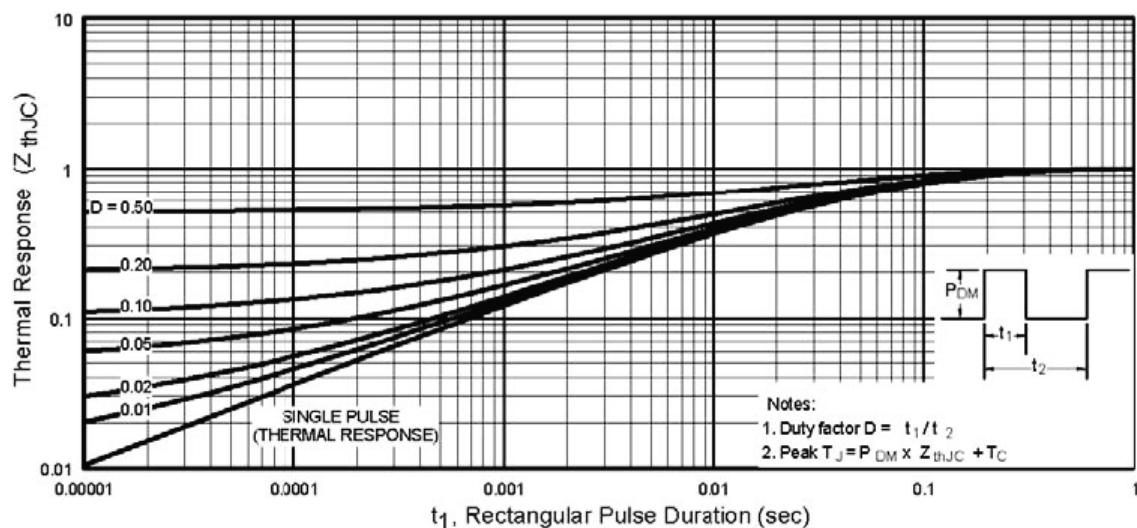


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

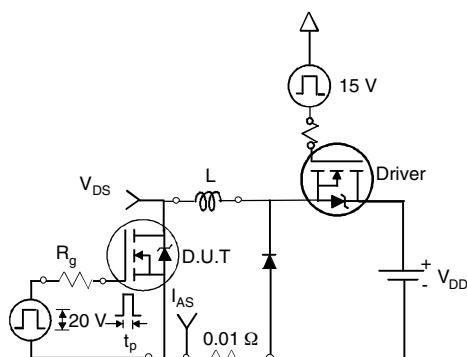


Fig. 12a - Unclamped Inductive Test Circuit

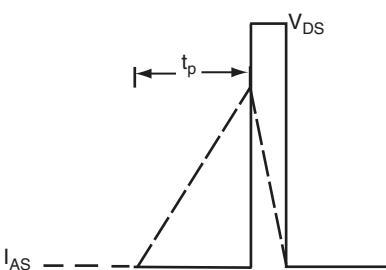


Fig. 12b - Unclamped Inductive Waveforms

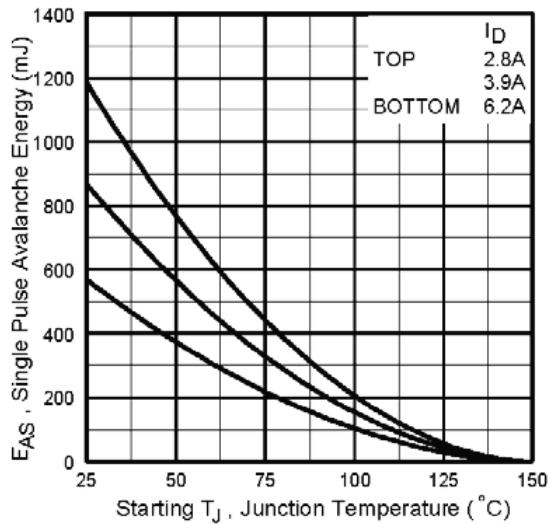


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

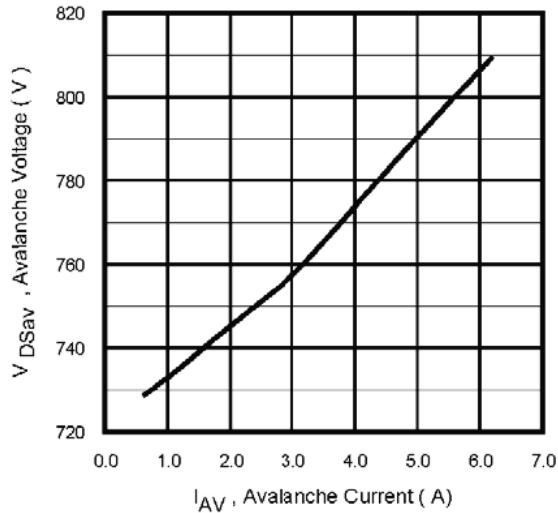


Fig. 12d - Maximum Avalanche Energy vs. Drain Current

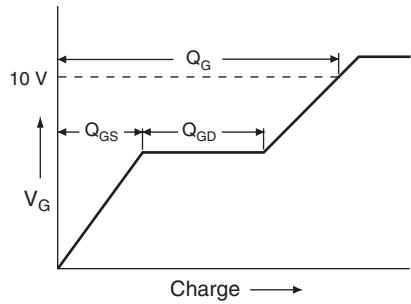


Fig. 13a - Basic Gate Charge Waveform

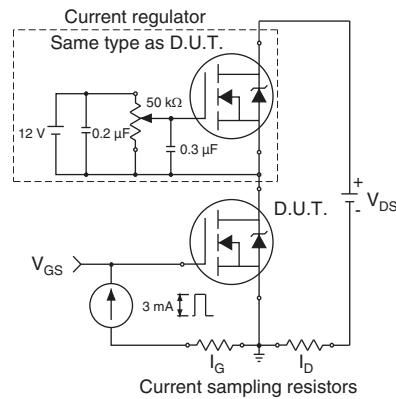
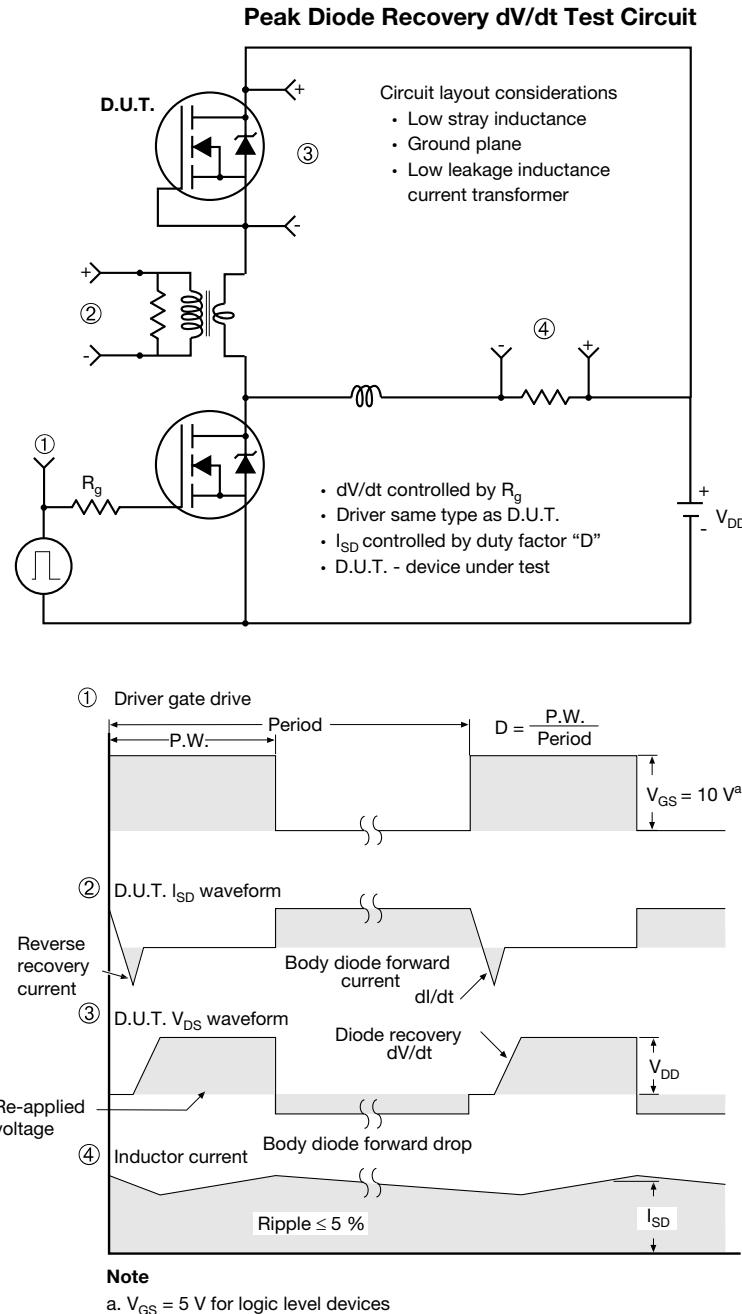


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)

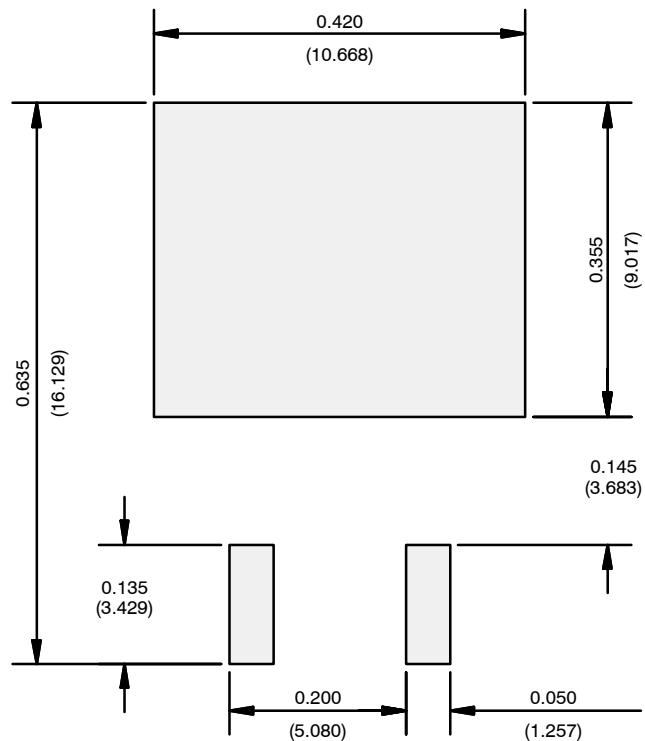


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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