Power supply IC series for TFT-LCD panels

12V Input Multi-Channel System Power Supply IC

BM81110MUW

General Description

BM81110MUW is a system power supply for TFT-LCD panels used for liquid crystal TVs. This IC is incorporated with Negative and Positive charge pump controllers and Gate Pulse Modulation (GPM) function. It also features built-in EEPROM to contain each setting voltage, soft start time, etc.

Features

- Step-up DC/DC converter (AVDD) (Synchronous rectification, built-in load switch)
- Step-down DC/DC converter 1 (VIO) (Non-synchronous rectification)
- Step-down DC/DC converter 2 (VCORE) (Synchronous rectification)
- Step-down DC/DC converter 3 (HAVDD) (Synchronous rectification)
- Positive charge pump controller (VGH)
- Negative charge pump controller (VGL)
- Gate Pulse Modulation (GPM) function
- Output voltage control by I2C
- Built-in EEPROM
- Switching Frequency 750kHz (AVDD, VIO)
- Switching Frequency 1MHz (VCORE, HAVDD)

Applications

- TFT-LCD panel

Key Specifications

- Input voltage range : 8.6V to 14.7V
- AVDD Output voltage range : 13.5V to 19.8V
- VIO Output voltage range : 2.2V to 3.7V
- VCORE Output voltage range : 0.8V to 3.3V
- HAVDD Output voltage range : 4.8V to 11.1V
- VGH Output voltage range : 20V to 35V
- VGL Output voltage range : -14.5V to -5.5V
- Switching Frequency : 750kHz(Typ) 1MHz(Typ)
- Operating temperature range : -40℃ to +85℃

Package

	W(Typ) x D(Typ) x H(Max)
VQFN40W6060A	6.00mm x 6.00mm x 0.8mm

Typical Application Circuit（TOP VIEW）

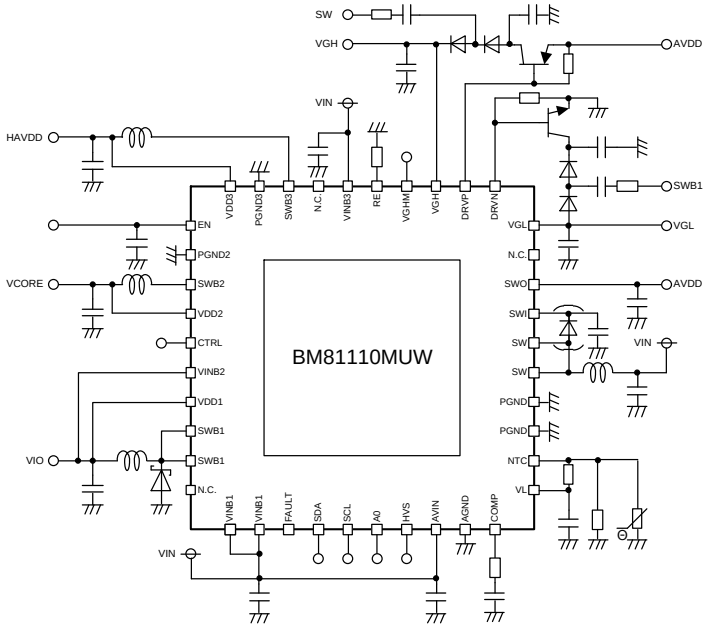


Figure1. Application Circuit

Contents

Pin Configuration (TOP View)

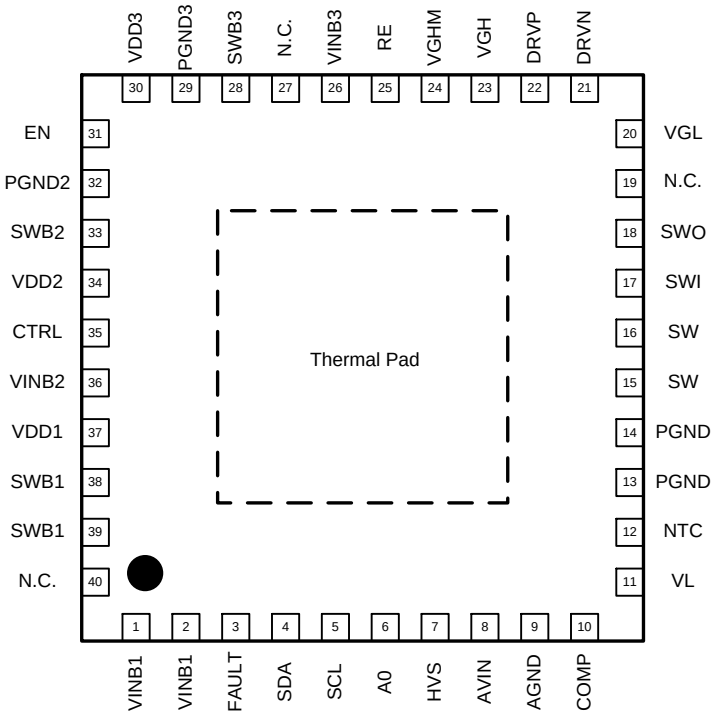


Figure 2. Pin Configuration

Pin Description

PIN No.	SYMBOL	FUNCTION	PIN No.	SYMBOL	FUNCTION
1	VINB1	Step-down DC/DC power supply input 1	21	DRVN	Negative charge pump drive pin
2	VINB1	Step-down DC/DC power supply input 1	22	DRVP	Positive charge pump drive pin
3	FAULT	FAULT signal output	23	VGH	Positive charge pump output
4	SDA	Serial data input	24	VGHM	GPM output
5	SCL	Serial clock input	25	RE	GPM Slope adjustment pin
6	A0	I2C address select pin	26	VINB3	Step-down DC/DC power supply input 3
7	HVS	HVS mode select pin	27	N.C.	—
8	AVIN	Power supply input	28	SWB3	Step-down DC/DC switching pin 3
9	AGND	Analog ground	29	PGND3	Step-down DC/DC ground 3
10	COMP	Error amplifier output	30	VDD3	Step-down DC/DC output 3
11	VL	Internal REG output	31	EN	Enable input
12	NTC	Thermistor connecting pin	32	PGND2	Step-down DC/DC ground 2
13	PGND	Step-up DC/DC ground	33	SWB2	Step-down DC/DC switching pin 2
14	PGND	Step-up DC/DC ground	34	VDD2	Step-down DC/DC output 2
15	SW	Step-up DC/DC switching pin	35	CTRL	GPM control pin
16	SW	Step-up DC/DC switching pin	36	VINB2	Step-down DC/DC power supply input 2
17	SWI	Load switch input	37	VDD1	Step-down DC/DC output 1
18	SWO	Load switch output	38	SWB1	Step-down DC/DC switching pin 1
19	N.C.	—	39	SWB1	Step-down DC/DC switching pin 1
20	VGL	Negative charge pump output	40	N.C.	—

Block Diagram (VGH Doubler)

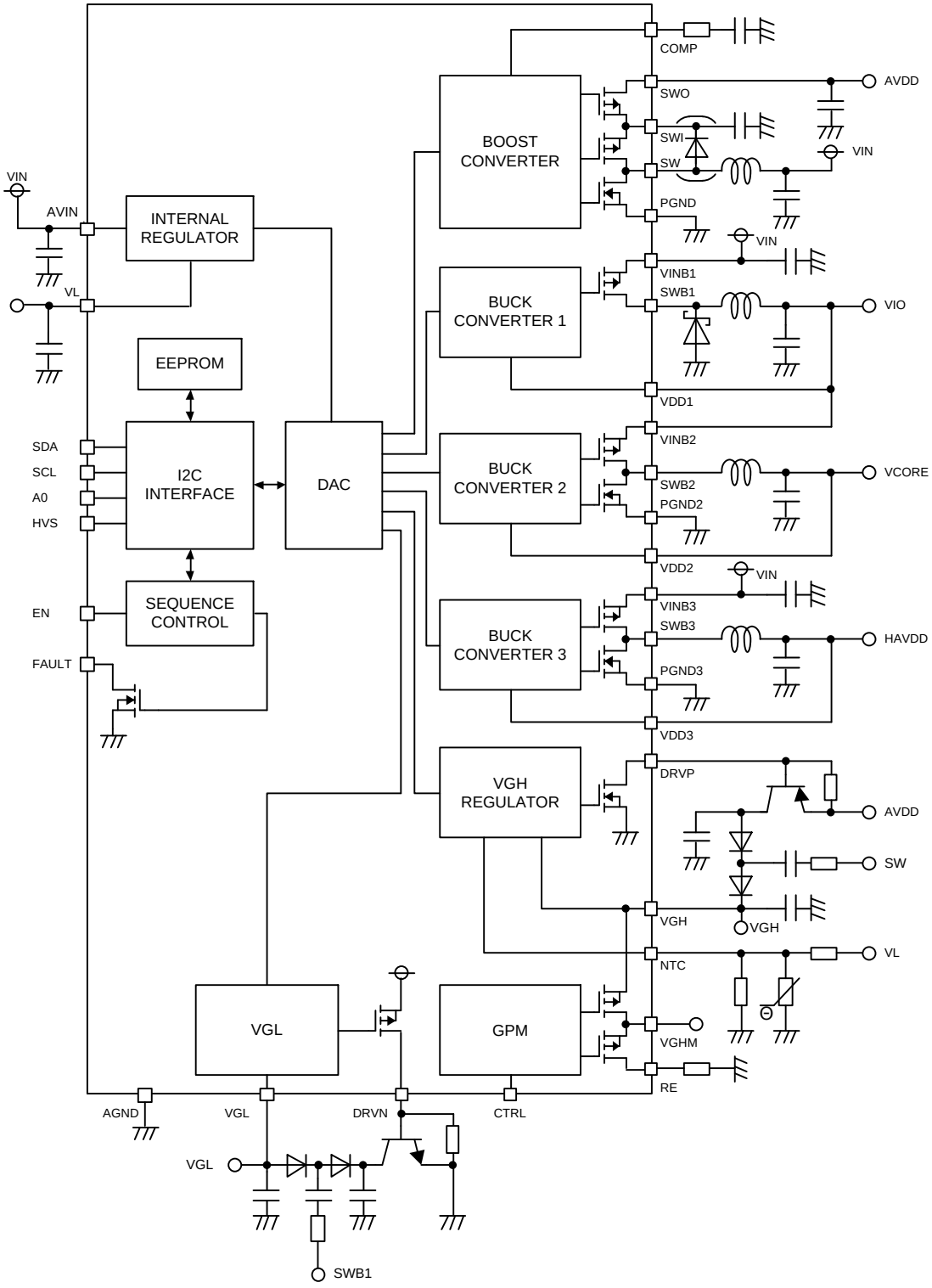


Figure 3. Block Diagram (VGH Doubler)

Block Diagram (VGH Trippler)

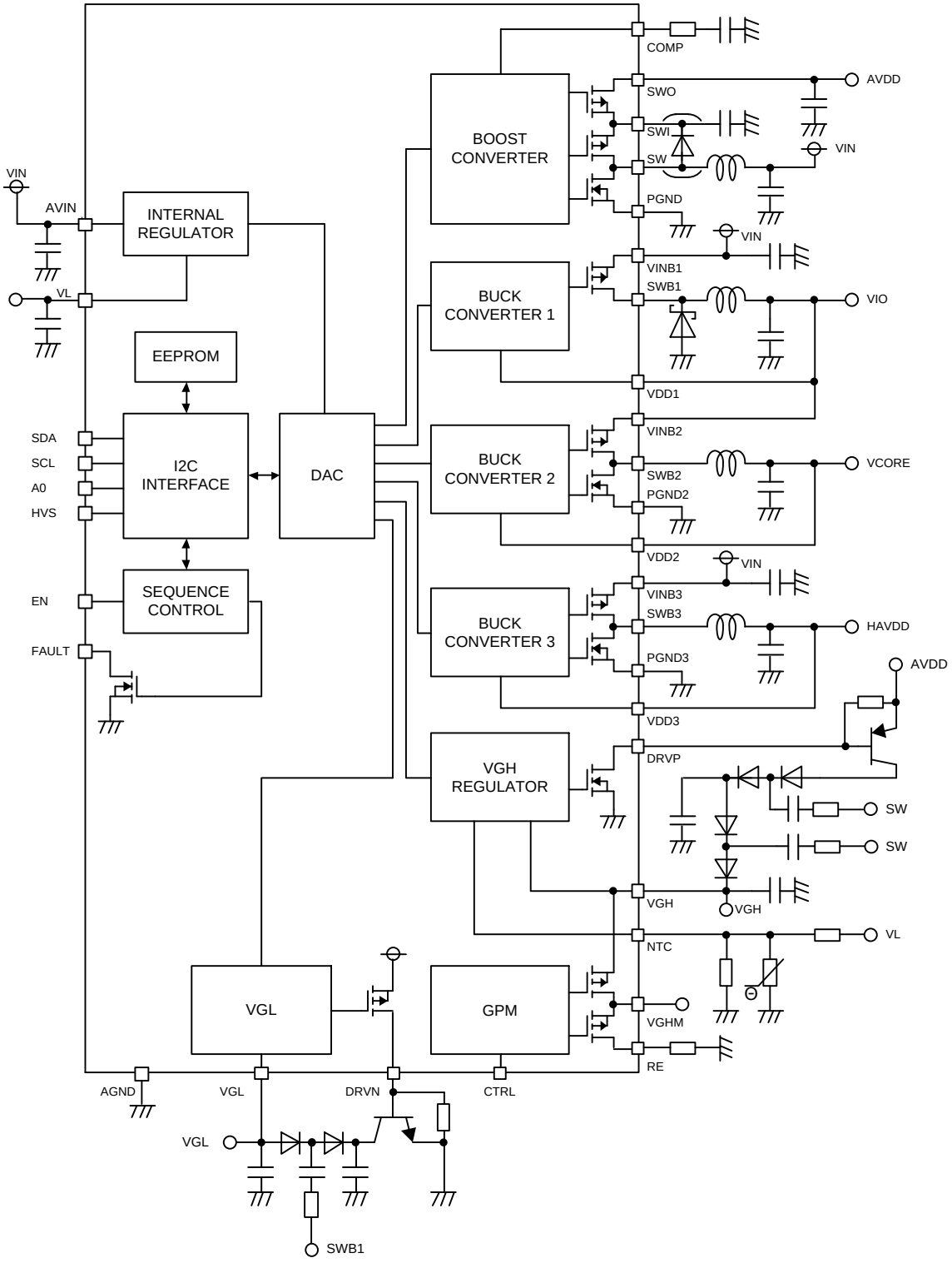


Figure 4. Block Diagram (VGH Trippler)

Description of each Block

① BUCK CONVERTER BLOCK 1

This block generates VIO (VDD1) voltage from Power supply voltage.
After releasing UVLO of VIN, VL starts activating. After Auto Read is operated to EEPROM, VIO will be activated.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

② BUCK CONVERTER BLOCK 2

This block generates VCORE (VDD2) voltage from Power supply voltage of VIO.
After completing VIO start-up, VCORE starts activating.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

③ VGL REGULATOR BLOCK

This block generates VGL voltage.
After completing VCORE start-up, VGL starts activating.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by UVP and OCP protection functions.

④ BOOST CONVERTER BLOCK

This block generates AVDD (SWO) voltage from Power supply voltage.
It activates when EN=H, and under condition where VIO and VGL are active.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

⑤ BUCK CONVERTER BLOCK 3

This block generates HAVDD (VDD3) voltage from Power supply voltage.
HAVDD starts up following AVDD output voltage.
The setting voltage range of the HAVDD voltage depends on the AVDD setting voltage, and the lower limit level of the HAVDD voltage is limited to AVDD × 0.4.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

⑥ VGH REGULATOR BLOCK

This block generates VGH voltage from AVDD voltage.
After completing AVDD star-up, VGH starts activating.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

⑦ GPM BLOCK

This is a switching circuit to drive a gate voltage for TFT consisted of PMOS FET.
VGHM output synchronizes with CTRL input and outputs High voltage = VGH at CTRL=H.
GPM Falling Limit voltage can be controlled by EEPROM.

※ Caution

・EN Input tolerant function is built-in. No need to be always EN < VIN.
・When FAULT pin is not used, FAULT pin must be connected to GND, or it should be open.
・When NTC pin is not used, NTC pin must be connected to GND.
・When HVS pin is not used, HVS pin must be connected to GND.

Absolute Maximum Ratings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN, VINB1, VINB3	-0.3	-	24	V
	VINB2	-0.3	-	7	V
Input Voltage	SDA, SCL, A0, HVS, NTC, EN, CTRL	-0.3	-	7	V
Output Voltage	VL	-0.3	-	6.5	V
	COMP, FAULT VDD2, SWB2	-0.3	-	7	V
	SW, SWI, SWO, VDD1, SWB1, VDD3, SWB3	-0.3	-	24	V
	VGL, DRVN	-15	-	7	V
	DRVP, VGH, VGHM, RE	-0.3	-	40	V
Operating Ambient Temperature Range	Ta	-40	-	85	℃
Storage Temperature Range	Tstg	-55	-	150	℃
Maximum Continuous Junction Temperature	Tjmax (*1)	-	-	150	℃
Power Dissipation (*2)	Pd	3.20			W
	θ ja	39.1			degC/W

*1 It shows junction temperature when stores.
*2 Derate by 25.6mW/℃ at Ta>25℃ when mounted on 4-layer 114.3mm × 74.2mm × 1.6mm glass epoxy board.

Recommended Operating Conditions (Ta=-40℃～85℃)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN	8.6	-	14.7	V
Functional pin voltage	EN, A0, HVS, CTRL	-0.1	-	5.5	V
2 wire serial pin voltage	SDA, SCL	-0.1	-	5.5	V
2 wire serial frequency	FCLK	-	-	400	kHz

Electrical Characteristics (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 GENERAL 】						
VIN Under Voltage Lockout Threshold	VIN_ UVLO	8.0	8.3	8.6	V	VIN rising
		7.25	7.55	7.85	V	VIN falling
Thermal shutdown	TSD	-	175	-	℃	
Internal Oscillator Frequency 1	FOSC1	600	750	900	kHz	AVDD, VIO
Internal Oscillator Frequency 2	FOSC2	800	1000	1200	kHz	VCORE, HAVDD
VL Voltage	VL	4.9	5	5.1	V	
Consumption Current	ICC	-	5.0	-	mA	No switching
【 LOGIC SIGNALS SDA, SCL, EN, A0, CTRL, HVS 】						
High Level Input Voltage	VIH	2	-	-	V	
Low Level Input Voltage	VIL	-	-	0.5	V	
Minimum Output Voltage	VSDA	-	-	0.4	V	SDA, ISDA=3mA
Pull-Down Resistance	RLOGIC	140	200	260	kΩ	EN, A0, CTRL, HVS
【 BOOST CONVERTER (AVDD) 】						
Output Voltage Range	AVDD	13.5	-	19.8	V	0.1V step
HVS Mode Offset Voltage	VHVS	0	-	3	V	0.2V step
Regulation Voltage	AVDD_R	14.85	15.0	15.15	V	Data：0Fh
Hi-Side Leakage Current	ILK_SWH	-	0	10	uA	SW=0V
Hi-Side SW ON-Resistance	RON_SWH	-	100	200	mΩ	ISW=-500mA
Lo-Side SW Leakage Current	ILK_SWL	-	0	10	uA	SW=24V
Lo-Side SW ON-Resistance	RON_SWL	-	100	200	mΩ	ISW=500mA
Load SW ON-Resistance	RON_LS	-	100	200	mΩ	ILS=500mA
SW Current Limit	ILIM_SW	4.25	5	5.75	A	L=10uH
SW Current Limit Offset	ILIM_SET	0	-	2.8	A	0.4A step
Over-Voltage Protection Rise	VOVP_AVDD_RISE	20.5	21.5	22.5	V	
Over-Voltage Protection Fall	VOVP_AVDD_FALL	20	-	-	V	
AVDD UVP Detecting Voltage	VUVP_ AVDD	-	AVDD x 0.8	-	V	
Soft Start Time	TSS_ AVDD	10	-	20	msec	
Load Switch Current Limit	ILIM_LSW	-	7	-	A	

Electrical Characteristics (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 BUCK CONVERTER 1 (VIO) 】						
Output Voltage Range	VIO	2.2	-	3.7	V	0.1V step
Regulation Voltage	VIO_R	2.45	2.5	2.55	V	Data：03h
Hi-Side SWB1 Leak Current	ILK_SWB1H	-	0	10	uA	SWB1=0V
Hi-Side SWB1 ON-Resistance	RON_SWB1H	-	200	300	mΩ	SWB1=-500mA
SWB1 Current Limit	ILIM_SWB1	2.8	3.5	4.2	A	L=10uH
VIO Over-Voltage Protection	VOVP_VIO	-	VIO x 1.1	-	V	
VIO UVP Detecting Voltage	VUVP_VIO	-	VIO x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VIO	-	3	-	msec	VIO=3.0V
【 BUCK CONVERTER 2 (VCORE) 】						
Output Voltage Range	VCORE	0.8	-	3.3	V	0.1V step
Regulation Voltage	VCORE_R	0.98	1.0	1.02	V	Data：02h
Hi-Side SWB2 Leak Current	ILK_SWB2H	-	0	10	uA	SWB2=0V
Hi-Side SWB2 ON-Resistance	RON_SWB2H	-	175	300	mΩ	SWB2=-500mA
Lo-Side SWB2 Leak Current	ILK_SWB2L	-	0	10	uA	SWB2=7V
Lo-Side SWB2 ON-Resistance	RON_SWB2L	-	175	300	mΩ	SWB2=500mA
SWB2 Current Limit	ILIM_SWB2	2.0	3.0	4.0	A	L=10uH
VCORE Over-Voltage Protection	VOVP_VCORE	-	VCORE x 1.1	-	V	
VCORE UVP Detecting Voltage	VUVP_VCORE	-	VCORE x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VCORE	-	4	-	msec	VCORE=2.0V
【 BUCK CONVERTER 3 (HAVDD) 】						
Output Voltage Range	HAVDD	4.8	-	11.1	V	0.1V step
Regulation Voltage	HAVDD_R	7.3875	7.5	7.6125	V	Data：1Bh
Hi-Side SWB3 Leak Current	ILK_SWB3H	-	0	10	uA	SWB3=0V
Hi-Side SWB3 ON-Resistance	RON_SWB3H	-	300	500	mΩ	SWB3=-500mA
Lo-Side SWB3 Leak Current	ILK_SWB3L	-	0	10	uA	SWB3=24V
Lo-Side SWB3 ON-Resistance	RON_SWB3L	-	300	500	mΩ	SWB3=500mA
SWB3 Current Limit	ILIM_SWB3	1.0	1.5	2.0	A	L=10uH
HAVDD Over-Voltage Protection	VOVP_HAVDD	-	HAVDD x 1.1	-	V	
HAVDD UVP Detecting Voltage	VUVP_HAVDD	-	HAVDD x 0.8	-	V	Frequency 1/4

Electrical Characteristics (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 VGH REGULATOR 】						
Output Voltage Range	VGH	20	-	35	V	1V step
Regulation Voltage	VGH_R	26.6	28	29.4	V	Data：08h Io=5mA
VGH_H Offset Voltage	VGHH_O	0	-	15	V	
Over-Current Protection	ILIM_DRVP	5	-	-	mA	
VGH UVP Detecting Voltage	VUVP_VGH	-	VGH x 0.8	-	V	
VGH Over-Voltage Protection	VOVP_VGH	36	38	40	V	
Soft Start Time	TSS_VGH	-	7	-	msec	VGH=28V
【 VGL REGULATOR 】						
Output Voltage Range	VGL	-14.5	-	-5.5	V	0.6V step
Regulation Voltage	VGL_R	-8.0975	-7.9	-7.7025	V	Data：04h Io=5mA
Over-Current Protection	ILIM_DRVN	5	-	-	mA	
VGL UVP Detecting Voltage	VUVP_VGL	-	VGL×0.8	-	V	
Delay Time	TDLY_VGL	-	2.5	-	msec	
DRVN Internal Register	R_DRVN	-	100	-	kΩ	
【 GATE PULSE MODULATION (GPM) 】						
VGH-VGHM ON-Resistance	RGHH	-	3	5	Ω	
RE-VGHM ON-Resistance	RGHL	-	3	-	Ω	
Propagation Delay	TGPM	150	250	350	nsec	

○This product has no designed protection against radioactive rays.

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

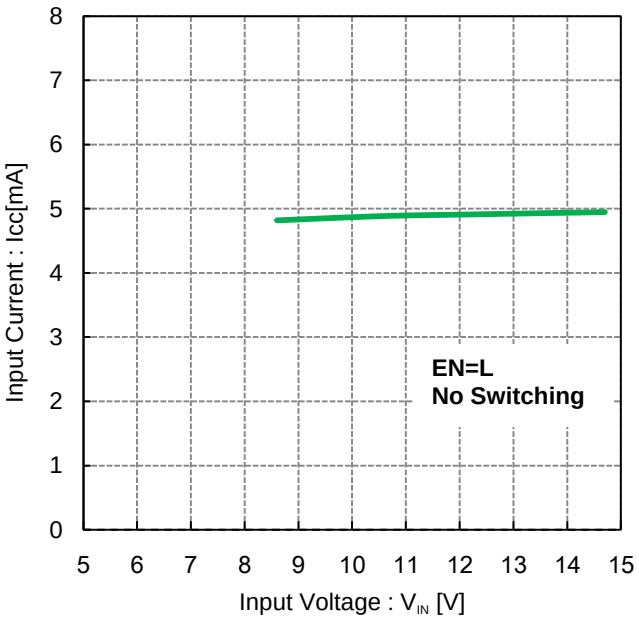


Figure 5. Input Current vs Input Voltage
(EN=L, no switching)

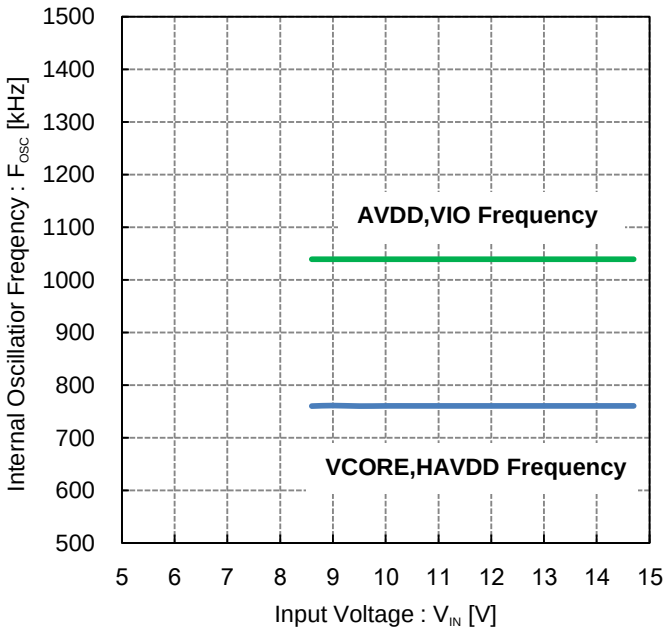


Figure 6. Internal Oscillator Frequency vs Input Voltage

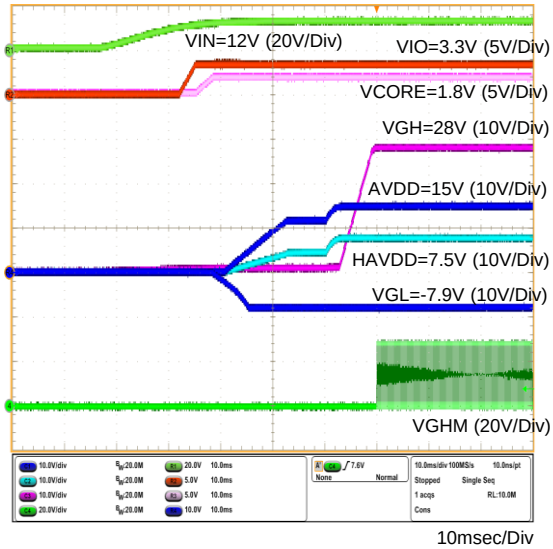


Figure 7. Power-on 1
(VGL driven by VIO switch node)

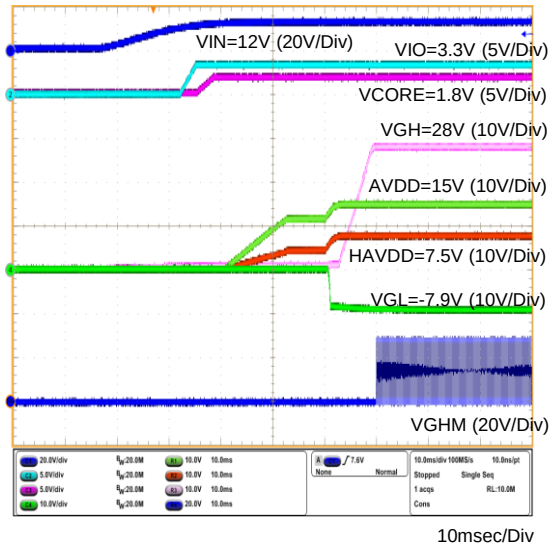


Figure 8. Power-on 2
(VGL driven AVDD switch node)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

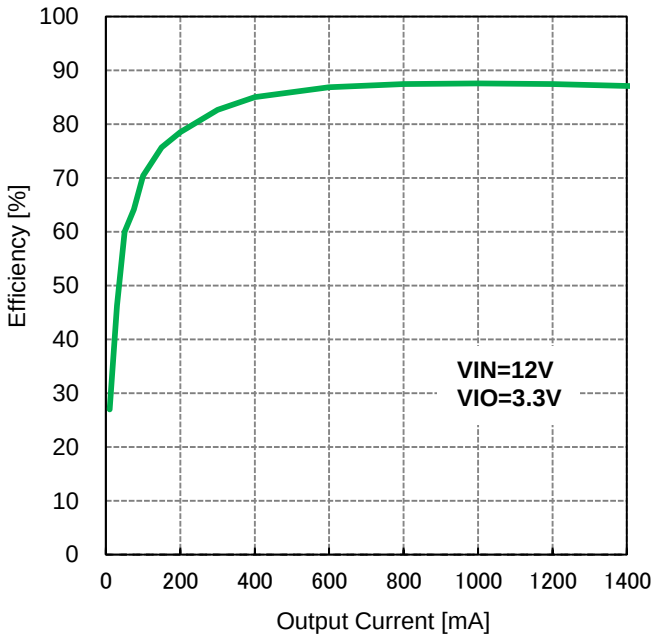


Figure 9. VIO Efficiency vs Output Current

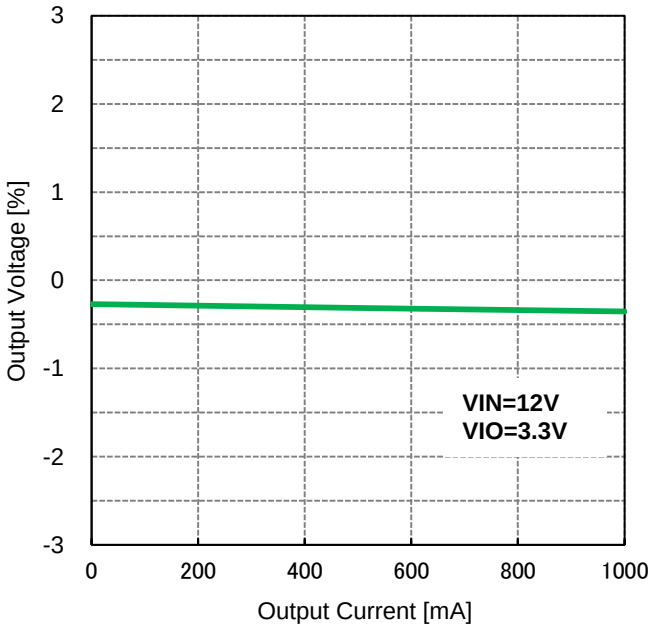


Figure 10. VIO Output Voltage vs Output Current

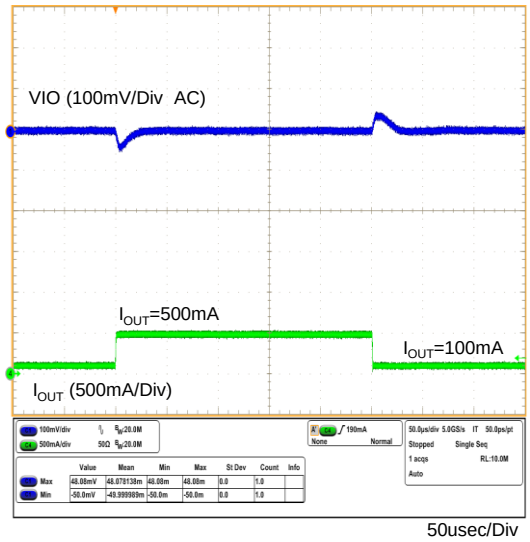


Figure 11. VIO Load Transient

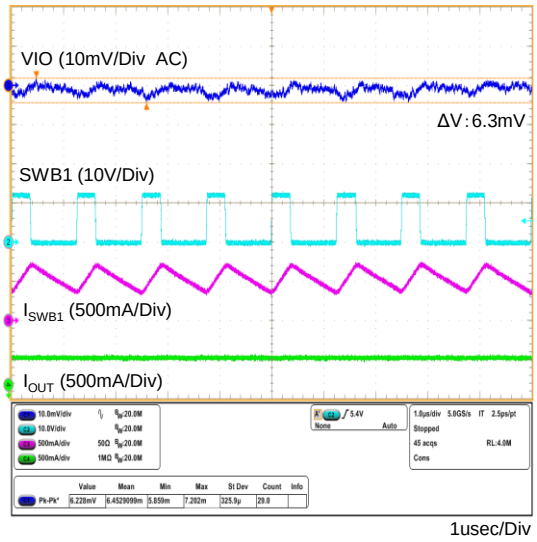


Figure 12. VIO Switching
(Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

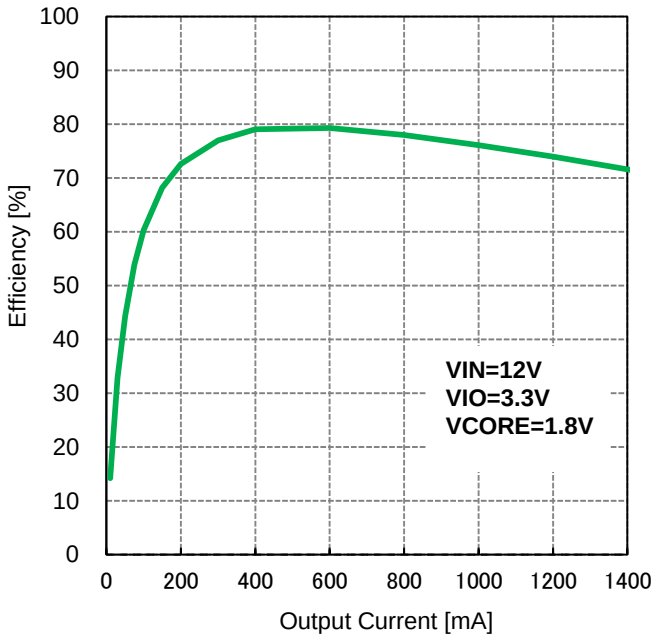


Figure 13. VCORE Efficiency vs Output Current

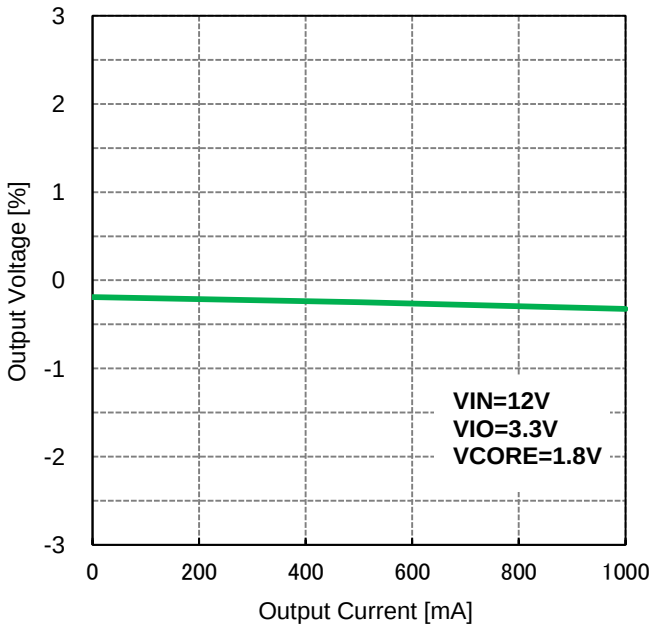


Figure 14. VCORE Output Voltage vs Output Current

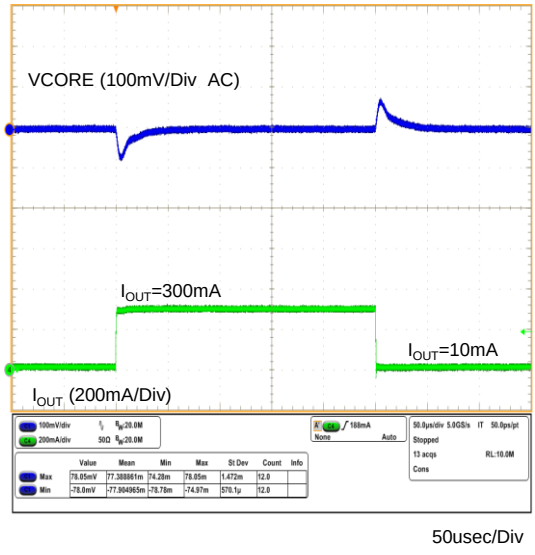


Figure 15. VCORE Load Transient

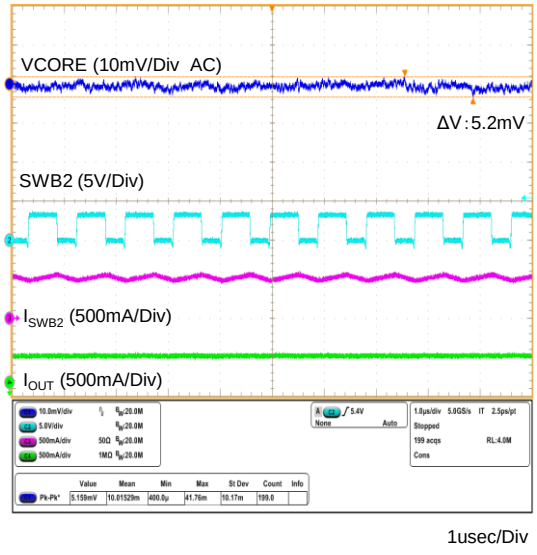


Figure 16. VCORE Switching (Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

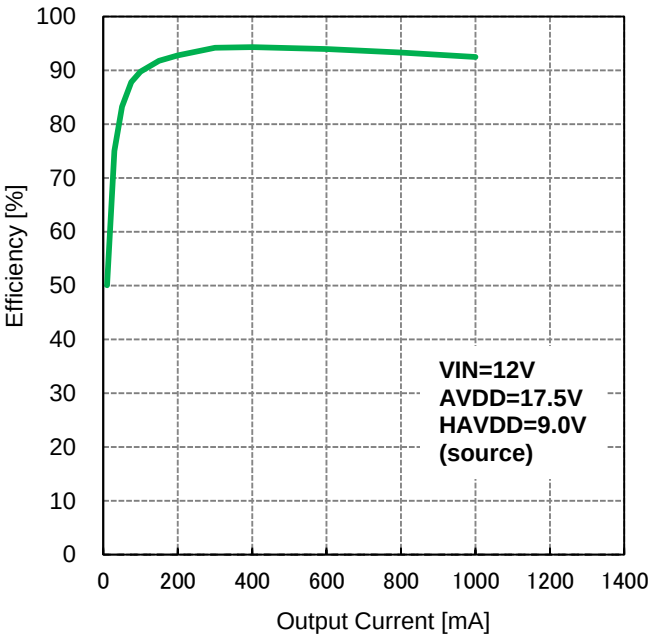


Figure 17. HAVDD Efficiency vs Output Current (source)

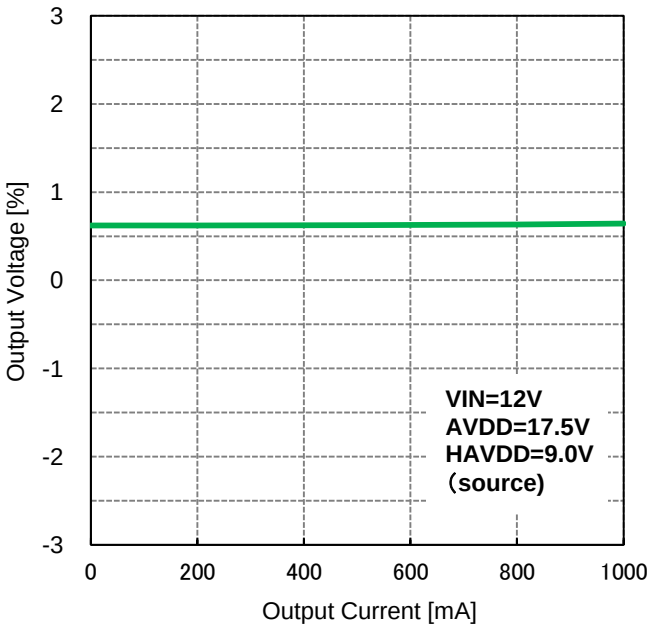


Figure 18. HAVDD Output Voltage vs Output Current (source)

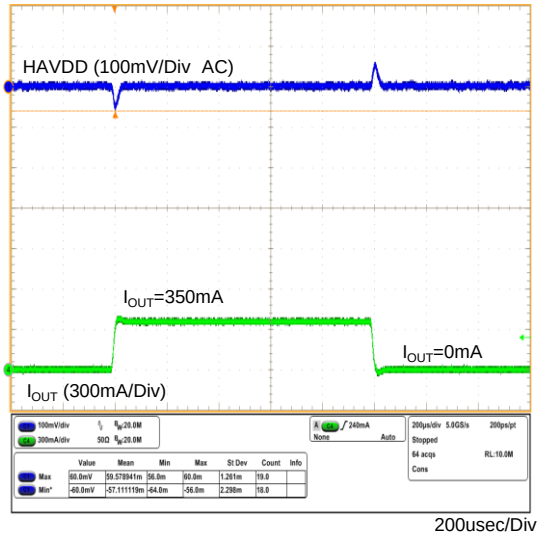


Figure 19. HAVDD Load Transient (source)

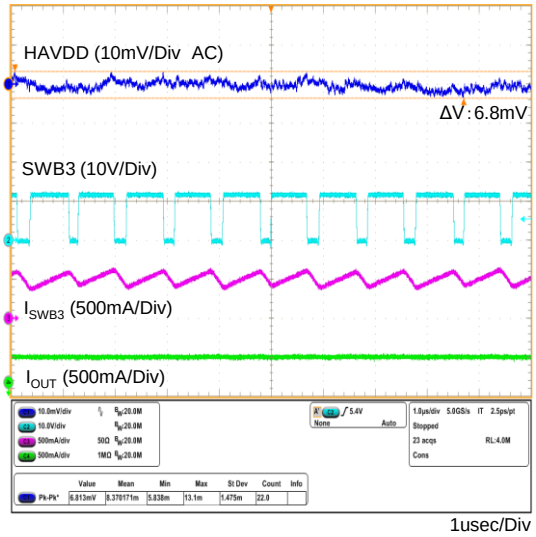


Figure 20. HAVDD Switching (source)
(Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

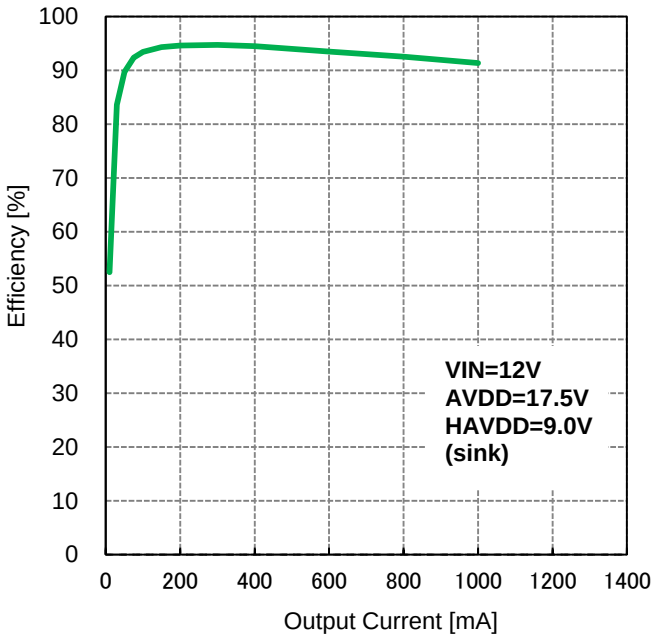


Figure 21. HAVDD Efficiency vs Output Current (sink)

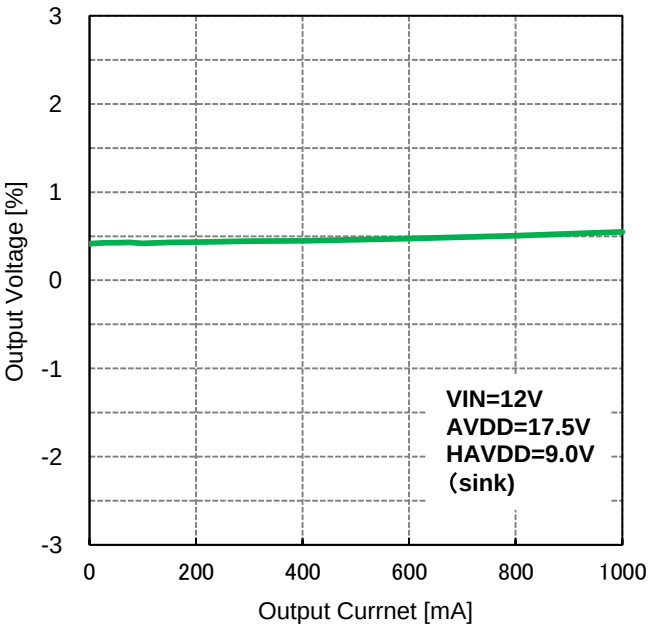


Figure 22. HAVDD Output Voltage vs Output Current (sink)

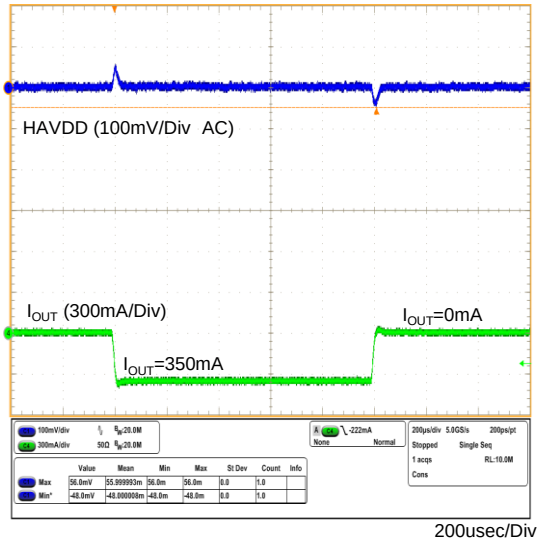


Figure 23. HAVDD Load Transient (sink)

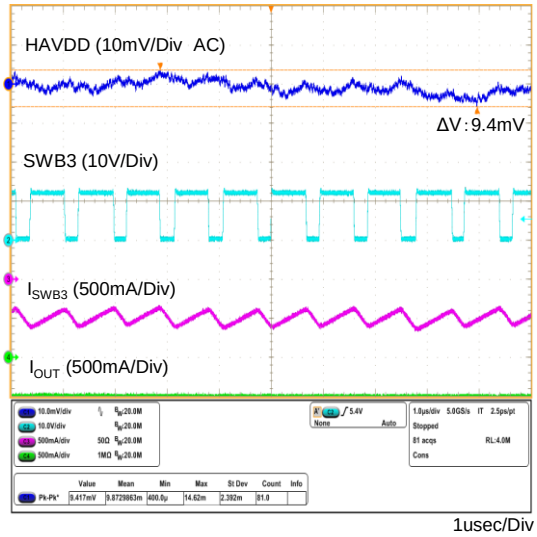


Figure 24. HAVDD Switching (sink)
(Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

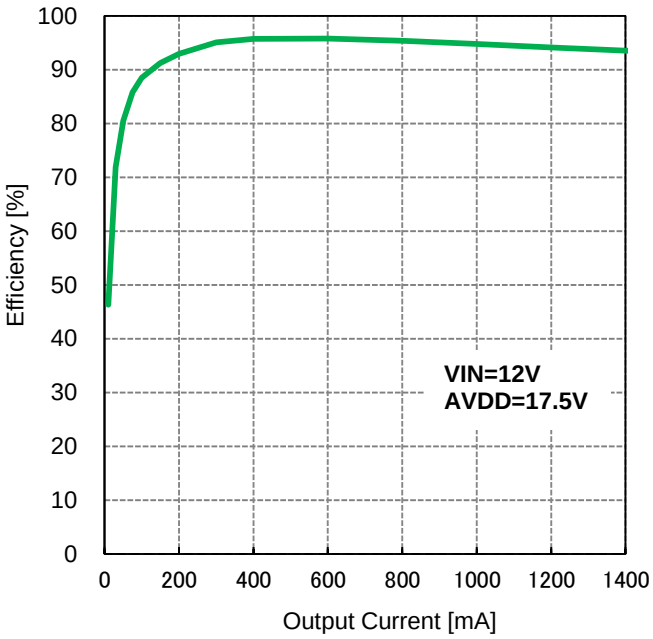


Figure 25. AVDD Efficiency vs Output Current

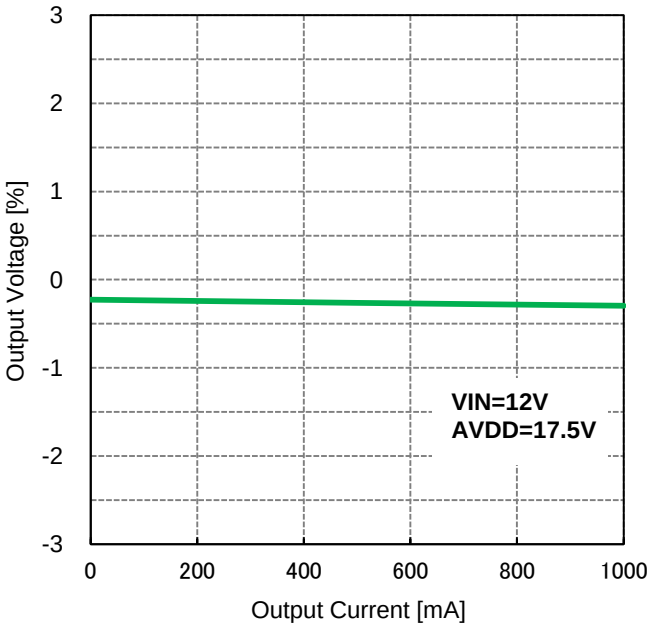


Figure 26. AVDD Output Voltage vs Output Current

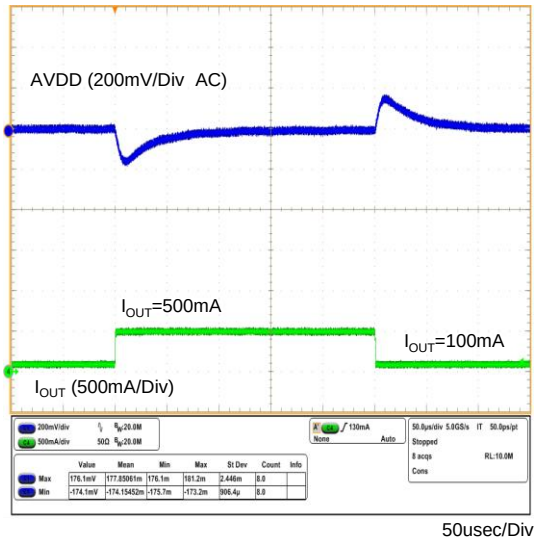


Figure 27. AVDD Load Transient

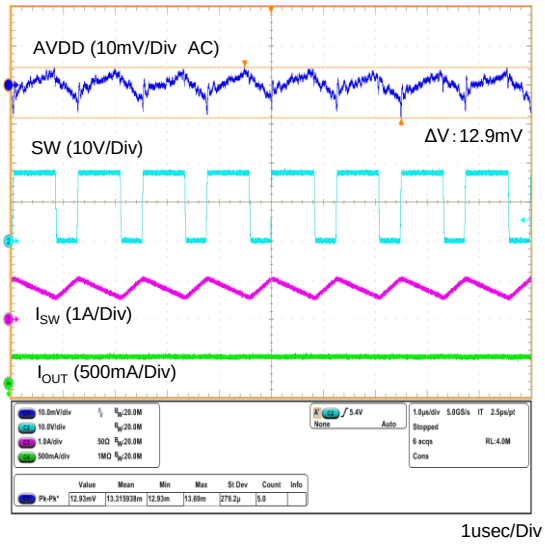


Figure 28. AVDD Switching (Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

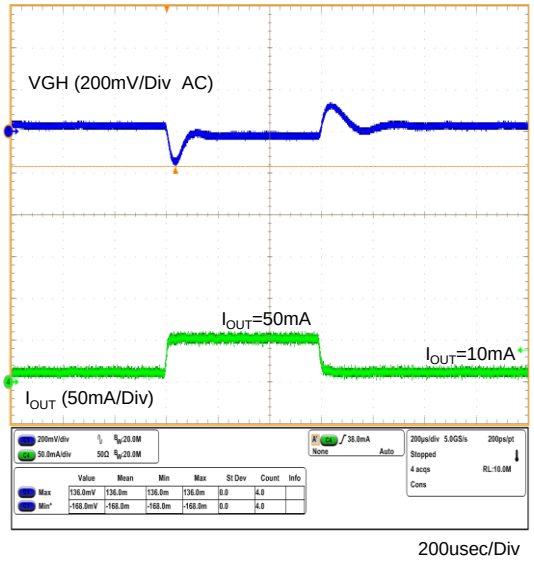


Figure 29. VGH Load Transient

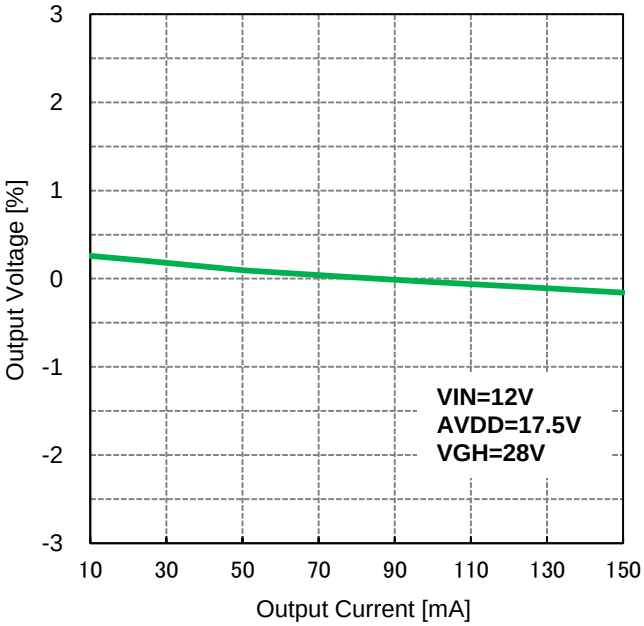


Figure 30. VGH Output Voltage vs Output Current

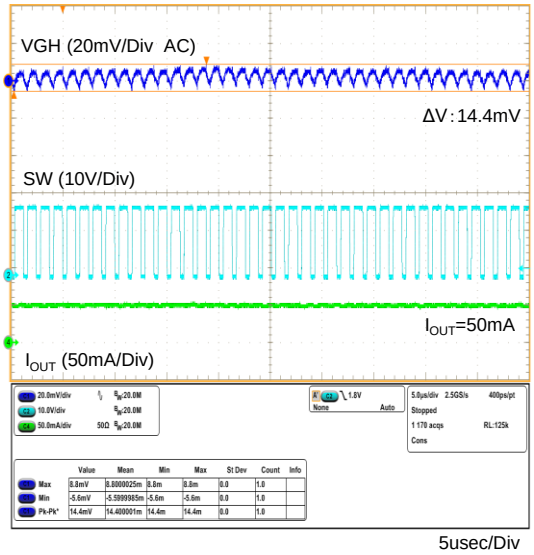
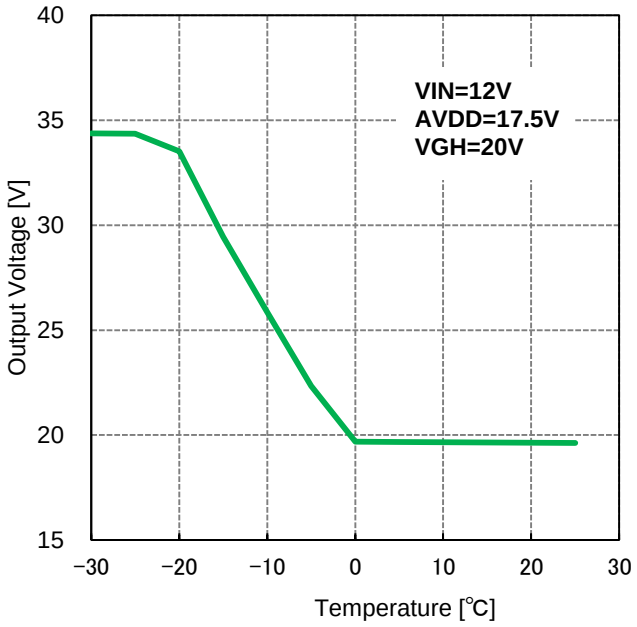


Figure 31. VGH Ripple Voltage

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)



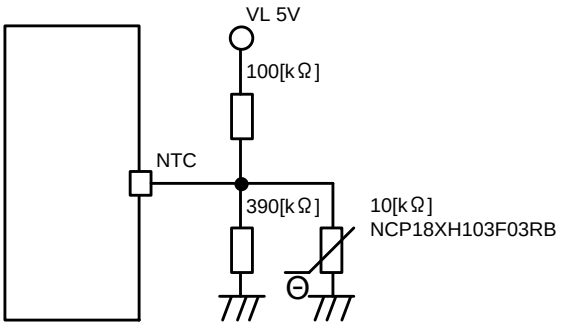


Figure 32. VGH Voltage vs Ta

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

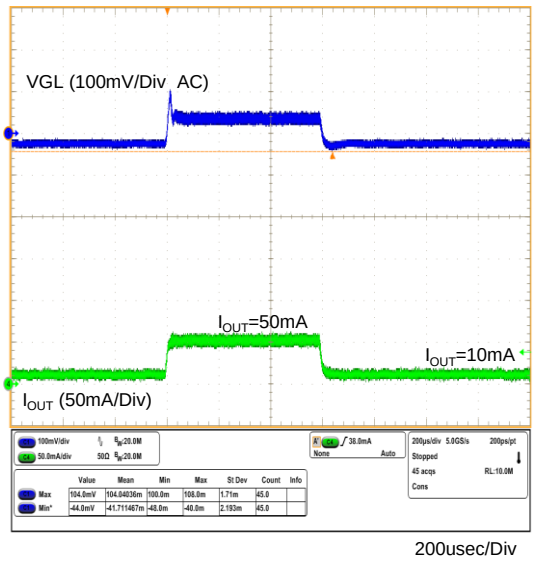


Figure 33. VGL Load Transient

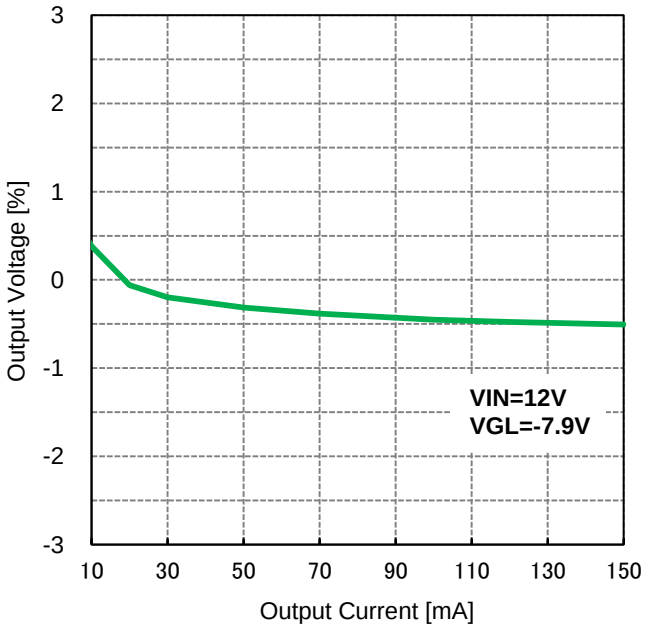


Figure 34. VGL Output Voltage vs Output Current

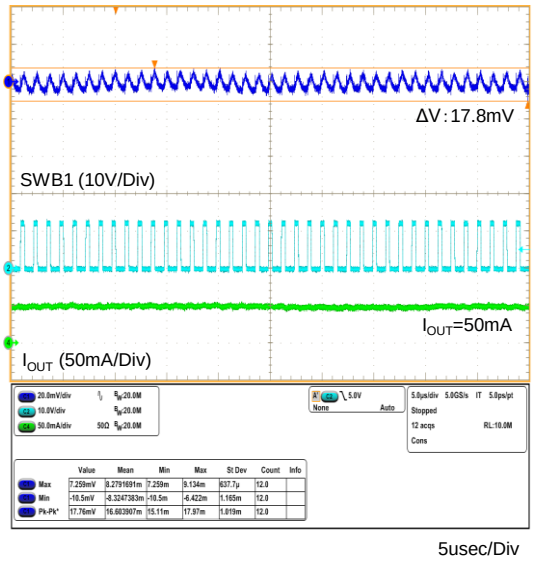


Figure 35. VGL Ripple Voltage

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

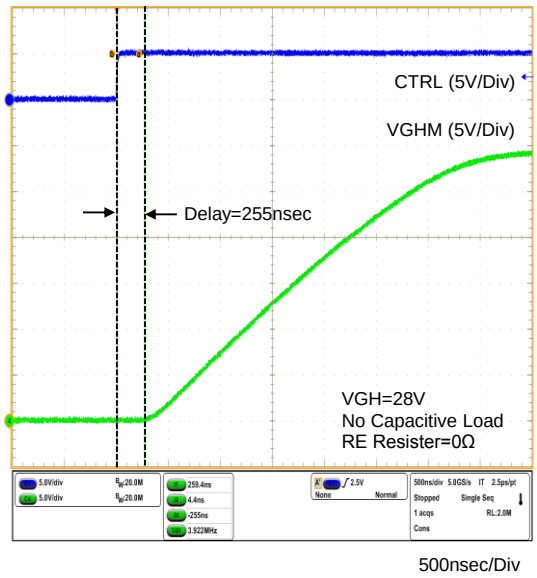


Figure 36. GPM Propagation Delay (rise)

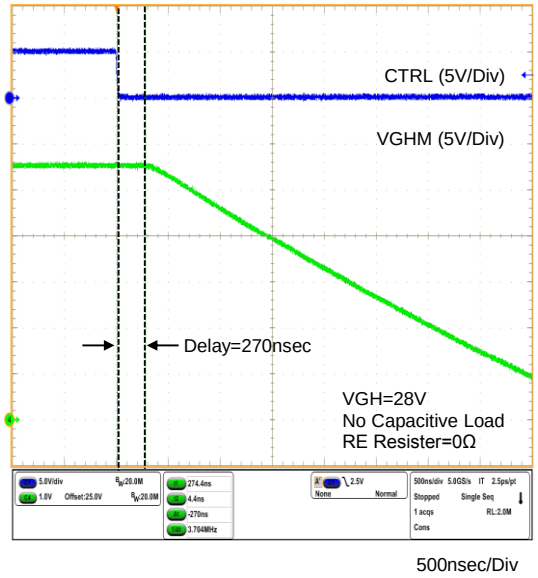


Figure 37. GPM Propagation Delay (fall)

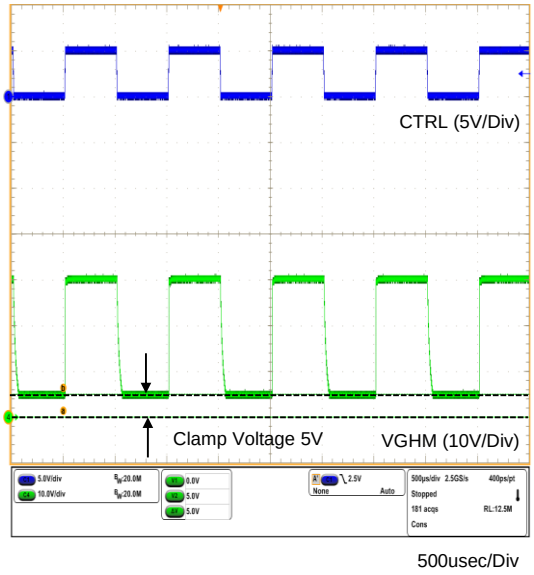


Figure 38. GPM Clamp Voltage (5V Clamp)

Timing Chart

ON and OFF Sequence of this IC are shown below.

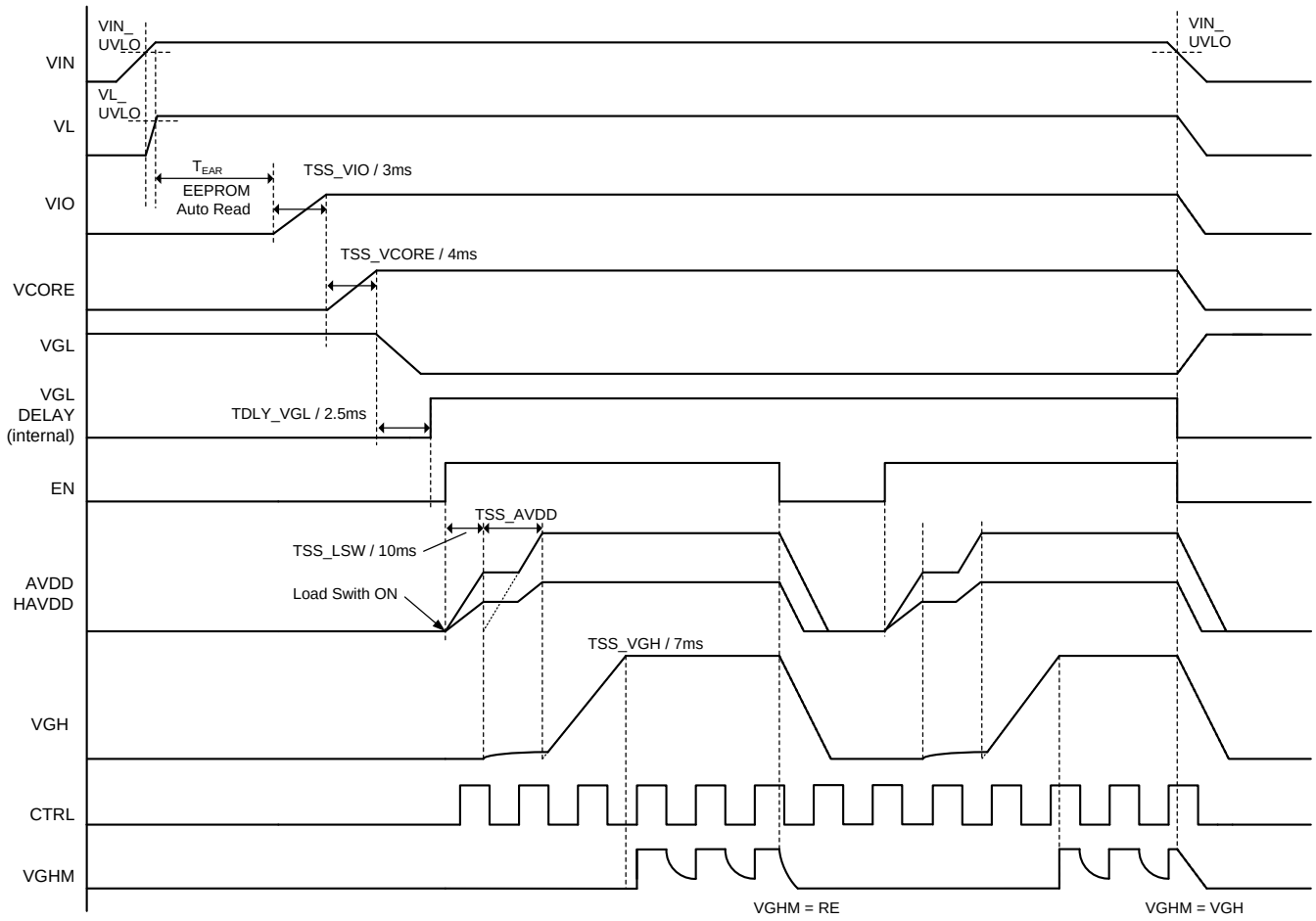


Figure 39. Timing Chart

VL activates with UVLO release of VIN.
It reads EEPROM data by Auto Read operation upon VL activation. (T_{EAR}=2msec)
After Auto Read completion, VIO activates. The Soft Start time of VIO is 3msec if the setting is 3.0V.
After VIO soft-start completion, VCORE activates. The Soft Start time of VCORE is 4msec if the setting is 2.0V.
After VCORE soft-start completion, VGL activates. The Soft Start time of VGL depends on output voltage setting, external capacitor, etc.
2.5msec after VCORE soft-start completion, Load SW turns ON (10msec) when EN=High then AVDD activates.
The Soft Start time of AVDD can be changed by register setting (10msec or 20msec).
After AVDD started, VGH activates. The Soft Start time of VGH is 7msec if the setting is 28V.
While VGH is active, CTRL rising or falling will be a trigger to activate GPM operation.
When VGHM voltage at CTRL=L reaches the GPM clamp voltage, VGHM output is high impedance.
GPM, VGH, AVDD, and HAVDD shut down when EN=Low. GPM output (VGHM) will be the same potential with RE.
All outputs shut down when a drop in VIN of UVLO is detected. VGHM will be the same potential with VGH.

Example Application（TOP VIEW, VGH Doubler）

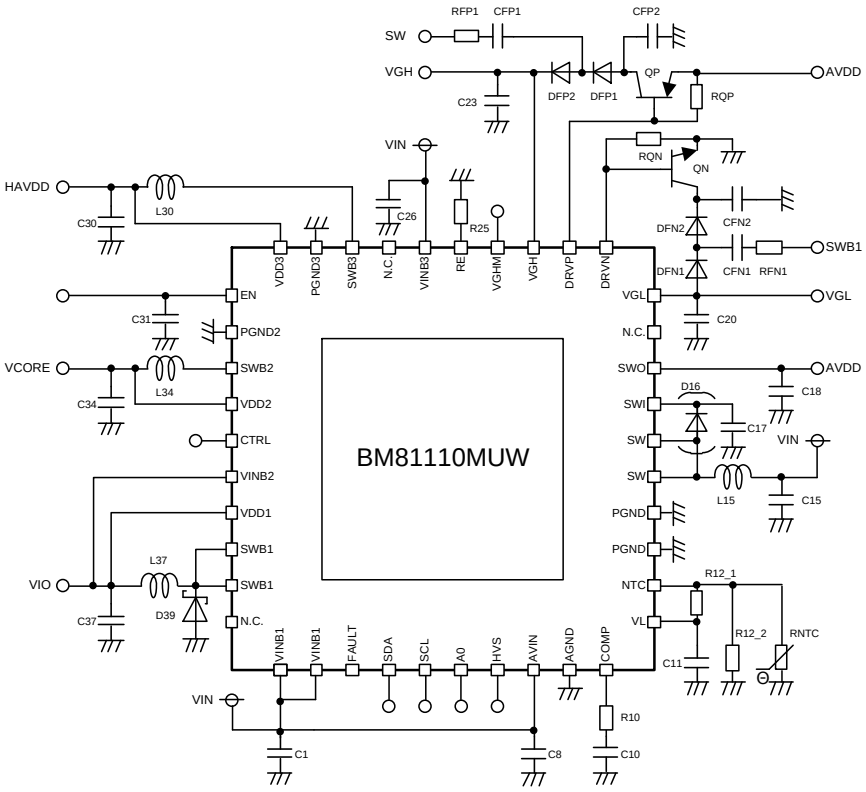


Figure 40. Example Application

Application circuit components list

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C1	10 [uF]×2	MURATA	GRM31CB31E106KA75	RQN	100 [kΩ]	ROHM	MCR03
C8	1 [uF]	MURATA	GRM188B31E105KA75	RQP	100 [kΩ]	ROHM	MCR03
R10	75 [kΩ]	ROHM	MCR03	QP	-	ROHM	2SAR513P
C10	470 [pF]	MURATA	GRM188B11H471KA01	CFP2	470 [pF]	MURATA	GRM188B11H471KA01
C11	1 [uF]	MURATA	GRM188B31E105KA75	DFP1	-	ROHM	RB558W
R12_1	100 [kΩ]	ROHM	MCR03	DFP2			
R12_2	390 [kΩ]	ROHM	MCR03	CFP1	0.47 [uF]	MURATA	GRM188B31E474KA75
RNTC	10 [kΩ]	MURATA	NCP18XH103F03RB	RFP1	2.2 [Ω]	ROHM	MCR15
L15	10 [uH]	TAIYO YUDEN	NS10165T100MNA	C23	4.7 [uF]×2	MURATA	GRM31CB31H475KA12
C15	10 [uF]×2	MURATA	GRM31CB31E106KA75	R25	300 [Ω]	ROHM	MCR03
D16	-	ROHM	RB080L-30TE25	C26	10 [uF]	MURATA	GRM31CB31E106KA75
C17	10 [uF]×2	MURATA	GRM31CB31E106KA75	L30	10[uH]	TAIYO YUDEN	NRS8040T100M
C18	10 [uF]×4	MURATA	GRM31CB31E106KA75	C30	10 [uF]×2	MURATA	GRM31CB31E106KA75
C20	4.7 [uF]×2	MURATA	GRM219B31C475KE15	C31	0.1 [uF]	MURATA	GRM152B30J104KE19
DFN1	-	ROHM	RB558W	L34	10[uH]	TAIYO YUDEN	NRS8040T100M
DFN2				C34	10 [uF]×2	MURATA	GRM21BB31A106KE18
CFN1	0.47 [uF]	MURATA	GRM188B31E474KA75	L37	10[uH]	TAIYO YUDEN	NRS8040T100M
RFN1	2.2 [Ω]	ROHM	MCR15	C37	10 [uF]×3	MURATA	GRM21BB31A106KE18
CFN2	0.22 [uF]	MURATA	GRM188B31E224KA87	D39	-	ROHM	RSX301L-30
QN	-	ROHM	2SCR513P				

Example Application（TOP VIEW, VGH Trippler）

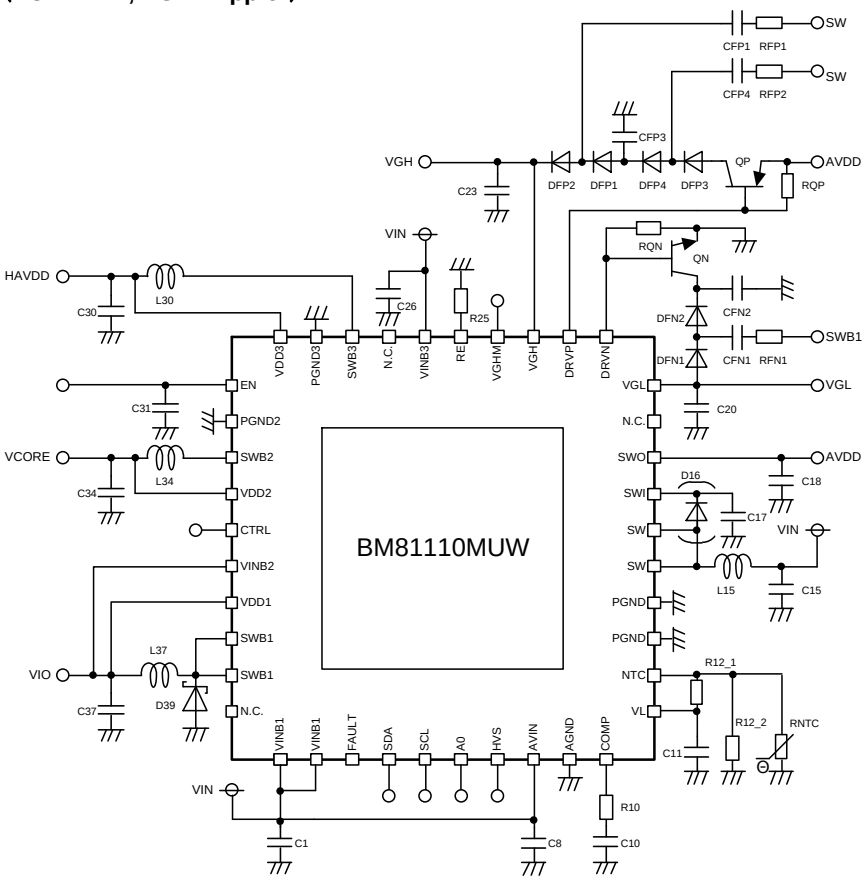


Figure 41. Example Application

Application circuit components list

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C1	10 [uF]×2	MURATA	GRM31CB31E106KA75	QP	-	ROHM	2SAR513P
C8	1 [uF]	MURATA	GRM188B31E105KA75	CFP1	0.1 [uF]	MURATA	GRM188B31E104KA75
R10	75 [kΩ]	ROHM	MCR03	RFP1	2.2 [Ω]	ROHM	MCR15
C10	470 [pF]	MURATA	GRM188B11H471KA01	DFP1	-	ROHM	RB558W
C11	1 [uF]	MURATA	GRM188B31E105KA75	DFP2			
R12_1	100 [kΩ]	ROHM	MCR03	DFP3	-	ROHM	RB558W
R12_2	390 [kΩ]	ROHM	MCR03	DFP4			
RNTC	10 [kΩ]	MURATA	NCP18XH103F03RB	CFP3	1[uF]	MURATA	GRM21BB31H105KA12
L15	10 [uH]	TAIYO YUDEN	NS10165T100MNA	RFP2	2.2 [Ω]	ROHM	MCR15
C15	10 [uF]×2	MURATA	GRM31CB31E106KA75	CFP4	0.1 [uF]	MURATA	GRM188B31E104KA75
D16	-	ROHM	RB080L-30TE25	C23	4.7 [uF]×2	MURATA	GRM31CB31H475KA12
C17	10 [uF]×2	MURATA	GRM31CB31E106KA75	R25	300 [Ω]	ROHM	MCR03
C18	10 [uF]×4	MURATA	GRM31CB31E106KA75	C26	10 [uF]	MURATA	GRM31CB31E106KA75
C20	4.7 [uF]×2	MURATA	GRM219B31C475KE15	L30	10[uH]	TAIYO YUDEN	NRS8040T100M
DFN1	-	ROHM	RB558W	C30	10 [uF]×2	MURATA	GRM31CB31E106KA75
DFN2				C31	0.1 [uF]	MURATA	GRM152B30J104KE19
CFN1	0.47 [uF]	MURATA	GRM188B31E474KA75	L34	10[uH]	TAIYO YUDEN	NRS8040T100M
RFN1	2.2 [Ω]	ROHM	MCR15	C34	10 [uF]×2	MURATA	GRM21BB31A106KE18
CFN2	0.22 [uF]	MURATA	GRM188B31E224KA87	L37	10[uH]	TAIYO YUDEN	NRS8040T100M
QN	-	ROHM	2SCR513P	C37	10 [uF]×3	MURATA	GRM21BB31A106KE18
RQN	100 [kΩ]	ROHM	MCR03	D39	-	ROHM	RSX301L-30
RQP	100 [kΩ]	ROHM	MCR03				

Protection function explanation of each block

1. BUCK CONVERTER BLOCK 1 (VIO)

1-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising VIO voltage.
Voltage inputted to VDD1 pin is monitored and if VIO voltage reaches VIO>110%(Typ), it is judged as unusual condition thus OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to VIO voltage. After OVP is released, switching is re-started.

1-2. Over Current Protection (OCP)

If excessive load current (SWB1 peak current>3.5A, Typ) is present, it limits current to flow to built–in Power MOS by controlling Switching.

1-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When the unusual condition (VIO<80%) is detected, SWB1 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues up to 10msec (Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

2. BUCK CONVERTER BLOCK 2 (VCORE)

2-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or others components from malfunctioning due to rising VCORE voltage.
Voltage inputted to VDD2 pin is monitored and if VCORE voltage reaches VCORE>110%(Typ), it is judged as unusual condition thus OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to VCORE voltage. After OVP is released, switching is re-started.

2-2. Over Current Protection (OCP)

If excessive load current (SWB2 peak current>3.0A, Typ) is present, it limits current to flow to built–in Power MOS by controlling Switching.

2-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When the unusual condition (VCORE<80%) is detected, SWB2 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues upto 10msec (Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

3. VGL REGULATOR BLOCK

3-1. Over Current Protection (OCP)

If excessive load current (I_DRVN>5mA, min.) is present, It controls source current (Base current of NPN Tr) of DRVN.

3-2. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When unusual condition is detected (VGL>80%), the UVP time counter starts. If the unusual condition continues up to 10msec (Typ), all output is latched in shut-down condition. Power reset is needed to cancel the latch state and to re-start.

4. BOOST CONVERTER BLOCK (AVDD)

4-1. Over Voltage Protection (OVP)

OVP function is built in to prevent IC or other components from malfunctioning due to excessive rise in AVDD voltage.
The voltage inputted to SWO pin is being monitored. If the SWO pin voltage becomes 21.5V(Typ), OVP is detected. Once OVP is detected, switching is stopped. After AVDD voltage falls below OVP detection release voltage 20V(min.), switching is restarted.

4-2. Over Current Protection (OCP)

If excessive load current over 5A (Typ) of SW peak current is present, OCP limits current to rush to built-in Power MOS by controlling its output switching.

4-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When an unusual condition is detected (AVDD<80%), UVP timer starts. If the unusual condition continues up to 10msec(Typ), all output is latched in shut-down condition. Power reset is needed to remove the latch state and to re-start.

4-4. Load Switch Over Current Protection (LSW_OCP)

If excessive load current (7A, Typ) is present, It controls current of load switch.

5. BUCK CONVERTER BLOCK 3 (HAVDD)

5-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising HAVDD voltage.
Voltage inputted to VDD3 pin is being monitored and if HAVDD voltage reaches HAVDD>110% (Typ), it is judged as unusual condition thus OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to HAVDD voltage. After OVP release, switching is re-started.

5-2. Over Current Protection (OCP)

If excessive load current (SWB3 peak current>1.5A, typ.) is present, it limits current to flow to built–in Power MOS by controlling Switching.

5-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When the unusual condition (HAVDD<80%) is detected, SWB3 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues up to 10msec(Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

6. VGH REGULATOR BLOCK

6-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to VGH voltage rising.
Voltage inputted to VGH pin is being monitored and if VGH voltage reaches VGH>38V(Typ), it is judged as unusual condition so that OVP function is operated. If OVP is detected, limit DRVP current until OVP release voltage (35V, Typ) falls to VGH voltage. After OVP release, the current limiting of the DRVP pin is canceled.

6-2. Over Current Protection (OCP)

If excessive load current (I_DRVP>5mA, min.) is present, it controls sink current (Base current of PNP Tr) of DRVP.

6-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When an unusual condition is detected (VGH<80%), UVP timer starts. If the unusual condition continues up to 10msec (Typ), all output is latched in shut-down condition. Power reset is needed to remove the latch state and to re-start.

7. GENERAL

7-1. Thermal shutdown

All outputs will shut down when the IC temperature exceeds 175℃(typ.). After the temperature falls below 150℃(Typ), the operation re-starts.

7-2. VIN Under Voltage Lock Out

VIN Under Voltage Lock Out prevents the circuit malfunction below the UVLO voltage. If VIN voltage is below the UVLO voltage (8.3V / 7.55V), it enters the standby state.

Protection function list

BLOCK	Protective Function	Working Condition	Action	Protective removal
BUCK CONVERTER 1	OVP	VIO>110%	Stops switching.	VIO<100%
	OCP	I_SWB1>3.5A	Controls switching pulse duty to not exceed over current limit.	I_SWB1<3.5A
	UVP	VIO<80%	Frequency becomes 1/4	VIO>80%
			IC shuts down if UVP status maintains in 10msec.	IC restart
BUCK CONVERTER 2	OVP	VCORE>110%	Stops switching.	VCORE<100%
	OCP	I_SWB2>3.0A	Controls switching pulse duty to not exceed over current limit.	I_SWB2<3.0A
	UVP	VCORE<80%	Frequency becomes 1/4	VCORE>80%
			IC shuts down if UVP status maintains in 10msec.	IC restart
VGL REGULATOR	OCP	I_DRVN> 5 mA	Limits DRVN current.	I_DRVN< 5 mA
	UVP	VGL<80%	IC shuts down if UVP status maintains in 10msec.	IC restart
BOOST CONVERTER	OVP	SWI>21.5V	Stops switching	SWI<20V
	OCP	I_SW>5A	Controls switching pulse duty to not exceed over current limit.	I_SW<5A
	UVP	SWO<80%	IC shuts down if UVP status maintains in 10msec.	IC restart
LOAD SW	OCP	I_SWO>7.0A	Off the Load Switch.	IC restart
BUCK CONVERTER 3	OVP	HAVDD>110%	Stops switching.	HAVDD<100%
	OCP	I_SWB3>1.5A	Controls switching pulse duty to not exceed over current limit.	I_SWB3<1.5A
	UVP	HAVDD<80%	Frequency becomes ¼	HAVDD>80%
			IC shuts down if UVP status maintains in 10msec.	IC restart
VGH REGULATOR VGH REGULATOR	OVP	VGH>38V	DRVP current limit to 0mA	VGH<35V
	OCP	I_DRVP> 5 mA	Limits DRVP current.	I_DRVP< 5 mA
	UVP	VGH<80%	IC shuts down if UVP status maintains in 10msec.	IC restart
GENERAL	TSD	Tj>175℃	IC shuts down	Tj<150℃
	UVLO	VIN<7.55V	IC shuts down	VIN>8.3V

Upper limit voltage setting of VGH thermal compensation

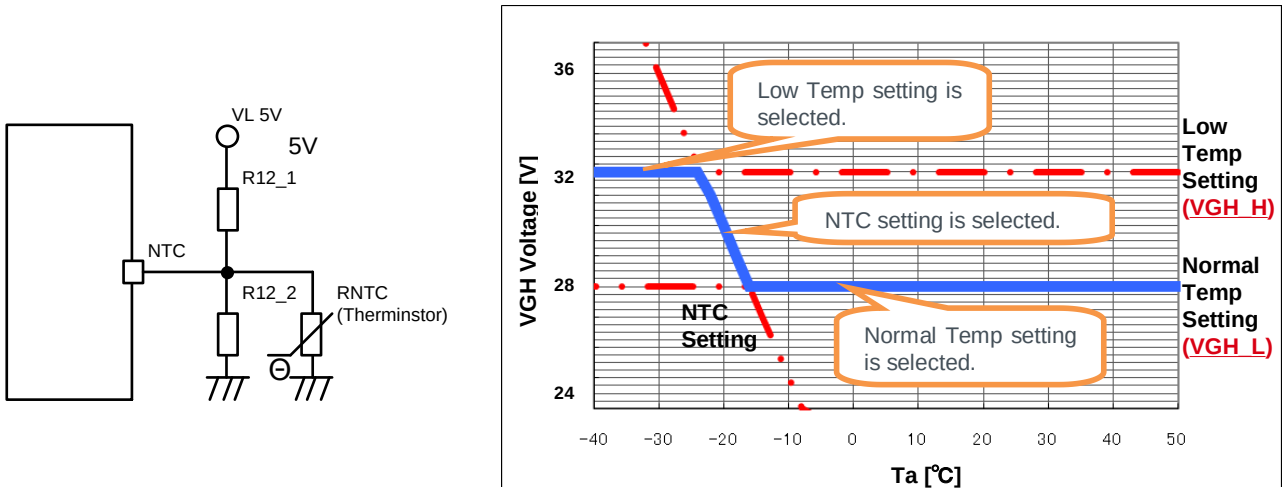


Figure 42. VGH thermal compensation

This IC installs the thermal compensation function for VGH voltage. VGH thermal compensation upper limit voltage (VGH_H) is settable by changing the EEPROM setting.
Thermal gradient setting is possible by the thermistor (R_NTC) connected to NTC pin and the resistor divider (R_NTC1, R_NTC2).

FAULT function

The FAULT output indicates the status of the protection circuit of this IC.
Because FAULT is an open-drain output, place a pull-up resistor externally.
When the FAULT output will not be used, leave the pin OPEN.

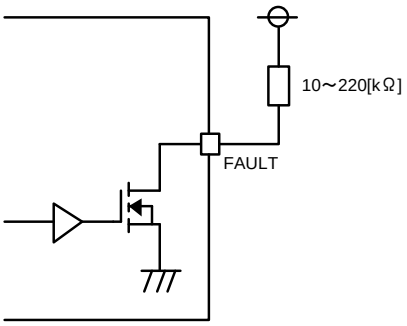


Figure 43. FAULT Terminal

The recommended external pull-up resistance for the FAULT output is 10kΩ to 220kΩ. An external resistance of under 10kΩ can generate an offset voltage during FAULT=L caused by the voltage drop across the internal ON resistance. On the other hand, an external resistance of more than 220kΩ can interfere with the output during FAULT=H because of leak current.
The conditions that FAULT terminal becomes Low are as follows.

・If UVLO operates ・If UVP operates ・If TSD operates

When FAULT function is not used, connect NTC pin to GND, or please make it open.

Serial transmission

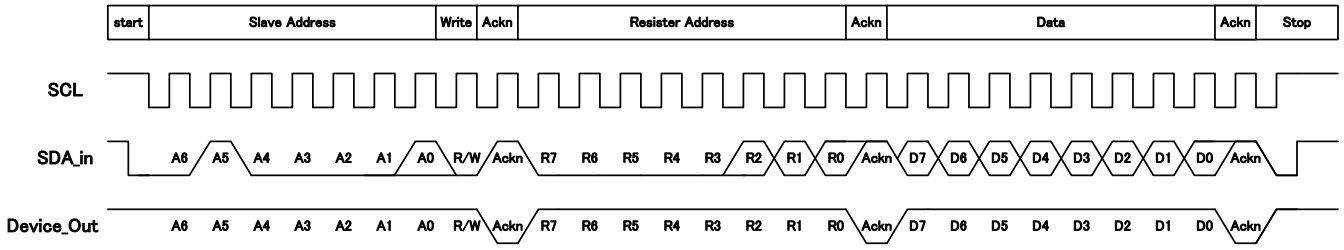
Use I^2C BUS control for command interface with Host.
Writing or reading by specifying 1 byte Register address besides Slave address.
I^2C BUS slave mode format is shown below.

Write operation	Start	Slave Address							R/W	A	Register Address	A	DATA	A	Stop
		0	1	0	0	0	0	A0	0	0	Select Register Address (8bit)	0	8bit DATA	0	
Read operation	Start	Slave Address							R/W	A	Register Address	A	DATA	A	Stop
		0	1	0	0	0	0	A0	1	0	Select Register Address (8bit)	0	8bit DATA	0	

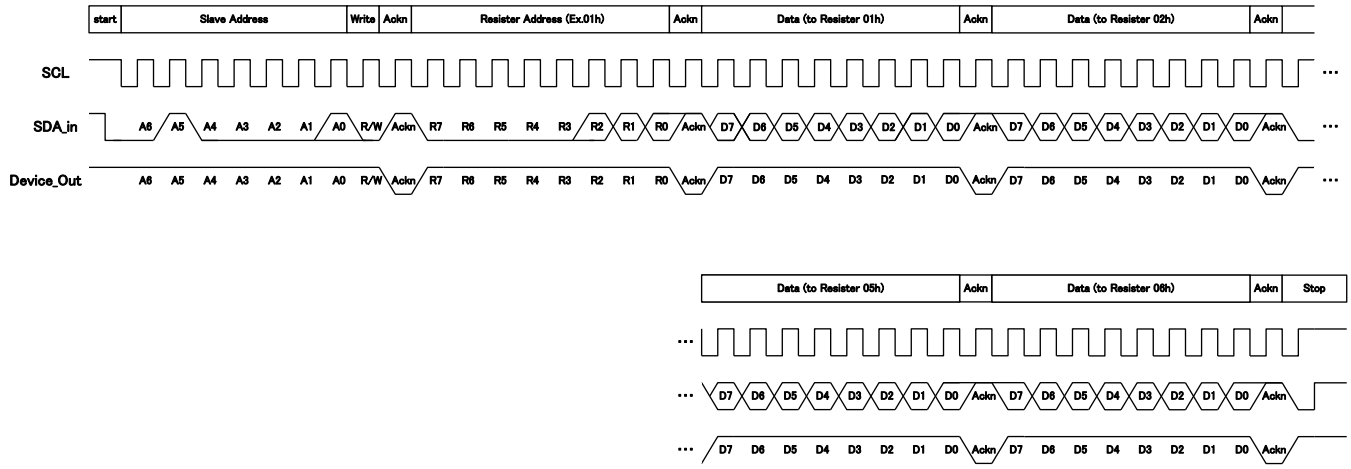
Start	:	Start condition
Slave Address	:	Send 7 bit data in all with bit of Read Mode (H) or Write Mode (L). (MSB First) A0 is selectable (1/0) with the slave address select pin.
ACK	:	Acknowledge Sending or receiving data includes acknowledge bit per byte. If the data is sent or received properly, 'L' is sent and received. If 'H' is sent and received, it means there is no Acknowledge.
Register Address	:	Use 1 byte select address.
Data	:	Data byte. Sending and Receiving data (MSB First)
STOP	:	Stop condition

For writing mode from I2C BUS to register, there is Single mode or Multi-mode.
On single mode, write data to one designated register.
On multi-mode, as a start address register specified in the second byte, writing data can be performed continuously, by entering multiple data.
Single mode or multi-mode setting can be configured by having or not having 'stop bit'.

①Single Mode Timing Chart



②Multi Mode Timing Chart



I2C Timing Diagram

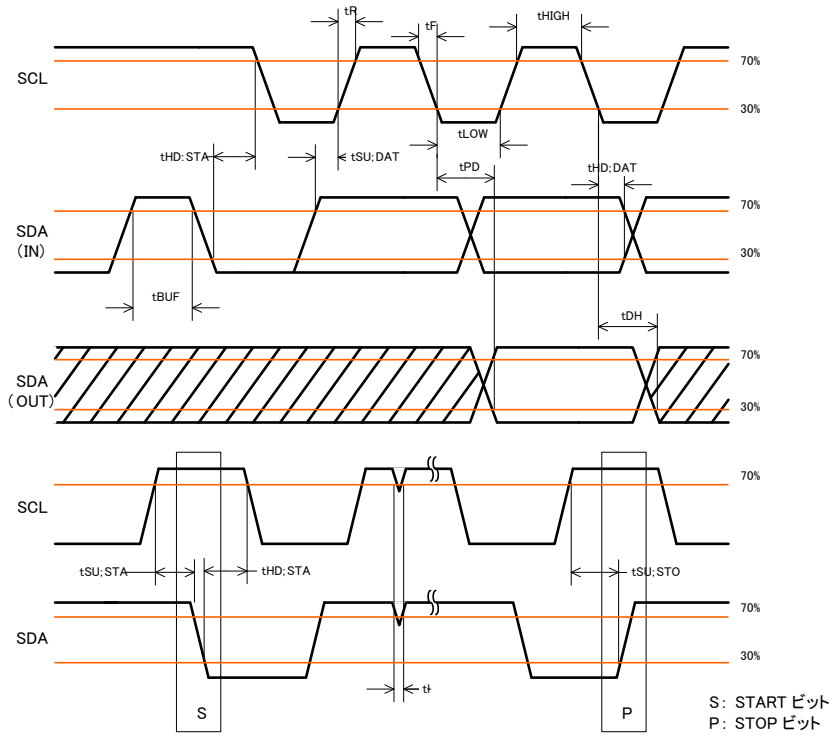


Figure 44. I2C Timing Diagram

・Timing standard values

Parameter	Symbol	NORMAL MODE			FAST MODE			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCL frequency	f SCL	-	-	100	-	-	400	kHz
SCL high time	tHIGH	4.0	-	-	0.6	-	-	us
SCL low time	tLOW	4.7	-	-	1.2	-	-	us
Rise Time	tR	-	-	1.0	-	-	0.3	us
Fall Time	tF	-	-	0.3	-	-	0.3	us
Start condition hold time	tHD；STA	4.0	-	-	0.6	-	-	us
Start condition setup time	tSU；STA	4.7	-	-	0.6	-	-	us
SDA hold time	tHD；DAT	200	-	-	100	-	-	ns
SDA setup time	tSU；DAT	200	-	-	100	-	-	ns
Acknowledge delay time	tPD	-	-	0.9	-	-	0.9	us
Acknowledge hold time	tDH	-	0.1	-	-	0.1	-	us
Stop condition setup time	tSU；STO	4.7	-	-	0.6	-	-	us
Bus release time	tBUF	4.7	-	-	1.2	-	-	us
Noise spike width	TI	-	0.1	-	-	0.1	-	us

Command interface

EEPROM transmission format for data sending and receiving is shown below.

I2C Write format

Start	Slave Address							R/W	A	Register Address	A	DATA	A	Stop
	0	1	0	0	0	0	A0	0	0	00h to 0Ch	0	N-bytes DATA	0	

It can enter further Register from 3 byte by entering data continuously.
DATA after 0Dh is invalid.
Inputted Data reflect to the Register at the ACK output timing.

I2C Read format

1. Read data from DAC Register

Start	Slave Address							R/W	A	Register Address	A	
	0	1	0	0	0	0	A0	0	0	00h to 0Ch	0	
Repeated Start	Slave Address							R/W	A	DATA	A	Stop
	0	1	0	0	0	0	A0	1	0	N-bytes DATA	0	

EEPROM Write format

Transmission format for Write operation of EEPROM (DAC Register) is shown below.

EEPROM Write format

Start	Slave Address							R/W	A	Register Address								A	DATA								A	Stop
	0	1	0	0	0	0	A0	0	0	1	1	1	1	1	1	1	1	0	1	X	X	X	X	X	X	X	0	

D6 to D0 : Don’t care

Automatic EEPROM Read Function at Start-up

Upon BM81110MUW start-up, a reset signal is generated and each register is initialized.
After VL activation is finished, data which is stored in the EEPROM is copied to the registers.
The automatic EEPROM read function at start-up is further explained by the flow chart below.

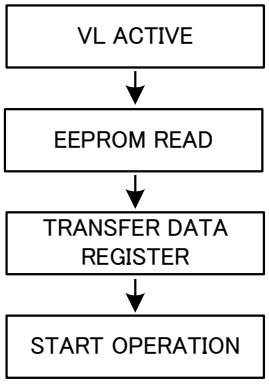


Figure 45. Automatic EEPROM Read Function at Start-up

Content of EEPROM setting

Register Address	Bits	Function	Default(*1)	Resolution
00h	6	Channel Disable Register	00h	-
01h	6	AVDD output voltage setting[5:0]	15.0V [0Fh]	0.1V [13.5V to 19.8V]
02h	4	AVDD HVS voltage setting[3:0]	1.0V [05h]	0.2V [0V to 3.0V]
03h	3	AVDD OCP offset setting[2:0]	0.0A [00h]	0.4A [0A to 2.8A]
04h	1	AVDD soft start time setting[0]	10msec [00h]	10msec [10msec or 20msec]
05h	4	VIO output voltage setting[3:0]	2.5V [03h]	0.1V [2.2V to 3.7V]
06h	5	VCORE output voltage setting[4:0]	1.0V [02h]	0.1V [0.8V to 3.3V]
07h	6	HAVDD output voltage setting[5:0]	7.5V [1Bh]	0.1V [4.8V to 11.1V]
08h	4	VGH_L output voltage setting[3:0]	28V [08h]	1V [20V to 35V]
09h	4	VGH_H offset voltage setting[3:0]	4V [04h]	1V [0V to 15V]
0Ah	2	GPM clamp voltage setting[1:0]	5V [01h]	5V [5V to 15V]
0Bh	4	VGL output voltage setting[3:0]	-7.9V [04h]	0.6V [-14.5V to -5.5V]
0Ch	4	HAVDD HVS voltage setting[3:0]	0.0V [00h]	0.1V [0.0V to 1.5V]
FFh	8	Control Register[7:0]		

*1 Factory value.
*2 Value of default voltage setting. The Soft start time of each output changes depending on the setting voltage.

Channel Disable Register

Register Address = 00h							
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
-	-	VCORE	HAVDD	VGH	VGL	GPM	NTC

0：Enable
1：Disable

Control Register

Register Address	DATA [BIN]	Function
FFh	1xxx_xxxx	Write to EEPROM from DAC Register data.

x：Don't care bit

Register Map

Resister Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	—	—	VCORE	HAVDD	VGH	VGL	GPM	NTC	00h
01h	—	—	AVDD[5:0]						0Fh
02h	—	—	—	—	AVDD HVS [3:0]				05h
03h	—	—	—	—	—	AVDD OCP offset[2:0]			00h
04h	—	—	—	—	—	—	—	AVDD SS	00h
05h	—	—	—	—	VIO [3:0]				03h
06h	—	—	—	VCORE [4:0]					02h
07h	—	—	HAVDD [5:0]						1Bh
08h	—	—	—	—	VGH_L [3:0]				08h
09h	—	—	—	—	VGH_H offset [3:0]				04h
0Ah	—	—	—	—	—	—	GPM clamp [1:0]		01h
0Bh	—	—	—	—	VGL [3:0]				04h
0Ch	—	—	—	—	HAVDD HVS [3:0]				00h
FFh	（ Control Register ）								—

Command Table

	Register Address											
	01	02	03	04	05	06	07	08	09	0A	0B	0C
	[5:0]	[3:0]	[2:0]	[0]	[3:0]	[4:0]	[5:0]	[3:0]	[3:0]	[1:0]	[3:0]	[3:0]
DATA (HEX)	AVDD [V]	AVDD HVS [V]	AVDD OCP offset [A]	AVDD soft start [msec]	VIO [V]	VCORE [V]	HAVDD [V]	VGH_L [V]	VGH_H offset [V]	GPM clamp [V]	VGL [V]	HAVDD HVS [V]
00	13.5	0.0	0.0	10	2.2	0.8	4.8	20	0	-	-5.5	0.0
01	13.6	0.2	0.4	20	2.3	0.9	4.9	21	1	5	-6.1	0.1
02	13.7	0.4	0.8		2.4	1.0	5.0	22	2	10	-6.7	0.2
03	13.8	0.6	1.2		2.5	1.1	5.1	23	3	15	-7.3	0.3
04	13.9	0.8	1.6		2.6	1.2	5.2	24	4		-7.9	0.4
05	14.0	1.0	2.0		2.7	1.3	5.3	25	5		-8.5	0.5
06	14.1	1.2	2.4		2.8	1.4	5.4	26	6		-9.1	0.6
07	14.2	1.4	2.8		2.9	1.5	5.5	27	7		-9.7	0.7
08	14.3	1.6			3.0	1.6	5.6	28	8		-10.3	0.8
09	14.4	1.8			3.1	1.7	5.7	29	9		-10.9	0.9
0A	14.5	2.0			3.2	1.8	5.8	30	10		-11.5	1.0
0B	14.6	2.2			3.3	1.9	5.9	31	11		-12.1	1.1
0C	14.7	2.4			3.4	2.0	6.0	32	12		-12.7	1.2
0D	14.8	2.6			3.5	2.1	6.1	33	13		-13.3	1.3
0E	14.9	2.8			3.6	2.2	6.2	34	14		-13.9	1.4
0F	15.0	3.0			3.7	2.3	6.3	35	15		-14.5	1.5
10	15.1					2.4	6.4					
11	15.2					2.5	6.5					
12	15.3					2.6	6.6					
13	15.4					2.7	6.7					
14	15.5					2.8	6.8					
15	15.6					2.9	6.9					
16	15.7					3.0	7.0					
17	15.8					3.1	7.1					
18	15.9					3.2	7.2					
19	16.0					3.3	7.3					
1A	16.1						7.4					
1B	16.2						7.5					
1C	16.3						7.6					
1D	16.4						7.7					
1E	16.5						7.8					
1F	16.6						7.9					
20	16.7						8.0					
21	16.8						8.1					
22	16.9						8.2					
23	17.0						8.3					
24	17.1						8.4					
25	17.2						8.5					
26	17.3						8.6					
27	17.4						8.7					
28	17.5						8.8					
29	17.6						8.9					
2A	17.7						9.0					
2B	17.8						9.1					
2C	17.9						9.2					
2D	18.0						9.3					
2E	18.1						9.4					
2F	18.2						9.5					
30	18.3						9.6					
31	18.4						9.7					
32	18.5						9.8					
33	18.6						9.9					
34	18.7						10.0					
35	18.8						10.1					
36	18.9						10.2					
37	19.0						10.3					
38	19.1						10.4					
39	19.2						10.5					
3A	19.3						10.6					
3B	19.4						10.7					
3C	19.5						10.8					
3D	19.6						10.9					
3E	19.7						11.0					
3F	19.8						11.1					

: Default Value

① AVDD HVS Voltage Setting (Register Address：02h)
When HVS=High, AVDD becomes AVDD setting voltage + AVDD HVS setting voltage [V].

② VGH _H offset Voltage Setting (Register Address：09h)
When NTC=High, VGH becomes VGH_L setting voltage + VGH_H offset setting voltage [V].

③ HAVDD HVS Voltage Setting (Register Address：0Ch)
When HVS=High, HAVDD becomes HAVDD setting voltage + HAVDD HVS setting voltage [V].

Selecting Application Components

1. Buck Converter

1-1. Selecting the Output LC Constant

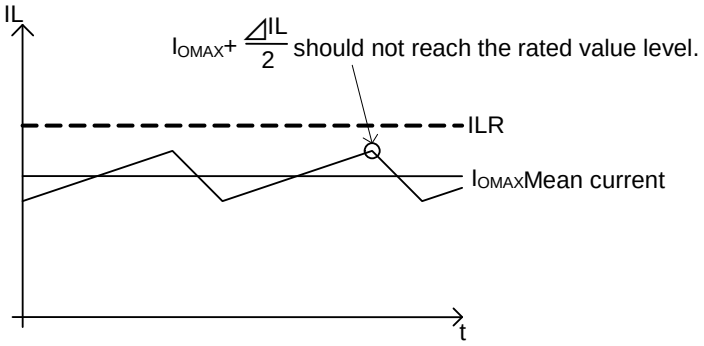


Figure 46. Inductor Current Waveform (Buck Converter)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{OMAX}) of the inductance.
Adjust so that $I_{OMAX} + \Delta I_L / 2$ do not reach the rated current value.

ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (VIN - VO) \times \frac{VO}{VIN} \times \frac{1}{f} [A]$$

where f is the switching frequency

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the coil current exceeds the rated current (I_{LR}), the IC may be damaged.

1-2. Selecting the Input/Output capacitor

The output capacitor (C_O) smoothens the ripple voltage at the output. Select a capacitor that will regulate the output ripple voltage within the specifications.

Output ripple voltage can be obtained by the following equation.

$$\Delta VPP = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2\,Co} \times \frac{VO}{VIN} \times \frac{1}{f}$$

However, since the aforementioned conditions are based on a lot of factors, verify the results using the actual product.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to be installed at the Input side. For this reason, a low ESR capacitor is recommended as an input capacitor with a value more than 10μF and less than 100mΩ ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform margin check using the actual product.

1-3. Selecting the Output rectifier diode

A schottky barrier is recommended as rectifier diode to be used at the output stage of the DC/DC converter. Select carefully in consideration of the maximum inductor current, maximum output voltage and power supply voltage.

Maximum inductor current $I_{OMAX} + \frac{\Delta I_L}{2}$ < Diode Maximum Absolute Current

Maximum input voltage V_{IN} < Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

2. Boost Converter

2-1. Selecting the Output LC Constant

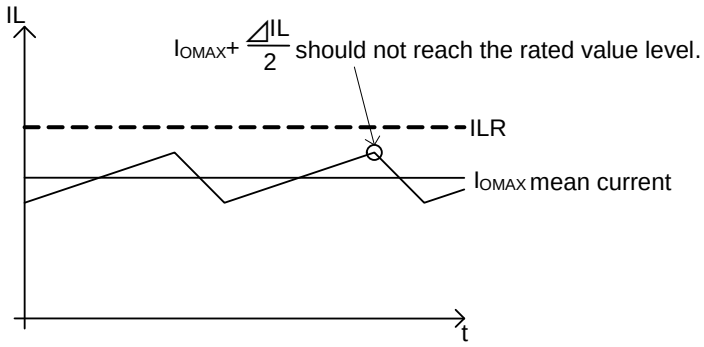


Figure 47. Inductor Current Waveform (Boost Converter)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{INMAX}) of the inductance.
Adjust so that $I_{INMAX} + \Delta I_L / 2$ does not reach the rated current value.

ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} VIN \times \frac{VO - VIN}{VO} \times \frac{1}{f} [A]$$

where f is the switching frequency

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the coil current exceeds the rated current (I_{LR}), this may damage the IC.

2-2. Selecting the Output capacitor

The output capacitor (C_O) smoothens the ripple voltage at the output. Select a capacitor that will regulate the output ripple voltage within the specifications.

Output ripple voltage can be obtained by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{f \times CO} \times \frac{VIN}{VO} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right)$$

However, since the aforementioned conditions are based on a lot of factors, verify the results using the actual product.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required at the Input side. For this reason, a low ESR capacitor is recommended as an input capacitor with a value more than 10μF and less than 100mΩ ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

2-3. Setting phase compensation

Phase setting procedure.
Stable negative feedback condition is achieved as follows:

・When the gain is set to 1 (0 dB), phase delay should not be more than 150°.Consequently, phase margin should not be less than 30°.
Also, since DC/DC converter applications are sampled according to the switching frequency, the whole system GBW should be set to not more than 1/10 of the switching frequency. The target characteristics of the applications can be summarized as follows:

・When the gain is set to 1 (0 dB), the phase delay should not be more than 150°.
And phase margin should not be less than 30°.
・The frequency when the gain is set to 0 dB should not be more than 1/10 of the switching frequency.

The responsiveness is determined by the GBW limitation. Consequently, to increase the circuit response, higher switching frequencies are required.
AVDD is in current mode control. The current mode control is a two-pole single-zero system. The poles are formed by the error amplifier and load while added zero is for phase compensation.
By placing poles appropriately, the circuit can maintain good stability and transient load response.
Board plot diagram of general DC/DC converter is described below. At point (a), gain starts falling via the output impedance of the error amplifier and forms a pole by capacitor C_{cp}. When point (b) is reached, a zero is formed by resistor R_{pc} and capacitor C_{cp} to cancel the pole by loading and balancing the variation of Gain and phase.
The GBW (i.e., frequency when the gain is 0 dB) is determined by phase compensation capacitor connected to the error amplifier. If GBW is to be reduced, increase the capacitance of the capacitor.

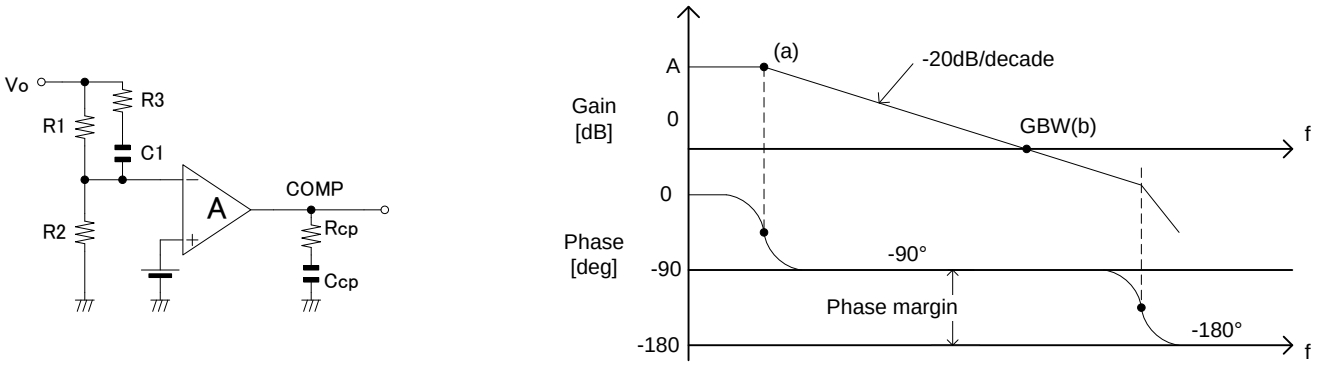


Figure 48. Setting phase compensation

Formed Zero (fz1) by R_{cp} resistor and C_{cp} Capacitor are shown by using the following equation.
And also, Feed-forward capacitor C1 and R1 resistor both create Formed Zero (fz2) and it is used as boosting phase margin in the limited frequency area.

$$\text{Phase lead} \quad fZ1 = \frac{1}{2\pi CcpRcp} \text{ [Hz]}$$

$$\text{Phase lead} \quad fZ2 = \frac{1}{2\pi C1R1} \text{ [Hz]}$$

The formed zero fz2 phase compensation is built-in to the IC.

3. Positive Charge Pump : VGH

3-1. Selecting the Output rectifier diode

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Maximum output current	I_{OMAX}	<	Diode Maximum Absolute Current
Maximum output voltage	AVDD	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

3-2. Selecting the Output PNP transistor

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Boost Converter Duty	$D = \frac{AVDD - VIN}{AVDD}$	
Maximum Output current	$\frac{I_{OMAX}}{D}$	＜Transistor Maximum Absolute Current
Power supply voltage	AVDD x 2	＜Transistor Maximum Absolute Voltage
DC gain	IOMAX / IBASE	＜Transistor hfe
Power dissipation (Doubler Mode)	(2 x AVDD – VGH – 2 x Vf) x IOUT	＜Transistor Power dissipation
Power dissipation (Tripler Mode)	(3 x AVDD – VGH – 4 x Vf) x IOUT	＜Transistor Power dissipation
Maximum DRVP current	IBASE（5mA）	

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

3-3. Selecting the base emitter resistor

100kΩ base-emitter resistor used to ensure proper operation.

3-4. Selecting the flying capacitor and the switch node resistor

0.1uF to 0.47uF flying capacitor and 1Ω to 20Ω resistor are appropriate for most applications.

3-5. Selecting the output capacitor

A 10uF ceramic capacitor is appropriate for most applications. More capacitor can be added to improve the load transient response.

4. Negative Charge Pump : VGL

4-1. Selecting the Output rectifier diode

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Maximum output current	I_{OMAX}	<	Diode Maximum Absolute Current
Maximum switching voltage	VIN	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

4-2. Selecting the Output NPN transistor

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Converter Duty	$D = \frac{VIN-VIO}{VIN}$ or $\frac{VIN}{AVDD}$	
Maximum output current	$\frac{I_{OMAX}}{D}$	＜Transistor Maximum Absolute Current
Power supply voltage	VIN	＜Transistor Maximum Absolute Voltage
DC gain	IOMAX / IBASE	＜Transistor hfe
Power dissipation (Doubler Mode)	(VIN - ｜ VGL ｜ – 2 x Vf) x IOUT	
Or	(AVDD - ｜ VGL ｜ – 2 x Vf) x IOUT	＜Transistor Power dissipation
Maximum DRVN current	IBASE（5mA）	

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

4-3. Selecting the base emitter resistor

100kΩ base-emitter resistor used to ensure proper operation.

4-4. Selecting the flying capacitor and the switch node resistor

0.1uF to 0.47uF flying capacitor and 1Ω to 20Ω resistor are appropriate for most applications.

4-5. Selecting the output capacitor

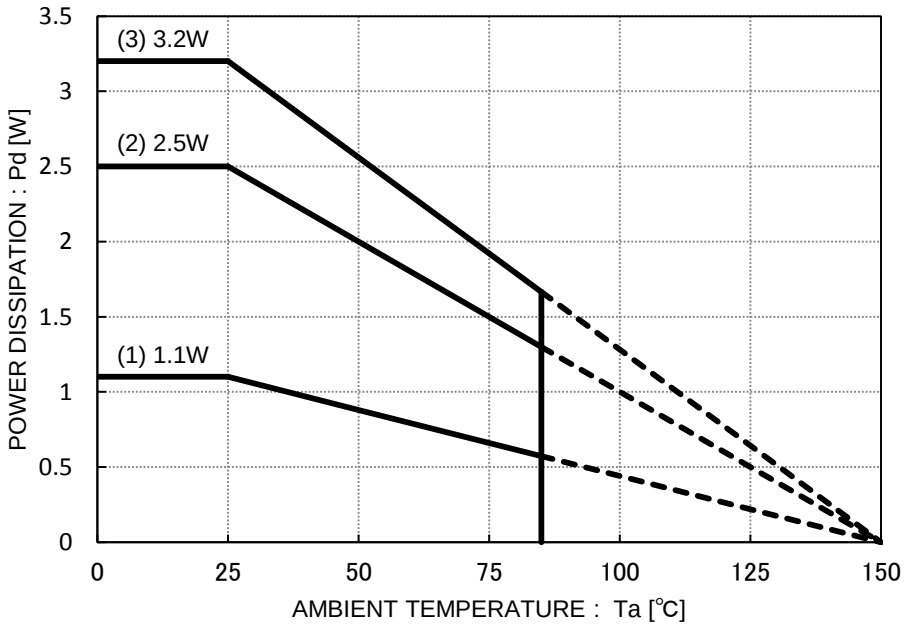
A 10uF ceramic capacitor is appropriate for most applications. More capacitor can be added to improve the load transient response.

Layout Guideline

DC/DC converter switching line must be as short and thick as possible to reduce line impedance. If the wiring is long, ringing caused by switching would increase and this may exceed the absolute maximum voltage ratings. If the parts are located far apart, consider inserting a snubber circuit.

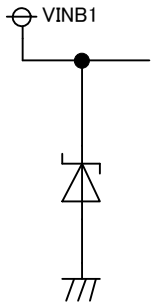
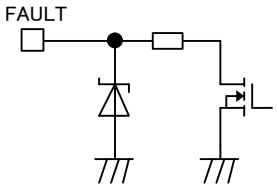
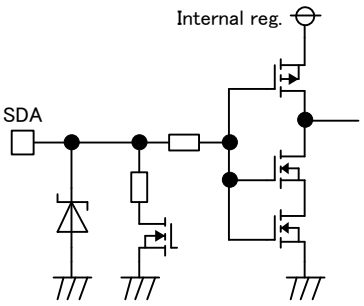
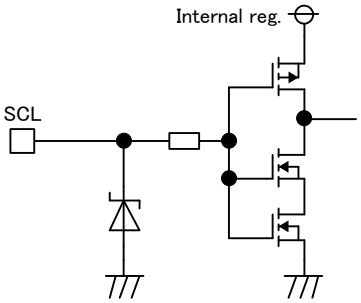
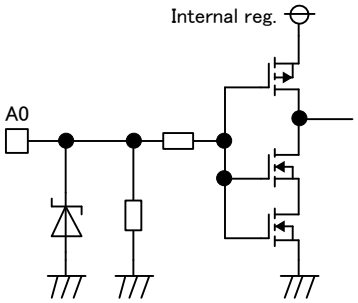
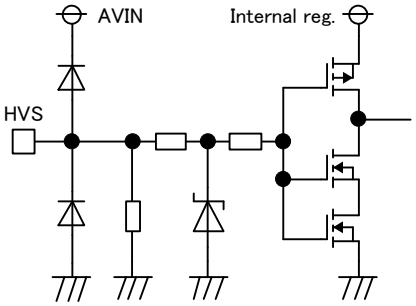
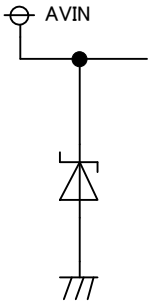
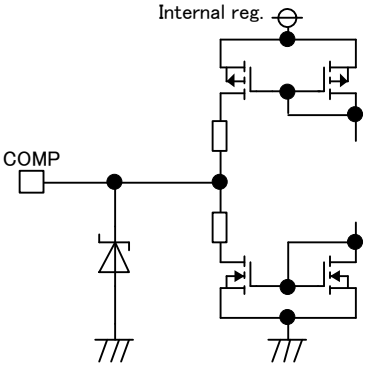
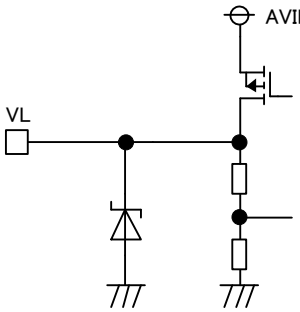
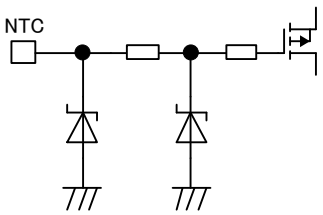
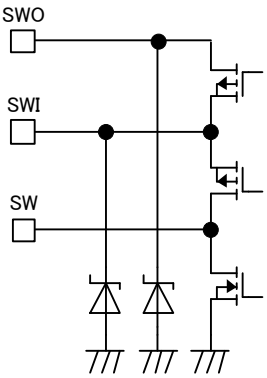
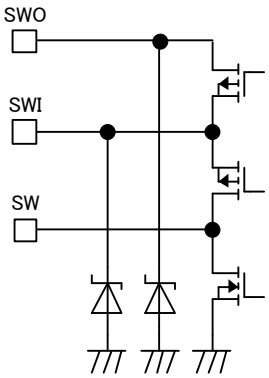
The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective. When there is unused area on PCB, please arrange the copper foil plain of DC nodes, such as GND, VIN and VOUT for helping heat dissipation of IC or circumference parts.

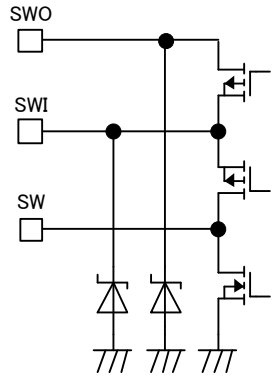
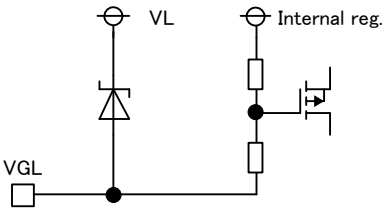
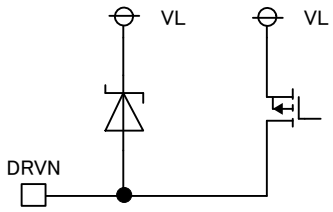
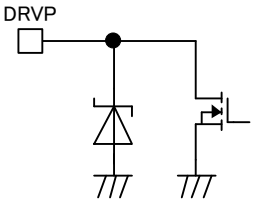
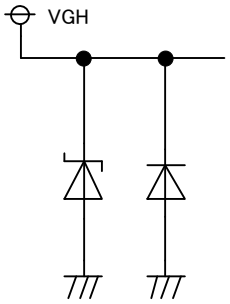
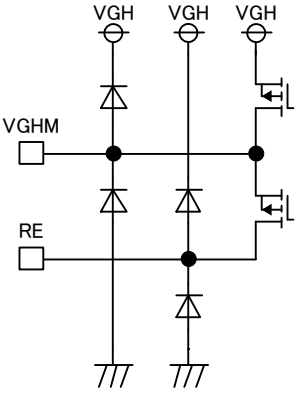
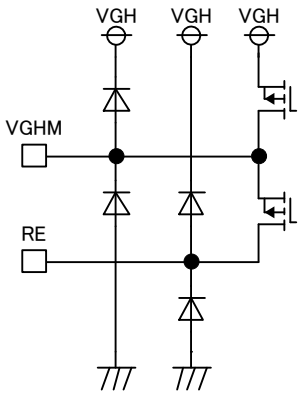
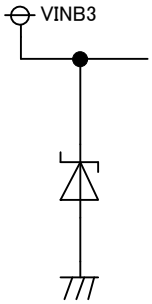
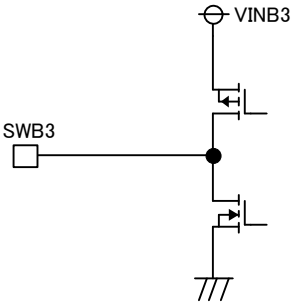
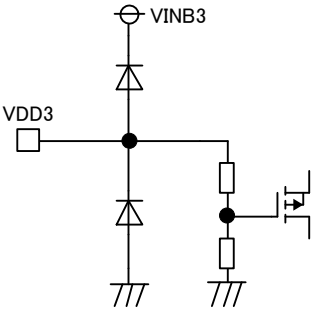
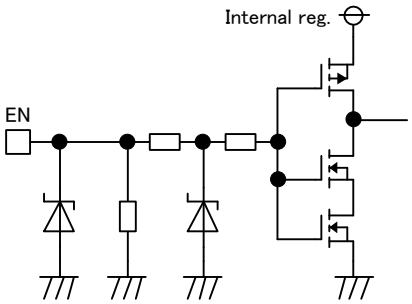
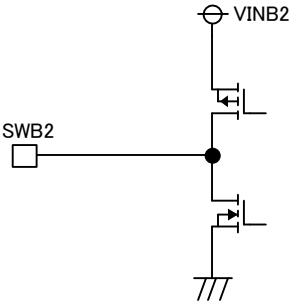
Power Dissipation

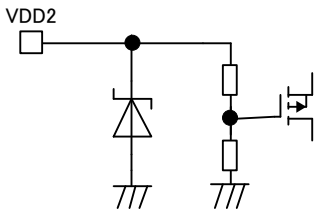
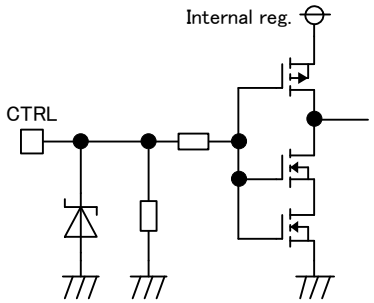
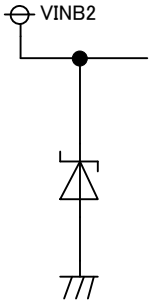
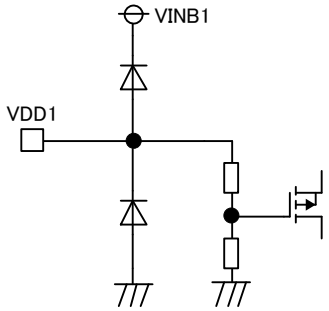
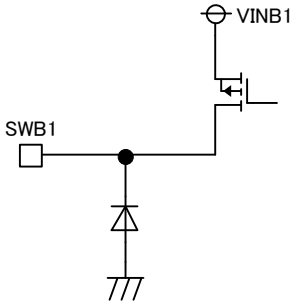


VQFN40W6060A Package
On 4-layer 114.3mm × 74.2mm × 1.6mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 74.2 mm × 74.2 mm)
(3) 4-layer board (The 2nd, 3rd layers and backside copper foil area 74.2 mm × 74.2 mm)

I/O Equivalence Circuit

1, 2.VINB1	3. FAULT	4.SDA
		
5.SCL	6.A0	7.HVS
		
8.AVIN	10.COMP	11.VL
		
12.NTC	15, 16.SW	17.SWI
		

18.SWO	20.VGL	21.DRVN
		
22.DRVP	23.VGH	24.VGHM
		
25.RE	26.VINB3	28.SWB3
		
30.VDD3	31.EN	33.SWB2
		

34.VDD2	35.CTRL	36.VINB2
		
37.VDD1	**38,39.SWB1**	
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

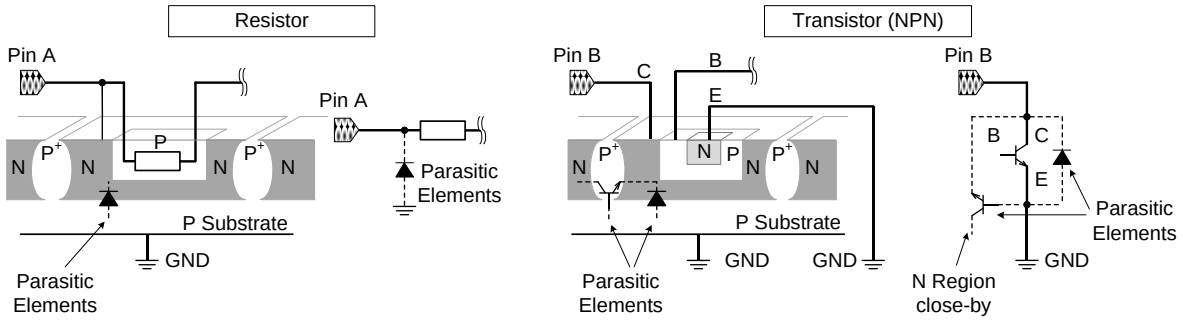


Figure 49. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

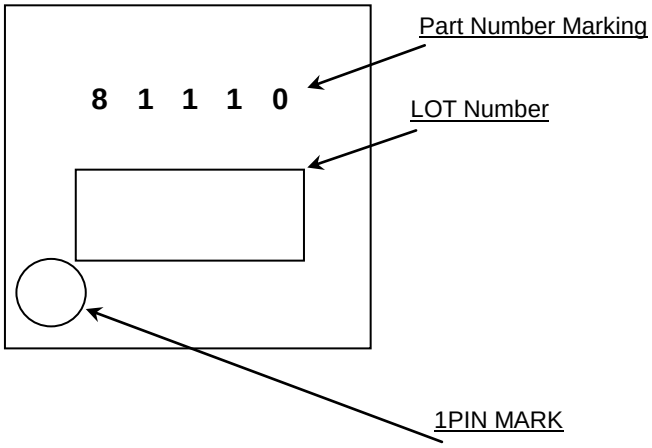
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B M 8 1 1 1 0 M U W	ZE2
Part Number	Package MUW: VQFN40W6060A
	Packaging and forming specification ZE2: Embossed tape and reel

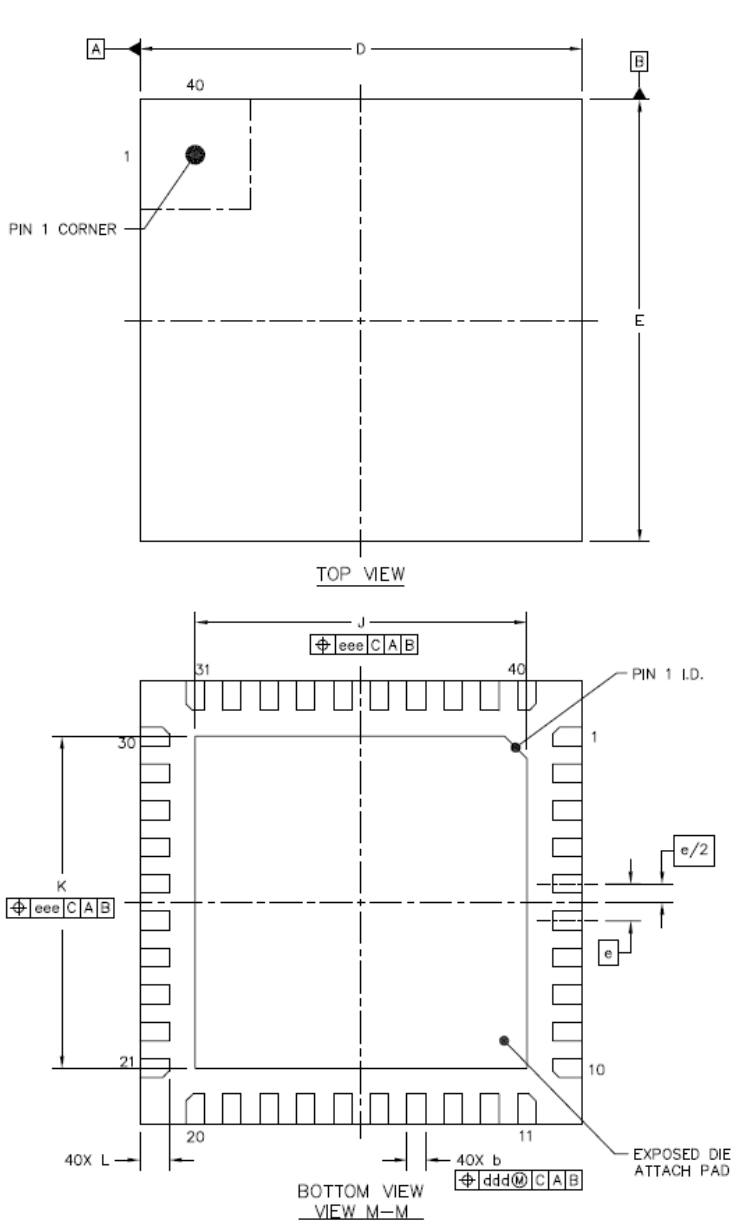
Marking Diagram

VQFN40W6060A (TOP VIEW)



Physical Dimension Tape and Reel Information

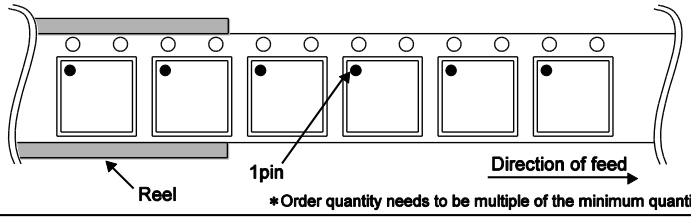
Package Name	VQFN40W6060A



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	5.95	6	6.05
	Y	E	5.95	6	6.05
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	4.4	4.5	4.6
	Y	K	4.4	4.5	4.6
LEAD LENGTH		L	0.35	0.4	0.45
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	ZE2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Contents
2013.09.11	001	New release
2015.08.10	002	P.1, 22, 23 Application circuit and Application circuit components list update

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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Mouser Electronics

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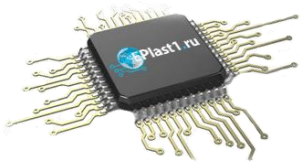
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.