STP16CPC26

Low voltage 16-bit constant current LED sink driver

Datasheet — production data

Features

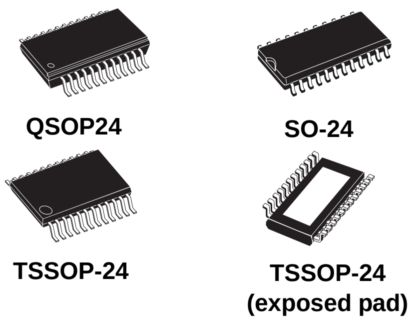
- 16 constant current output channels
- Adjustable output current through external resistor
- Output current: 5 mA to 90 mA
- ±1% typical current accuracy bit to bit
- Max clock frequency: 30 MHz
- 20 V current generators rated voltage
- 3 - 5.5 V power supply
- Thermal shutdown for overtemperature protection

Applications

- Video display panel LED driver
- Special lighting

Description

The STP16CPC26 is a monolithic, low voltage, 16-bit constant current LED sink driver. The device contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. In the output stage sixteen regulated current generators provide 5 mA to 90 mA constant current to drive LEDs. The current is externally adjusted through a resistor. LED brightness can be adjusted from 0% to 100% via $\overline{OE}$ pin.



The STP16CPC26 guarantees a 20 V driving capability, allowing users to connect more LEDs in series to each current source.

The high 30 MHz clock frequency makes the device suitable for high data rate transmission.

The thermal shutdown (170°C with about 15°C hysteresis) assures protection from overtemperature events.

The STP16CPC26 is housed in four different packages: QSOP24, SO-24, TSSOP-24 and HTSSOP-24 (with exposed pad).

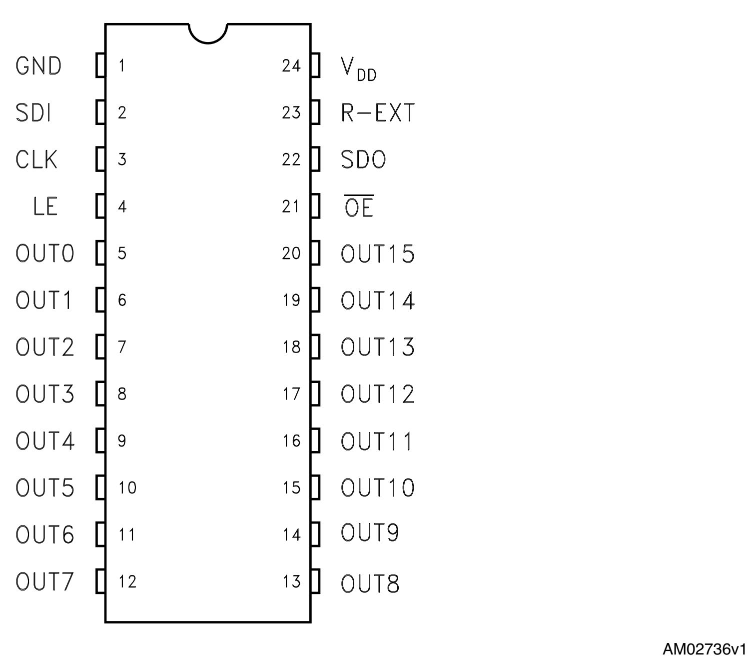
Table 1. Device summary

Order codes	Package	Packaging
STP16CPC26MTR	SO-24	1000 parts per reel
STP16CPC26TTR	TSSOP24	2500 parts per reel
STP16CPC26XTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPC26PTR	QSOP24	2500 parts per reel

Contents

1 Pin description

Figure 2. Pin connection



Note: The exposed-pad (if present) should be electrically connected to a metal land electrically isolated or connected to ground.

Table 2. Pin description

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	90	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	1600	mA
ESD	Electrostatic discharge protection HBM human body model	±2	kV
f_{CLK}	Clock frequency	30	MHz

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter		Value	Unit
T_A	Operating free-air temperature range		-40 to +125	°C
T_{OPR}	Operating temperature range		-40 to +150	
T_{STG}	Storage temperature range		-55 to +150	
R_{thJA}	Thermal resistance junction-case (1)	SO-24	60	°C/W
		TSSOP24	85	
		TSSOP24(2)	37.5	
		QSOP24	72	

1. According with JEDEC standard 51-7B.
2. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

3 Electrical characteristics

V_{DD} = 3.3 V - 5 V, T_A = 25°C, unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Vdd	Supply voltage		3		5.5	V
V_{IH}	Input voltage high Level		0.8*Vdd	-	Vdd	
V_{IL}	Input voltage low Level		GND	-	0.2*Vdd	
V_{OL}	Serial data output voltage (SDO) [1]	I_{OH} =- 1mA I_{OL} =+ 1mA	-	-	0.4	
V_{OH}			V_{DD} -0.4	-	-	
I_{OH}	Output leakage current	Vo = 20V, Outn = OFF	-	-	0.5	μA
ΔI_{OL1}	Current accuracy channel to channel [2] [3]	Vds=0.3V, Rext=900Ω, I_{OL} = 22mA	-	±1	±3	%
ΔI_{OL2}		Vds=0.6V, Rext=360Ω, I_{OL} = 55mA	-	±1	±3	
ΔI_{OL3}	Current accuracy device to device [2]	Vds=0.3V, Rext=900Ω, I_{OL} = 22mA	-	-	±6	%
ΔI_{OL4}		Vds=0.6V, Rext=360Ω, I_{OL} = 55mA	-	-	±6	
R_{IN}(up)	Pull-up resistor for OE pin		250	500	800	KΩ
R_{IN}(down)	Pull-down resistor for LE pin		250	500	800	
IDD(OFF1)	Supply current (OFF)	REXT = OPEN OUT 0 to 15 = OFF	-	3	7	mA
IDD(OFF2)		REXT = 900Ω OUT 0 to 15 = OFF	-	7	10	
IDD(OFF3)		REXT = 360Ω OUT 0 to 15 = OFF	-	11	13.5	
IDD(ON1)	Supply current (ON)	REXT = 900Ω OUT 0 to 15 = ON	-	7	11	
IDD(ON2)		REXT = 360 Ù OUT 0 to 15 = ON	-	11	15	
%/dV_{DS}	Output current vs. output voltage regulation[4]	V_{DS} from 1.0V to 3.0V Io=22mA Io=55mA	-	±0.1	-	%/V
%/dV_{DD}	Output current vs. supply voltage regulation[4]	Io=22mA; V_{DS}=0.3V Io=55mA; V_{DS}=0.6V	-	±1	-	%/V
Tsd	Thermal shutdown		-	170	-	°C
Tsd-hy	Thermal shutdown hysteresis[4]		-	15	20	

1. Specification referred to T_J from -40 °C to +125 °C. Specification over the -40 to +125 °C T_J temperature range are assured by design, characterization and statistical correlation.
2. Tested with just one output ON.
3. $\Delta_{IOL+} = ((I_{OLmax} - I_{OLmean}) / I_{OLmean})*100$, $\Delta_{IOL-} = ((I_{OLmin} - I_{OLmean}) / I_{OLmean})*100$, where $I_{OLmean} = (I_{OLout1} + I_{OLout2} + \ldots + I_{OLout16}) / 16$
4. Guaranteed by design.

V_{DD} = 3.3 V - 5 V, Tj = 25°C, unless otherwise specified

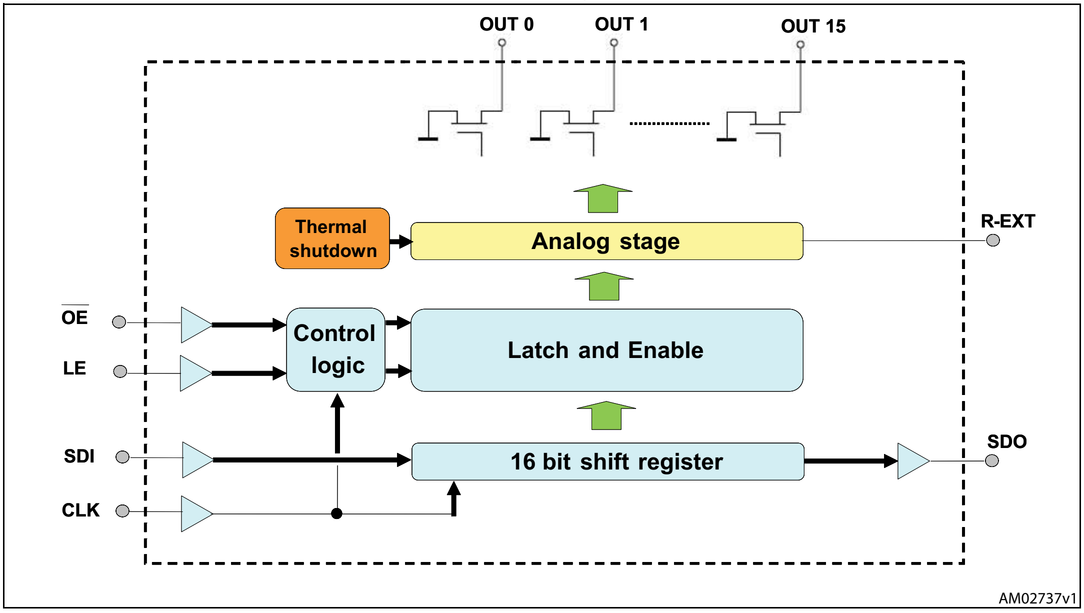
Table 6. Switching characteristics

Symbol	Parameter		Conditions		Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency				-	-	30	MHz
t_{PLH1}	CLK - OUTn	Propagation delay time (“L” to “H”)	VDS = 0.8 V VIH= VDD VIL= GND Rext = 900 Ohm RL = 50 Ohm CL=10pF		-	100	-	ns
t_{PLH2}	LE - OUTn				-	100	-	
t_{PLH3}	OE – OUTn				-	100	-	
t_{PLHa}	CLK - SDO			VDD=3.3V	-	30	-	
t_{PLHb}				VDD=5V	-	20	-	
t_{PHL1}	CLK - OUTn	Propagation delay time (“H” to “L”)			-	28	-	
t_{PHL2}	LE - OUTn				-	28	-	
t_{PHL3}	OE – OUTn				-	25	-	
t_{PHLa}	CLK - SDO			VDD=3.3V	-	30	-	
t_{PHLb}				VDD=5V	-	20	-	
$t_{w(CLK)}$	CLK	Pulse width			20	-	-	
$t_{w(L)}$	LE				20	-	-	
$t_{w(OE)}$	OE				150	-	-	
$t_{su(L)}$	Setup time for LE				5	-	-	
$t_{h(L)}$	Hold time for LE				5	-	-	
$t_{su(D)}$	Setup time for SDI				5	-	-	
$t_{h(D)}$	Hold time for SDI				10	-	-	
tr(1)	Maximum CLK rise time				-	-	5000	
tf(1)	Maximum CLK fall time				-	-	5000	
t_{or1a}	Output rise time of Vout		VIH= VDD, VIL= GND VDS = 0.8V, RL = 50 Ohm CL=10pF , Iout= 22mA	VDD=3.3V	-	95	-	
t_{or1b}				VDD=5V	-	85	-	
t_{of1a}	Output fall time of Vout			VDD=3.3V	-	40	-	
t_{of1b}				VDD=5V	-	25	-	
t_{or2a}	Output rise time of Vout		VIH= VDD, VIL= GND VDS = 0.8V, RL = 50 Ohm CL=10pF , Iout= 55mA	VDD=3.3V	-	80	-	
t_{or2b}				VDD=5V	-	70	-	
t_{of2a}	Output fall time of Vout			VDD=3.3V	-	40	-	
t_{of2b}				VDD=5V	-	30	-	
I_{out-ov}	Output current turn-on overshoot		VDS = 0.6 to 3V CL=10pF; Iout= 5 to 60mA		-	-	0	%

1. If devices are connected in cascade and tr or tf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices

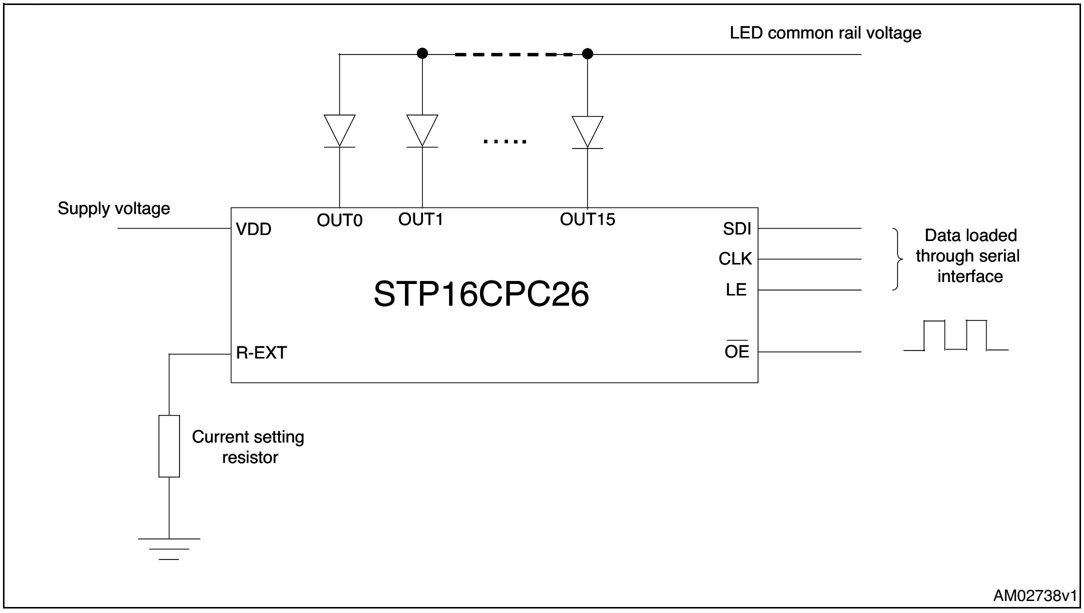
4 Simplified internal block diagram

Figure 3. STP16CPC26 simplified block diagram



5 Typical application circuit

Figure 4. Typical application circuit



6 Equivalent circuits for inputs and outputs

Input terminals LE and $\overline{OE}$ have pull-down and pull-up connection respectively. CLK and SDI must be connected to external circuit to fix the logic level.

Figure 5. $\overline{OE}$ terminal

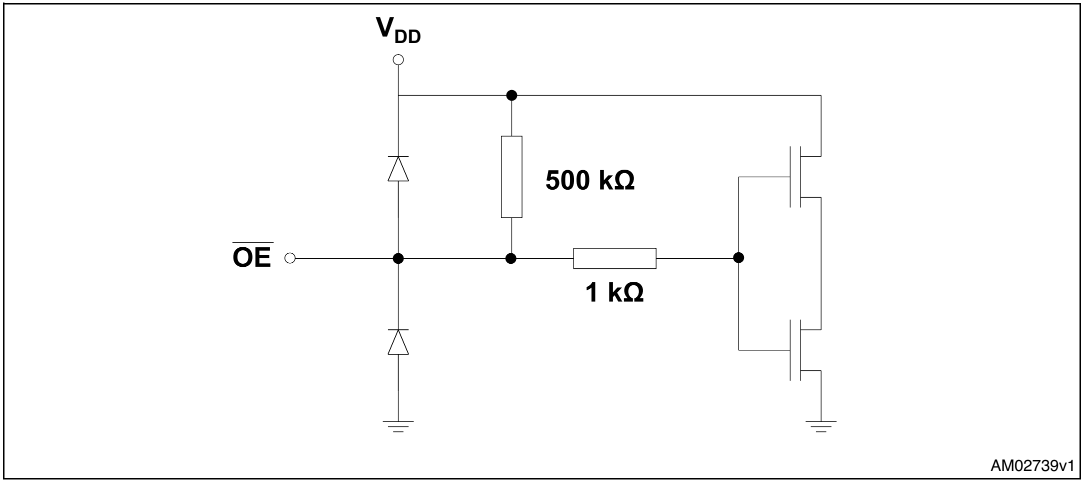


Figure 6. LE terminal

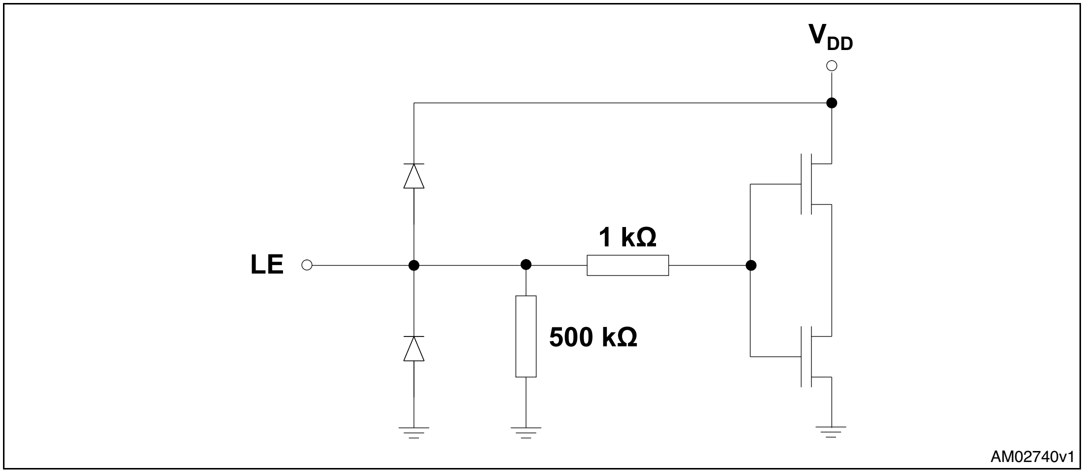


Figure 7. CLK, SDI terminal

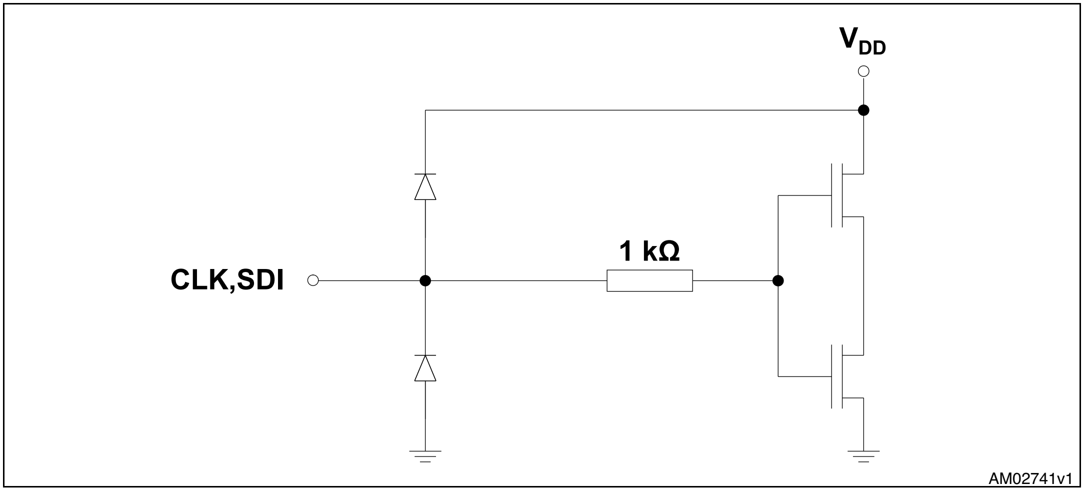
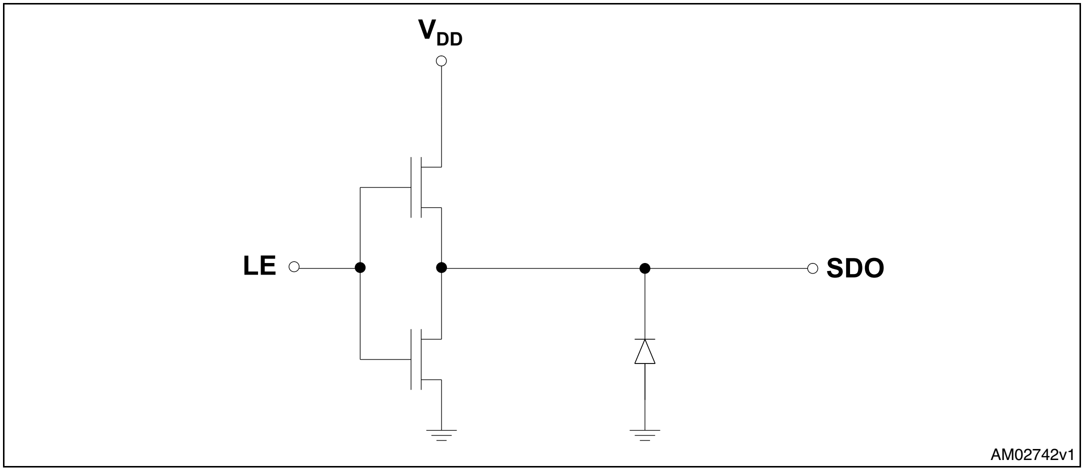


Figure 8. SDO terminal



7 Typical test circuits

Figure 9 and *Figure 10* show respectively the typical test circuit used measuring electrical (e.g. input voltage high/low level, output leakage current, supply current, etc.) and switching characteristics (propagation delays, set-up and hold time, rise and fall time of V_{OUT}, etc.).

The resistor R_L and capacitor C_L in parallel connected to each output in *Figure 9* simulate a LED behavior.

Figure 9. Typical test circuit for electrical characteristics

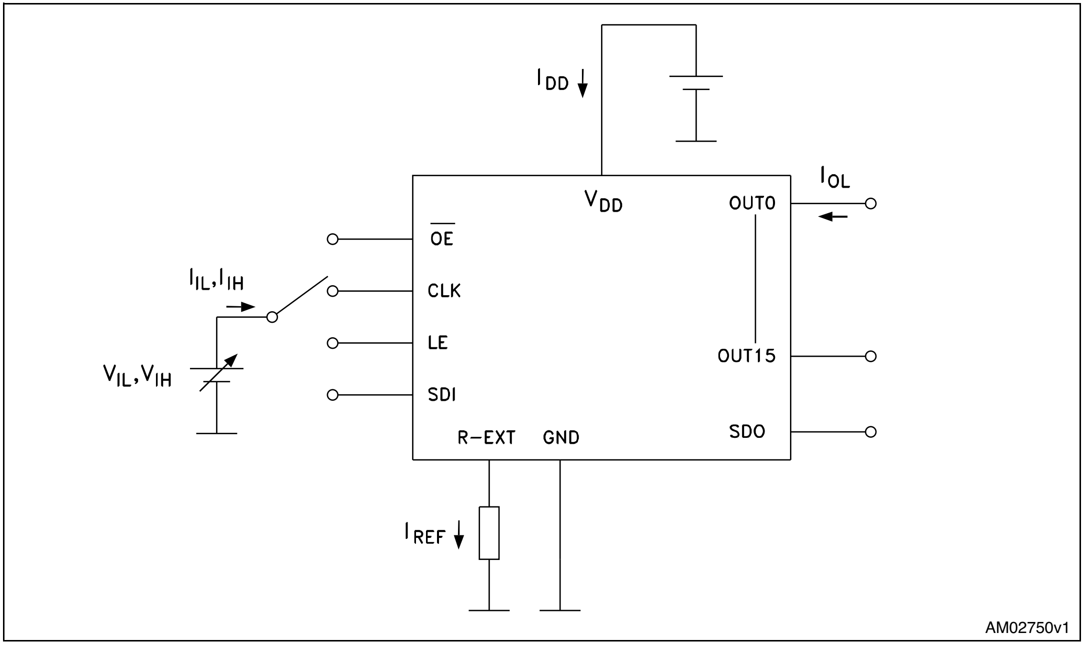
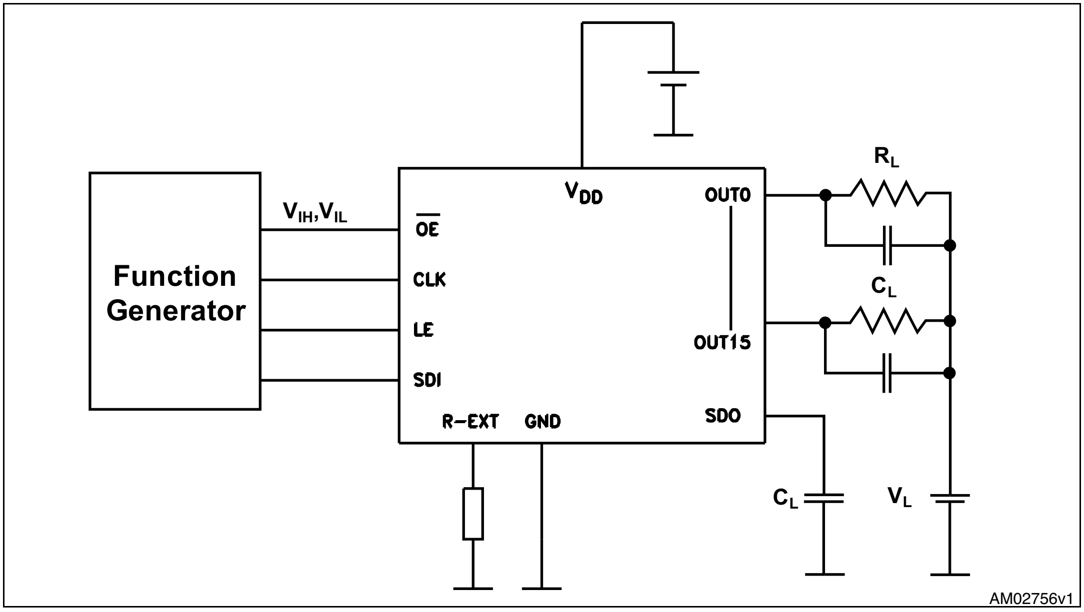


Figure 10. Typical test circuit for switching characteristics



8 Timing diagrams

The timing diagram shown in *Figure 11* and the truth table in *Table 7* explain how to send data to the device. This can be summarized in the following points:

- LE and $\overline{\text{OE}}$ are level sensitive and not synchronized with the CLK signal
- When LE is at low level, the latch circuit holds previous data
- If LE is high level, data present in the shift register are latched
- When $\overline{\text{OE}}$ is at low level, the status of the outputs OUT0 to OUT15 depends on the data in the latch circuits
- With $\overline{\text{OE}}$ at high level, all outputs are switched off independently on the data stored in the latch circuits
- Every rising edge of the CLK signal, a new data on SDI pin is sampled. This data is loaded into the shift register, whereas a bit is shifted out from SDO.

Figure 11. Timing diagram

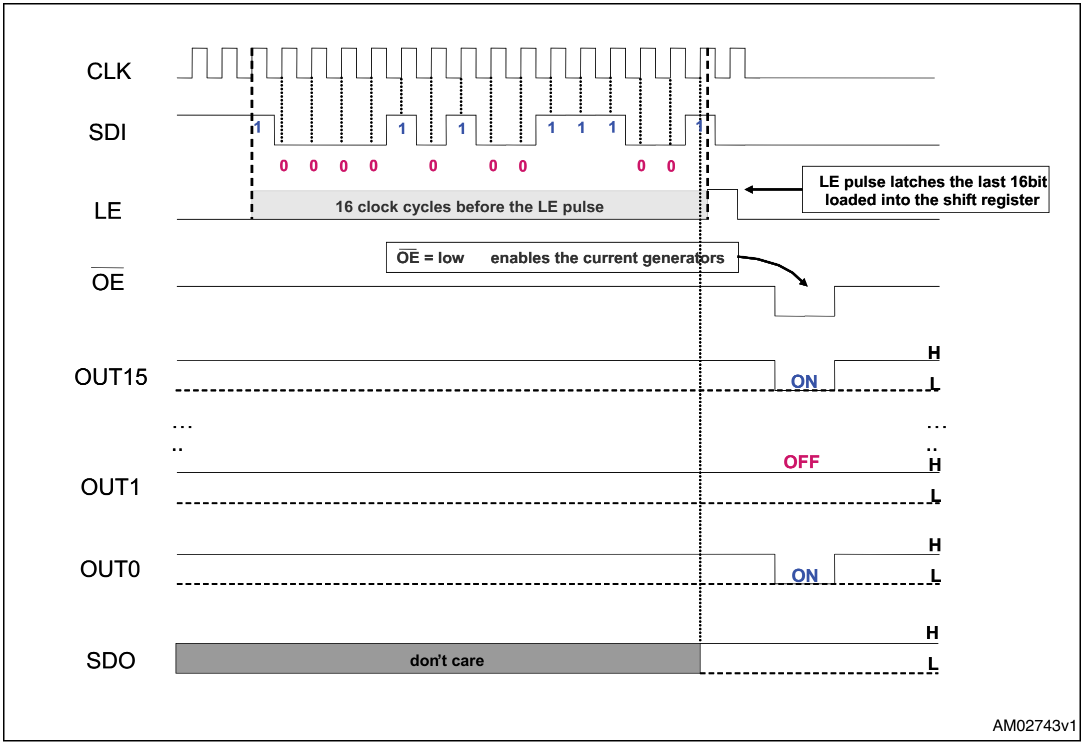
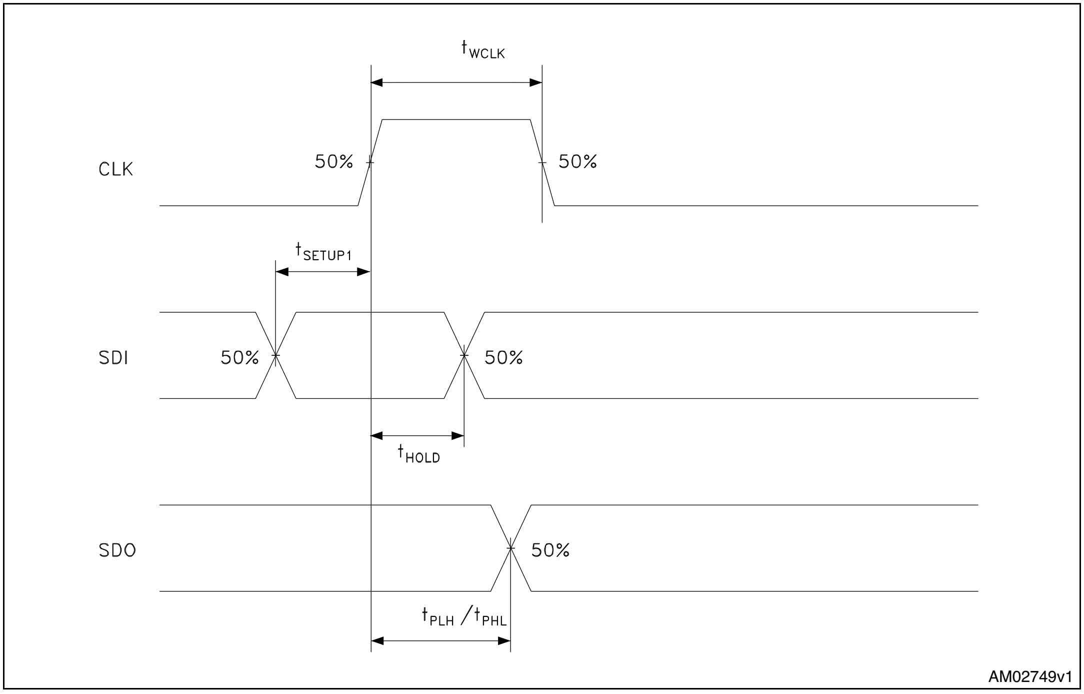


Table 7. Truth table

CLOCK	LE	$\overline{OE}$	Serial-IN	OUT0 .... OUT7 .... OUT15[(1)]	SDO
↑	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
↑	L	L	Dn + 1	No change	Dn - 14
↑	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
↓	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
↓	X	H	Dn + 3	OFF	Dn - 13

1. OUTn = ON when Dn = H, OUTn = OFF when Dn = L

Figure 12. Timing for clock signal, serial-in and serial out data



The correct sampling of the data depends on the stability of the data at SDI on the rising edge of the clock signal and it is assured by a proper data setup and hold time (t_{SETUP1} And t_{HOLD}), as shown in *Figure 12*. The same figure shows the propagation delay from CLK to SDO (t_{PLH}/t_{PHL}).

Figure 13 describes the setup times for LE and $\overline{OE}$ signals (t_{SETUP2} and t_{SETUP3} respectively), the minimum duration of these signals (t_{WLAT} and t_{WENA} respectively) and the propagation delay from CLK to OUT_n, LE to OUT_n and OE to OUT_n (t_{PLH1}/t_{PHL1}, t_{PLH2}/t_{PHL2} and t_{PLH3}/t_{PHL3} respectively).

Finally *Figure 14* defines the turn-on and turn-off time (t_r and t_f) of the current generators.

Figure 13. Timing for clock signal serial-in data, latch enable, output enable and outputs

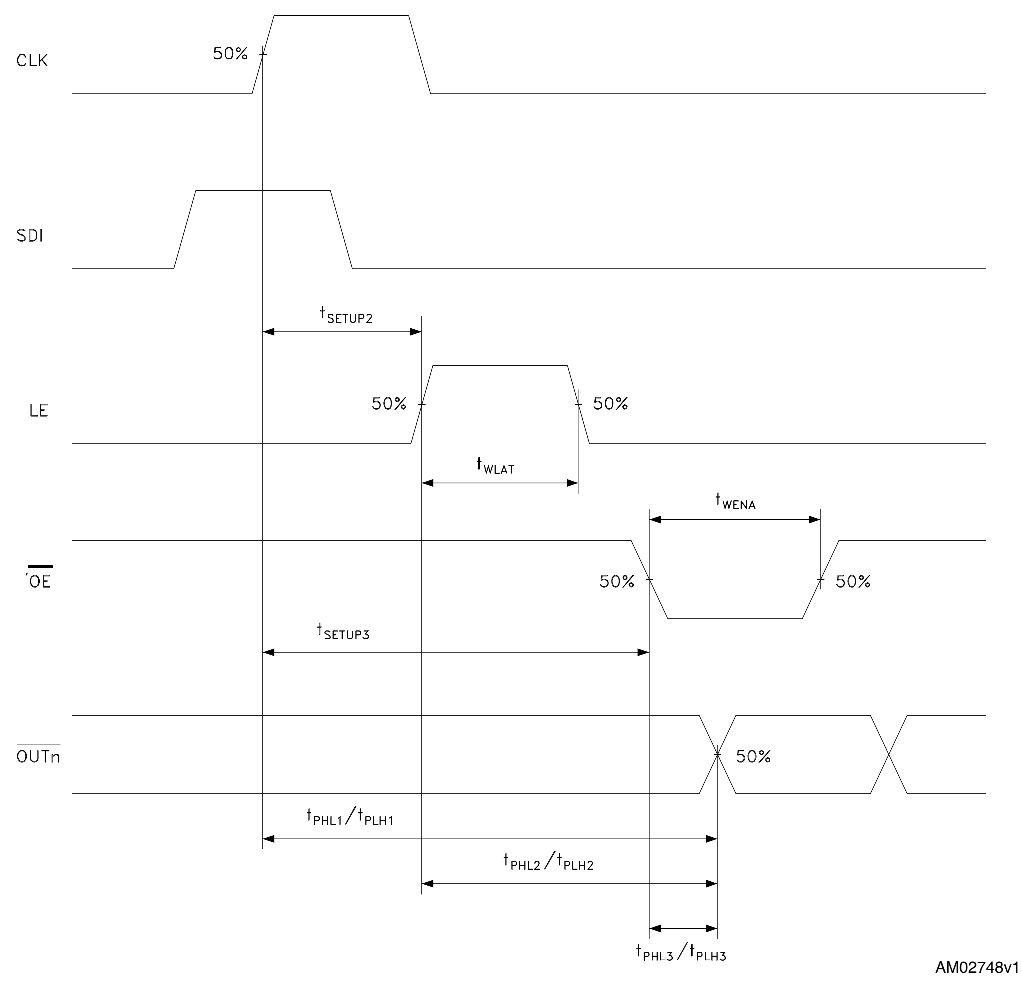
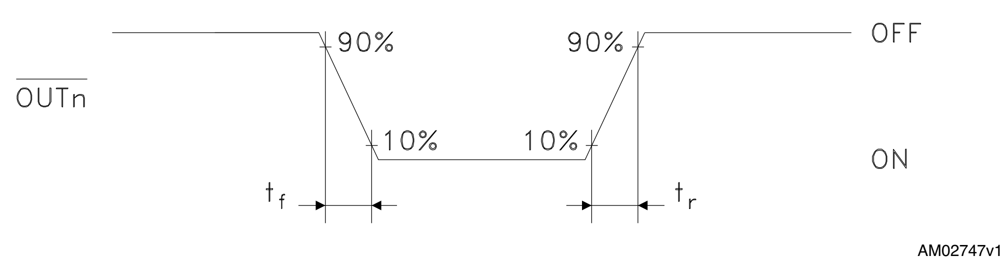


Figure 14. Outputs



9 Current generators characteristics

9.1 Current setting

The current of all outputs is programmed through an external resistor connected to R-EXT pin, as shown in *Figure 15*.

The curve in *Figure 16* describes the relation between the current and the resistor connected to R-EXT pin, whereas the *Table 8* shows how to set some typical current values.

Figure 15. Resistor for current programming

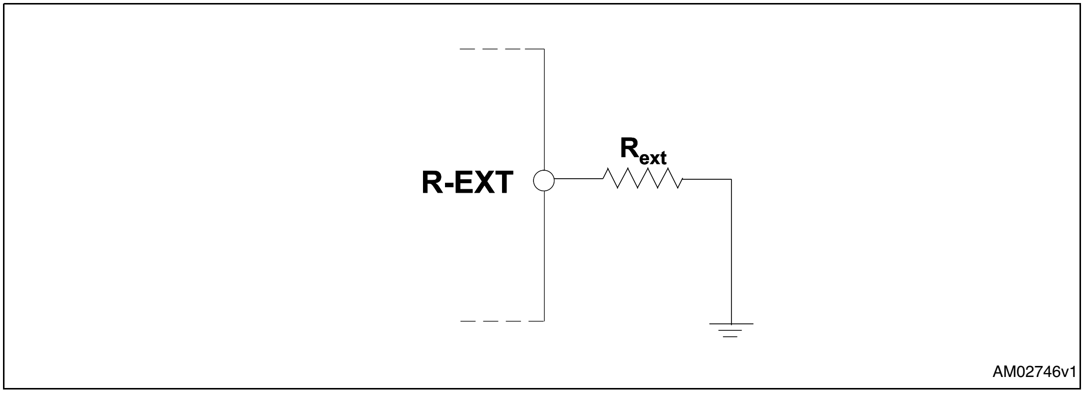


Figure 16. Output current vs R-EXT resistor

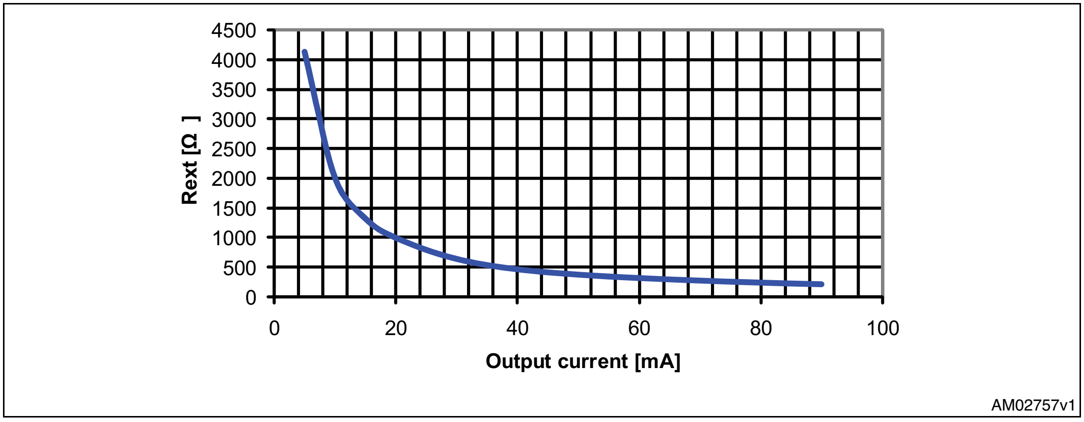


Table 8. Recommended values of Rext for some output current value

Output current [mA]	R_{ext} [Ω]	Closer standard value (E24 series) [Ω]
5	4129	4300
10	2005	200
20	999	1000
40	471	470
60	322	330
90	217	220

9.2 Current accuracy

A typical current accuracy of ±1% (±3% maximum) between channels is guaranteed at 22 mA and 55 mA output current (refer to *Table 6*) and ± 6% (maximum) current accuracy between ICs.

9.3 Generators voltage drop

In order to correctly regulate the current, a minimum dropout voltage must be assured across the current generators.

Figure 17 and *Table 9* provides just an indicative idea about the dropout voltage to assure over the current range. However it is recommended to use value of V_{DROP} slightly higher than those indicated in *Figure 17* and *Table 9*.

Figure 17. Dropout voltage vs output current

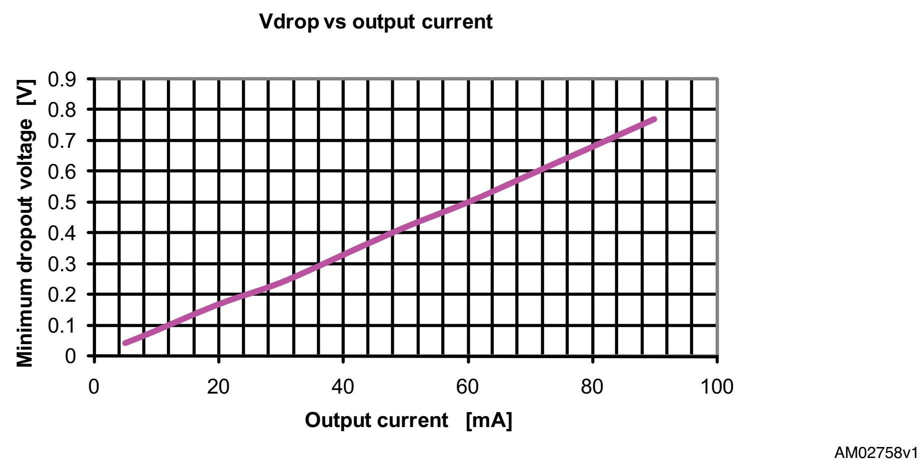


Table 9. Dropout voltage vs output current

Output current [mA]	V_{DROP} @ 3.3V [mV]	V_{DROP} @ 5V [mV]
5	44	44
10	85	85
20	170	170
40	350	330
60	530	500
90	820	770

10 Thermal shutdown

The STP16CPC26 is featured with a thermal shutdown. This protection is triggered if the junction temperature reaches 170°C. When the thermal shutdown is activated, all outputs are turned off independently on the data latched.

Once the temperature decreases (thermal shutdown hysteresis is typically 15°C), the outputs are enabled again and the device keeps on working.

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 10. QSOP-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.54	1.62	1.73	0.061	0.064	0.068
A1	0.1	0.15	0.25	0.004	0.006	0.010
A2		1.47			0.058	
b	0.31	0.2		0.012	0.008	
c	0.254	0.17		0.010	0.007	
D	8.56	8.66	8.76	0.337	0.341	0.345
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.91	4.01	0.150	0.154	0.158
e		0.635			0.025	
L	0.4	0.635	0.89	0.016	0.025	0.035
h	0.25	0.33	0.41	0.010	0.013	0.016
<	8°	0°				

Figure 18. QSOP-24 package dimensions

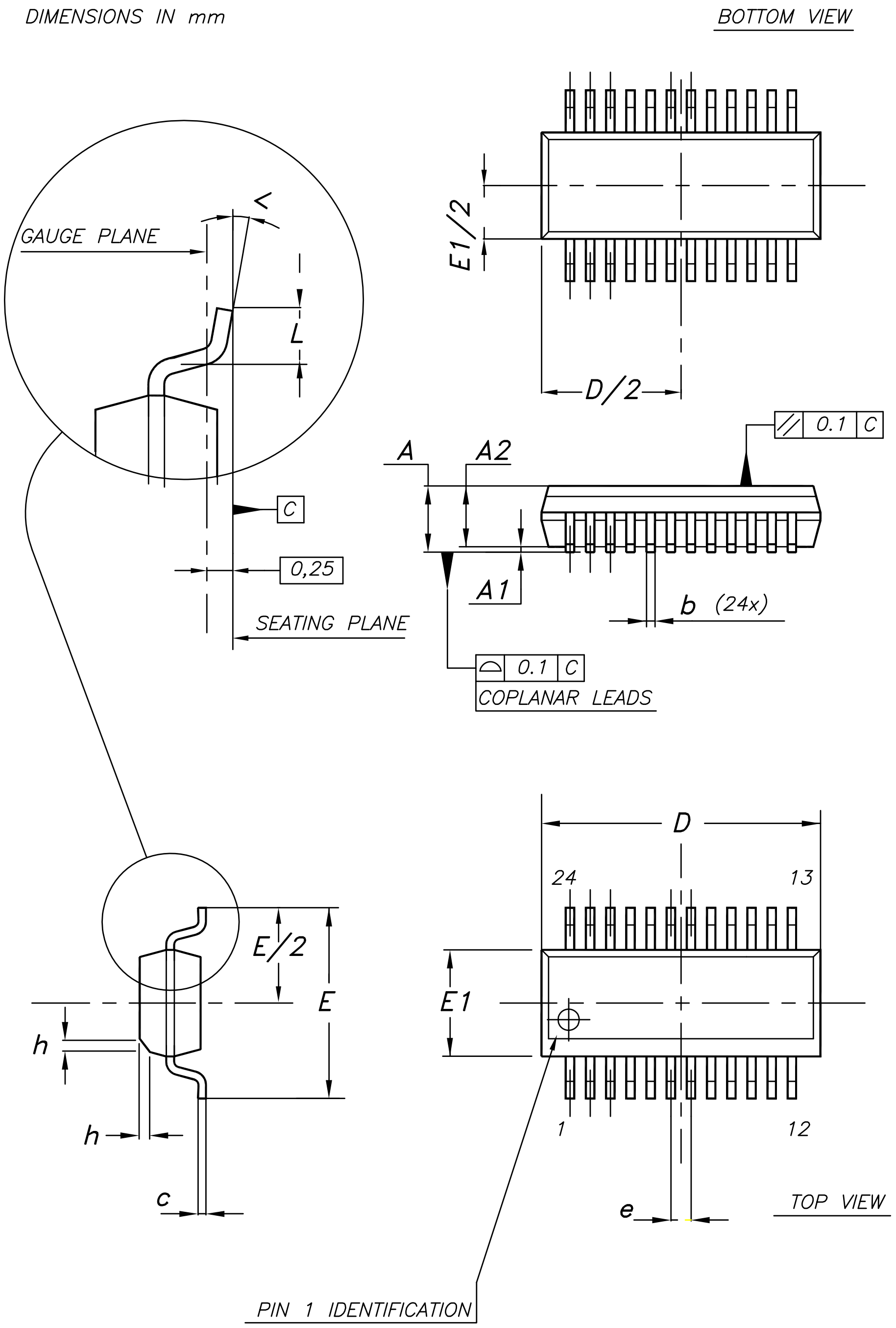


Table 11. TSSOP24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 19. TSSOP24 package dimensions

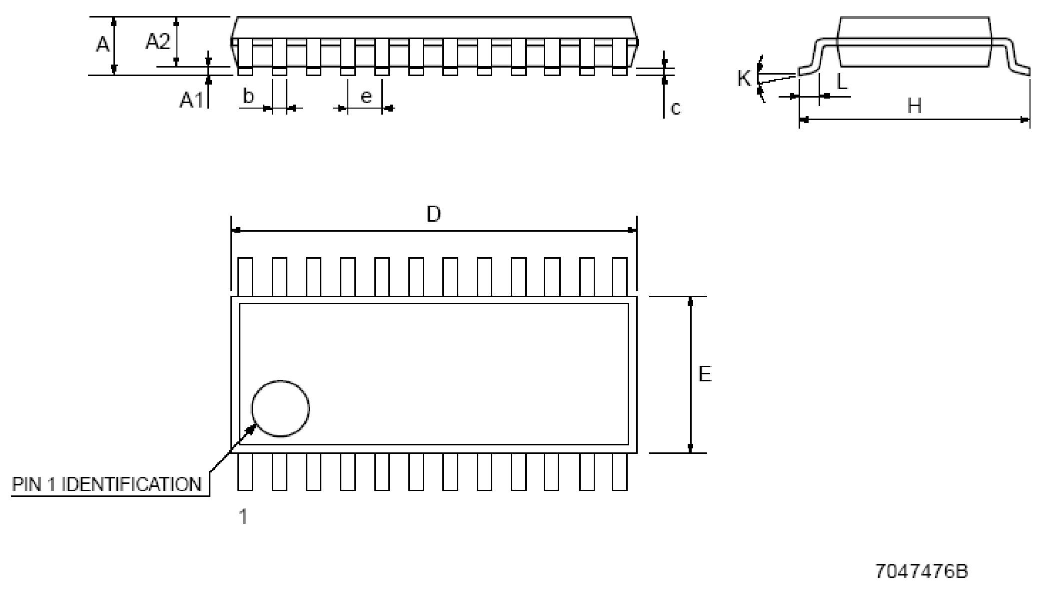


Table 12. Tape and reel TSSOP24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A		-	330		-	12.992
C	12.8	-	13.2	0.504	-	0.519
D	20.2	-		0.795	-	
N	60	-		2.362	-	
T		-	22.4		-	0.882
Ao	6.8	-	7	0.268	-	0.276
Bo	8.2	-	8.4	0.323	-	0.331
Ko	1.7	-	1.9	0.067	-	0.075
Po	3.9	-	4.1	0.153	-	0.161
P	11.9	-	12.1	0.468	-	0.476

Figure 20. Reel dimensions

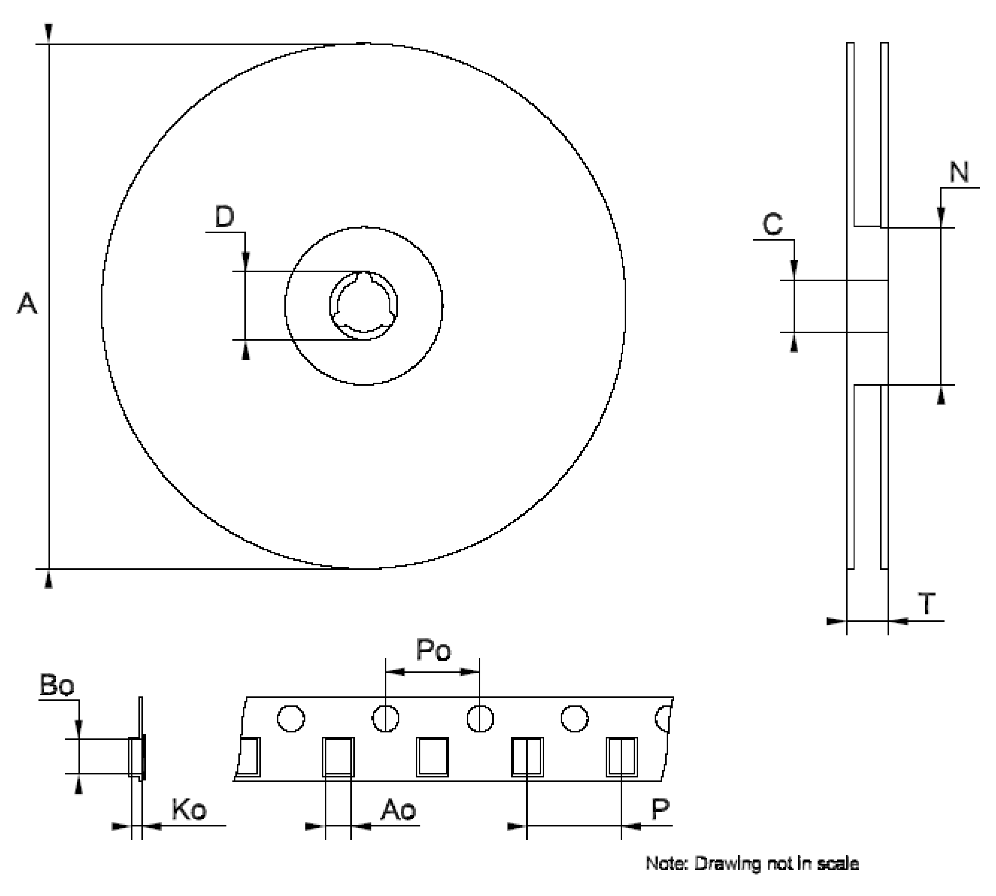


Table 13. SO-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 21. SO-24 package dimensions

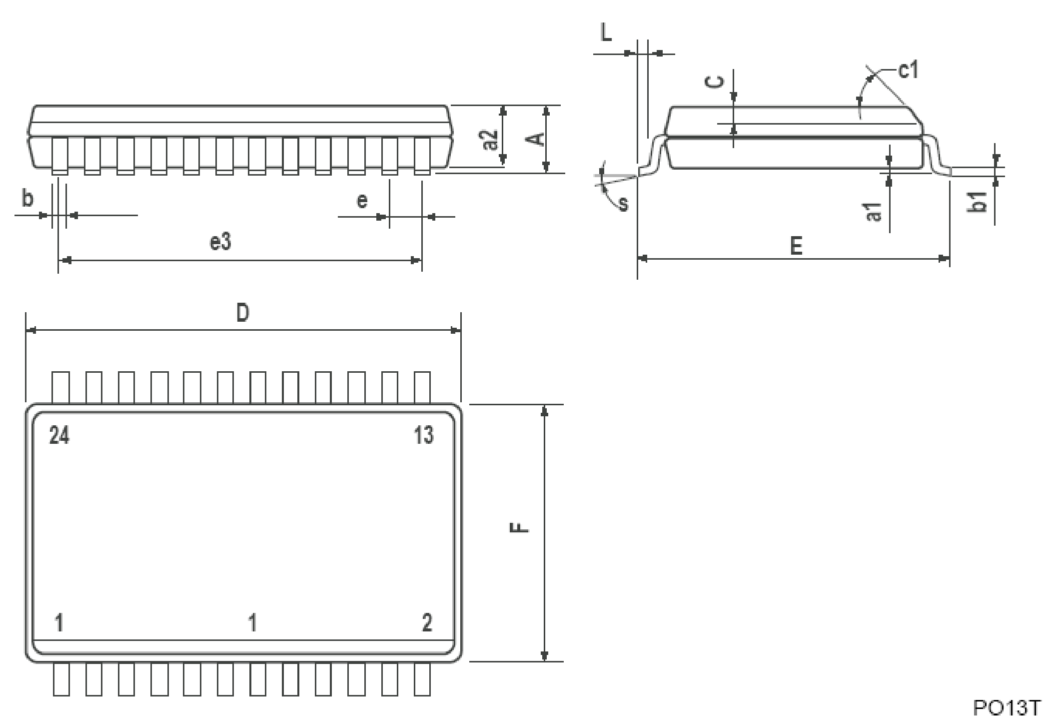


Table 14. Tape and reel SO-24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A		-	330		-	12.992
C	12.8	-	13.2	0.504	-	0.519
D	20.2	-		0.795	-	
N	60	-		2.362	-	
T		-	30.4		-	1.197
Ao	10.8	-	11.0	0.425	-	0.433
Bo	15.7	-	15.9	0.618	-	0.626
Ko	2.9	-	3.1	0.114	-	0.122
Po	3.9	-	4.1	0.153	-	0.161
P	11.9	-	12.1	0.468	-	0.476

Figure 22. Reel dimensions

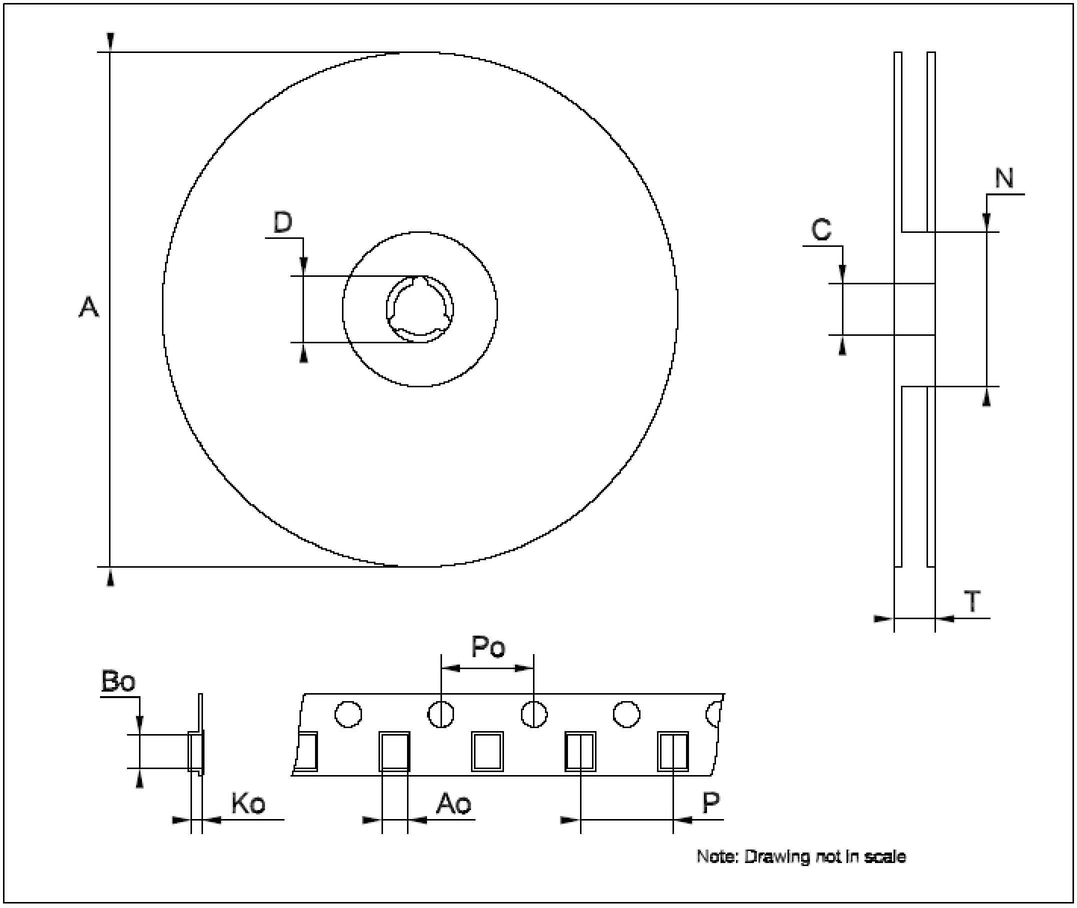
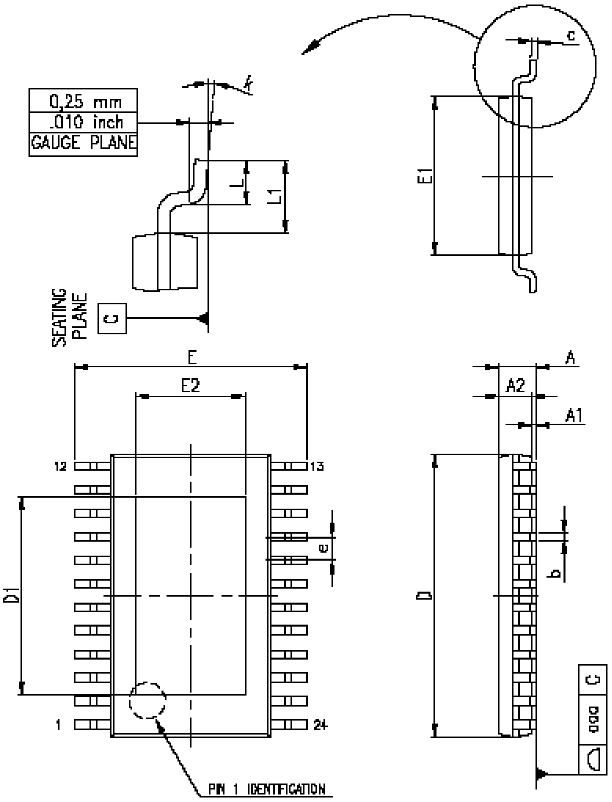


Table 15. TSSOP24 exposed pad

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.7	5.0	5.3	0.185	0.197	0.209
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.2	3.5	0.114	0.126	0.138
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 23. TSSOP24 dimensions



12 Revision history

Table 16. Document revision history

Date	Revision	Changes
04-Mar-2011	1	First release
05-Apr-2011	2	Updated *Table 6*
19-Jul-2012	3	Updated *Table 7*.
29-Jan-2013	4	Updated characteristics in *Table 5: Electrical characteristics* and *Table 6: Switching characteristics*. Minor text changes.

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