3.3-V IEEE 1394-1995 Backplane PHY

FEATURES

- **Provides a Backplane 1394 Environment That Supports an Asynchronous Transfer Rate of 50 or 100 Mbits/s Across 2 Etches**
- **Single 3.3-V Supply Operation With 5-V Tolerance on the Transceiver Receive Interface**
- **Allows Utilization of 3-State Drivers as Well as Open-Collector Drivers**
- **Software Compatible With the TSB14CO1APM**
- **Enhanced Compatibility With the 1394 Cable Link Layer. Compatible With 1394–1995 and 1394a–2000 Link Layers; PHY/link Interface is 1394a Compliant[1]**
- **Supports Provisions of IEEE 1394–1995[2][3]**
- **Extensive Testability and Debug Functions Added. Expanded Register Set Including Automatic Saving of ID and Priority for Last Node Winning Arbitration**
- **100 MHz or 50 MHz Oscillator Provides Transmit, Receive Data, and Link Layer Controller (LLC) Clocks**
- **Logic Performs System Initialization Arbitration Functions. Encode And Decode Functions Included for Data-Strobe Bit Level Encoding. Incoming Data Resynchronized to Local Clock.**
- **Operates Over the Extended Temperature Ranges of 0°C to 70°C (no suffix), –40°C to 85°C (I suffix), and –40°C to 105°C (T suffix)**
- **Packaged in the Very Compact 48-Pin 7 x 7 x 1 mm PFB Package**

(1) IEEE Std 1394a–2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*

(2) IEEE Std 1394–1995, *IEEE Standard for a High Performance Serial Bus*

(3) Implements technology covered by one or more patents of Apple Computer, Inc. and ST Microelectronics.

DESCRIPTION

The TSB14AA1A (TSB14AA1A refers to all three devices: TSB14AA1A, TSB14AA1AI, and TSB14AA1AT) is the second-generation 1394 backplane physical layer device. It is recommended for use in all new designs instead of the first generation TSB14C01A. It provides the physical layer functions needed to implement a single port node in a backplane based 1394 network. The TSB14AA1A provides two pins for transmitting, two for receiving, and two pins to externally control the transceivers for data and strobe. In addition to supporting open-collector drivers, the TSB14AA1A can also support 3-state(1) (high-impedance) drivers. The TSB14AA1A is not designed to drive the backplane directly; this function must be provided externally. The TSB14AA1A is designed to interface with a link-layer controller (LLC), such as the TSB12LV01B, TSB12LV32, TSB12LV21B, etc.

The TSB14AA1A requires an external 98.304-MHz reference oscillator input for S100 asynchronous only operation or 49.152-MHz for S50 asynchronous only operation. Two clock select pins (CLK_SEL0, CLK_SEL1) select the speed mode for the TSB14AA1A. For S100 operation, the 98.304-MHz reference signal is internally divided to provide the 49.152-MHz system clock signals used to control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. For S50 operation, a 49.152-MHz reference signal is used. This reference signal is internally divided to provide the 24.576-MHz system clock signals for S50 operations.

During packet transmit, data bits to be transmitted are received from the LLC on two parallel paths and are latched internally in the TSB14AA1A in synchronization with the system clock. These bits are combined serially, encoded, and transmitted as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted on TDATA, and the encoded strobe information is transmitted on TSTRB.

(1) 3-State means a driver may drive high, low, or may be placed in a high-impedance state

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During packet reception, the data information is received on RDATA and strobe information is received on RSTRB. The received data and strobe information is decoded to recover the received clock signal and the serial data bits, which are resynchronized to the local system clock. The serial data bits are split into two parallel streams and sent to the associated LLC. The PHY-Link interface has been made compliant to IEEE 1394a–2000 including timing and transfer of register 0 to the link-layer automatically after every 1394 bus reset.

The TSB14AA1A is a 3.3 V device that provides LVCMOS level outputs. The TSB14AA1A is an asynchronous only device.

NOTE:

This product is for high-volume applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSB14AA1AIPFB	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSB14AA1AIPFBG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSB14AA1APFB	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TSB14AA1APFBG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

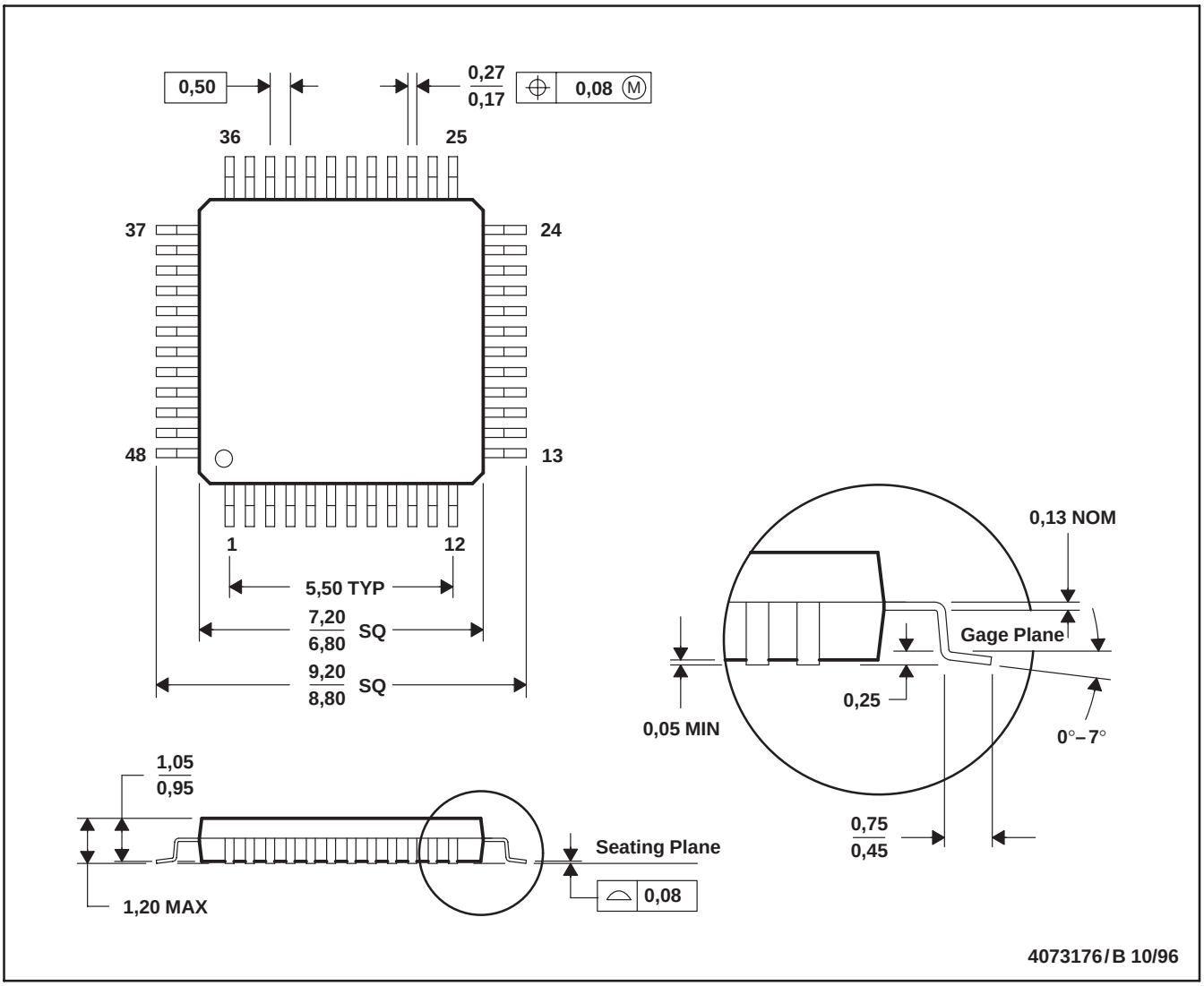
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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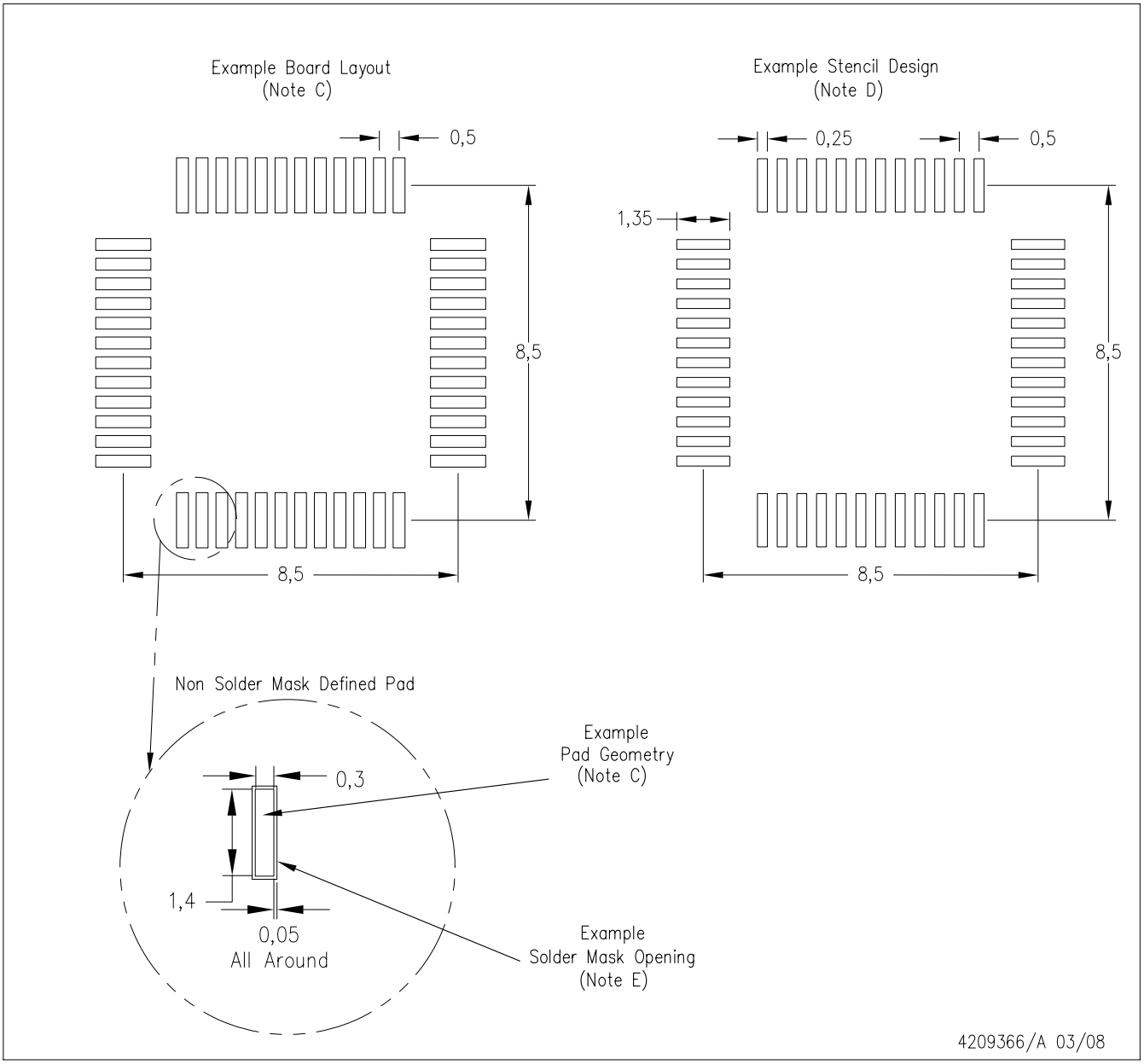
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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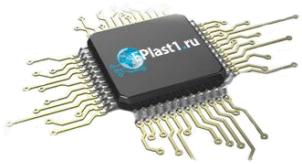
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