

The CY91520 series is a Cypress 32-bit microcontroller designed for automotive devices. This series contains the FR81S CPU which is compatible with the FR family.

Note:This series is a composition of the end of the above-mentioned each name of articles of presence, According to Presence of sub-clock, CSV initial value and LVD initial value. Please see "Ordering Information" for details.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
- General-purpose register : 32 bits × 16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
 - Memory-to-memory transfer instruction
 - Bit processing instruction
 - Barrel shift order etc.
- High-level language support instructions
- Function entry/exit instructions
- Register content multi-load and store instructions
- Bit search instructions
 - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
- Overhead reduction during branch process
- Register interlock function
- Easy assembler writing
- The support at the built-in / instruction level of the multiplier
- Signed 32-bit multiplication: 5 cycles
- Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
 - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
 - Eight protection areas can be specified commonly for instructions and the data.
 - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
 - IEEE754 compliant
 - Floating-point register 32-bit × 16 sets

Peripheral Functions

- Clock generation (equipped with SSCG function)
 - Main oscillation (4 MHz to 16 MHz)
 - Sub oscillation (32 kHz) or none sub oscillation
 - PLL multiplication rate : 1 to 20 times
 - Equipped with a 100 kHz CR oscillator
- Built-in program flash memory capacity
 - CY91F522: 256 +64 KB
 - CY91F523: 384 + 64 KB
 - CY91F524: 512 + 64 KB
 - CY91F525: 768 + 64 KB
 - CY91F526: 1024 + 64 KB
- Flash memory for built-in data (WorkFlash) 64 KB
- Built-in RAM capacity
 - Main RAM
 - CY91F522: 48 KB
 - CY91F523: 48 KB
 - CY91F524: 64 KB
 - CY91F525: 96 KB
 - CY91F526: 128 KB
 - Backup RAM 8 KB
- General-purpose ports:
 - CY91F52xB 44 sets (No sub oscillation), 42 sets (sub oscillation)
 - CY91F52xD 56 sets (No sub oscillation), 54 sets (sub oscillation)
 - CY91F52xF 76 sets (No sub oscillation), 74 sets (sub oscillation)
 - CY91F52xJ 96 sets (No sub oscillation), 94 sets (sub oscillation)
 - CY91F52xK 120 sets (No sub oscillation), 118 sets (sub oscillation)
 - CY91F52xL 152 sets (No sub oscillation), 150 sets (sub oscillation)
 - Included I²C open drain corresponding ports:16 sets
- External bus interface
 - 22-bit address, 16-bit data
- DMA Controller
 - Up to 16 channels can be started simultaneously.
 - 2 transfer factors (Internal peripheral request and software)
- A/D converter (successive approximation type)
 - 12-bit resolution : Max. 48 ch (32 ch + 16 ch)
 - Conversion time : 1.4 µs

- D/A converter (R-2R type)
 - 8-bit resolution : 2 ch
- External interrupt input: 8 channels × 2 units total
16 channels
 - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
 - 5 V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11
CMOS hysteresis input
< UART (Asynchronous serial interface) >
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - Parity or no parity is selectable.
 - Built-in dedicated baud rate generator
 - An external clock can be used as the transfer clock
 - Parity, frame, and overrun error detection functions provided
 - DMA transfer support
<CSIO (Synchronous serial interface) >
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
 - Built-in dedicated baud rate generator (Master operation)
 - An external clock can be entered. (Slave operation)
 - Overrun error detection function is provided
 - DMA transfer support
 - Serial chip select SPI function
<LIN (Asynchronous Serial Interface for LIN) >
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - LIN protocol revision 2.1 supported
 - Master and slave systems supported
 - Framing error and overrun error detection
 - LIN synch break generation and detection; LIN synch delimiter generation
 - Built-in dedicated baud rate generator
 - An external clock can be adjusted by the reload counter
 - DMA transfer support
 - Hard assist function
< I²C >
 - 2 channels ch.3 , ch.4 Standard mode/fast mode supported.
 - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - Standard mode (Max. 100 kbps) / fast mode (Max. 400 kbps) supported
 - DMA transfer supported (for transmission only)
- CAN Controller (CAN) : 3 channels
 - Transfer speed : Up to 1 Mbps
 - 128-transmission/reception message buffering : 1 channel (ch.0),

64-transmission/reception message buffering :
2 channels (ch.1 and ch.2)

- PPG: 16-bit × Max. 48 channels
 - LED drive output 4 channels 11 ch to 14 ch
 - Reload timer : 16-bit × Max.8 channels
 - Free-run timer :
 - 16-bit × 3 channels
 - 32-bit × Max 3 channels
- Input capture :
 - 16-bit × 4 channels (linked to the free-run timer)
 - 32-bit × Max 6 channels (linked to the free-run timer)
- Output compare :
 - 16-bit × 6 channels (linked to the free-run timer)
 - 32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
 - 8-/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
 - Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
 - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
 - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32 kHz) (dual clock products) of the outside and main oscillation (4 MHz)
 - When abnormality is detected, it switches to the CR clock.
 - Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
 - 16-bit timer
 - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
 - As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascade mode
- CRC generation
- Watchdog timer
 - Hardware watchdog
 - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
 - The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
 - Peripheral function pins can be reassigned.
- Low-power consumption mode
 - Sleep / Stop / Watch / Sub RUN mode
 - Stop (power shutdown) / Watch (power shutdown) mode

- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
 - The external power supply can select initial value ON/OFF by the part number.
- Device Package : 176/144/120/100/80/64
- CMOS 90 nm Technology
- Power supplies
 - 5 V Power supply
 - The internal 1.2 V is generated from 5 V with the voltage step-down circuit

Contents

1. Product Lineup	5
2. Pin Assignment	12
3. Pin Description	18
4. I/O Circuit Type	35
5. Handling Precautions	40
6. Handling Devices	44
7. Block Diagram.....	47
8. Memory Map	53
9. I/O Map.....	55
10. Interrupt Vector Table	109
11. Electrical Characteristics.....	133
12. Example Characteristics	193
13. Ordering Information CY91F52xxxB ^{*1}	196
14. Ordering Information CY91F52xxxC ^{*1}	203
15. Ordering Information CY91F52xxxD	210
16. Ordering Information CY91F52xxxE	214
17. Package Dimensions	218
18. Errata.....	225
19. Major Changes.....	228

1. Product Lineup

Product Lineup Comparison 64 Pins

	CY91F522B	CY91F523B	CY91F524B	CY91F525B	CY91F526B
System Clock		On chip PLL Clock multiple method			
Minimum instruction execution time		12.5 ns (80 MHz)			
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)		64 KB			
RAM Capacity	(48+8) KB	(64+8) KB	(96+8) KB	(128+8) KB	
External BUS I/F (22 address/16 data/4 cs)		None			
DMA Transfer		16 ch			
16-bit Base Timer		None			
Free-run Timer		16 bit × 3 ch, 32 bit × 1 ch			
Input capture		16 bit × 4 ch, 32 bit × 5 ch			
Output Compare		16 bit × 6 ch, 32 bit × 4 ch			
16-bit Reload Timer		7 ch			
PPG		16 bit × 21 ch			
Up/down Counter		2 ch			
Clock Supervisor		Yes			
External Interrupt		8 ch × 2 units			
A/D converter		12 bit × 13 ch (1 unit), 12 bit × 13 ch (1 unit)			
D/A converter (8 bit)		1 ch			
Multi-Function Serial Interface		8 ch ^{*1}			
CAN		64 msg × 2 ch/128 msg × 1 ch			
Hardware Watchdog Timer		Yes			
CRC Formation		Yes			
Low-voltage detection reset		Yes			
Flash Security		Yes			
ECC Flash/WorkFlash		Yes			
ECC RAM		Yes			
Memory Protection Function (MPU)		Yes			
Floating point arithmetic (FPU)		Yes			
Real Time Clock (RTC)		Yes			
General-purpose port (#GPIOs)		44 ports			
SSCG		Yes			
Sub clock		Yes			
CR oscillator		Yes			
OCD (On Chip Debug)		Yes			
TPU (Timing Protection Unit)		Yes			
Key code register		Yes			
Waveform generator		6 ch			
NMI request function		Yes			
Operation guaranteed temperature (T _A)		-40 °C to +125 °C			
Power supply		2.7 V to 5.5 V ^{*2}			
Package		LQD064			

*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 80 Pins

	CY91F522D	CY91F523D	CY91F524D	CY91F525D	CY91F526D
System Clock		On chip PLL	Clock multiple method		
Minimum instruction execution time		12.5 ns (80 MHz)			
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)		64 KB			
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)		None			
DMA Transfer		16 ch			
16-bit Base Timer		1 ch			
Free-run Timer		16 bit × 3 ch, 32 bit × 2 ch			
Input capture		16 bit × 4 ch, 32 bit × 5 ch			
Output Compare		16 bit × 6 ch, 32 bit × 4 ch			
16-bit Reload Timer		7 ch			
PPG		16 bit × 27 ch			
Up/down Counter		2 ch			
Clock Supervisor		Yes			
External Interrupt		8 ch × 2 units			
A/D converter		12 bit × 16 ch (1 unit), 12 bit × 16 ch (1 unit)			
D/A converter (8 bit)		1 ch			
Multi-Function Serial Interface		9 ch ^{*1}			
CAN		64 msg × 2 ch/128 msg × 1 ch			
Hardware Watchdog Timer		Yes			
CRC Formation		Yes			
Low-voltage detection reset		Yes			
Flash Security		Yes			
ECC Flash/WorkFlash		Yes			
ECC RAM		Yes			
Memory Protection Function (MPU)		Yes			
Floating point arithmetic (FPU)		Yes			
Real Time Clock (RTC)		Yes			
General-purpose port (#GPIOs)		56 ports			
SSCG		Yes			
Sub clock		Yes			
CR oscillator		Yes			
NMI request function		Yes			
OCD (On Chip Debug)		Yes			
TPU (Timing Protection Unit)		Yes			
Key code register		Yes			
Waveform generator		6 ch			
Operation guaranteed temperature (T _A)		-40 °C to +125 °C			
Power supply		2.7 V to 5.5 V ^{*2}			
Package		LQH080			

*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 100 Pins

	CY91F522F	CY91F523F	CY91F524F	CY91F525F	CY91F526F
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)	64 KB				
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)	None				
DMA Transfer	16 ch				
16-bit Base Timer	1 ch				
Free-run Timer	16 bit × 3 ch, 32 bit × 3 ch				
Input capture	16 bit × 4 ch, 32 bit × 6 ch				
Output Compare	16 bit × 6 ch, 32 bit × 6 ch				
16-bit Reload Timer	8 ch				
PPG	16 bit × 34 ch				
Up/down Counter	2 ch				
Clock Supervisor	Yes				
External Interrupt	8 ch × 2 units				
A/D converter	12 bit × 21 ch (1 unit), 12 bit × 16 ch (1 unit)				
D/A converter (8 bit)	2 ch				
Multi-Function Serial Interface	12 ch ^{*1}				
CAN	64 msg × 2 ch/128 msg × 1 ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	76 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6 ch				
Operation guaranteed temperature (T _A)	-40 °C to +125 °C				
Power supply	2.7 V to 5.5 V ^{*2}				
Package	LQI100				

^{*1}: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

^{*2}: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 120 Pins

	CY91F522J	CY91F523J	CY91F524J	CY91F525J	CY91F526J
System Clock			On chip PLL Clock multiple method		
Minimum instruction execution time			12.5 ns (80 MHz)		
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)			64 KB		
RAM Capacity	(48+8) KB	(64+8) KB	(96+8) KB	(128+8) KB	
External BUS I/F (22 address/16 data/4 cs)			None		
DMA Transfer			16 ch		
16-bit Base Timer			2 ch		
Free-run Timer			16 bit × 3 ch, 32 bit × 3 ch		
Input capture			16 bit × 4 ch, 32 bit × 6 ch		
Output Compare			16 bit × 6 ch, 32 bit × 6 ch		
16-bit Reload Timer			8 ch		
PPG			16 bit × 38 ch		
Up/down Counter			2 ch		
Clock Supervisor			Yes		
External Interrupt			8 ch × 2 units		
A/D converter			12 bit × 26 ch (1 unit), 12 bit × 16 ch (1 unit)		
D/A converter (8 bit)			2 ch		
Multi-Function Serial Interface			12 ch ^{*1}		
CAN			64 msg × 2 ch/128 msg × 1 ch		
Hardware Watchdog Timer			Yes		
CRC Formation			Yes		
Low-voltage detection reset			Yes		
Flash Security			Yes		
ECC Flash/WorkFlash			Yes		
ECC RAM			Yes		
Memory Protection Function (MPU)			Yes		
Floating point arithmetic (FPU)			Yes		
Real Time Clock (RTC)			Yes		
General-purpose port (#GPIOs)			96 ports		
SSCG			Yes		
Sub clock			Yes		
CR oscillator			Yes		
NMI request function			Yes		
OCD (On Chip Debug)			Yes		
TPU (Timing Protection Unit)			Yes		
Key code register			Yes		
Waveform generator			6 ch		
Operation guaranteed temperature (T_A)			-40 °C to +125 °C		
Power supply			2.7 V to 5.5 V ^{*2}		
Package			LQM120		

*1: Only channel 3 and channel 4 support the I²C (fast mode/standard mode).

Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 144 Pins

	CY91F522K	CY91F523K	CY91F524K	CY91F525K	CY91F526K
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)	64 KB				
RAM Capacity	(48+8) KB	(64+8) KB	(96+8) KB	(128+8) KB	
External BUS I/F (22 address/16 data/4 cs)	Yes				
DMA Transfer	16 ch				
16-bit Base Timer	2 ch				
Free-run Timer	16 bit × 3 ch, 32 bit × 3 ch				
Input capture	16 bit × 4 ch, 32 bit × 6 ch				
Output Compare	16 bit × 6 ch, 32 bit × 6 ch				
16-bit Reload Timer	8 ch				
PPG	16 bit × 44 ch				
Up/down Counter	2 ch				
Clock Supervisor	Yes				
External Interrupt	8 ch × 2 units				
A/D converter	12 bit × 32 ch (1 unit), 12 bit × 16 ch (1 unit)				
D/A converter (8 bit)	2 ch				
Multi-Function Serial Interface	12 ch ^{*1}				
CAN	64 msg × 2 ch/128 msg × 1 ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	120 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6 ch				
Operation guaranteed temperature (T_A)	-40 °C to +125 °C				
Power supply	2.7 V to 5.5 V ^{*2}				
Package	LQS144, LQN144				

*1: Only channel 3 and channel 4 support the I²C (fast mode/standard mode).

Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product Lineup Comparison 176 Pins

	CY91F522L	CY91F523L	CY91F524L	CY91F525L	CY91F526L
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5 ns (80 MHz)				
Flash Capacity (Program)	(256+64) KB	(384+64) KB	(512+64) KB	(768+64) KB	(1024+64) KB
Flash Capacity (Data)				64 KB	
RAM Capacity	(48+8) KB		(64+8) KB	(96+8) KB	(128+8) KB
External BUS I/F (22 address/16 data/4 cs)				Yes	
DMA Transfer			16 ch		
16-bit Base Timer			2 ch		
Free-run Timer		16 bit × 3 ch, 32 bit × 3 ch			
Input capture		16 bit × 4 ch, 32 bit × 6 ch			
Output Compare		16 bit × 6 ch, 32 bit × 6 ch			
16-bit Reload Timer		8 ch			
PPG		16 bit × 48 ch			
Up/down Counter		2 ch			
Clock Supervisor		Yes			
External Interrupt		8 ch × 2 units			
A/D converter		12 bit × 32 ch (1 unit), 12 bit × 16 ch (1 unit)			
D/A converter (8 bit)		2 ch			
Multi-Function Serial Interface		12 ch ^{*1}			
CAN		64 msg × 2 ch/128 msg × 1 ch			
Hardware Watchdog Timer		Yes			
CRC Formation		Yes			
Low-voltage detection reset		Yes			
Flash Security		Yes			
ECC Flash/WorkFlash		Yes			
ECC RAM		Yes			
Memory Protection Function (MPU)		Yes			
Floating point arithmetic (FPU)		Yes			
Real Time Clock (RTC)		Yes			
General-purpose port (#GPIOs)		152 ports			
SSCG		Yes			
Sub clock		Yes			
CR oscillator		Yes			
NMI request function		Yes			
OCD (On Chip Debug)		Yes			
TPU (Timing Protection Unit)		Yes			
Key code register		Yes			
Waveform generator		6 ch			
Operation guaranteed temperature (T_A)		-40 °C to +125 °C			
Power supply		2.7 V to 5.5 V ^{*2}			
Package		LQP176			

*1: Only channel 3 and channel 4 support the I²C (fast mode/standard mode).

Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Table for Clock Supervisor and External Low Voltage Detection Reset Initial Value ON/OFF

Clock	CSV Initial Value	LVD Initial Value	Function
single	ON	ON	S
		OFF	U
	OFF	ON	H
		OFF	K
Dual	ON	ON	W
		OFF	Y
	OFF	ON	J
		OFF	L

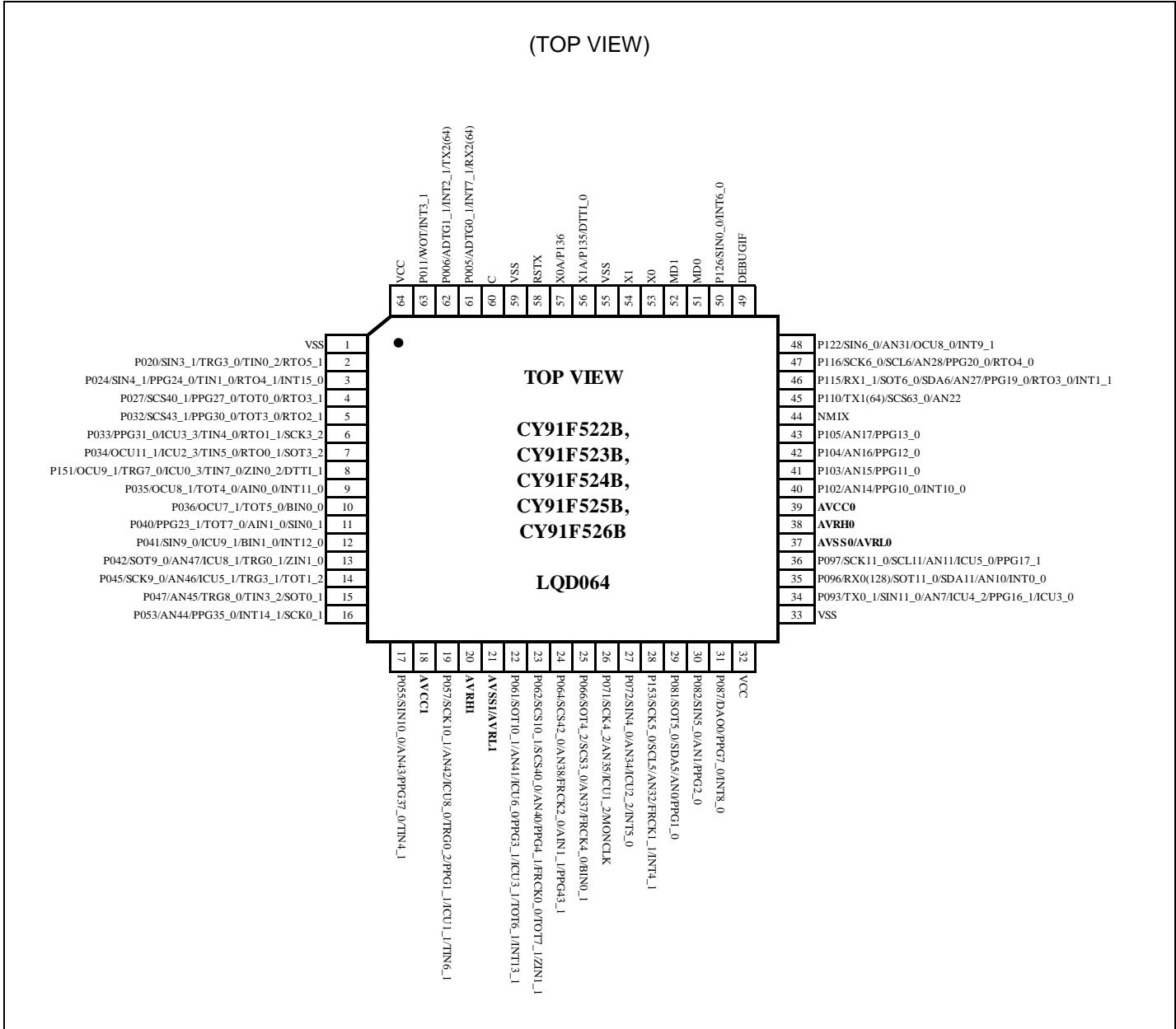
CY91F52X□△○

| └→R e v i s i o n : B, C, D, E
 | └→F u n c t i o n : See the table for clock supervisor and external
 low voltage detection reset initial value ON/OFF.
 | └→P K G T y p e : B 6 4 p i n
 D 8 0 p i n
 F 1 0 0 p i n
 J 1 2 0 p i n
 K 1 4 4 p i n
 L 1 7 6 p i n
 └→M e m o r y S i z e : 2 2 5 6 K B
 3 3 8 4 K B
 4 5 1 2 K B
 5 7 6 8 K B
 6 1 M B

2. Pin Assignment

CY91F52xB

CY91F522B, CY91F523B, CY91F524B, CY91F525B, CY91F526B

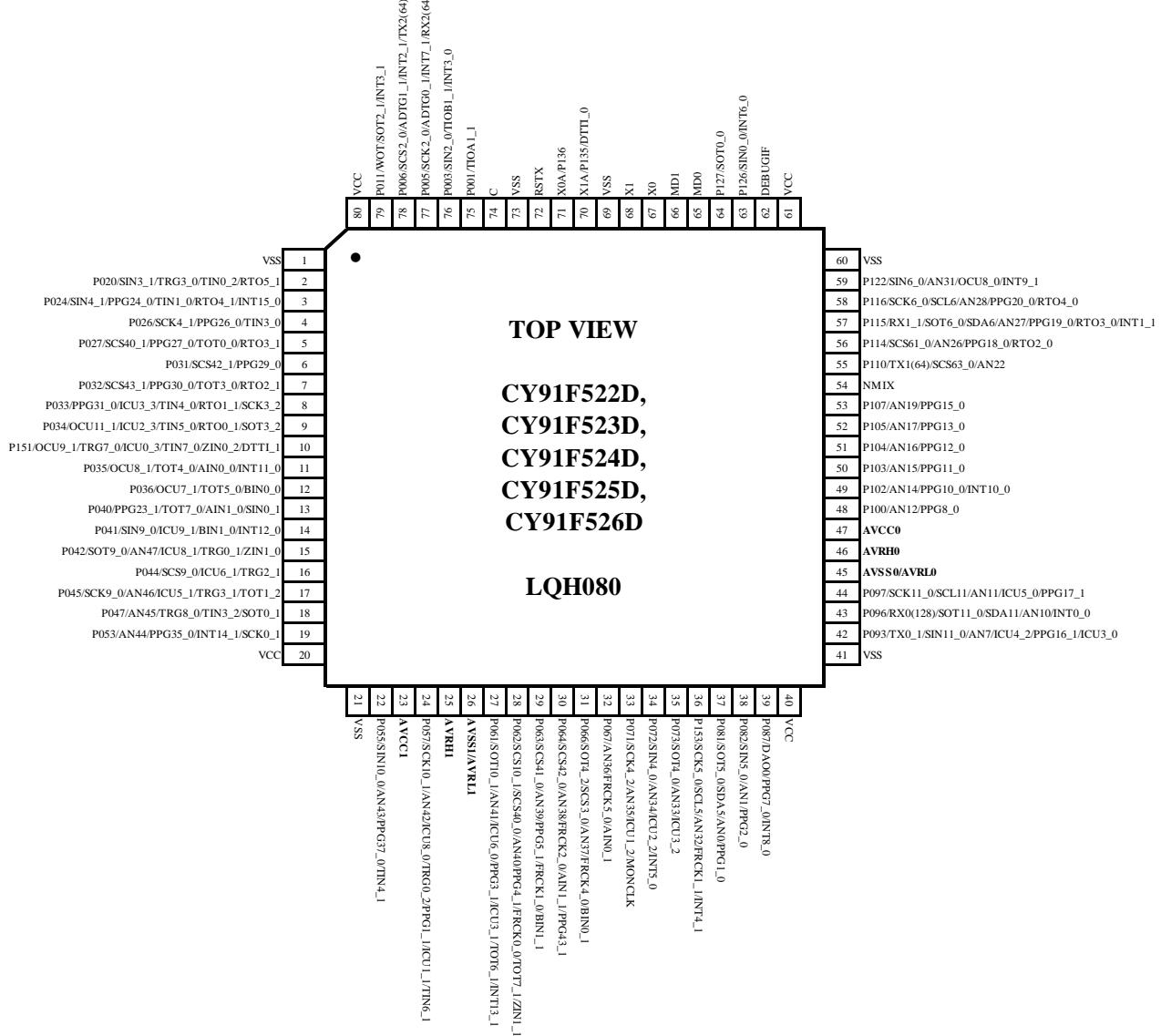


* In a single clock product, pin 56 and pin 57 are the general-purpose ports.

CY91F52xD

CY91F522D, CY91F523D, CY91F524D, CY91F525D, CY91F526D

(TOP VIEW)

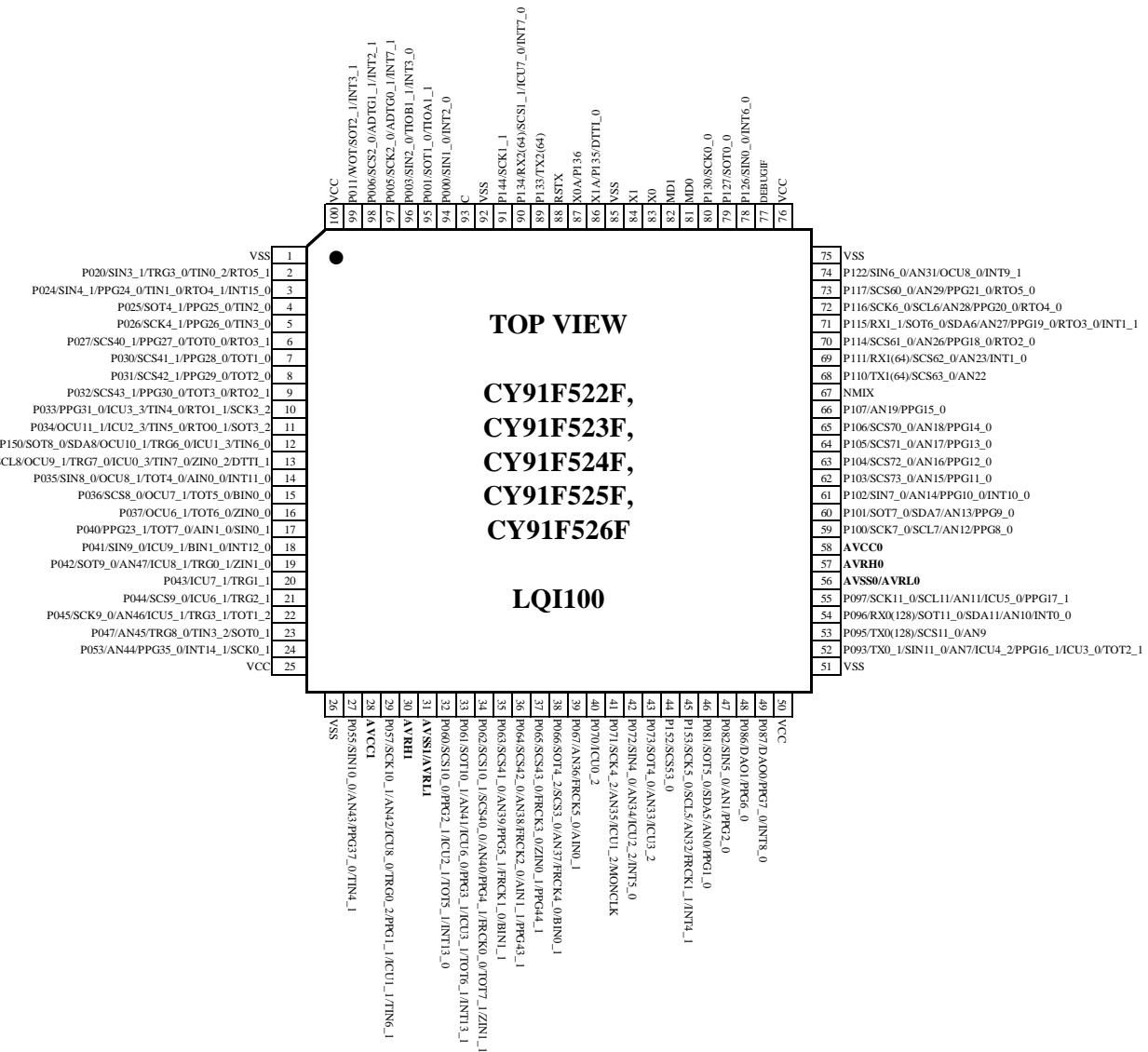


* In a single clock product, pin 70 and pin 71 are the general-purpose ports.

CY91F52xF

CY91F522F, CY91F523F, CY91F524F, CY91F525F, CY91F526F

(TOP VIEW)

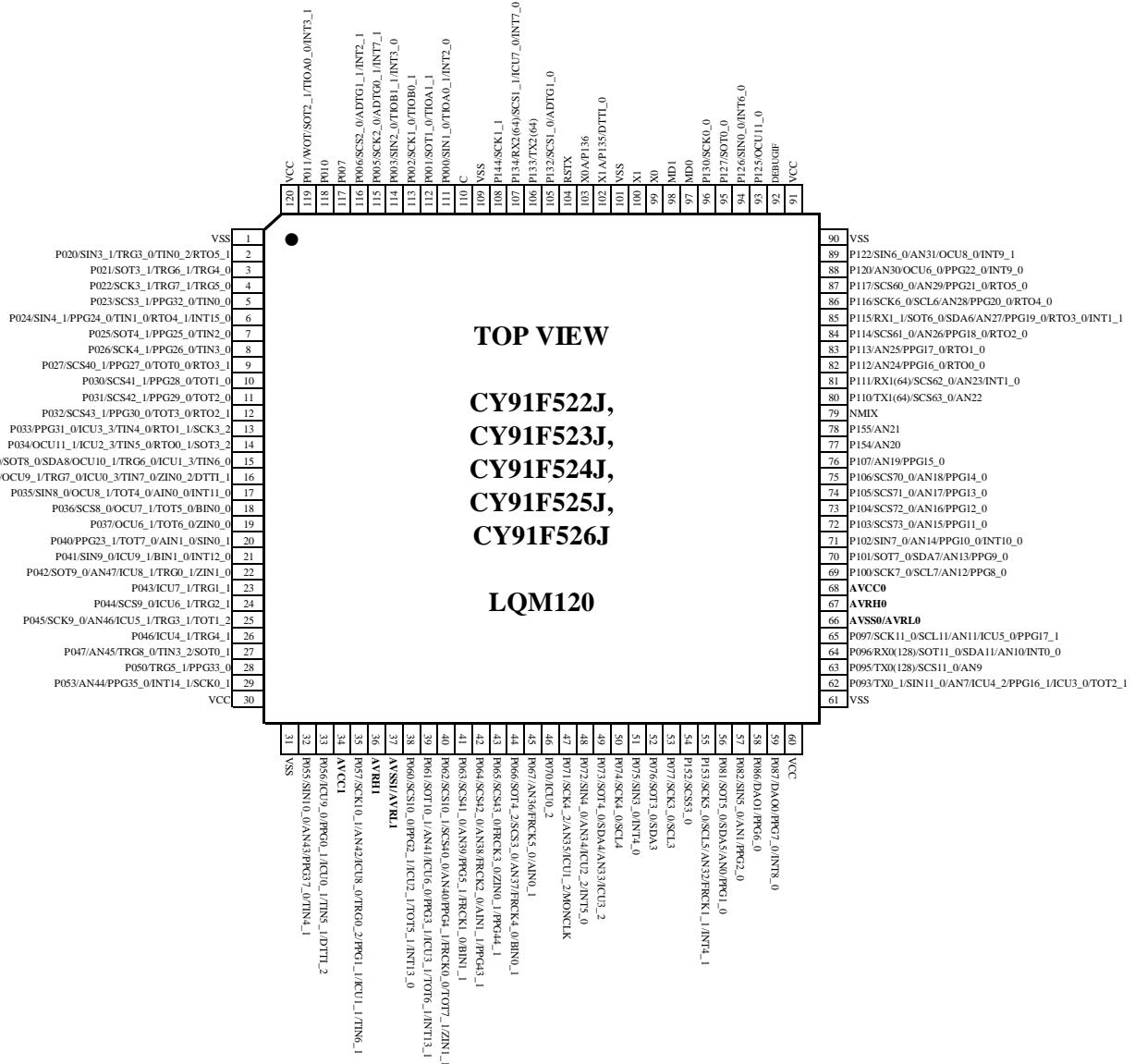


* In a single clock product, pin 86 and pin 87 are the general-purpose ports.

CY91F52xJ

CY91F522J, CY91F523J, CY91F524J, CY91F525J, CY91F526J

(TOP VIEW)

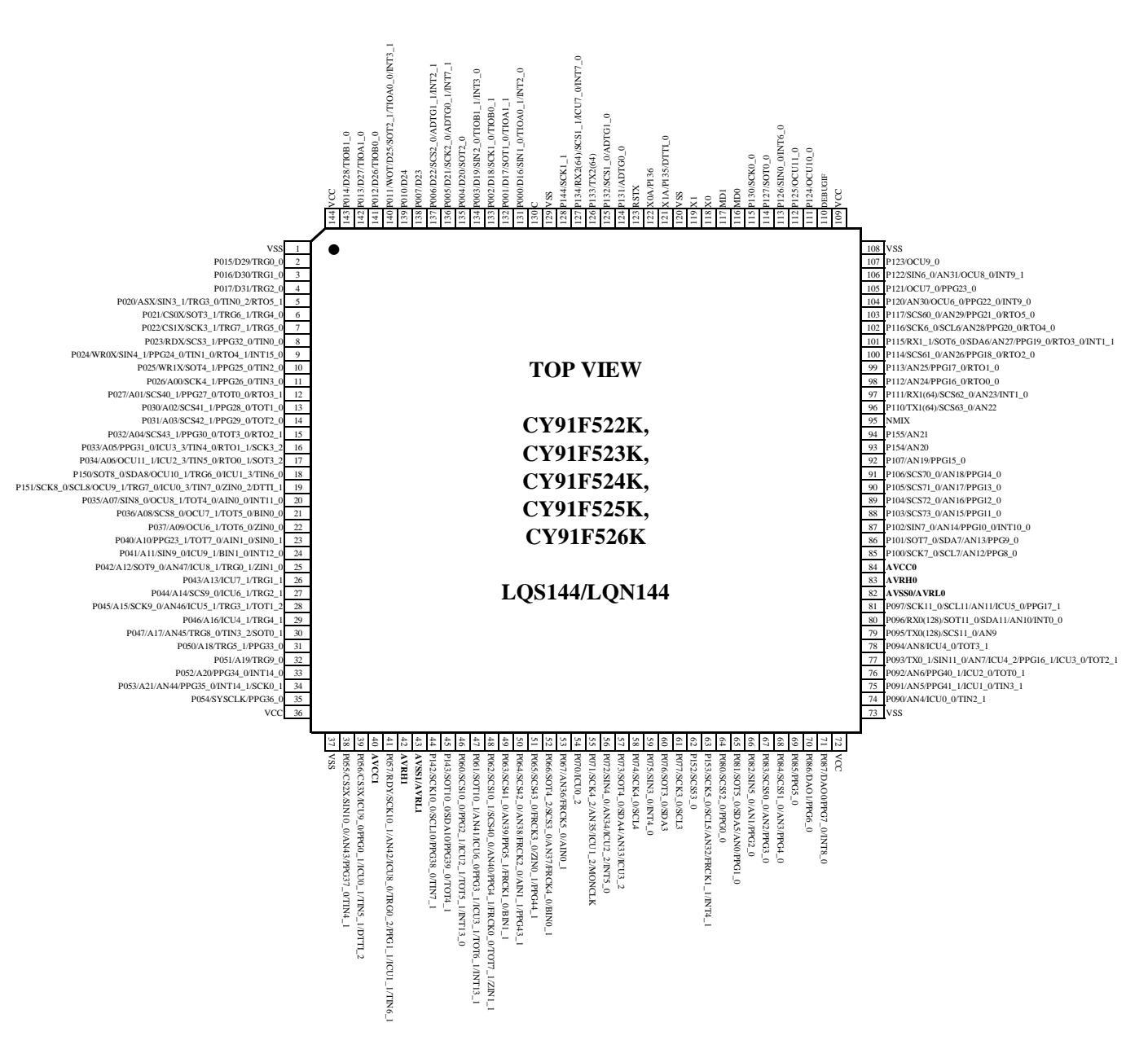


* In a single clock product, pin 102 and pin 103 are the general-purpose ports.

CY91F52xK

CY91F522K, CY91F523K, CY91F524K, CY91F525K, CY91F526K

(TOP VIEW)



**CY91F522K,
CY91F523K,
CY91F524K,
CY91F525K,
CY91F526K**

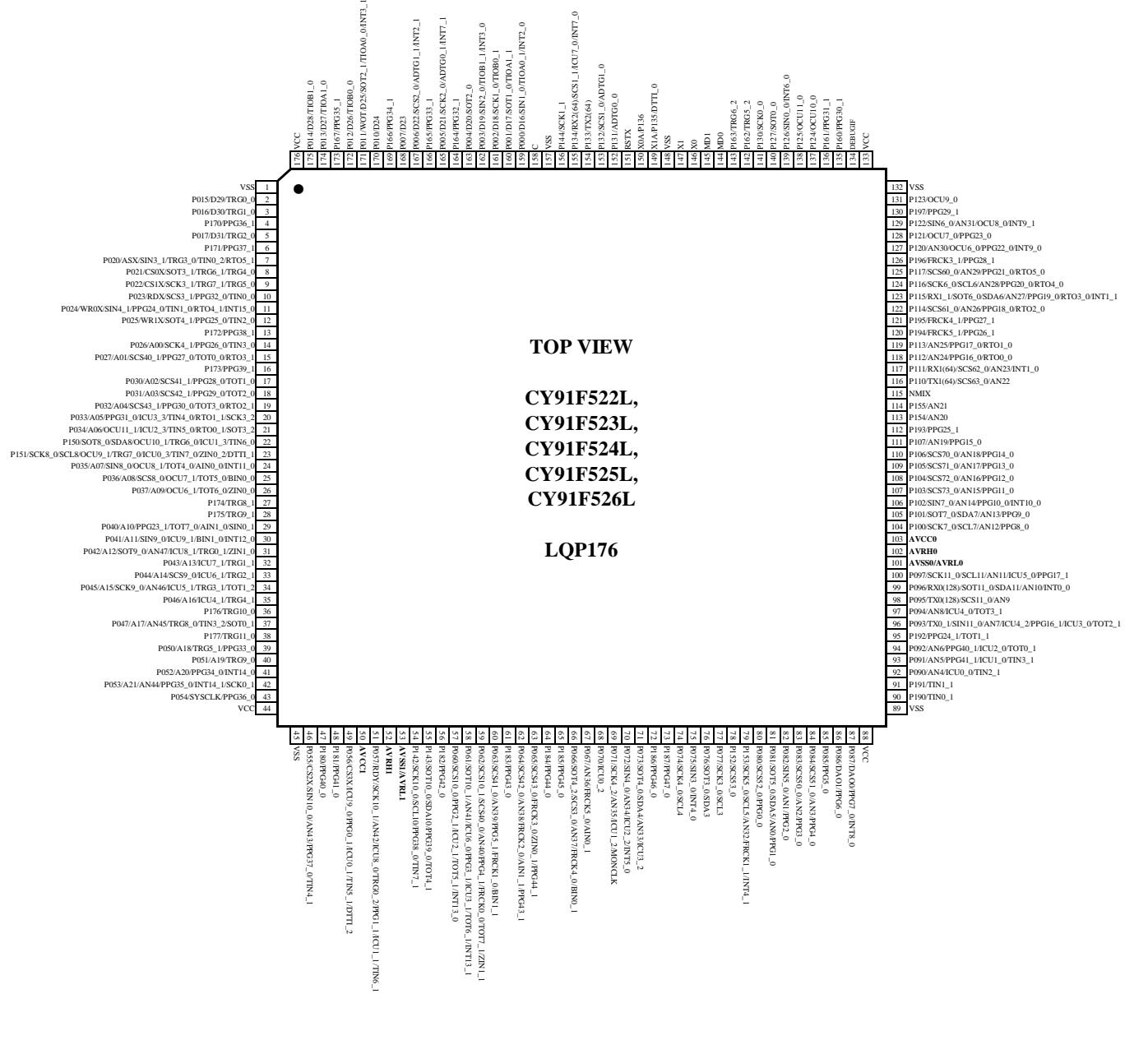
LQS144/LQN144

* In a single clock product, pin 121 and pin 122 are the general-purpose ports.

CY91F52xL

CY91F522L, CY91F523L, CY91F524L, CY91F525L, CY91F526L

(TOP VIEW)



* In a single clock product, pin 149 and pin 150 are the general-purpose ports.

3. Pin Description

Pin No.						Pin Name	Polarity	I/O Circuit types ^{*8}	Function ^{*9}
64	80	100	120	144	176				
-	-	-	-	2	2	P015	-	A	General-purpose I/O port
-	-	-	-	3	3	D29	-		External bus data bit29 I/O (0)
-	-	-	-	4	4	TRG0_0	-		PPG trigger 0 input (0)
-	-	-	-	5	5	P016	-	A	General-purpose I/O port
-	-	-	-	4	3	D30	-		External bus data bit30 I/O (0)
-	-	-	-	6	3	TRG1_0	-		PPG trigger 1 input (0)
-	-	-	-	7	4	P170	-	A	General-purpose I/O port
-	-	-	-	8	4	PPG36_1	-		PPG ch.36 output (1)
-	-	-	-	9	5	P017	-	A	General-purpose I/O port
-	-	-	-	10	5	D31	-		External bus data bit31 I/O (0)
-	-	-	-	11	5	TRG2_0	-		PPG trigger 2 input (0)
-	-	-	-	12	6	P171	-	A	General-purpose I/O port
-	-	-	-	13	6	PPG37_1	-		PPG ch.37 output (1)
2 ^{*1}	2 ^{*1}	2 ^{*1}	2 ^{*1}	5	7	P020	-	F	General-purpose I/O port
						ASX ^{*2, *3, *4, *5}	-		External bus/Address strobe output
						SIN3_1	-		Multi-function serial ch.3 serial data input (1)
						TRG3_0	-		PPG trigger 3 input (0)
						TIN0_2	-		Reload timer ch.0 event input (2)
						RTO5_1	-		Waveform generator ch.5 output pin (1)
-	-	-	3 ^{*1}	6	8	P021	-	A	General-purpose I/O port
-	-	-				CS0X ^{*5}	-		External bus chip select 0 output
-	-	-				SOT3_1	-		Multi-function serial ch.3 serial data output (1)
-	-	-				TRG6_1	-		PPG trigger 6 input (1)
-	-	-				TRG4_0	-		PPG trigger 4 input (0)
-	-	-	4 ^{*1}	7	9	P022	-	F	General-purpose I/O port
-	-	-				CS1X ^{*5}	-		External bus chip select 1 output
-	-	-				SCK3_1	-		Multi-function serial ch.3 clock I/O (1)
-	-	-				TRG7_1	-		PPG trigger 7 input (1)
-	-	-				TRG5_0	-		PPG trigger 5 input (0)
-	-	-	5 ^{*1}	8	10	P023	-	A	General-purpose I/O port
-	-	-				RDX ^{*5}	-		External bus/Read strobe output
-	-	-				SCS3_1	-		Serial chip select 3 output (1)
-	-	-				PPG32_0	-		PPG ch.32 output (0)
-	-	-				TIN0_0	-		Reload timer ch.0 event input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
3 ^{*1}	3 ^{*1}	3 ^{*1}	6 ^{*1}	9	11	P024	-	F	General-purpose I/O port
						WR0X ^{*2, *3, *4, *5}	-		External bus/W/rte strobe 0 output
						SIN4_1	-		Multi-function serial ch.4 serial data input (1)
						PPG24_0	-		PPG ch.24 output (0)
						TIN1_0	-		Reload timer ch.1 event input (0)
						RTO4_1	-		Waveform generator ch.4 output pin (1)
						INT15_0	-		INT15 External interrupt input (0)
-	-	4 ^{*1}	7 ^{*1}	10	12	P025	-	A	General-purpose I/O port
						WR1X ^{*4, *5}	-		External bus/W/rte strobe 1 output
						SOT4_1	-		Multi-function serial ch.4 serial data output (1)
						PPG25_0	-		PPG ch.25 output (0)
						TIN2_0	-		Reload timer ch.2 event input (0)
-	-	-	-	-	13	P172	-	A	General-purpose I/O port
						PPG38_1	-		PPG ch.38 output (1)
-	4 ^{*1}	5 ^{*1}	8 ^{*1}	11	14	P026	-	F	General-purpose I/O port
						A00 ^{*3, *4, *5}	-		External bus/Address bit0 output (0)
						SCK4_1	-		Multi-function serial ch.4 clock I/O (1)
						PPG26_0	-		PPG ch.26 output (0)
						TIN3_0	-		Reload timer ch.3 event input (0)
4 ^{*1}	5 ^{*1}	6 ^{*1}	9 ^{*1}	12	15	P027	-	A	General-purpose I/O port
						A01 ^{*2, *3, *4, *5}	-		External bus/Address bit1 output (0)
						SCS40_1	-		Serial chip select 40 I/O (1)
						PPG27_0	-		PPG ch.27 output (0)
						TOT0_0	-		Reload timer ch.0 output (0)
						RTO3_1	-		Waveform generator ch.3 output pin (1)
-	-	-	-	-	16	P173	-	A	General-purpose I/O port
						PPG39_1	-		PPG ch.39 output (1)
-	-	7 ^{*1}	10 ^{*1}	13	17	P030	-	A	General-purpose I/O port
						A02 ^{*4, *5}	-		External bus/Address bit2 output (0)
						SCS41_1	-		Serial chip select 41 output (1)
						PPG28_0	-		PPG ch.28 output (0)
						TOT1_0	-		Reload timer ch.1 output (0)
-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	P031	-	A	General-purpose I/O port
						A03 ^{*3, *4, *5}	-		External bus/Address bit3 output (0)
						SCS42_1	-		Serial chip select 42 output (1)
						PPG29_0	-		PPG ch.29 output (0)
						TOT2_0 ^{*3}	-		Reload timer ch.2 output (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	P032	-	A	General-purpose I/O port
						A04 ^{*2, *3, *4, *5}	-		External bus/Address bit4 output (0)
						SCS43_1	-		Serial chip select 43 output (1)
						PPG30_0	-		PPG ch.30 output (0)
						TOT3_0	-		Reload timer ch.3 output (0)
						RTO2_1	-		Waveform generator ch.2 output pin (1)
6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	P033	-	A	General-purpose I/O port
						A05 ^{*2, *3, *4, *5}	-		External bus/Address bit5 output (0)
						PPG31_0	-		PPG ch.31 output (0)
						ICU3_3	-		Input capture ch.3 input (3)
						TIN4_0	-		Reload timer ch.4 event input (0)
						RTO1_1	-		Waveform generator ch.1 output pin (1)
						SCK3_2	-		Multi-function serial ch.3 clock I/O (2)
7 ^{*1}	9 ^{*1}	11 ^{*1}	14 ^{*1}	17	21	P034	-	A	General-purpose I/O port
						A06 ^{*2, *3, *4, *5}	-		External bus/Address bit6 output (0)
						OCU11_1	-		Output compare ch.11 output (1)
						ICU2_3	-		Input capture ch.2 input (3)
						TIN5_0	-		Reload timer ch.5 event input (0)
						RTO0_1	-		Waveform generator ch.0 output pin (1)
						SOT3_2	-		Multi-function serial ch.3 serial data output (2)
-	-	12	15	18	22	P150	-	F	General-purpose I/O port
						SOT8_0/ SDA8	-		Multi-function serial ch.8 serial data output (0)/ I ² C bus serial data I/O
						OCU10_1	-		Output compare ch.10 output (1)
						TRG6_0	-		PPG trigger 6 input (0)
						ICU1_3	-		Input capture ch.1 input (3)
						TIN6_0	-		Reload timer ch.6 event input (0)
						P151	-		General-purpose I/O port
8 ^{*1}	10 ^{*1}	13	16	19	23	SCK8_0/ SCL8 ^{*2, *3}	-	F	Multi-function serial ch.8 clock I/O (0)/ I ² C bus serial clock I/O
						OCU9_1	-		Output compare ch.9 output (1)
						TRG7_0	-		PPG trigger 7 input (0)
						ICU0_3	-		Input capture ch.0 input (3)
						TIN7_0	-		Reload timer ch.7 event input (0)
						ZIN0_2	-		U/D counter ch.0 ZIN input (2)
						DTT1_1	-		Waveform generator ch.1 input pin (1)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
9 ^{*1}	11 ^{*1}	14 ^{*1}	17 ^{*1}	20	24	P035	-	I	General-purpose I/O port
						A07 ^{*2, *3, *4, *5}	-		External bus/Address bit7 output
						SIN8_0 ^{*2, *3}	-		Multi-function serial ch.8 serial data input (0)
						OCU8_1	-		Output compare ch.8 output (1)
						TOT4_0	-		Reload timer ch.4 output (0)
						AIN0_0	-		U/D counter ch.0 AIN input (0)
						INT11_0	-		INT11 External interrupt input (0)
10 ^{*1}	12 ^{*1}	15 ^{*1}	18 ^{*1}	21	25	P036	-	A	General-purpose I/O port
						A08 ^{*2, *3, *4, *5}	-		External bus/Address bit8 output (0)
						SCS8_0 ^{*2, *3}	-		Serial chip select 8 I/O (0)
						OCU7_1	-		Output compare ch.7 output (1)
						TOT5_0	-		Reload timer ch.5 output (0)
						BIN0_0	-		U/D counter ch.0 BIN input (0)
-	-	16 ^{*1}	19 ^{*1}	22	26	P037	-	A	General-purpose I/O port
						A09 ^{*4, *5}	-		External bus/Address bit9 output (0)
						OCU6_1	-		Output compare ch.6 output (1)
						TOT6_0	-		Reload timer ch.6 output (0)
						ZIN0_0	-		U/D counter ch.0 ZIN input (0)
-	-	-	-	-	27	P174	-	A	General-purpose I/O port
						TRG8_1	-		PPG trigger 8 input (1)
-	-	-	-	-	28	P175	-	A	General-purpose I/O port
						TRG9_1	-		PPG trigger 9 input (1)
11 ^{*1}	13 ^{*1}	17 ^{*1}	20 ^{*1}	23	29	P040	-	A	General-purpose I/O port
						A10 ^{*2, *3, *4, *5}	-		External bus/Address bit10 output (0)
						PPG23_1	-		PPG ch.23 output (1)
						TOT7_0	-		Reload timer ch.7 output (0)
						AIN1_0	-		U/D counter ch.1 AIN input (0)
						SIN0_1	-		Multi-function serial ch.0 serial data input (1)
12 ^{*1}	14 ^{*1}	18 ^{*1}	21 ^{*1}	24	30	P041	-	I	General-purpose I/O port
						A11 ^{*2, *3, *4, *5}	-		External bus/Address bit11 output (0)
						SIN9_0	-		Multi-function serial ch.9 serial data input (0)
						ICU9_1	-		Input capture ch.9 input (1)
						BIN1_0	-		U/D counter ch.1 BIN input (0)
						INT12_0	-		INT12 External interrupt input (0)
13 ^{*1}	15 ^{*1}	19 ^{*1}	22 ^{*1}	25	31	P042	-	B	General-purpose I/O port
						A12 ^{*2, *3, *4, *5}	-		External bus/Address bit12 output
						SOT9_0	-		Multi-function serial ch.9 serial data output (0)
						AN47	-		ADC analog 47 input
						ICU8_1	-		Input capture ch.8 input (1)
						TRG0_1	-		PPG trigger 0 input (1)
						ZIN1_0	-		U/D counter ch.1 ZIN input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
-	-	20 ^{*1}	23 ^{*1}	26	32	P043	-	A	General-purpose I/O port
						A13 ^{*4, *5}	-		External bus/Address bit13 output (0)
						ICU7_1	-		Input capture ch.7 input (1)
						TRG1_1	-		PPG trigger 1 input (1)
-	16 ^{*1}	21 ^{*1}	24 ^{*1}	27	33	P044	-	A	General-purpose I/O port
						A14 ^{*3, *4, *5}	-		External bus/Address bit14 output (0)
						SCS9_0	-		Serial chip select 9 I/O (0)
						ICU6_1	-		Input capture ch.6 input (1)
						TRG2_1	-		PPG trigger 2 input (1)
14 ^{*1}	17 ^{*1}	22 ^{*1}	25 ^{*1}	28	34	P045	-	G	General-purpose I/O port
						A15 ^{*2, *3, *4, *5}	-		External bus/Address bit15 output (0)
						SCK9_0	-		Multi-function serial ch.9 clock I/O (0)
						AN46	-		ADC analog 46 input
						ICU5_1	-		Input capture ch.5 input (1)
						TRG3_1	-		PPG trigger 3 input (1)
						TOT1_2	-		Reload timer ch.1 output (2)
-	-	-	26 ^{*1}	29	35	P046	-	A	General-purpose I/O port
						A16 ^{*5}	-		External bus/Address bit16 output (0)
						ICU4_1	-		Input capture ch.4 input (1)
						TRG4_1	-		PPG trigger 4 input (1)
-	-	-	-	-	36	P176	-	A	General-purpose I/O port
						TRG10_0	-		PPG trigger 10 input (0)
15 ^{*1}	18 ^{*1}	23 ^{*1}	27 ^{*1}	30	37	P047	-	B	General-purpose I/O port
						A17 ^{*2, *3, *4, *5}	-		External bus/Address bit17 output (0)
						AN45	-		ADC analog 45 input
						TRG8_0	-		PPG trigger 8 input (0)
						TIN3_2	-		Reload timer ch.3 event input (2)
						SOT0_1	-		Multi-function serial ch.0 serial data output (1)
-	-	-	-	-	38	P177	-	A	General-purpose I/O port
						TRG11_0	-		PPG trigger 11 input (0)
-	-	-	28 ^{*1}	31	39	P050	-	A	General-purpose I/O port
						A18 ^{*5}	-		External bus/Address bit18 output
						TRG5_1	-		PPG trigger 5 input (1)
						PPG33_0	-		PPG ch.33 output (0)
-	-	-	-	32	40	P051	-	A	General-purpose I/O port
						A19	-		External bus/Address bit19 output
						TRG9_0	-		PPG trigger 9 input (0)
-	-	-	-	33	41	P052	-	A	General-purpose I/O port
						A20	-		External bus/Address bit20 output
						PPG34_0	-		PPG ch.34 output (0)
						INT14_0	-		INT14 External interrupt input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
16 * ¹	19 * ¹	24 * ¹	29 * ¹	34	42	P053	-	B	General-purpose I/O port
						A21 * ^{2, *^{3, *^{4, *⁵}}}	-		External bus/Address bit21 output
						AN44	-		ADC analog 44 input
						PPG35_0	-		PPG ch.35 output (0)
						INT14_1	-		INT14 External interrupt input (1)
						SCK0_1	-		Multi-function serial ch.0 clock I/O (1)
-	-	-	-	35	43	P054	-	A	General-purpose I/O port
						SYSCLK	-		External bus/System clock output
						PPG36_0	-		PPG ch.36 output (0)
17 * ¹	22 * ¹	27 * ¹	32 * ¹	38	46	P055	-	G	General-purpose I/O port
						CS2X * ^{2, *^{3, *^{4, *⁵}}}	-		External bus chip select 2 output
						SIN10_0	-		Multi-function serial ch.10 serial data input (0)
						AN43	-		ADC analog 43 input
						PPG37_0	-		PPG ch.37 output (0)
						TIN4_1	-		Reload timer ch.4 event input (1)
-	-	-	-	-	47	P180	-	A	General-purpose I/O port
						PPG40_0	-		PPG ch.40 output (0)
-	-	-	-	-	48	P181	-	A	General-purpose I/O port
						PPG41_0	-		PPG ch.41 output (0)
-	-	-	33 * ¹	39	49	P056	-	A	General-purpose I/O port
						CS3X * ⁵	-		External bus chip select 3 output
						ICU9_0	-		Input capture ch.9 input (0)
						PPG0_1	-		PPG ch.0 output (1)
						ICU0_1	-		Input capture ch.0 input (1)
						TIN5_1	-		Reload timer ch.5 event input (1)
						DTT1_2	-		Waveform generator ch.0-ch.5 input pin (2)
19 * ¹	24 * ¹	29 * ¹	35 * ¹	41	51	P057	-	G	General-purpose I/O port
						RDY * ^{2, *^{3, *^{4, *⁵}}}	-		External bus/Ready input (0)
						SCK10_1	-		Multi-function serial ch.10 clock I/O (1)
						AN42	-		ADC analog 42 input
						ICU8_0	-		Input capture ch.8 input (0)
						TRG0_2	-		PPG trigger 0 input (2)
						PPG1_1	-		PPG ch.1 output (1)
						ICU1_1	-		Input capture ch.1 input (1)
						TIN6_1	-		Reload timer ch.6 event input (1)
-	-	-	-	44	54	P142	-	F	General-purpose I/O port
						SCK10_0/ SCL10	-		Multi-function serial ch.10 clock I/O (0)/ I ² C bus serial clock I/O
						PPG38_0	-		PPG ch.38 output (0)
						TIN7_1	-		Reload timer ch.7 event input (1)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
-	-	-	-	45	55	P143	-	F	General-purpose I/O port
						SOT10_0/SDA1	-		Multi-function serial ch.10 serial data output (0)/ I ² C bus serial data I/O
						0	-		PPG ch.39 output (0)
						PPG39_0	-		Reload timer ch.4 output (1)
-	-	-	-	-	56	TOT4_1	-	A	General-purpose I/O port
						P182	-		PPG ch.42 output (0)
-	-	32	38	46	57	PPG42_0	-	A	General-purpose I/O port
						P060	-		Serial chip select 10 I/O (0)
						SCS10_0	-		PPG ch.2 output (1)
						PPG2_1	-		Input capture ch.2 input (1)
						ICU2_1	-		Reload timer ch.5 output (1)
						TOT5_1	-		INT13_0
22	27	33	39	47	58	P061	-	B	General-purpose I/O port
						SOT10_1	-		Multi-function serial ch.10 serial data output (1)
						AN41	-		ADC analog 41 input
						ICU6_0	-		Input capture ch.6 input (0)
						PPG3_1	-		PPG ch.3 output (1)
						ICU3_1	-		Input capture ch.3 input (1)
						TOT6_1	-		Reload timer ch.6 output (1)
						INT13_1	-		INT13 External interrupt input (1)
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)
-	-	40	46	54	68	P070	-	A	General-purpose I/O port
						ICU0_2	-		Input capture ch.0 input (2)
26	33	41	47	55	69	P071	-	G	General-purpose I/O port
						SCK4_2	-		Multi-function serial ch.4 clock I/O (2)
						AN35	-		ADC analog 35 input
						ICU1_2	-		Input capture ch.1 input (2)
						MONCLK	-		Clock monitor output pin
27	34	42	48	56	70	P072	-	G	General-purpose I/O port
						SIN4_0	-		Multi-function serial ch.4 serial data input (0)
						AN34	-		ADC analog 34 input
						ICU2_2	-		Input capture ch.2 input (2)
						INT5_0	-		INT5 External interrupt input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
-	35 * ³	43 * ⁴	49	57	71	P073	-	D	General-purpose I/O port
						SOT4_0/ SDA4 * ^{3, 4}	-		Multi-function serial ch.4 serial data output (0)/I ² C bus serial data I/O
						AN33	-		ADC analog 33 input
						ICU3_2	-		Input capture ch.3 input (2)
-	-	-	-	-	72	P186	-	A	General-purpose I/O port
						PPG46_0	-		PPG ch.46 output (0)
-	-	-	-	-	73	P187	-	A	General-purpose I/O port
						PPG47_0	-		PPG ch.47 output (0)
-	-	-	50	58	74	P074	-	E	General-purpose I/O port
						SCK4_0/ SCL4	-		Multi-function serial ch.4 clock I/O (0)/I ² C bus serial clock I/O
-	-	-	51	59	75	P075	-	F	General-purpose I/O port
						SIN3_0	-		Multi-function serial ch.3 serial data input (0)
						INT4_0	-		INT4 External interrupt input (0)
-	-	-	52	60	76	P076	-	E	General-purpose I/O port
						SOT3_0/ SDA3	-		Multi-function serial ch.3 serial data output (0)/I ² C bus serial data I/O
-	-	-	53	61	77	P077	-	E	General-purpose I/O port
						SCK3_0/ SCL3	-		Multi-function serial ch.3 clock I/O (0)/I ² C bus serial clock I/O
-	-	44	54	62	78	P152	-	A	General-purpose I/O port
						SCS53_0	-		Serial chip select 53 output (0)
28	36	45	55	63	79	P153	-	G	General-purpose I/O port
						SCK5_0/ SCL5	-		Multi-function serial ch.5 clock I/O (0)/I ² C bus serial clock I/O
						AN32	-		ADC analog 32 input
						FRCK1_1	-		Free-run timer 1 clock input (1)
						INT4_1	-		INT4 External interrupt input (1)
-	-	-	-	64	80	P080	-	A	General-purpose I/O port
						SCS52_0	-		Serial chip select 52 output (0)
						PPG0_0	-		PPG ch.0 output (0)
29	37	46	56	65	81	P081	-	G	General-purpose I/O port
						SOT5_0/ SDA5	-		Multi-function serial ch.5 serial data output (0)/I ² C bus serial data I/O
						AN0	-		ADC analog 0 input
						PPG1_0	-		PPG ch.1 output (0)
30	38	47	57	66	82	P082	-	G	General-purpose I/O port
						SIN5_0	-		Multi-function serial ch.5 serial data input (0)
						AN1	-		ADC analog 1 input
						PPG2_0	-		PPG ch.2 output (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
-	-	-	-	67	83	P083	-	B	General-purpose I/O port
						SCS50_0	-		Serial chip select 50 I/O (0)
						AN2	-		ADC analog 2 input
						PPG3_0	-		PPG ch.3 output (0)
-	-	-	-	68	84	P084	-	B	General-purpose I/O port
						SCS51_0	-		Serial chip select 51 output (0)
						AN3	-		ADC analog 3 input
						PPG4_0	-		PPG ch.4 output (0)
-	-	-	-	69	85	P085	-	A	General-purpose I/O port
						PPG5_0	-		PPG ch.5 output (0)
-	-	48	58	70	86	P086	-	C	General-purpose I/O port
						DAO1	-		DAC analog 1 output
						PPG6_0	-		PPG ch.6 output (0)
31	39	49	59	71	87	P087	-	C	General-purpose I/O port
						DAO0	-		DAC analog 0 output
						PPG7_0	-		PPG ch.7 output (0)
						INT8_0	-		INT8 External interrupt input (0)
-	-	-	-	-	90	P190	-	A	General-purpose I/O port
						TIN0_1	-		Reload timer ch.0 event input (1)
-	-	-	-	-	91	P191	-	A	General-purpose I/O port
						TIN1_1	-		Reload timer ch.1 event input (1)
-	-	-	-	74	92	P090	-	B	General-purpose I/O port
						AN4	-		ADC analog 4 input
						ICU0_0	-		Input capture ch.0 input (0)
						TIN2_1	-		Reload timer ch.2 event input (1)
-	-	-	-	75	93	P091	-	B	General-purpose I/O port
						AN5	-		ADC analog 5 input
						PPG41_1	-		PPG ch.41 output (1)
						ICU1_0	-		Input capture ch.1 input (0)
						TIN3_1	-		Reload timer ch.3 event input (1)
-	-	-	-	76	94	P092	-	B	General-purpose I/O port
						AN6	-		ADC analog 6 input
						PPG40_1	-		PPG ch.40 output (1)
						ICU2_0	-		Input capture ch.2 input (0)
						TOT0_1	-		Reload timer ch.0 output (1)
-	-	-	-	-	95	P192	-	A	General-purpose I/O port
						PPG24_1	-		PPG ch.24 output (1)
						TOT1_1	-		Reload timer ch.1 output (1)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
34 *1	42 *1	52	62	77	96	P093	-	J	General-purpose I/O port
						TX0_1	-		CAN transmission data 0 output (1)
						SIN11_0	-		Multi-function serial ch.11 serial data input (0)
						AN7	-		ADC analog 7 input
						ICU4_2	-		Input capture ch.4 input (2)
						PPG16_1	-		PPG ch.16 output (1)
						ICU3_0	-		Input capture ch.3 input (0)
						TOT2_1 *2, *3	-		Reload timer ch.2 output (1)
-	-	-	-	78	97	P094	-	B	General-purpose I/O port
						AN8	-		ADC analog 8 input
						ICU4_0	-		Input capture ch.4 input (0)
						TOT3_1	-		Reload timer ch.3 output (1)
-	-	53	63	79	98	P095	-	B	General-purpose I/O port
						TX0(128)	-		CAN transmission data 0 output
						SCS11_0	-		Serial chip select 11 I/O (0)
						AN9	-		ADC analog 9 input
35	43	54	64	80	99	P096	-	G	General-purpose I/O port
						RX0(128)	-		CAN reception data 0 input
						SOT11_0/ SDA11	-		Multi-function serial ch.11 serial data output (0)/I ² C bus serial data I/O
						AN10	-		ADC analog 10 input
						INT0_0	-		INT0 External interrupt input (0)
36	44	55	65	81	100	P097	-	G	General-purpose I/O port
						SCK11_0/ SCL11	-		Multi-function serial ch.11 clock I/O (0)/ I ² C bus serial clock I/O
						AN11	-		ADC analog 11 input
						ICU5_0	-		Input capture ch.5 input (0)
						PPG17_1	-		PPG ch.17 output (1)
-	48 *1	59	69	85	104	P100	-	G	General-purpose I/O port
						SCK7_0/ SCL7 *3	-		Multi-function serial ch.7 clock I/O (0)/ I ² C bus serial clock I/O
						AN12	-		ADC analog 12 input
						PPG8_0	-		PPG ch.8 output (0)
-	-	60	70	86	105	P101	-	G	General-purpose I/O port
						SOT7_0/ SDA7	-		Multi-function serial ch.7 serial data output (0)/I ² C bus serial data I/O
						AN13	-		ADC analog 13 input
						PPG9_0	-		PPG ch.9 output (0)
40 *1	49 *1	61	71	87	106	P102	-	G	General-purpose I/O port
						SIN7_0 *2, *3	-		Multi-function serial ch.7 serial data input (0)
						AN14	-		ADC analog 14 input
						PPG10_0	-		PPG ch.10 output (0)
						INT10_0	-		INT10 External interrupt input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
41 *1	50 *1	62	72	88	107	P103	-	H	General-purpose I/O port
						SCS73_0 * ^{2, *3}	-		Serial chip select 73 output (0)
						AN15	-		ADC analog 15 input
						PPG11_0	-		PPG ch.11 output (0)
42 *1	51 *1	63	73	89	108	P104	-	H	General-purpose I/O port
						SCS72_0 * ^{2, *3}	-		Serial chip select 72 output (0)
						AN16	-		ADC analog 16 input
						PPG12_0	-		PPG ch.12 output (0)
43 *1	52 *1	64	74	90	109	P105	-	H	General-purpose I/O port
						SCS71_0 * ^{2, *3}	-		Serial chip select 71 output (0)
						AN17	-		ADC analog 17 input
						PPG13_0	-		PPG ch.13 output (0)
-	-	65	75	91	110	P106	-	H	General-purpose I/O port
						SCS70_0	-		Serial chip select 70 I/O (0)
						AN18	-		ADC analog 18 input
						PPG14_0	-		PPG ch.14 output (0)
-	53	66	76	92	111	P107	-	B	General-purpose I/O port
						AN19	-		ADC analog 19 input
						PPG15_0	-		PPG ch.15 output (0)
-	-	-	-	-	112	P193	-	A	General-purpose I/O port
						PPG25_1	-		PPG ch.25 output (1)
-	-	-	77	93	113	P154	-	B	General-purpose I/O port
						AN20	-		ADC analog 20 input
-	-	-	78	94	114	P155	-	B	General-purpose I/O port
						AN21	-		ADC analog 21 input
44	54	67	79	95	115	NMIX	N	M	Non-masking interrupt input
45	55	68	80	96	116	P110	-	B	General-purpose I/O port
						TX1(64)	-		CAN transmission data 1 output
						SCS63_0	-		Serial chip select 63 output (0)
						AN22	-		ADC analog 22 input
-	-	69	81	97	117	P111	-	G	General-purpose I/O port
						RX1(64)	-		CAN reception data 1 input
						SCS62_0	-		Serial chip select 62 output (0)
						AN23	-		ADC analog 23 input
						INT1_0	-		INT1 External interrupt input (0)
-	-	-	82	98	118	P112	-	B	General-purpose I/O port
						AN24	-		ADC analog 24 input
						PPG16_0	-		PPG ch.16 output (0)
						RTO0_0	-		Waveform generator ch. 0 output pin (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
-	-	-	83	99	119	P113	-	B	General-purpose I/O port
						AN25	-		ADC analog 25 input
						PPG17_0	-		PPG ch.17 output (0)
						RTO1_0	-		Waveform generator ch. 1 output pin (0)
-	-	-	-	-	120	P194	-	A	General-purpose I/O port
						FRCK5_1	-		Free-run timer 5 clock input (1)
						PPG26_1	-		PPG ch.26 output (1)
-	-	-	-	-	121	P195	-	A	General-purpose I/O port
						FRCK4_1	-		Free-run timer 4 clock input (1)
						PPG27_1	-		PPG ch.27 output (1)
-	56	70	84	100	122	P114	-	B	General-purpose I/O port
						SCS61_0	-		Serial chip select 61 output (0)
						AN26	-		ADC analog 26 input
						PPG18_0	-		PPG ch.18 output (0)
						RTO2_0	-		Waveform generator ch.2 output pin (0)
46	57	71	85	101	123	P115	-	G	General-purpose I/O port
						RX1_1	-		CAN reception data 1 input (1)
						SOT6_0/ SDA6	-		Multi-function serial ch.6 serial data output (0)/I ² C bus serial data I/O
						AN27	-		ADC analog 27 input
						PPG19_0	-		PPG ch.19 output (0)
						RTO3_0	-		Waveform generator ch.3 output pin (0)
						INT1_1	-		INT1 External interrupt input (1)
47	58	72	86	102	124	P116	-	G	General-purpose I/O port
						SCK6_0/ SCL6	-		Multi-function serial ch.6 clock I/O (0)/ I ² C bus serial clock I/O
						AN28	-		ADC analog 28 input
						PPG20_0	-		PPG ch.20 output (0)
						RTO4_0	-		Waveform generator ch.4 output pin (0)
-	-	73	87	103	125	P117	-	B	General-purpose I/O port
						SCS60_0	-		Serial chip select 60 I/O (0)
						AN29	-		ADC analog 29 input
						PPG21_0	-		PPG ch.21 output (0)
						RTO5_0	-		Waveform generator ch.5 output pin (0)
-	-	-	-	-	126	P196	-	A	General-purpose I/O port
						FRCK3_1	-		Free-run timer 3 clock input (1)
						PPG28_1	-		PPG ch.28 output (1)
-	-	-	88	104	127	P120	-	B	General-purpose I/O port
						AN30	-		ADC analog 30 input
						OCU6_0	-		Output compare ch.6 output (0)
						PPG22_0	-		PPG ch.22 output (0)
						INT9_0	-		INT9 External interrupt input (0)

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
-	-	-	-	105	128	P121	-	A	General-purpose I/O port
48	59	74	89	106		OCU7_0	-		Output compare ch.7 output (0)
						PPG23_0	-		PPG ch.23 output (0)
-	-	-	-	-	129	P122	-	J	General-purpose I/O port
						SIN6_0	-		Multi-function serial ch.6 serial data input (0)
						AN31	-		ADC analog 31 input
						OCU8_0	-		Output compare ch.8 output (0)
						INT9_1	-		INT9 External interrupt input (1)
-	-	-	-	-	130	P197	-	A	General-purpose I/O port
						PPG29_1	-		PPG ch.29 output (1)
-	-	-	-	107	131	P123	-	A	General-purpose I/O port
						OCU9_0	-		Output compare ch.9 output (0)
49	62	77	92	110	134	DEBUGIF	-	L	MDI I/O for debugger (OCD)
-	-	-	-	-	135	P160	-	A	General-purpose I/O port
						PPG30_1	-		PPG ch.30 output (1)
-	-	-	-	-	136	P161	-	A	General-purpose I/O port
						PPG31_1	-		PPG ch.31 output (1)
-	-	-	-	111	137	P124	-	A	General-purpose I/O port
						OCU10_0	-		Output compare ch.10 output (0)
-	-	-	93	112	138	P125	-	A	General-purpose I/O port
						OCU11_0	-		Output compare ch.11 output (0)
50	63	78	94	113	139	P126	-	F	General-purpose I/O port
						SIN0_0	-		Multi-function serial ch.0 serial data input (0)
						INT6_0	-		INT6 External interrupt input (0)
-	64	79	95	114	140	P127	-	A	General-purpose I/O port
						SOT0_0	-		Multi-function serial ch.0 serial data output (0)
-	-	80	96	115	141	P130	-	F	General-purpose I/O port
						SCK0_0	-		Multi-function serial ch.0 clock I/O (0)
-	-	-	-	-	142	P162	-	A	General-purpose I/O port
						TRG5_2	-		PPG trigger 5 input (2)
-	-	-	-	-	143	P163	-	A	General-purpose I/O port
						TRG6_2	-		PPG trigger 6 input (2)
51	65	81	97	116	144	MD0	-	K	Mode pin 0
52	66	82	98	117	145	MD1	-	K	Mode pin 1
53	67	83	99	118	146	X0	-	N	Main clock oscillation input
54	68	84	100	119	147	X1	-	N	Main clock oscillation output
56	70	86	102	121	149	P135	-	A	General-purpose I/O port
						DTTI_0	-		Waveform generator ch.0-ch.5 input pin (0)
						X1A	-	O	Sub clock oscillation output
57	71	87	103	122	150	P136	-	A	General-purpose I/O port
						X0A	-	O	Sub clock oscillation input

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹	
64	80	100	120	144	176					
58	72	88	104	123	151	RSTX	N	M	External reset input	
-	-	-	-	124	152	P131	-	A	General-purpose I/O port	
-	-	-	-	124		ADTG0_0	-		A/D converter external trigger input 0 (0)	
-	-	-	105	125	153	P132	-	A	General-purpose I/O port	
-	-	-	105	125		SCS1_0	-		Serial chip select 1 I/O (0)	
-	-	-	105	125		ADTG1_0	-		A/D converter external trigger input 1 (0)	
-	-	89	106	126	154	P133	-	A	General-purpose I/O port	
-	-	89	106	126		TX2(64)	-		CAN transmission data 2 output	
-	-	90	107	127	155	P134	-	F	General-purpose I/O port	
-	-	90	107	127		RX2(64)	-		CAN reception data 2 input	
-	-	90	107	127		SCS1_1	-		Serial chip select 1 I/O (1)	
-	-	90	107	127		ICU7_0	-		Input capture ch.7 input (0)	
-	-	90	107	127		INT7_0	-		INT7 External interrupt input (0)	
-	-	91	108	128	156	P144	-	F	General-purpose I/O port	
-	-	91	108	128		SCK1_1	-		Multi-function serial ch.1 clock I/O (1)	
-	-	94* ¹	111* ¹	131	159	P000	-	F	General-purpose I/O port	
-	-	94* ¹				D16* ^{4, *5}	-		External bus data bit16 I/O (0)	
-	-	94* ¹				SIN1_0	-		Multi-function serial ch.1 serial data input (0)	
-	-	94* ¹				TIOA0_1* ⁴	-		TIOA output of Base timer ch.0 (1)	
-	-	94* ¹				INT2_0	-		INT2 External interrupt input (0)	
-	75* ¹	95* ¹	112* ¹	132	160	P001	-	A	General-purpose I/O port	
-	75* ¹	95* ¹				D17* ^{3, *4, *5}	-		External bus data bit17 I/O	
-	-	-	113* ¹	133		SOT1_0* ³	-		Multi-function serial ch.1 serial data output (0)	
-	-	-				TIOA1_1	-		TIOA I/O of Base timer ch.1 (1)	
-	-	-	113* ¹	133	161	P002	-	F	General-purpose I/O port	
-	-	-				D18* ⁵	-		External bus data bit18 I/O	
-	-	-				SCK1_0	-		Multi-function serial ch.1 clock I/O (0)	
-	-	-				TIOB0_1	-		TIOB input of Base timer ch.0 (1)	
-	76* ¹	96* ¹	114* ¹	134	162	P003	-	F	General-purpose I/O port	
-	76* ¹	96* ¹				D19* ^{3, *4, *5}	-		External bus data bit19 I/O	
-	76* ¹	96* ¹				SIN2_0	-		Multi-function serial ch.2 serial data input (0)	
-	76* ¹	96* ¹				TIOB1_1	-		TIOB input of Base timer ch.1 (1)	
-	76* ¹	96* ¹				INT3_0	-		INT3 External interrupt input (0)	
-	-	-	-	135	163	P004	-	A	General-purpose I/O port	
-	-	-				D20	-		External bus data bit20 I/O (0)	
-	-	-				SOT2_0	-		Multi-function serial ch.2 serial data output (0)	
-	-	-	-	-	164	P164	-	A	General-purpose I/O port	
-	-	-	-	-		PPG32_1	-		PPG ch.32 output (1)	

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
61 *1	77 *1	97 *1	115 *1	136 *1	165 *1	P005	-	F	General-purpose I/O port
						D21 *2, *3, *4, *5	-		External bus data bit21 I/O (0)
						SCK2_0 *2	-		Multi-function serial ch.2 clock I/O (0)
						ADTG0_1	-		A/D converter external trigger input 0 (1)
						INT7_1	-		INT7 External interrupt input (1)
						RX2(64) *4, *5, *6, *7	-		CAN reception data 2 input
-	-	-	-	-	166	P165	-	A	General-purpose I/O port
						PPG33_1	-		PPG ch.33 output (1)
62 *1	78 *1	98 *1	116 *1	137 *1	167 *1	P006	-	A	General-purpose I/O port
						D22 *2, *3, *4, *5	-		External bus data bit22 I/O (0)
						SCS2_0 *2	-		Serial chip select 2 I/O (0)
						ADTG1_1	-		A/D converter external trigger input 1 (1)
						INT2_1	-		INT2 External interrupt input (1)
						TX2(64) *4, *5, *6, *7	-		CAN transmission data 2 output
-	-	-	117 *1	138	168	P007	-	A	General-purpose I/O port
						D23 *5	-		External bus data bit23 I/O
-	-	-	-	-	169	P166	-	A	General-purpose I/O port
						PPG34_1	-		PPG ch.34 output (1)
-	-	-	118 *1	139	170	P010	-	A	General-purpose I/O port
						D24 *5	-		External bus data bit24 I/O
63 *1	79 *1	99 *1	119 *1	140	171	P011	-	A	General-purpose I/O port
						WOT	-		RTC output signal
						D25 *2, *3, *4, *5	-		External bus data bit25 I/O
						SOT2_1 *2	-		Multi-function serial ch.2 serial data output (1)
						TIOA0_0 *2, *3, *4	-		TIOA output of Base timer ch.0 (0)
						INT3_1	-		INT3 External interrupt input (1)
-	-	-	-	141	172	P012	-	A	General-purpose I/O port
						D26	-		External bus data bit26 I/O
						TIOB0_0	-		TIOB input of Base timer ch.0 (0)
-	-	-	-	-	173	P167	-	A	General-purpose I/O port
						PPG35_1	-		PPG ch.35 output (1)
-	-	-	-	142	174	P013	-	A	General-purpose I/O port
						D27	-		External bus data bit27 I/O
						TIOA1_0	-		TIOA I/O of Base timer ch.1 (0)
-	-	-	-	143	175	P014	-	A	General-purpose I/O port
						D28	-		External bus data bit28 I/O
						TIOB1_0	-		TIOB input of Base timer ch.1 (0)
18	23	28	34	40	50	AVCC1	-	-	Analog power supply for AD/DA convertor unit1
39	47	58	68	84	103	AVCC0	-	-	Analog power supply for AD/DA convertor unit0

Pin No.						Pin Name	Polarity	I/O Circuit types* ⁸	Function* ⁹
64	80	100	120	144	176				
20	25	30	36	42	52	AVRH1	-	-	Upper limit reference voltage for AD convertor unit1
38	46	57	67	83	102	AVRH0	-	-	Upper limit reference voltage for AD convertor unit0
21	26	31	37	43	53	AVSS1/ AVRL1	-	-	GND for AD/DA convertor unit1 Lower limit reference voltage for AD convertor unit1
37	45	56	66	82	101	AVSS0/ AVRL0	-	-	GND for AD/DA convertor unit0 Lower limit reference voltage for AD convertor unit0
60	74	93	110	130	158	C	-	-	External capacity connection output
-	20	25	30	36	44	VCC	-	-	+5.0V power supply
32	40	50	60	72	88				
-	61	76	91	109	133				
64	80	100	120	144	176				
1	1	1	1	1	1	VSS	-	-	GND
-	21	26	31	37	45				
33	41	51	61	73	89				
-	60	75	90	108	132				
55	69	85	101	120	148				
59	73	92	109	129	157				

*1: There is a restriction of pin functions. See "Pin Name" of this table.

*2: not supported in 64 pin

*3: not supported in 80 pin

*4: not supported in 100 pin

*5: not supported in 120 pin

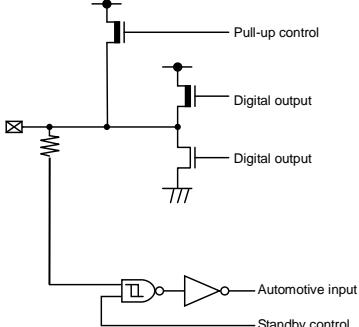
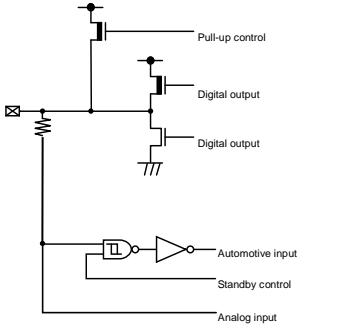
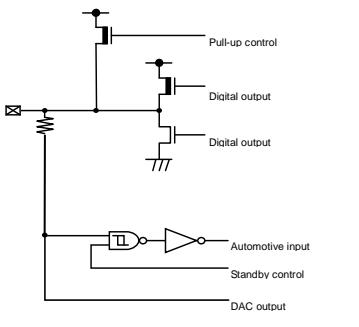
*6: not supported in 144 pin

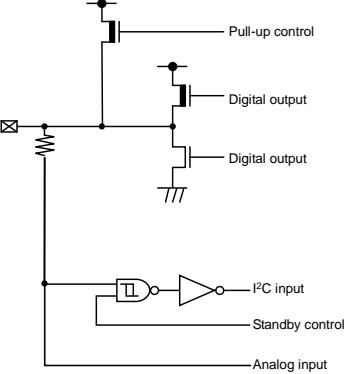
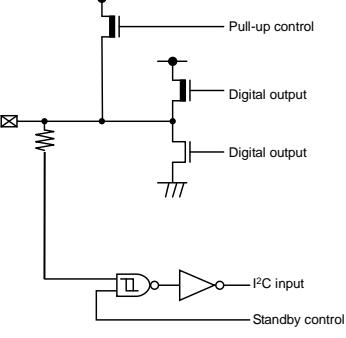
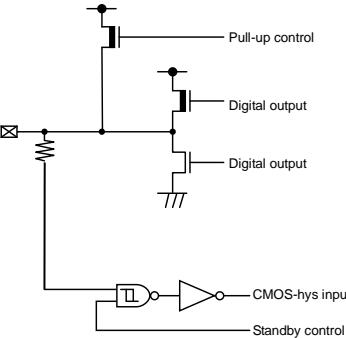
*7: not supported in 176 pin

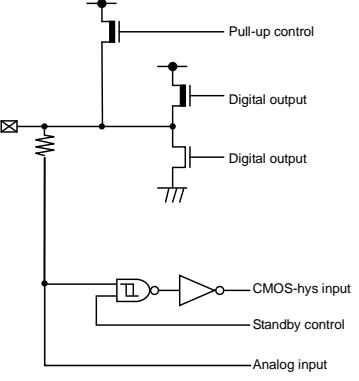
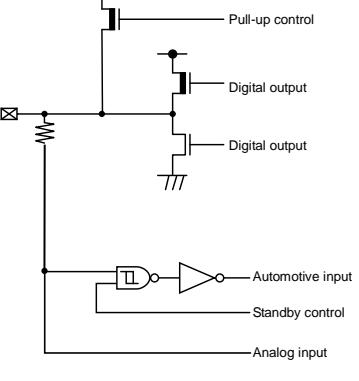
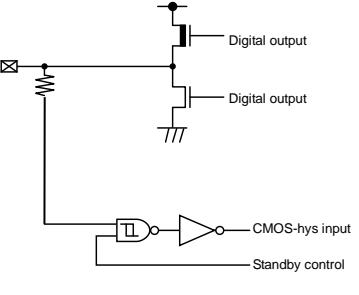
*8: For the I/O circuit types, see [I/O Circuit Type](#).

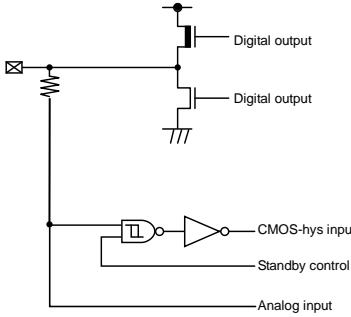
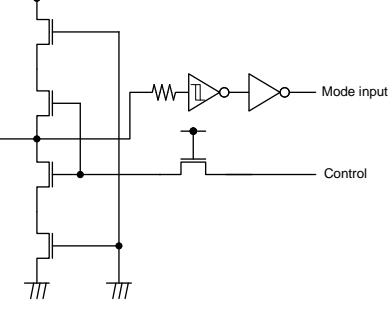
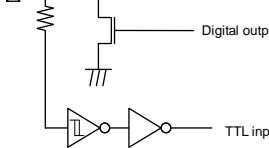
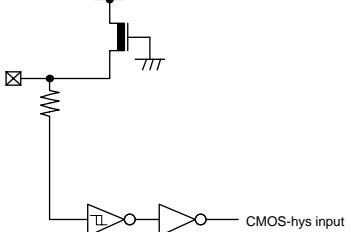
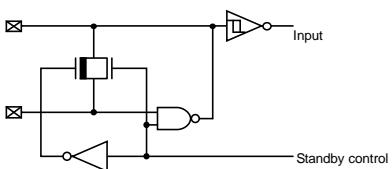
*9: For switching, see "I/O Port" in HARDWARE MANUAL.

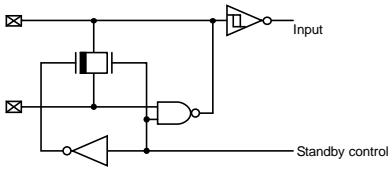
4. I/O Circuit Type

Type	Circuit	Remarks
A	 <p>Pull-up control Digital output Digital output Automotive input Standby control</p>	<ul style="list-style-type: none"> General-purpose I/O port Output 4 mA Pull-up resistor control 50 kΩ Automotive input
B	 <p>Pull-up control Digital output Digital output Automotive input Standby control Analog input</p>	<ul style="list-style-type: none"> Analog input, General-purpose I/O port Output 4 mA Pull-up resistor control 50 kΩ Automotive input
C	 <p>Pull-up control Digital output Digital output Automotive input Standby control DAC output</p>	<ul style="list-style-type: none"> DAC output, General-purpose I/O port Output 4 mA Pull-up resistor control 50 kΩ Automotive input

Type	Circuit	Remarks
D	 <p>Pull-up control Digital output Digital output I²C input Standby control Analog input</p>	<ul style="list-style-type: none"> •I²C Analog input, General-purpose I/O port •Output 3 mA •Pull-up resistor control 50 kΩ •I²C hysteresis input
E	 <p>Pull-up control Digital output Digital output I²C input Standby control</p>	<ul style="list-style-type: none"> •I²C,General-purpose I/O port •Output 3 mA •Pull-up resistor control 50 kΩ •I²C hysteresis input
F	 <p>Pull-up control Digital output Digital output CMOS-hys input Standby control</p>	<ul style="list-style-type: none"> •General-purpose I/O port •Output 4 mA •Pull-up resistor control 50 kΩ •CMOS hysteresis input

Type	Circuit	Remarks
G	 <p>Pull-up control Digital output Digital output CMOS-hys input Standby control Analog input</p>	<ul style="list-style-type: none"> • Analog input, General-purpose I/O port • Output 4 mA • Pull-up resistor control 50 kΩ • CMOS hysteresis input
H	 <p>Pull-up control Digital output Digital output Automotive input Standby control Analog input</p>	<ul style="list-style-type: none"> • Analog input, General-purpose I/O port • Output 12 mA • Pull-up resistor control 50 kΩ • Automotive input
I	 <p>Digital output Digital output CMOS-hys input Standby control</p>	<ul style="list-style-type: none"> • General-purpose I/O port (5 V tolerant) • Output 4 mA • CMOS hysteresis input

Type	Circuit	Remarks
J	 <p>Digital output Digital output CMOS-hys input Standby control Analog input</p>	<ul style="list-style-type: none"> • Analog input, General-purpose I/O port (5 V tolerant) • Output 4 mA • CMOS hysteresis input
K	 <p>Mode input Control</p>	<ul style="list-style-type: none"> • Mode I/O • CMOS hysteresis input
L	 <p>Digital output TTL input</p>	<ul style="list-style-type: none"> • Open-drain I/O • Output 25 mA (Nch open-drain) • TTL input
M	 <p>CMOS-hys input</p>	<ul style="list-style-type: none"> • CMOS hysteresis input • Pull-up resistor 50 kΩ
N	 <p>Input Standby control</p>	<ul style="list-style-type: none"> • Main oscillation I/O

Type	Circuit	Remarks
O	 <p>Input</p> <p>Standby control</p>	<ul style="list-style-type: none"> •Sub oscillation I/O

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause

absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70 % relative humidity, and at temperatures between 5 °C and 30 °C.
When you open Dry Package that recommends humidity 40 % to 70 % relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40 % and 70 %. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

This section explains the latch-up prevention and pin processing.

- For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC, AVRH) and analog input must not exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

- Treatment of unused pins

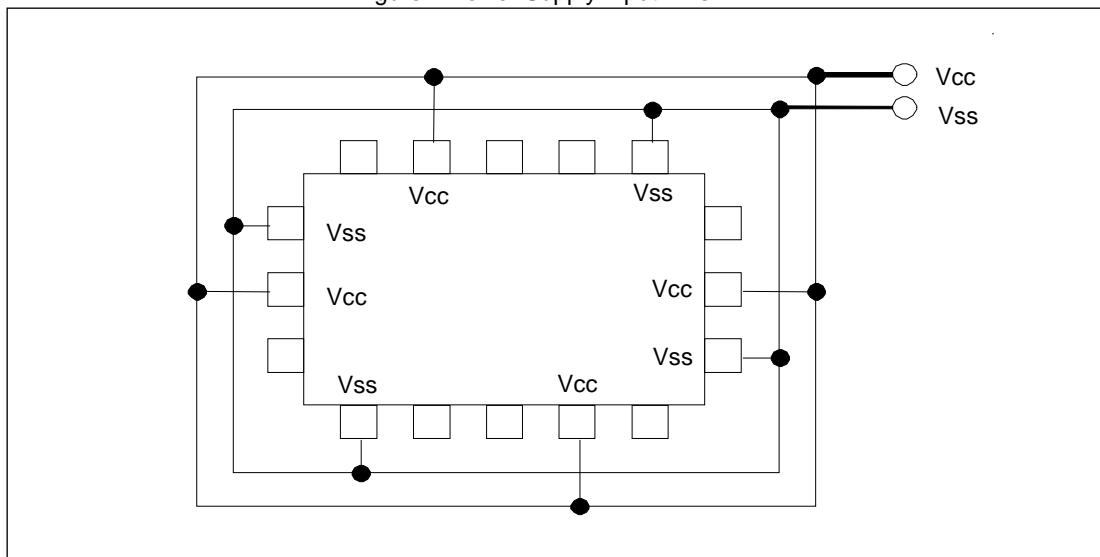
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2 kΩ resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

- Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins



The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

■ Crystal oscillation circuit

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

■ Mode pins (MD1, MD0)

Connect the MD1 and MD0 mode pins to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■ During power-on

To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

■ Notes during PLL clock operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

■ Treatment of A/D converter power supply pins

Connect the pins to have AVCC = AVRH = VCC and AVSS/AVRL = VSS even if the A/D converter is not used.

■ Notes on using external clock

An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

■ Power-on sequence of A/D converter analog inputs

Be sure to turn on the digital power supply (Vcc) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN47). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc). When the AVRH pin voltage is turned on or off, it must not exceed AVCC. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

■ Treatment of C pin

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

Note: Please see the latest data sheet for a detailed specification of the operation voltage.

■ Function switching of a multiplexed port

To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see "I/O PORTS" in the hardware manual.

■ Low-power consumption mode

To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of "POWER CONSUMPTION CONTROL" in the hardware manual.

Take the following notes when using a monitor debugger.

- Do not set a break point for the low-power consumption transition program.
- Do not execute an operation step for the low-power consumption transition program.

■ Notes When Writing Data in a Register Having the Status Flag

When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

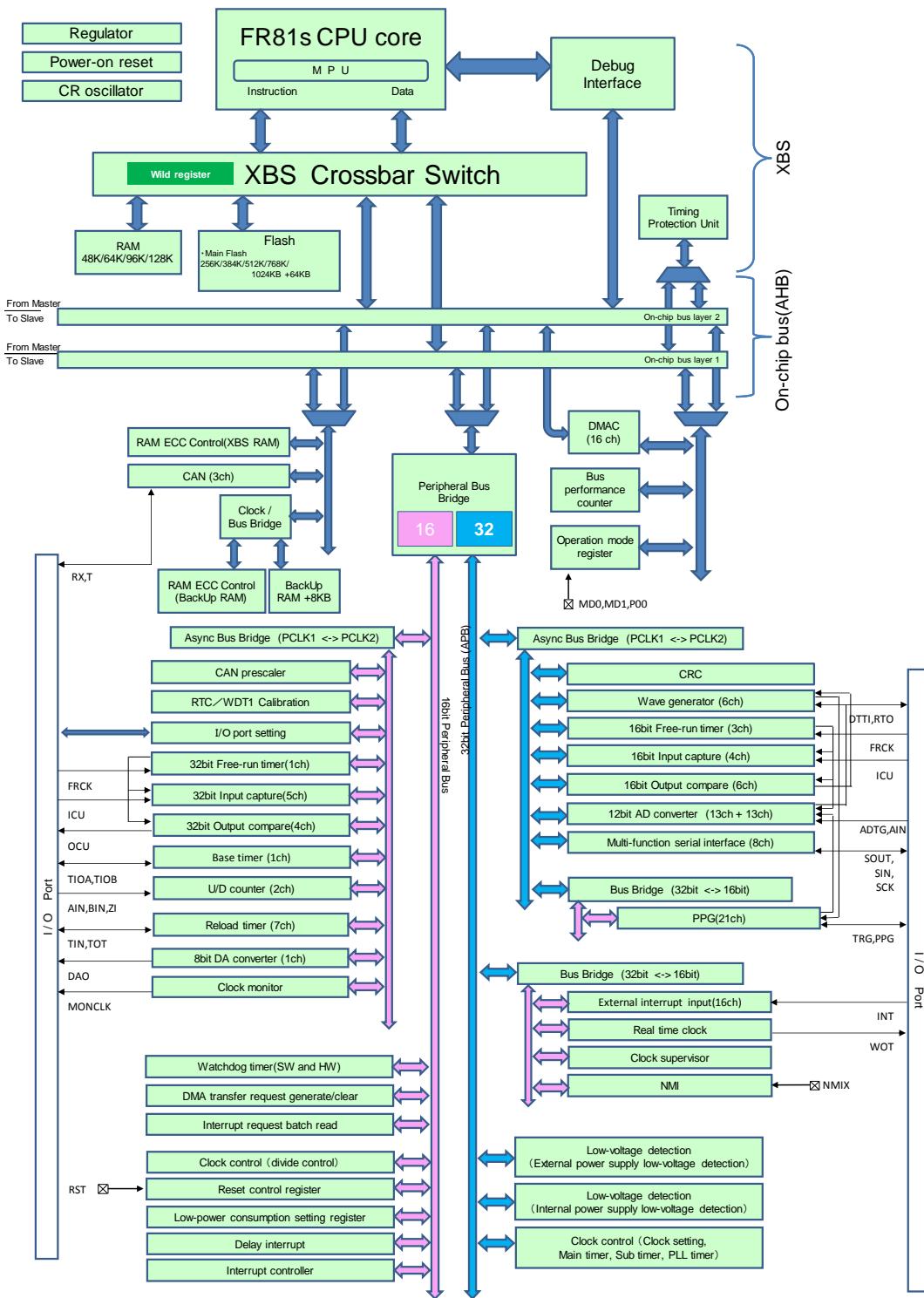
The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

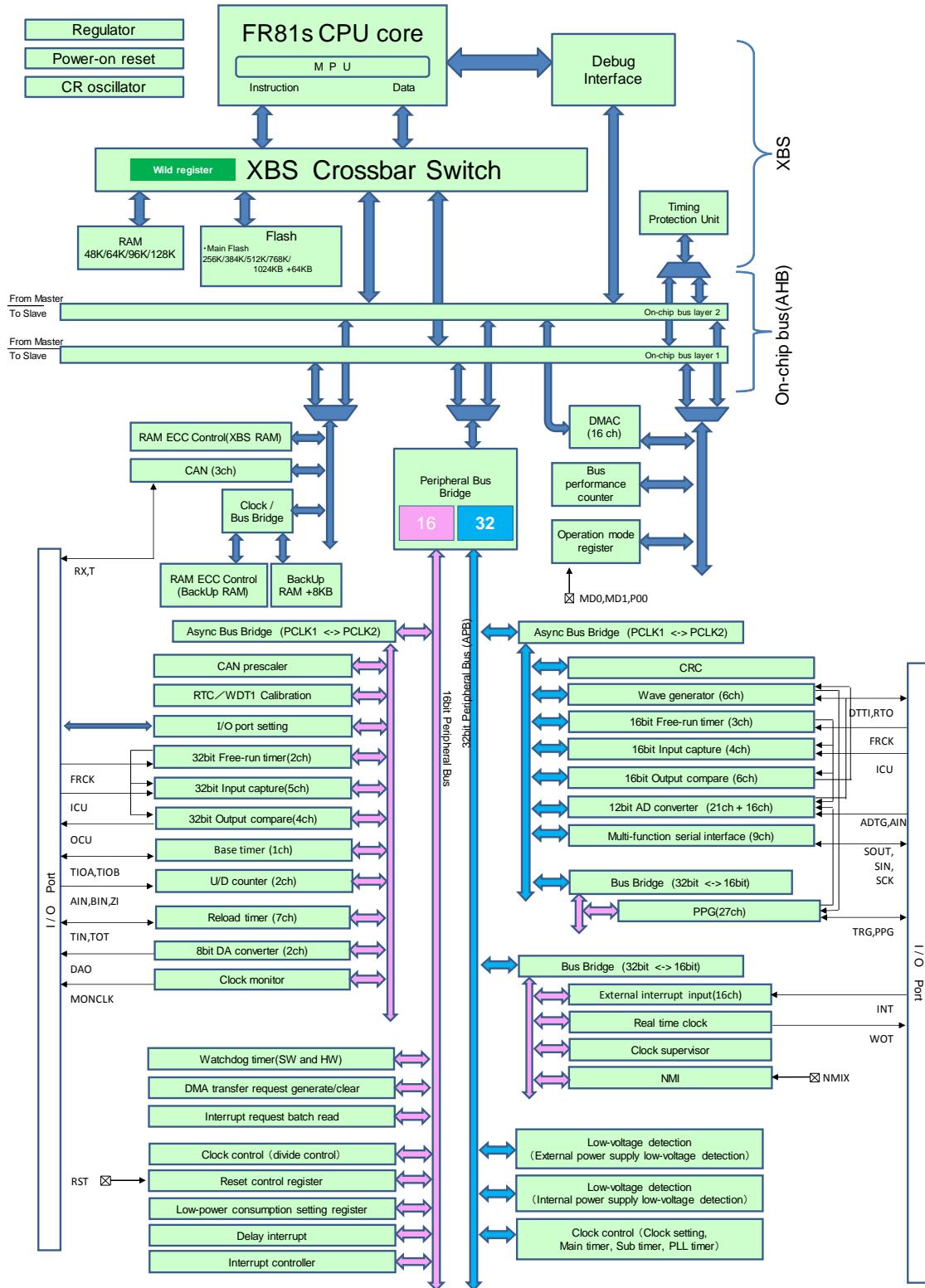
Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

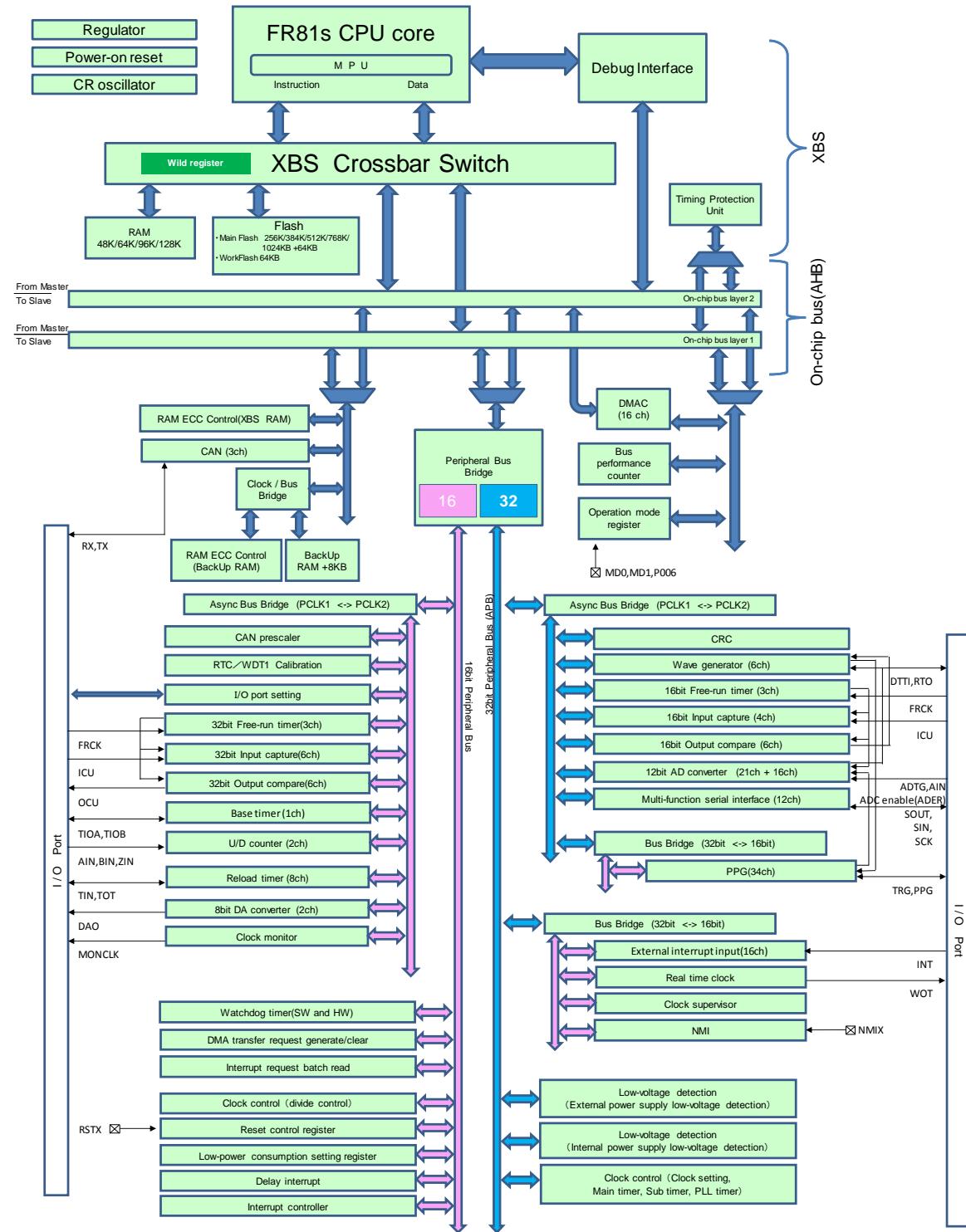
Note: These points can be ignored because the bit instructions are already taken the points into consideration.

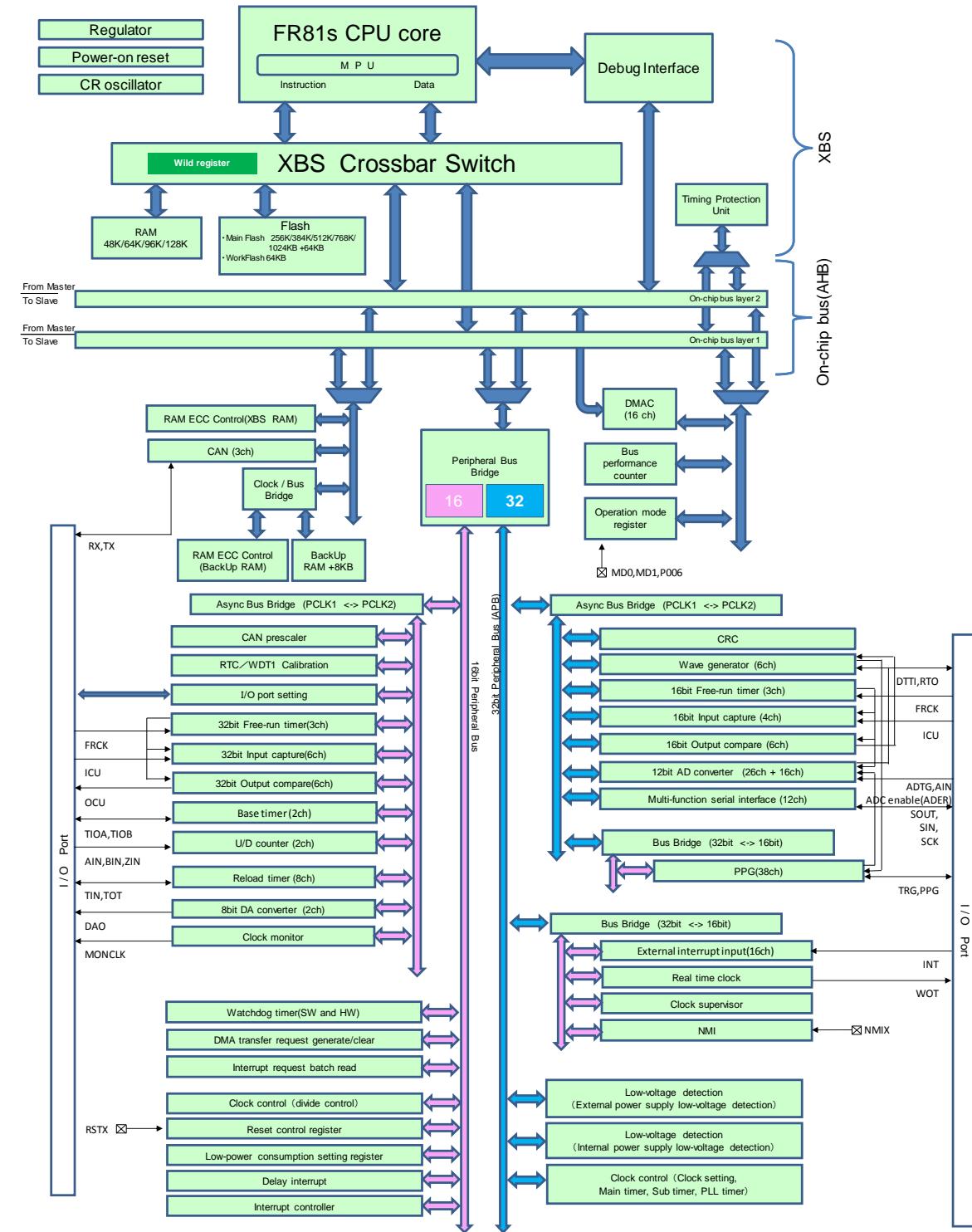
7. Block Diagram

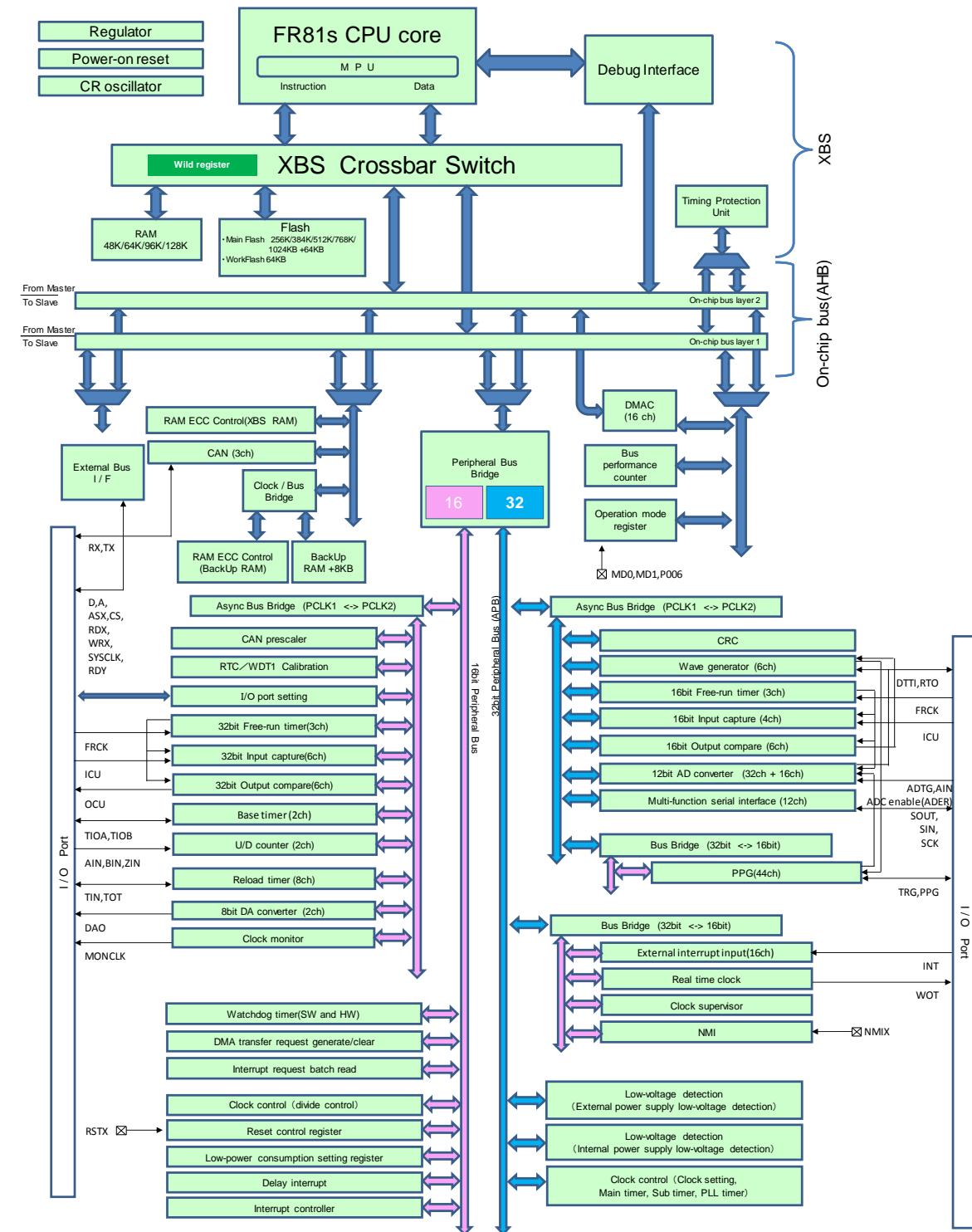
CY91F522B, CY91F523B, CY91F524B, CY91F525B, CY91F526B

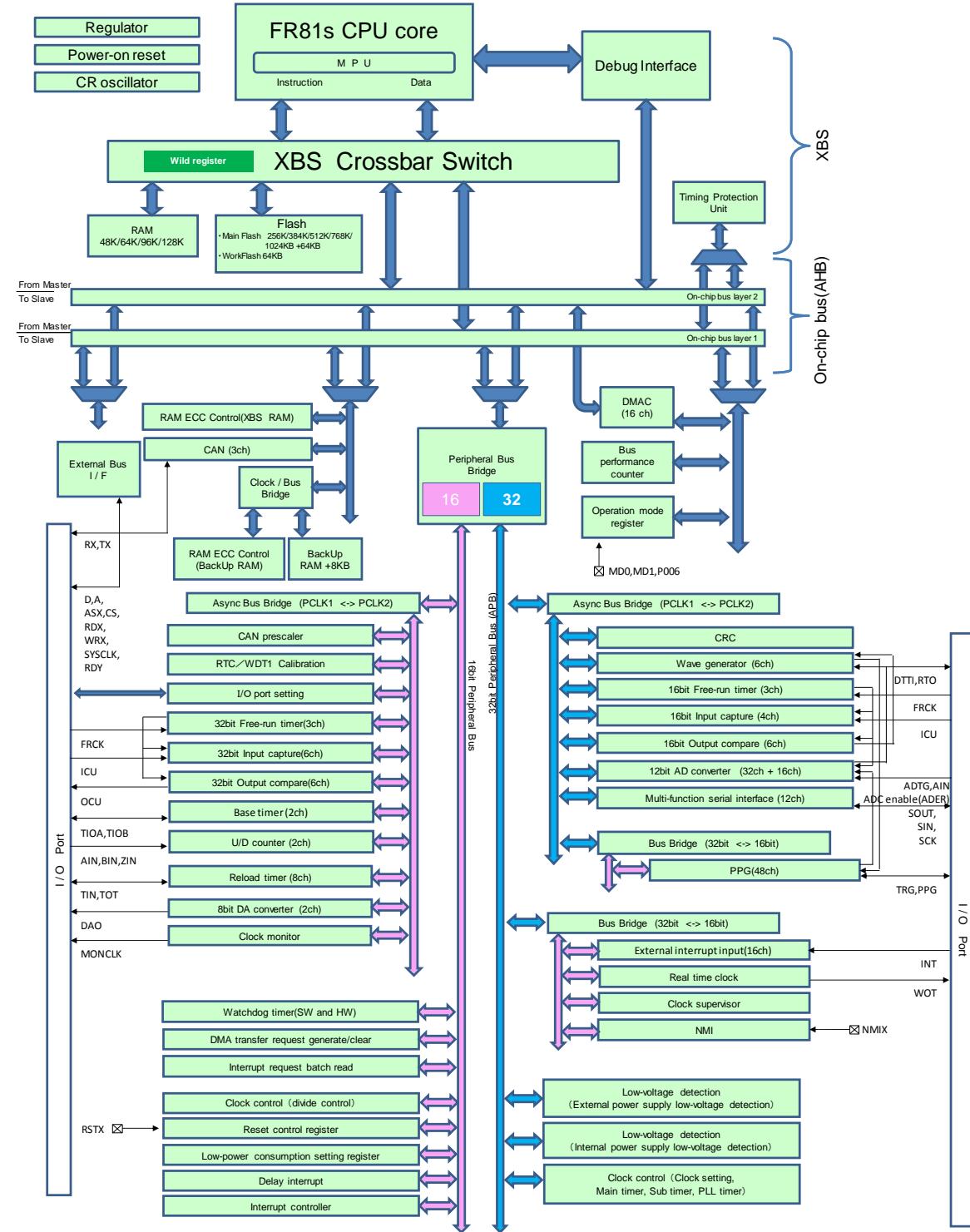


CY91F522D, CY91F523D, CY91F524D, CY91F525D, CY91F526D


CY91F522F, CY91F523F, CY91F524F, CY91F525F, CY91F526F


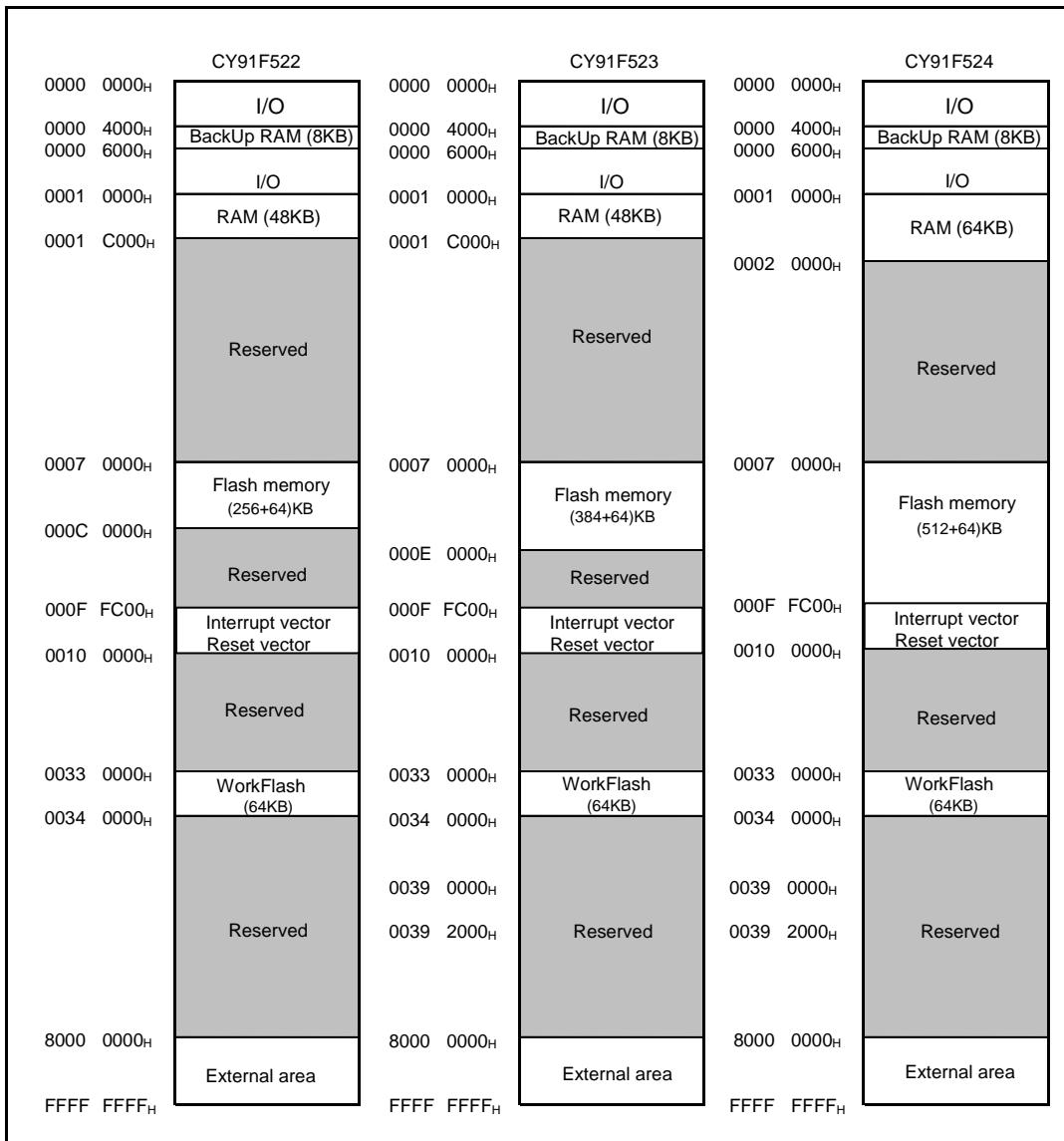
CY91F522J, CY91F523J, CY91F524J, CY91F525J, CY91F526J


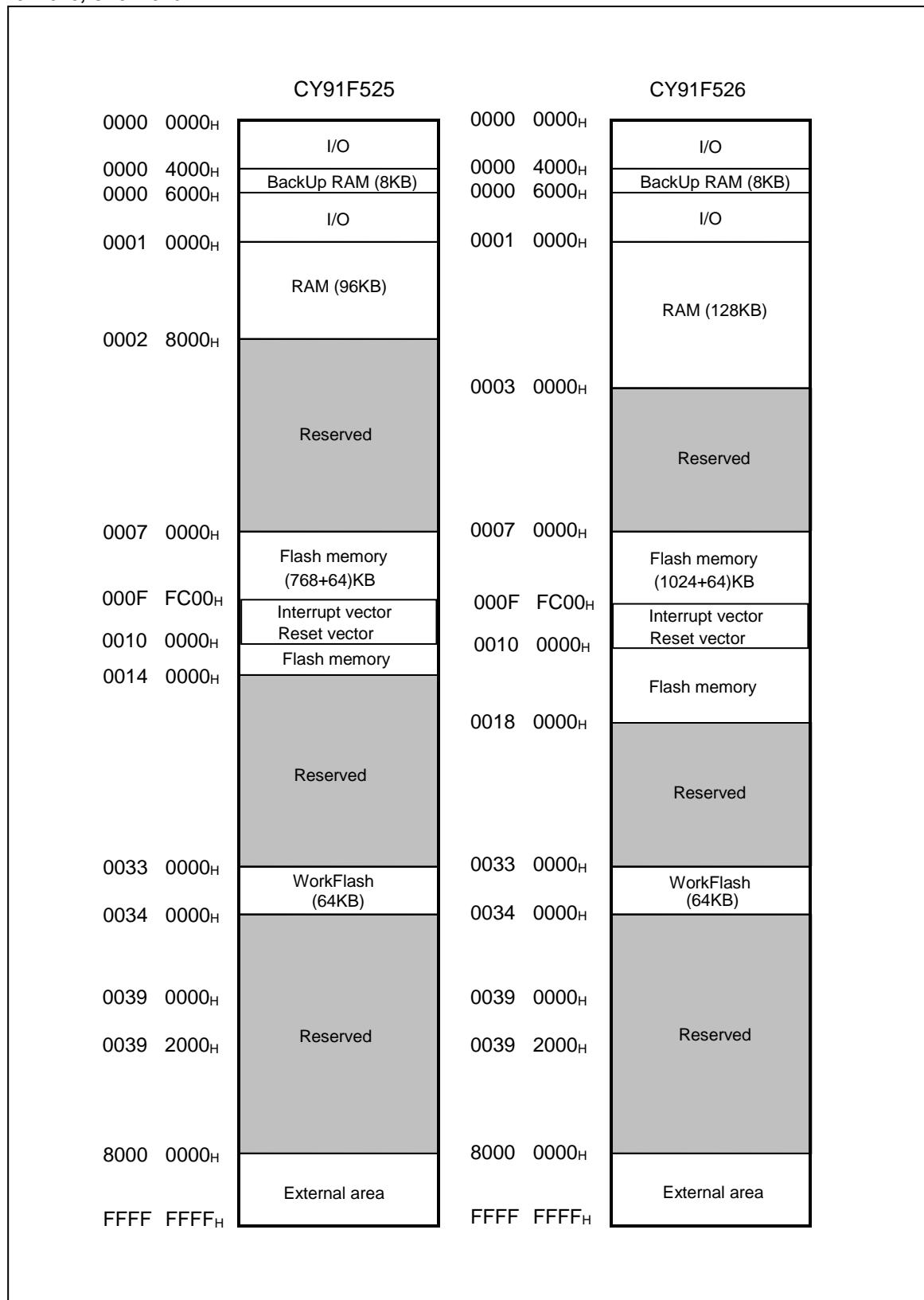
CY91F522K, CY91F523K, CY91F524K, CY91F525K, CY91F526K


CY91F522L, CY91F523L, CY91F524L, CY91F525L, CY91F526L


8. Memory Map

CY91F522, CY91F523, CY91F524



CY91F525, CY91F526


9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map

Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090 _H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 _H	-	BT1STC[R/W] B 00000000	-	-	
000098 _H	BT1PCSR/BT1PRLL[R/W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
00009C _H	BTSEL[R/W] B ---000 0	-	BTSSSR[W] B,H -----11		
0000A0 _H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 _H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W -----XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 _H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

Initial register value after reset

Read/Write attribute (R: Read W: Write)
 Data access attribute
 B: Byte
 H: Half-word
 W: Word
 (Note)The access by the data
 access attribute not described
 is disabled.

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000000H	PDR00 [R/W] B,H,W XXXXXXXXXX	PDR01 [R/W] B,H,W XXXXXXXXXX	PDR02 [R/W] B,H,W XXXXXXXXXX	PDR03 [R/W] B,H,W XXXXXXXXXX	Port Data Register
000004H	PDR04 [R/W] B,H,W XXXXXXXXXX	PDR05 [R/W] B,H,W XXXXXXXXXX	PDR06 [R/W] B,H,W XXXXXXXXXX	PDR07 [R/W] B,H,W XXXXXXXXXX	
000008H	PDR08 [R/W] B,H,W XXXXXXXXXX	PDR09 [R/W] B,H,W XXXXXXXXXX	PDR10 [R/W] B,H,W XXXXXXXXXX	PDR11 [R/W] B,H,W XXXXXXXXXX	
00000CH	PDR12 [R/W] B,H,W XXXXXXXXXX	PDR13 [R/W] B,H,W -XXXXXXXX	PDR14 [R/W] B,H,W ---XXX--	PDR15 [R/W] B,H,W --XXXXXX	
000010H	—	—	—	—	
000014H	—	—	—	—	
000018H	PDR16 [R/W] B,H,W XXXXXXXXXX	PDR17 [R/W] B,H,W XXXXXXXXXX	PDR18 [R/W] B,H,W XXXXXXXXXX	PDR19 [R/W] B,H,W XXXXXXXXXX	
00001CH to 000034H	—	—	—	—	Reserved
000038H	WDTECR0 [R/W] B,H,W ---00000	—	—	—	Watchdog Timer [S]
00003CH	WDTCR0 [R/W] B,H,W -0--0000	WDTCPRO [W] B,H,W 00000000	WDTCR1 [R] B,H,W ----0110	WDTCPRI [W] B,H,W 00000000	
000040H	—	—	—	—	Reserved
000044H	DICR [R/W] B,H,W -----0	—	—	—	Delayed Interrupt
000048H to 00005CH	—	—	—	—	Reserved
000060H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload Timer 0
000064H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B,H,W 00000000 0-000000		
000068H	TMRLRA7 [R/W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload Timer 7
00006CH	TMRLRB7 [R/W] H XXXXXXXX XXXXXXXX		TMCSR7 [R/W] B,H,W 00000000 0-000000		
000070H	—	FRS8 [R/W] B,H,W --00--00 --00--00 --00--00			Free-run timer selection register 8
000074H	—	FRS9 [R/W] B,H,W --00--00 --00--00 --00--00			Free-run timer selection register 9
000078H	—	—	—	OCLS67 [R/W] B,H,W ----0000	OCU67 Output level control register
00007CH	—	—	—	OCLS89 [R/W] B,H,W ----0000	OCU89 Output level control register
000080H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -000--00 -000-000		Base Timer 0

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
000084H	BT0TMCR2 [R/W] B -----0	BT0STC [R/W] B -0-0-0-0	—	—		
000088H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000			
00008CH	—	—	—	—	Reserved	
000090H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00-000-000		Base Timer 1	
000094H	BT1TMCR2 [R/W] B -----0	BT1STC [R/W] B -0-0-0-0	—	—		
000098H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000			
00009CH	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -----11		Base Timer 0,1	
0000A0H to 0000FCH	—	—	—	—	Reserved	
000100H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1	
000104H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000			
000108H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2	
00010CH	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000			
000110H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3	
000114H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000			
000118H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45	
00011CH	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000120H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU	
000124H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000					
000128H	—	—	OCSH67 [R/W] B,H,W ---0--0	OCSL67 [R/W] B,H,W 0000--00		
00012CH	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU	
000130H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000					
000134H	—	—	OCSH89 [R/W] B,H,W ---0--0	OCSL89 [R/W] B,H,W 0000--00		
000138H to 0001B4H	—	—	—	—	Reserved	

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
0001B8H	EPFR64 [R/W] B,H,W ----00-	EPFR65 [R/W] B,H,W 0000-000	EPFR66 [R/W] B,H,W --000000	EPFR67 [R/W] B,H,W ----0000	Extended port function register	
0001BCH	EPFR68 [R/W] B,H,W ----0000	EPFR69 [R/W] B,H,W ----0000	EPFR70 [R/W] B,H,W ---00000	EPFR71 [R/W] B,H,W -0-0-0-0		
0001C0H	EPFR72 [R/W] B,H,W 0000000-0	EPFR73 [R/W] B,H,W 00000000	EPFR74 [R/W] B,H,W 00000000	EPFR75 [R/W] B,H,W 00000000		
0001C4H	EPFR76 [R/W] B,H,W 00000000	EPFR77 [R/W] B,H,W --000000	EPFR78 [R/W] B,H,W ----00	EPFR79 [R/W] B,H,W 00000000		
0001C8H	EPFR80 [R/W] B,H,W ---00000	EPFR81 [R/W] B,H,W 00000000	EPFR82 [R/W] B,H,W 00000000	EPFR83 [R/W] B,H,W -0000000		
0001CCH	EPFR84 [R/W] B,H,W 00000000	EPFR85 [R/W] B,H,W --000000	EPFR86 [R/W] B,H,W ---00000	EPFR87 [R/W] B,H,W ----00		
0001D0H	EPFR88 [R/W] B,H,W -----0	—	—	—		
0001D4H	—	—	—	—	Reserved	
0001D8H	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXXX		Reload Timer 4	
0001DCH	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000			
0001E0H to 0001ECH	—	—	—	—	Reserved	
0001F0H	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXXX		Reload Timer 5	
0001F4H	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000			
0001F8H	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXXX		Reload Timer 6	
0001FCH	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000			
000200H to 000238H	—	—	—	—	Reserved	
00023CH	DACR0 [R/W] B,H,W -----0	DADRO [R/W] B,H,W XXXXXXXXX	DACR1 [R/W] B,H,W -----0	DADR1 [R/W] B,H,W XXXXXXXXX	DA Converter	
000240H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT	
000244H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000					
000248H	TCCSH3 [R/W] B,H,W 0----00	TCCSL3 [R/W] B,H,W -1-00000	—	—		
00024CH	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT	
000250H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000					
000254H	TCCSH4 [R/W] B,H,W 0----00	TCCSL4 [R/W] B,H,W -1-00000	—	—		

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
000258 _H to 0002C0 _H	—	—	—	—	Reserved	
0002C4 _H to 0002FC _H	—	—	—	—	Reserved	
000300 _H to 00030C _H	—	—	—	—	Reserved	
000310 _H	—	—	MPUCR [R/W] H 000000-0 ---0100		MPU [S] (Only CPU core can access this area)	
000314 _H	—	—	—	—		
000318 _H	—					
00031C _H	—	—	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000320 _H	DPVSR [R/W] H ----- 00000~0					
000324 _H	—	—	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000328 _H	DESR [R/W] H ----- 00000~0					
00032C _H	—	—	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000			
000330 _H	PACR0 [R/W] H 000000-0 00000--0					
000334 _H	—	—	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000			
000338 _H	—	—	PACR1 [R/W] H 000000-0 00000--0			
000340 _H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000					
000344 _H	—	—	PACR2 [R/W] H 000000-0 00000--0			
000348 _H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000					
00034C _H	—	—	PACR3 [R/W] H 000000-0 00000--0			
000350 _H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000					
000354 _H	—	—	PACR4 [R/W] H 000000-0 00000--0			
000358 _H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000					
00035C _H	—	—	PACR5 [R/W] H 000000-0 00000--0			
000360 _H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000					
000364 _H	—	—	PACR6 [R/W] H 000000-0 00000--0			

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000368H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only CPU core can access this area)
00036CH	—	—	PACR7 [R/W] H 000000-0 00000--0	—	—
000370H to 0003ACH	—				Reserved [S]
0003B0H to 0003FCH	—	—	—	—	Reserved [S]
000400H	ICSEL0 [R/W] B,H,W ----000	ICSEL1 [R/W] B,H,W ----000	ICSEL2 [R/W] B,H,W -----0	ICSEL3 [R/W] B,H,W -----0	DMA request generation and clear
000404H	—	ICSEL5 [R/W] B,H,W ----000	ICSEL6 [R/W] B,H,W ---0000	ICSEL7 [R/W] B,H,W ---0000	
000408H	ICSEL8 [R/W] B,H,W ----00	ICSEL9 [R/W] B,H,W -----00	ICSEL10 [R/W] B,H,W -----00	ICSEL11 [R/W] B,H,W -----000	
00040CH	—	ICSEL13 [R/W] B,H,W -----00	ICSEL14 [R/W] B,H,W -----00	ICSEL15 [R/W] B,H,W -----00	
000410H	ICSEL16 [R/W] B,H,W ----0000	ICSEL17 [R/W] B,H,W -----00	ICSEL18 [R/W] B,H,W ---00000	ICSEL19 [R/W] B,H,W -----000	
000414H	ICSEL20 [R/W] B,H,W ----000	ICSEL21 [R/W] B,H,W -----00	ICSEL22 [R/W] B,H,W -----00	ICSEL23 [R/W] B,H,W -----00	
000418H	IRPR0H [R] B,H,W 00-----	IRPR0L [R] B,H,W 00-----	IRPR1H [R] B,H,W 00-----	IRPR1L [R] B,H,W 00-----	Interrupt Request Batch Reading Register
00041CH	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 000----	
000424H	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00---	IRPR7L [R] B,H,W -----00	
000428H	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -00-----	IRPR9H [R] B,H,W -0-----	IRPR9L [R] B,H,W -0-----	
00042CH	IRPR10H [R] B,H,W -0-----	IRPR10L [R] B,H,W -0-----	IRPR11H [R] B,H,W 0-----	IRPR11L [R] B,H,W 0-----	
000430H	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ----00--	IRPR13H [R] B,H,W 00-----	IRPR13L [R] B,H,W 00-----	
000434H	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000-----	IRPR15L [R] B,H,W 0000000-	
000438H	ICSEL24 [R/W] B,H,W ----00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -----0	ICSEL27 [R/W] B,H,W -----0	DMA request generation and clear
00043CH	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440 _H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444 _H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448 _H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
00044C _H	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450 _H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454 _H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458 _H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
00045C _H	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460 _H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464 _H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468 _H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
00046C _H	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470 _H to 00047C _H	—	—	—	—	Reserved [S]
000480 _H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484 _H	—	—	—	—	Reserved [S]
000488 _H	DIVR0 [R/W] B,H,W 000----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
00048C _H	—	—	—	—	Reserved [S]
000490 _H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494 _H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498 _H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	
00049C _H	IORR12 [R/W] B,H,W -0000000	IORR13 [R/W] B,H,W -0000000	IORR14 [R/W] B,H,W -0000000	IORR15 [R/W] B,H,W -0000000	
0004A0 _H	—	—	—	—	Reserved
0004A4 _H	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
0004A8 _H	—	—	CSCFG[R/W]B,H,W ---0----	CMCFG[R/W]B,H,W 00000000	Clock monitor control register
0004AC _H	ADERH0[R/W] B,H 11111111 11111111	—	ADERL0[R/W] B,H 11111111 11111111	—	Analog input control register 0

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
0004B0 _H	—		ADERL1[R/W] B,H 11111111 11111111		Analog input control register 1	
0004B4 _H	—	—	—	—	Reserved	
0004B8 _H	CUCR0 [R/W] B,H,W -----0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration	
0004BC _H	CUTR0 [R] B,H,W -----00000000 00000000 00000000					
0004C0 _H	—	—	—	—		
0004C4 _H	CUCR1 [R/W] B,H,W -----0--00		CUTD1 [R/W] B,H,W 11000011 01010000			
0004C8 _H	CUTR1 [R] B,H,W -----00000000 00000000 00000000					
0004CC _H to 00050C _H	—	—	—	—	Reserved	
000510 _H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock Control [S]	
000514 _H	PLLCR [R/W] B,H,W -----11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00-----		
000518 _H	—	—	CPUAR [R/W] B,H,W 0----XXX	—		
00051C _H	—	—	—	—	Reset Control [S]	
000520 _H	CCPSSELR [R/W] B,H,W -----0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2 [S]	
000524 _H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000		
000528 _H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000-----			
00052C _H	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000		
000530 _H	CCRTSELR [R/W] B,H,W 0-----0	—	CCPMUCR0 [R/W] B,H,W 0----00	CCPMUCR1 [R/W] B,H,W 0-00000	Clock Control 2 [S]	
000534 _H to 00054C _H	—	—	—	—		
000550 _H	EIRR0 [R/W] B,H,W XXXXXXXXXX	ENIRO [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External Interrupt (INT0 to 7)	
000554 _H	EIRR1 [R/W] B,H,W XXXXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External Interrupt (INT8 to 15)	
000558 _H	—	—	—	—	Reserved	

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
00055C _H	—	—	WTDR [R/W] H 00000000 00000000		Real Time Clock (RTC)	
000560 _H	—	WTCRH [R/W] B -----00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H -----00-0		
000564 _H	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX		
000568 _H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—		
00056C _H	—	CSVCR [R/W] B 000111--	—	—		
000570 _H to 00057C _H	—	—	—	—	Reserved	
000580 _H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator Control / Low Voltage Detection	
000584 _H	LVD5R [R/W] B,H,W -----1	LVD5F [R/W] B,H,W 00000001	LVD [R/W] B,H,W 01000--0	—		
000588 _H to 00058C _H	—	—	—	—		
000590 _H	PMUSTR [R/W] B,H,W 0----1X	PMUCTLR [R/W] B,H,W 0-00---	PWRTMCTL [R/W] B,H,W ----011	—	PMU	
000594 _H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—		
000598 _H	—	—	—	—		
00059C _H to 0005BC _H	—	—	—	—	Reserved	
0005C0 _H to 0005FC _H	—	—	—	—	Reserved	
000600 _H	ASR0 [R/W] W 00000000 00000000 ----- 1111-001				External Bus Interface [S]	
000604 _H	ASR1 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0					
000608 _H	ASR2 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0					
00060C _H	ASR3 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0					
000610 _H to 00063C _H	—	—	—	—	Reserved [S]	

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
000640 _H	ACR0 [R/W] W -----01--00--				External Bus Interface [S]	
000644 _H	ACR1 [R/W] W -----XX--XX--					
000648 _H	ACR2 [R/W] W -----XX--XX--					
00064C _H	ACR3 [R/W] W -----XX--XX--					
000650 _H to 00067C _H	—	—	—	—	Reserved [S]	
000680 _H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]	
000684 _H	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-					
000688 _H	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				External Bus Interface [S]	
00068C _H	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-					
000690 _H to 0006FC _H	—	—	—	—	Reserved [S]	
000700 _H to 00070C _H	—	—	—	—	Reserved	
000710 _H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter	
000714 _H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000					
000718 _H	BPCTRBR [R/W] W 00000000 00000000 00000000 00000000					
00071C _H	BPCTRC [R/W] W 00000000 00000000 00000000 00000000					
000720 _H to 0007F8 _H	—	—	—	—	Reserved	
0007FC _H	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register	
000800 _H to 00083C _H	—	—	—	—	Reserved [S]	
000840 _H	FCTLR [R/W] H -0--1000 0-0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]	
000844 _H to 000854 _H	—	—	—	—	Reserved [S]	
000858 _H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]	
00085C _H to 00087C _H	—	—	—	—	Reserved [S]	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000880 _H	WRAR00 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000884 _H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888 _H	WRAR01 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
00088C _H	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890 _H	WRAR02 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
000894 _H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898 _H	WRAR03 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
00089C _H	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A0 _H	WRAR04 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008A4 _H	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A8 _H	WRAR05 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008AC _H	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0 _H	WRAR06 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
0008B4 _H	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8 _H	WRAR07 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008BC _H	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0 _H	WRAR08 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008C4 _H	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8 _H	WRAR09 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008CC _H	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0 _H	WRAR10 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008D4 _H	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8 _H	WRAR11 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008DC _H	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0 _H	WRAR12 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0008E4 _H	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild Register [S]
0008E8 _H	WRAR13 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008EC _H	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0 _H	WRAR14 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008F4 _H	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild Register [S]
0008F8 _H	WRAR15 [R/W] W ----- XXXXXX XXXXXXXX XXXXXX--				
0008FC _H	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900 _H	TPUUNLOCK [R/W] W 00000000 00000000 00000000 00000000				
000904 _H	TPULST [R] B,H,W -----0	—	TPUVST [R/W] B,H,W -----000	—	Time Protection Unit [S]
000908 _H	TPUCFG [R/W] B,H,W -----0 0-000000 -----0				
00090C _H	TPUTIR [R] B,H,W 00000000	—	—	—	
000910 _H	TPUTST [R] B,H,W 00000000	—	—	—	
000914 _H	TPUTIE [R/W] B,H,W 00000000	—	—	—	
000918 _H	TPUTMID [R] B,H,W 00000000 00000000 00000000 00000000				
00091C _H to 00092C _H	—	—	—	—	
000930 _H	TPUTCN00 [R/W] B,H,W 000000- 00000000 00000000 00000000				
000934 _H	TPUTCN01 [R/W] B,H,W 000000- 00000000 00000000 00000000				
000938 _H	TPUTCN02 [R/W] B,H,W 000000- 00000000 00000000 00000000				
00093C _H	TPUTCN03 [R/W] B,H,W 000000- 00000000 00000000 00000000				
000940 _H	TPUTCN04 [R/W] B,H,W 000000- 00000000 00000000 00000000				
000944 _H	TPUTCN05 [R/W] B,H,W 000000- 00000000 00000000 00000000				
000948 _H	TPUTCN06 [R/W] B,H,W 000000- 00000000 00000000 00000000				
00094C _H	TPUTCN07 [R/W] B,H,W 000000- 00000000 00000000 00000000				
000950 _H	TPUTCN10 [R/W] B,H,W ---00000	—	—	—	

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
000954H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—		
000958H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—		
00095CH	TPUTCN13 [R/W] B,H,W ---00000	—	—	—		
000960H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—		
000964H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—		
000968H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—		
00096CH	TPUTCN17 [R/W] B,H,W ---00000	—	—	—		
000970H	TPUTCC0 [R] B,H,W ----- 00000000 00000000 00000000				Time Protection Unit [S]	
000974H	TPUTCC1 [R] B,H,W ----- 00000000 00000000 00000000					
000978H	TPUTCC2 [R] B,H,W ----- 00000000 00000000 00000000					
00097CH	TPUTCC3 [R] B,H,W ----- 00000000 00000000 00000000					
000980H	TPUTCC4 [R] B,H,W ----- 00000000 00000000 00000000					
000984H	TPUTCC5 [R] B,H,W ----- 00000000 00000000 00000000					
000988H	TPUTCC6 [R] B,H,W ----- 00000000 00000000 00000000					
00098CH	TPUTCC7 [R] B,H,W ----- 00000000 00000000 00000000					
000990H to 0009FCH	—	—	—	—		
000A00H to 000BECH	—	—	—	—	Reserved	
000BF0H	HSCFR [R/W] B,H,W ----- 00 0000000 0000000				OCDU	
000BF4H	—	—	—	—		
000BF8H	—	—	MBR [R/W] B,H,W 00----- XXXXXXXX			
000BFCH	—	—	UER [W] B,H,W ----- X		OCDU	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000C00 _H	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				
000C04 _H	DCSR0 [R/W] H 0-----000	DTCR0 [R/W] H 00000000 00000000			
000C08 _H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0C _H	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10 _H	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
000C14 _H	DCSR1 [R/W] H 0-----000	DTCR1 [R/W] H 00000000 00000000			
000C18 _H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1C _H	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20 _H	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
000C24 _H	DCSR2 [R/W] H 0-----000	DTCR2 [R/W] H 00000000 00000000			
000C28 _H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2C _H	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30 _H	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
000C34 _H	DCSR3 [R/W] H 0-----000	DTCR3 [R/W] H 00000000 00000000			
000C38 _H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3C _H	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40 _H	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
000C44 _H	DCSR4 [R/W] H 0-----000	DTCR4 [R/W] H 00000000 00000000			
000C48 _H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C4C _H	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C50 _H	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
000C54 _H	DCSR5 [R/W] H 0-----000	DTCR5 [R/W] H 00000000 00000000			
000C58 _H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C5C _H	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C60 _H	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				

DMA
Controller
[S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000C64H	DCSR6 [R/W] H 0-----000		DTCR6 [R/W] H 00000000 00000000		
000C68H		DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C6CH		DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C70H		DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000			
000C74H	DCSR7 [R/W] H 0-----000		DTCR7 [R/W] H 00000000 00000000		
000C78H		DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C7CH		DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C80H		DCCR8 [R/W] W 0----000 --00--00 00000000 0-000000			
000C84H	DCSR8 [R/W] H 0-----000		DTCR8 [R/W] H 00000000 00000000		
000C88H		DSAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C8CH		DDAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C90H		DCCR9 [R/W] W 0----000 --00--00 00000000 0-000000			
000C94H	DCSR9 [R/W] H 0-----000		DTCR9 [R/W] H 00000000 00000000		
000C98H		DSAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000C9CH		DDAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000CA0H		DCCR10 [R/W] W 0----000 --00--00 00000000 0-000000			
000CA4H	DCSR10 [R/W] H 0-----000		DTCR10 [R/W] H 00000000 00000000		
000CA8H		DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000CACH		DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000CB0H		DCCR11 [R/W] W 0----000 --00--00 00000000 0-000000			
000CB4H	DCSR11 [R/W] H 0-----000		DTCR11 [R/W] H 00000000 00000000		
000CB8H		DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000CBCH		DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
000CC0H		DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000			
000CC4H	DCSR12 [R/W] H 0-----000		DTCR12 [R/W] H 00000000 00000000		

DMA
Controller
[S]

Address	Address offset value / Register name				Block					
	+0	+1	+2	+3						
000CC8H	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA Controller [S]					
000CCC _H	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000CD0H	DCCR13 [R/W] W 0---000 --00--00 00000000 0-000000									
000CD4H	DCSR13 [R/W] H 0-----000	DTCR13 [R/W] H 00000000 00000000								
000CD8H	DSAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000CDC _H	DDAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000CE0H	DCCR14 [R/W] W 0---000 --00--00 00000000 0-000000									
000CE4H	DCSR14 [R/W] H 0-----000	DTCR14 [R/W] H 00000000 00000000								
000CE8H	DSAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000CECH	DDAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000CF0H	DCCR15 [R/W] W 0---000 --00--00 00000000 0-000000									
000CF4H	DCSR15 [R/W] H 0-----000	DTCR15 [R/W] H 00000000 00000000								
000CF8H	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000CFC _H	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
000D00H to 000DF0H	—	—	—	—	Reserved [S]					
000DF4H	—	—	DNMIR [R/W] B 0-----0	DILVR [R/W] B ---1111	DMA Controller [S]					
000DF8H	DMACR[R/W] W 0-----0-----									
000DFCH	—	—	—	—	Reserved [S]					
000E00H	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register					
000E04H	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000						
000E08H	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register					
000E0CH	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -00000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000						
000E10H	—	—	—	—						
000E14H	—	—	—	—						
000E18H	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	Reserved					
000E1CH	—	—	—	—	Reserved					

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E20 _H	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
000E24 _H	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
000E28 _H	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
000E2C _H	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -00000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
000E30 _H	—	—	—	—	
000E34 _H	—	—	—	—	
000E38 _H	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	
000E3C _H	—	—	—	—	Reserved
000E40 _H	PDDR00 [R] B,H,W XXXXXXXXXX	PDDR01 [R] B,H,W XXXXXXXXXX	PDDR02 [R] B,H,W XXXXXXXXXX	PDDR03 [R] B,H,W XXXXXXXXXX	Port Direct Read Register
000E44 _H	PDDR04 [R] B,H,W XXXXXXXXXX	PDDR05 [R] B,H,W XXXXXXXXXX	PDDR06 [R] B,H,W XXXXXXXXXX	PDDR07 [R] B,H,W XXXXXXXXXX	
000E48 _H	PDDR08 [R] B,H,W XXXXXXXXXX	PDDR09 [R] B,H,W XXXXXXXXXX	PDDR10 [R] B,H,W XXXXXXXXXX	PDDR11 [R] B,H,W XXXXXXXXXX	
000E4C _H	PDDR12 [R] B,H,W XXXXXXXXXX	PDDR13 [R] B,H,W -XXXXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
000E50 _H	—	—	—	—	
000E54 _H	—	—	—	—	
000E58 _H	PDDR16 [R] B,H,W XXXXXXXXXX	PDDR17 [R] B,H,W XXXXXXXXXX	PDDR18 [R] B,H,W XXXXXXXXXX	PDDR19 [R] B,H,W XXXXXXXXXX	
000E5C _H	—	—	—	—	Reserved
000E60 _H	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ---0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
000E64 _H	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---0000	
000E68 _H	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W -----0000	EPFR11 [R/W] B,H,W -----0000	
000E6C _H	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W -----00	EPFR14 [R/W] B,H,W -----00	EPFR15 [R/W] B,H,W -----000	
000E70 _H	—	—	—	—	
000E74 _H	—	—	—	—	
000E78 _H	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0---	
000E7C _H	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80 _H	—	EPFR33 [R/W] B,H,W ----00-	EPFR34 [R/W] B,H,W ----00-	EPFR35 [R/W] B,H,W ---00000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E84 _H	EPFR36 [R/W] B,H,W ----000-	—	—	—	Extended Port Function Register
000E88 _H	—	—	EPFR42 [R/W] B,H,W -----00	EPFR43 [R/W] B,H,W 0--0000-	
000E8C _H	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
000E90 _H	—	—	—	—	
000E94 _H	—	—	—	—	
000E98 _H	EPFR56 [R/W] B,H,W ----0-0	EPFR57 [R/W] B,H,W ----00-0	EPFR58 [R/W] B,H,W ----00-0	EPFR59 [R/W] B,H,W ----00-0	
000E9C _H	EPFR60 [R/W] B,H,W ----00-0	EPFR61 [R/W] B,H,W ----00-	EPFR62 [R/W] B,H,W ----00-	EPFR63 [R/W] B,H,W ---0000-	
000EA0 _H to 000EBC _H	—	—	—	—	
000EC0 _H	PPER00 [R/W] B,H,W 00000000	PPER01 [R/W] B,H,W 00000000	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000EC4 _H	PPER04 [R/W] B,H,W 00000000	PPER05 [R/W] B,H,W 00000000	PPER06 [R/W] B,H,W 00000000	PPER07 [R/W] B,H,W 00000000	
000EC8 _H	PPER08 [R/W] B,H,W 00000000	PPER09 [R/W] B,H,W 00000000	PPER10 [R/W] B,H,W 00000000	PPER11 [R/W] B,H,W 00000000	
000ECC _H	PPER12 [R/W] B,H,W 00000000	PPER13 [R/W] B,H,W -0000000	PPER14 [R/W] B,H,W ---000--	PPER15 [R/W] B,H,W --000000	
000ED0 _H	—	—	—	—	
000ED4 _H	—	—	—	—	
000ED8 _H	PPER16 [R/W] B,H,W 00000000	PPER17 [R/W] B,H,W 00000000	PPER18 [R/W] B,H,W 00000000	PPER19 [R/W] B,H,W 00000000	Port Enable Register
000EDC _H to 000F3C _H	—	—	—	—	
000F40 _H	PORTEN [R/W] B,H,W -----0	—	—	—	
000F44 _H	KEYCDR [R/W] H 00000000 00000000		—	—	
000F48 _H to 000F64 _H	—	—	—	—	

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
000F68H	MSCY6 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 Cycle measurement data register 67	
000F6CH	MSCY7 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000F70H	RCRH0 [W] H,W XXXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/Down Counter 0	
000F74H	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000		
000F78H to 000F7CH	—	—	—	—	Reserved	
000F80H	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/Down Counter 1	
000F84H	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000		
000F88H	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W -----00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45	
000F8CH	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W -----00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67	
000F90H	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU	
000F94H	OCCP11 [R/W] W 00000000 00000000 00000000 00000000					
000F98H	—	—	OCSH1011 [R/W] B,H,W ---0--0	OCSL1011 [R/W] B,H,W 0000--00	Output Compare 10,11 32-bit OCU	
000F9CH	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU1011 Output level control register	
000FA0H	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT	
000FA4H	TCDT5 [R/W] W 00000000 00000000 00000000 00000000					
000FA8H	TCCSH5 [R/W]B,H,W 0----00	TCCSL5 [R/W]B,H,W -1-00000	—	—		
000FACH to 000FCCH	—	—	—	—	Reserved	
000FD0H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 32-bit ICU	
000FD4H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000FD8H	—	—	LSYN1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000		

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
000FDC _H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 32-bit ICU	
000FE0 _H	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000FE4 _H	—	—	—	ICS67 [R/W] B,H,W 00000000		
000FE8 _H	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU	
000FEC _H	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000FF0 _H	—	—	—	ICS89 [R/W] B,H,W 00000000		
000FF4 _H	MSCY8 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU Cycle measurement data register 89	
000FF8 _H	MSCY9 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000FFC _H	—	—	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W -----00		
001000 _H	SACR [R/W] B,H,W -----0	PICD [R/W] B,H,W ----0011	—	—	Clock Control	
001004 _H to 00112C _H	—	—	—	—	Reserved	
001130 _H	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit	
001134 _H	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111					
001138 _H	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000					
00113C _H	CRCR [R] B,H,W 11111111 11111111 11111111 11111111					
001140 _H to 0011FC _H	—	—	—	—	Reserved	
001200 _H	TCGS [R/W] B,H,W -----00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation	
001204 _H	CPCLR0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 0	
001208 _H	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 -----					
00120C _H	CPCLR1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000			
001210 _H	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 -----				16-bit Free-run Timer 1	
001214 _H	CPCLR2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 2	
001218 _H	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 -----					

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
00121CH to 001230H	—	—	—	—	Reserved	
001234H	FRS0 [R/W] B,H,W -----00--00 --00--00 --00--00				16-bit Free-run timer selection	
001238H	FRS1 [R/W] B,H,W --00--00 --00--00					
00123CH	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00					
001240H	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00					
001244H	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00					
001248H	—	—	—	—	Reserved	
00124CH	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000	OCCPB1/OCCP1 [R/W] H,W 00000000 00000000			16-bit Output compare 0/1	
001250H	OCS01 [R/W] B,H,W -110--00 00001100	—	OCMOD01 [R/W] B,H,W -----00	—		
001254H	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000	OCCPB3/OCCP3 [R/W] H,W 00000000 00000000				
001258H	OCS23 [R/W] B,H,W -110--00 00001100	—	OCMOD23 [R/W] B,H,W -----00	—	16-bit Output compare 2/3	
00125CH	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000	OCCPB5/OCCP5 [R/W] H,W 00000000 00000000			16-bit Output compare 4/5	
001260H	OCS45 [R/W] B,H,W -110--00 00001100	—	OCMOD45 [R/W] B,H,W -----00	—		
001264H to 001278H	—	—	—	—	Reserved	
00127CH	IPCP0 [R] H,W 00000000 00000000	IPCP1 [R] H,W 00000000 00000000			16-bit Input capture 0/1	
001280H	ICS01 [R/W] B,H,W -----00 00000000	—	LSYNS [R/W] B,H,W -----0000	—		
001284H	IPCP2 [R] H,W 00000000 00000000	IPCP3 [R] H,W 00000000 00000000				
001288H	ICS23 [R/W] B,H,W -----00 00000000	—	—	—	16-bit Input capture 2/3	
00128CH to 001298H	—	—	—	—	Reserved	
00129CH	—	—	—	—	Reserved	

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
0012A0 _H	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2	
0012A4 _H	TMRR2 [R/W] H,W 00000000 00000001		—	—		
0012A8 _H	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—		
0012AC _H	—	DTIRO [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000		
0012B0 _H	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1		
0012B4 _H	PICS0 [R/W] B,H,W 000000-- -----					
0012B8 _H to 0012CC _H	—	—	—	—	Reserved	
0012D0 _H	FRS5 [R/W] B,H,W --00-00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare	
0012D4 _H	FRS6 [R/W] B,H,W --00-00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare	
0012D8 _H	FRS7 [R/W] B,H,W --00-00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare	
0012DC _H to 0012FC _H	—	—	—	—	Reserved	
001300 _H	—				Reserved	
001304 _H	ADTSS0[R/W] B,H,W -----0	—	—	—	12-bit A/D converter 1/2 unit	
001308 _H	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000					
00130C _H	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000			
001310 _H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000			
001314 _H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000			
001318 _H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000			
00131C _H	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000			
001320 _H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000			
001324 _H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000			
001328 _H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000			

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00132C _H	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000	ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000			12-bit A/D converter 1/2 unit
001330 _H	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000	ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000			
001334 _H	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000	ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000			
001338 _H	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000	ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000			
00133C _H	ADCOMP24/ADCOMPB24[R/W] H,W 00000000 00000000	ADCOMP25/ADCOMPB25[R/W] H,W 00000000 00000000			
001340 _H	ADCOMP26/ADCOMPB26[R/W] H,W 00000000 00000000	ADCOMP27/ADCOMPB27[R/W] H,W 00000000 00000000			
001344 _H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000	ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000			
001348 _H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000	ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000			
00134C _H	ADTCS0[R/W] B,H,W 00000000 0010----	ADTCS1[R/W] B,H,W 00000000 0010----			
001350 _H	ADTCS2[R/W] B,H,W 00000000 0010----	ADTCS3[R/W] B,H,W 00000000 0010----			
001354 _H	ADTCS4[R/W] B,H,W 00000000 0010----	ADTCS5[R/W] B,H,W 00000000 0010----			
001358 _H	ADTCS6[R/W] B,H,W 00000000 0010----	ADTCS7[R/W] B,H,W 00000000 0010----			
00135C _H	ADTCS8[R/W] B,H,W 00000000 0010----	ADTCS9[R/W] B,H,W 00000000 0010----			
001360 _H	ADTCS10[R/W] B,H,W 00000000 0010----	ADTCS11[R/W] B,H,W 00000000 0010----			
001364 _H	ADTCS12[R/W] B,H,W 00000000 0010----	ADTCS13[R/W] B,H,W 00000000 0010----			
001368 _H	ADTCS14[R/W] B,H,W 00000000 0010----	ADTCS15[R/W] B,H,W 00000000 0010----			
00136C _H	ADTCS16[R/W] B,H,W 00000000 0010----	ADTCS17[R/W] B,H,W 00000000 0010----			
001370 _H	ADTCS18[R/W] B,H,W 00000000 0010----	ADTCS19[R/W] B,H,W 00000000 0010----			
001374 _H	ADTCS20[R/W] B,H,W 00000000 0010----	ADTCS21[R/W] B,H,W 00000000 0010----			
001378 _H	ADTCS22[R/W] B,H,W 00000000 0010----	ADTCS23[R/W] B,H,W 00000000 0010----			
00137C _H	ADTCS24[R/W] B,H,W 00000000 0010----	ADTCS25[R/W] B,H,W 00000000 0010----			
001380 _H	ADTCS26[R/W] B,H,W 00000000 0010----	ADTCS27[R/W] B,H,W 00000000 0010----			
001384 _H	ADTCS28[R/W] B,H,W 00000000 0010----	ADTCS29[R/W] B,H,W 00000000 0010----			
001388 _H	ADTCS30[R/W] B,H,W 00000000 0010----	ADTCS31[R/W] B,H,W 00000000 0010----			
00138C _H	ADTCD0[R] B,H,W 10--0000 00000000	ADTCD1[R] B,H,W 10--0000 00000000			

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001390 _H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		12-bit A/D converter 1/2 unit
001394 _H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001398 _H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
00139C _H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
0013A0 _H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
0013A4 _H	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
0013A8 _H	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
0013AC _H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
0013B0 _H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
0013B4 _H	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
0013B8 _H	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
0013BC _H	ADTCD24[R] B,H,W 10--0000 00000000		ADTCD25[R] B,H,W 10--0000 00000000		
0013C0 _H	ADTCD26[R] B,H,W 10--0000 00000000		ADTCD27[R] B,H,W 10--0000 00000000		
0013C4 _H	ADTCD28[R] B,H,W 10--0000 00000000		ADTCD29[R] B,H,W 10--0000 00000000		
0013C8 _H	ADTCD30[R] B,H,W 10--0000 00000000		ADTCD31[R] B,H,W 10--0000 00000000		
0013CC _H	ADTECS0[R/W] B,H,W -----0 ---00000		ADTECS1[R/W] B,H,W -----0 ---00000		
0013D0 _H	ADTECS2[R/W] B,H,W -----0 ---00000		ADTECS3[R/W] B,H,W -----0 ---00000		
0013D4 _H	ADTECS4[R/W] B,H,W -----0 ---00000		ADTECS5[R/W] B,H,W -----0 ---00000		
0013D8 _H	ADTECS6[R/W] B,H,W -----0 ---00000		ADTECS7[R/W] B,H,W -----0 ---00000		
0013DC _H	ADTECS8[R/W] B,H,W -----0 ---00000		ADTECS9[R/W] B,H,W -----0 ---00000		
0013E0 _H	ADTECS10[R/W] B,H,W -----0 ---00000		ADTECS11[R/W] B,H,W -----0 ---00000		
0013E4 _H	ADTECS12[R/W] B,H,W -----0 ---00000		ADTECS13[R/W] B,H,W -----0 ---00000		
0013E8 _H	ADTECS14[R/W] B,H,W -----0 ---00000		ADTECS15[R/W] B,H,W -----0 ---00000		
0013EC _H	ADTECS16[R/W] B,H,W -----0 ---00000		ADTECS17[R/W] B,H,W -----0 ---00000		
0013F0 _H	ADTECS18[R/W] B,H,W -----0 ---00000		ADTECS19[R/W] B,H,W -----0 ---00000		

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
0013F4 _H	ADTECS20[R/W] B,H,W -----0 ---00000		ADTECS21[R/W] B,H,W -----0 ---00000			
0013F8 _H	ADTECS22[R/W] B,H,W -----0 ---00000		ADTECS23[R/W] B,H,W -----0 ---00000			
0013FC _H	ADTECS24[R/W] B,H,W -----0 ---00000		ADTECS25[R/W] B,H,W -----0 ---00000			
001400 _H	ADTECS26[R/W] B,H,W -----0 ---00000		ADTECS27[R/W] B,H,W -----0 ---00000			
001404 _H	ADTECS28[R/W] B,H,W -----0 ---00000		ADTECS29[R/W] B,H,W -----0 ---00000			
001408 _H	ADTECS30[R/W] B,H,W -----0 ---00000		ADTECS31[R/W] B,H,W -----0 ---00000			
00140C _H	ADRCUT0[R/W] B,H,W ----0000 00000000		ADRCLT0[R/W] B,H,W ----0000 00000000			
001410 _H	ADRCUT1[R/W] B,H,W ----0000 00000000		ADRCLT1[R/W] B,H,W ----0000 00000000			
001414 _H	ADRCUT2[R/W] B,H,W ----0000 00000000		ADRCLT2[R/W] B,H,W ----0000 00000000			
001418 _H	ADRCUT3[R/W] B,H,W ----0000 00000000		ADRCLT3[R/W] B,H,W ----0000 00000000			
00141C _H	ADRCCS0[R/W] B,H,W 00000000	ADRCCS1[R/W] B,H,W 00000000	ADRCCS2[R/W] B,H,W 00000000	ADRCCS3[R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit	
001420 _H	ADRCCS4[R/W] B,H,W 00000000	ADRCCS5[R/W] B,H,W 00000000	ADRCCS6[R/W] B,H,W 00000000	ADRCCS7[R/W] B,H,W 00000000		
001424 _H	ADRCCS8[R/W] B,H,W 00000000	ADRCCS9[R/W] B,H,W 00000000	ADRCCS10[R/W] B,H,W 00000000	ADRCCS11[R/W] B,H,W 00000000		
001428 _H	ADRCCS12[R/W] B,H,W 00000000	ADRCCS13[R/W] B,H,W 00000000	ADRCCS14[R/W] B,H,W 00000000	ADRCCS15[R/W] B,H,W 00000000		
00142C _H	ADRCCS16[R/W] B,H,W 00000000	ADRCCS17[R/W] B,H,W 00000000	ADRCCS18[R/W] B,H,W 00000000	ADRCCS19[R/W] B,H,W 00000000		
001430 _H	ADRCCS20[R/W] B,H,W 00000000	ADRCCS21[R/W] B,H,W 00000000	ADRCCS22[R/W] B,H,W 00000000	ADRCCS23[R/W] B,H,W 00000000		
001434 _H	ADRCCS24[R/W] B,H,W 00000000	ADRCCS25[R/W] B,H,W 00000000	ADRCCS26[R/W] B,H,W 00000000	ADRCCS27[R/W] B,H,W 00000000		
001438 _H	ADRCCS28[R/W] B,H,W 00000000	ADRCCS29[R/W] B,H,W 00000000	ADRCCS30[R/W] B,H,W 00000000	ADRCCS31[R/W] B,H,W 00000000		
00143C _H	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000					
001440 _H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000					
001444 _H	ADSCANS0[R/W] B,H,W 000----	—	—	—		

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
001448 _H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	12-bit A/D converter 1/2 unit	
00144C _H	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00		
001450 _H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00		
001454 _H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00		
001458 _H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000					
00145C _H	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111					
001460 _H	ADCS0[R] B,H,W 0-----		ADCH0[R] B,H,W ----00000	ADMD0[R/W] B,H,W 0---0000		
001464 _H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000		
001468 _H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000		
00146C _H	—					
001470 _H	ADTSS1[R/W] B,H,W -----0	—	—	—	12-bit A/D converter 2/2 unit	
001474 _H	ADTSE1[R/W] B,H,W -----00000000 00000000					
001478 _H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000			
00147C _H	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000			
001480 _H	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit	
001484 _H	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000			
001488 _H	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000			
00148C _H	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000			
001490 _H	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000			
001494 _H	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000			
001498 _H to 0014B4 _H	—	—	—	—	Reserved	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0014B8 _H	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		12-bit A/D converter 2/2 unit
0014BC _H	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
0014C0 _H	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
0014C4 _H	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
0014C8 _H	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
0014CC _H	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
0014D0 _H	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
0014D4 _H	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		
0014D8 _H to 0014F4 _H	—	—	—	—	Reserved
0014F8 _H	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
0014FC _H	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		
001500 _H	ADTCD36[R] B,H,W 10--0000 00000000		ADTCD37[R] B,H,W 10--0000 00000000		
001504 _H	ADTCD38[R] B,H,W 10--0000 00000000		ADTCD39[R] B,H,W 10--0000 00000000		
001508 _H	ADTCD40[R] B,H,W 10--0000 00000000		ADTCD41[R] B,H,W 10--0000 00000000		
00150C _H	ADTCD42[R] B,H,W 10--0000 00000000		ADTCD43[R] B,H,W 10--0000 00000000		
001510 _H	ADTCD44[R] B,H,W 10--0000 00000000		ADTCD45[R] B,H,W 10--0000 00000000		
001514 _H	ADTCD46[R] B,H,W 10--0000 00000000		ADTCD47[R] B,H,W 10--0000 00000000		
001518 _H to 001534 _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
001538 _H	ADTECS32[R/W] B,H,W -----0 ---0000		ADTECS33[R/W] B,H,W -----0 ---0000		12-bit A/D converter 2/2 unit	
00153C _H	ADTECS34[R/W] B,H,W -----0 ---0000		ADTECS35[R/W] B,H,W -----0 ---0000			
001540 _H	ADTECS36[R/W] B,H,W -----0 ---0000		ADTECS37[R/W] B,H,W -----0 ---0000			
001544 _H	ADTECS38[R/W] B,H,W -----0 ---0000		ADTECS39[R/W] B,H,W -----0 ---0000			
001548 _H	ADTECS40[R/W] B,H,W -----0 ---0000		ADTECS41[R/W] B,H,W -----0 ---0000			
00154C _H	ADTECS42[R/W] B,H,W -----0 ---0000		ADTECS43[R/W] B,H,W -----0 ---0000			
001550 _H	ADTECS44[R/W] B,H,W -----0 ---0000		ADTECS45[R/W] B,H,W -----0 ---0000			
001554 _H	ADTECS46[R/W] B,H,W -----0 ---0000		ADTECS47[R/W] B,H,W -----0 ---0000			
001558 _H to 001574 _H	—	—	—	—	Reserved	
001578 _H	ADRCUT4[R/W] B,H,W ----0000 00000000		ADRCLT4[R/W] B,H,W ----0000 00000000		12-bit A/D converter 2/2 unit	
00157C _H	ADRCUT5[R/W] B,H,W ----0000 00000000		ADRCLT5[R/W] B,H,W ----0000 00000000			
001580 _H	ADRCUT6[R/W] B,H,W ----0000 00000000		ADRCLT6[R/W] B,H,W ----0000 00000000			
001584 _H	ADRCUT7[R/W] B,H,W ----0000 00000000		ADRCLT7[R/W] B,H,W ----0000 00000000			
001588 _H	ADRCCS32[R/W] B,H,W 00000000	ADRCCS33[R/W] B,H,W 00000000	ADRCCS34[R/W] B,H,W 00000000	ADRCCS35[R/W] B,H,W 00000000	12-bit A/D converter 2/2 unit	
00158C _H	ADRCCS36[R/W] B,H,W 00000000	ADRCCS37[R/W] B,H,W 00000000	ADRCCS38[R/W] B,H,W 00000000	ADRCCS39[R/W] B,H,W 00000000		
001590 _H	ADRCCS40[R/W] B,H,W 00000000	ADRCCS41[R/W] B,H,W 00000000	ADRCCS42[R/W] B,H,W 00000000	ADRCCS43[R/W] B,H,W 00000000		
001594 _H	ADRCCS44[R/W] B,H,W 00000000	ADRCCS45[R/W] B,H,W 00000000	ADRCCS46[R/W] B,H,W 00000000	ADRCCS47[R/W] B,H,W 00000000		
001598 _H to 0015A4 _H	—	—	—	—	Reserved	
0015A8 _H	ADRCOT1 [R] B,H,W -----00000000 00000000				12-bit A/D converter 2/2 unit	
0015AC _H	ADRCIF1 [R,W] B,H,W -----00000000 00000000					
0015B0 _H	ADSCANS1 [R/W] B,H,W 000----	—	—	—		

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
0015B4H	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	12-bit A/D converter 2/2 unit	
0015B8H	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00		
0015BCH	—	—	—	—		
0015C0H	—	—	—	—		
0015C4H	ADPRTF1 [R] B,H,W ----- 00000000 00000000					
0015C8H	ADEOCF1 [R] B,H,W ----- 11111111 11111111					
0015CCH	ADCS1 [R] B,H,W 0-----		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000		
0015D0H	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000		
0015D4H to 00174CH	—	—	—	—	Reserved	
001750H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W]] B,H,W 00000000	Multi-UART0 	
001754H	— /(RDR10/(TDR10))[R/W] B,H,W ----- *3	RDR00/(TDR00)[R/W] B,H,W -----0 00000000 *1				
001758H	SACSR0[R/W] B,H,W 0----000 00000000	STMRO[R] B,H,W 00000000 00000000				
00175CH	STMCRO[R/W] B,H,W 00000000 00000000	— /(SCSRO/SFUR0)[R/W] B,H,W ----- *3 *4				
001760H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W ----- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W ----- *3	— /(SCSTR10) (SFLR10) [R/W] B,H,W ----- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W ----- *3		
001764H	—	— /(SCSFR20) [R/W] B,H,W ----- *3	— /(SCSFR10) [R/W] B,H,W ----- *3	— /(SCSFR00) [R/W] B,H,W ----- *3	*2: Reserved because I ² C mode is not set immediately after reset.	
001768H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W ----- *3	—/(TBYTE20) (LAMERT0) [R/W] B,H,W ----- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W ----- *3	TBYTE00/(LAMRID0) / (LAMTIDO) [R/W] B,H,W 00000000	*3: Reserved because CSIO mode is not set immediately after reset.	
00176CH	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W ----- *2	— /(ISBA0) [R/W] B,H,W ----- *2	*4: Reserved because LIN2.1 mode is not set immediately after reset.	
001770H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -00000000	FBYTE0[R/W] B,H,W 00000000 00000000			
001774H	FTICR0[R/W] B,H,W 00000000 00000000		—	—		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001778H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W]] B,H,W 00000000	Multi-UART1
00177CH	— /(RDR11/(TDR11))[R/W] B,H,W ----- *3	-----	RDR01/(TDR01)[R/W] B,H,W -----0 00000000 *1	-----	
001780H	SACSR1[R/W] B,H,W 0---000 00000000	-----	STMR1[R] B,H,W 00000000 00000000	-----	Multi-UART1
001784H	STMCR1[R/W] B,H,W 00000000 00000000	-----	— /(SCSCR1/SFUR1)[R/W] B,H,W ----- *3 *4	-----	
001788H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W ----- *3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W ----- *3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W ----- *3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W ----- *3	*1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
00178CH	—	— /(SCSFR21)[R/W] B,H,W ----- *3	— /(SCSFR11) [R/W] B,H,W ----- *3	— /(SCSFR01) [R/W] B,H,W ----- *3	
001790H	—/(TBYTE31)/ (LAMESR1) [R/W] B,H,W ----- *3	—/(TBYTE21)/ (LAMERT1) [R/W] B,H,W ----- *3	—/(TBYTE11)/ (LAMIER1) [R/W] B,H,W ----- *3	TBYTE01/(LAMRID1) / (LAMTID1) [R/W] B,H,W 00000000	Multi-UART1 *3: Reserved because CSIO mode is not set immediately after reset.
001794H	BGR1[R/W] H,W 00000000 00000000	-----	— /(ISMK1)[R/W] B,H,W ----- *2	— /(ISBA1)[R/W] B,H,W ----- *2	
001798H	FCR11[R/W] B,H,W ---00100	FCR01[R/W] B,H,W -00000000	-----	FBYTE1[R/W] B,H,W 00000000 00000000	*4: Reserved because LIN2.1 mode is not set immediately after reset.
00179CH	FTICR1[R/W] B,H,W 00000000 00000000	-----	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017A0 _H	SCR2/(IBCR2)[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2/(IBSR2)[R/W]] B,H,W 00000000	Multi-UART2
0017A4 _H	— /(RDR12/(TDR12))[R/W] B,H,W ----- * ³	— RDR02/(TDR02)[R/W] B,H,W -----0 00000000 * ¹			
0017A8 _H	SACSR2[R/W] B,H,W 0---000 00000000		STMR2[R] B,H,W 00000000 00000000		
0017AC _H	STMCR2[R/W] B,H,W 00000000 00000000	— /(SCSCR2/SFUR2)[R/W] B,H,W ----- * ³ * ⁴			
0017B0 _H	— /(SCSTR32)/ (LAMSR2) [R/W] B,H,W ----- * ³	— /(SCSTR22)/ (LAMCR2) [R/W] B,H,W ----- * ³	— /(SCSTR12)/ (SFLR12) [R/W] B,H,W ----- * ³	— /(SCSTR02)/ (SFLR02) [R/W] B,H,W ----- * ³	
0017B4 _H	—	— /(SCSFR22) [R/W] B,H,W ----- * ³	— /(SCSFR12) [R/W] B,H,W ----- * ³	— /(SCSFR02) [R/W] B,H,W ----- * ³	
0017B8 _H	—/(TBYTE32)/ (LAMESR2) [R/W] B,H,W ----- * ³	—/(TBYTE22)/ (LAMERT2) [R/W] B,H,W ----- * ³	—/(TBYTE12)/ (LAMIER2) [R/W] B,H,W ----- * ³	TBYTE02/(LAMRID2) / (LAMTID2) [R/W] B,H,W 00000000	
0017BC _H	BGR2[R/W] H, W 00000000 00000000		— /(ISMK2)[R/W] B,H,W ----- * ²	— /(ISBA2)[R/W] B,H,W ----- * ²	
0017C0 _H	FCR12[R/W] B,H,W ---00100	FCR02[R/W] B,H,W -0000000		FBYTE2[R/W] B,H,W 00000000 00000000	Multi-UART2
0017C4 _H	FTICR2[R/W] B,H,W 00000000 00000000		—	—	

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017C8 _H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W]] B,H,W 00000000	Multi-UART3
0017CC _H	— /(RDR13/(TDR13))[R/W] B,H,W ----- *3	-----	RDR03/(TDR03)[R/W] B,H,W -----0 00000000 *1	-----	
0017D0 _H	SACSR3[R/W] B,H,W 0---000 00000000	-----	-----	STMR3[R] B,H,W 00000000 00000000	
0017D4 _H	-----	STMCR3[R/W] B,H,W 00000000 00000000	-----	— /(SCSCR3/SFUR3)[R/W] B,H,W ----- *3 *4	
0017D8 _H	— /(SCSTR33)/ (LAMSR3) [R/W] B,H,W ----- *3	— /(SCSTR23)/ (LAMCR3) [R/W] B,H,W ----- *3	— /(SCSTR13)/ (SFLR13) [R/W] B,H,W ----- *3	— /(SCSTR03)/ (SFLR03) [R/W] B,H,W ----- *3	
0017DC _H	—	— /(SCSFR23) [R/W] B,H,W ----- *3	— /(SCSFR13) [R/W] B,H,W ----- *3	— /(SCSFR03) [R/W] B,H,W ----- *3	
0017E0 _H	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W ----- *3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W ----- *3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W ----- *3	TBYTE03/(LAMRID3) / (LAMTID3) [R/W] B,H,W 00000000	
0017E4 _H	BGR3[R/W] H, W 00000000 00000000	-----	— /(ISMK3)[R/W] B,H,W ----- *2	— /(ISBA3)[R/W] B,H,W ----- *2	
0017E8 _H	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	-----	FBYTE3[R/W] B,H,W 00000000 00000000	
0017EC _H	FTICR3[R/W] B,H,W 00000000 00000000	-----	—	—	
0017F0 _H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W]] B,H,W 00000000	Multi-UART4
0017F4 _H	— /(RDR14/(TDR14))[R/W] B,H,W ----- *3	-----	RDR04/(TDR04)[R/W] B,H,W -----0 00000000 *1	-----	
0017F8 _H	SACSR4[R/W] B,H,W 0---000 00000000	-----	-----	STMR4[R] B,H,W 00000000 00000000	
0017FC _H	-----	STMCR4[R/W] B,H,W 00000000 00000000	-----	— /(SCSCR4/SFUR4)[R/W] B,H,W ----- *3 *4	
001800 _H	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W ----- *3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W ----- *3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W ----- *3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W ----- *3	

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
001804H	—	— /(SCSFR24) [R/W] B,H,W ----- *3	— /(SCSFR14) [R/W] B,H,W ----- *3	— /(SCSFR04) [R/W] B,H,W ----- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.	
001808H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W ----- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W ----- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W ----- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000		
00180CH	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W ----- *2	— /(ISBA4)[R/W] B,H,W ----- *2		
001810H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000			
001814H	FTICR4[R/W] B,H,W 00000000 00000000		—	—		
001818H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W]] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.	
00181CH	— /(RDR15/(TDR15))[R/W] B,H,W ----- *3		RDR05/(TDR05)[R/W] B,H,W -----0 00000000 *1			
001820H	SACSR5[R/W] B,H,W 0---000 00000000		STMR5[R] B,H,W 00000000 00000000			
001824H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W ----- ----- *3 *4			
001828H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W ----- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W ----- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W ----- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W ----- *3		
00182CH	—	— /(SCSFR25) [R/W] B,H,W ----- *3	— /(SCSFR15) [R/W] B,H,W ----- *3	— /(SCSFR05) [R/W] B,H,W ----- *3	Multi-UART6 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.	
001830H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W ----- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W ----- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W ----- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000		
001834H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W ----- *2	— /(ISBA5)[R/W] B,H,W ----- *2		
001838H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000			
00183CH	FTICR5[R/W] B,H,W 00000000 00000000		—	—		
001840H	SCR6/(IBCR6) [R/W] B,H,W 0--00000	SMR6[R/W] B,H,W 000-00-0	SSR6[R/W] B,H,W 0-000011	ESCR6/(IBSR6)[R/W]] B,H,W 00000000	Multi-UART6	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001844H	— /(RDR16/(TDR16))[R/W] B,H,W ----- *3	RDR06/(TDR06)[R/W] B,H,W -----0 00000000 *1			Multi-UART6
001848H	SACSR6[R/W] B,H,W 0---000 00000000	STMR6[R] B,H,W 00000000 00000000			
00184CH	STMCR6[R/W] B,H,W 00000000 00000000	— /(SCSCR6/SFUR6)[R/W] B,H,W ----- *3 *4			
001850H	— /(SCSTR36)/ (LAMSR6) [R/W] B,H,W ----- *3	— /(SCSTR26)/ (LAMCR6) [R/W] B,H,W ----- *3	— /(SCSTR16)/ (SFLR16) [R/W] B,H,W ----- *3	— /(SCSTR06)/ (SFLR06) [R/W] B,H,W ----- *3	
001854H	—	— /(SCSFR26) [R/W] B,H,W ----- *3	— /(SCSFR16) [R/W] B,H,W ----- *3	— /(SCSFR06) [R/W] B,H,W ----- *3	
001858H	—/(TBYTE36)/ (LAMESR6) [R/W] B,H,W ----- *3	—/(TBYTE26)/ (LAMERT6) [R/W] B,H,W ----- *3	—/(TBYTE16)/ (LAMIER6) [R/W] B,H,W ----- *3	TBYTE06/(LAMRID6) / (LAMTID6) [R/W] B,H,W 00000000	
00185CH	BGR6[R/W] H, W 00000000 00000000	— /(ISMK6)[R/W] B,H,W ----- *2	— /(ISBA6)[R/W] B,H,W ----- *2		
001860H	FCR16[R/W] B,H,W ---00100	FCR06[R/W] B,H,W -0000000	FBYTE6[R/W] B,H,W 00000000 00000000		
001864H	FTICR6[R/W] B,H,W 00000000 00000000	—	—		
001868H	SCR7/(IBCR7) [R/W] B,H,W 0--00000	SMR7[R/W] B,H,W 000-00-0	SSR7[R/W] B,H,W 0-000011	ESCR7/(IBSR7)[R/W]] B,H,W 00000000	Multi-UART7
00186CH	— /(RDR17/(TDR17))[R/W] B,H,W ----- *3	RDR07/(TDR07)[R/W] B,H,W -----0 00000000 *1			
001870H	SACSR7[R/W] B,H,W 0---000 00000000	STMR7[R] B,H,W 00000000 00000000			
001874H	STMCR7[R/W] B,H,W 00000000 00000000	— /(SCSCR7/SFUR7)[R/W] B,H,W ----- *3 *4			
001878H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W ----- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W ----- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W ----- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W ----- *3	Multi-UART7
00187CH	—	— /(SCSFR27) [R/W] B,H,W ----- *3	— /(SCSFR17) [R/W] B,H,W ----- *3	— /(SCSFR07) [R/W] B,H,W ----- *3	
001880H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W ----- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W ----- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W ----- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
001884H	BGR7[R/W] H,W 00000000 00000000		— /(ISMK7)[R/W] B,H,W ----- *2	— /(ISBA7)[R/W] B,H,W ----- *2	Multi-UART7	
001888H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000			
00188CH	FTICR7[R/W] B,H,W 00000000 00000000		—	—		
001890H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W]] B,H,W 00000000		
001894H	— /(RDR18/(TDR18))[R/W] B,H,W ----- *3		RDR08/(TDR08)[R/W] B,H,W -----0 00000000 *1			
001898H	SACSR8[R/W] B,H,W 0---000 00000000		STMR8[R] B,H,W 00000000 00000000			
001899H	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W ----- ----- *3 *4			
0018A0H	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W ----- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W ----- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W ----- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W ----- *3		
0018A4H	—	— /(SCSFR28) [R/W] B,H,W ----- *3	— /(SCSFR18) [R/W] B,H,W ----- *3	— /(SCSFR08) [R/W] B,H,W ----- *3		
0018A8H	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W ----- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W ----- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W ----- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000		
0018ACH	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W ----- *2	— /(ISBA8)[R/W] B,H,W ----- *2		
0018B0H	FCR18[R/W] B,H,W ---00100	FCR08[R/W] B,H,W -0000000	FBYTE8[R/W] B,H,W 00000000 00000000		Multi-UART8	
0018B4H	FTICR8[R/W] B,H,W 00000000 00000000		—	—		

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0018B8 _H	SCR9/(IBCR9) [R/W] B,H,W 0--00000	SMR9[R/W] B,H,W 000-00-0	SSR9[R/W] B,H,W 0-000011	ESCR9/(IBSR9)[R/W]] B,H,W 00000000	Multi-UART9 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018BC _H	— /(RDR19/(TDR19))[R/W] B,H,W ----- ----- * ³	— RDR09/(TDR09)[R/W] B,H,W -----0 00000000 * ¹			
0018C0 _H	SACSR9[R/W] B,H,W 0---000 00000000	STMR9[R] B,H,W 00000000 00000000			
0018C4 _H	STMCR9[R/W] B,H,W 00000000 00000000	— /(SCSCR9/SFUR9)[R/W] B,H,W ----- ----- * ³ * ⁴			
0018C8 _H	— /(SCSTR39)/ (LAMSR9) [R/W] B,H,W ----- * ³	— /(SCSTR29)/ (LAMCR9) [R/W] B,H,W ----- * ³	— /(SCSTR19)/ (SFLR19) [R/W] B,H,W ----- * ³	— /(SCSTR09)/ (SFLR09) [R/W] B,H,W ----- * ³	
0018CC _H	—	— /(SCSFR29) [R/W] B,H,W ----- * ³	— /(SCSFR19) [R/W] B,H,W ----- * ³	— /(SCSFR09) [R/W] B,H,W ----- * ³	
0018D0 _H	—/(TBYTE39)/ (LAMESR9) [R/W] B,H,W ----- * ³	—/(TBYTE29)/ (LAMERT9) [R/W] B,H,W ----- * ³	—/(TBYTE19)/ (LAMIERT9) [R/W] B,H,W ----- * ³	TBYTE09/(LAMRID9) / (LAMTID9) [R/W] B,H,W 00000000	
0018D4 _H	BGR9[R/W] H, W 00000000 00000000	— /(ISMK9)[R/W] B,H,W ----- * ²	— /(ISBA9)[R/W] B,H,W ----- * ²		
0018D8 _H	FCR19[R/W] B,H,W ---00100	FCR09[R/W] B,H,W -00000000	FBYTE9[R/W] B,H,W 00000000 00000000		
0018DC _H	FTICR9[R/W] B,H,W 00000000 00000000	—	—		
0018E0 _H	SCR10/(IBCR10) [R/W] B,H,W 0--00000	SMR10[R/W] B,H,W 000-00-0	SSR10[R/W] B,H,W 0-000011	ESCR10/(IBSR10) [R/W] B,H,W 00000000	Multi-UART10 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
0018E4 _H	— /(RDR110/(TDR110))[R/W] B,H,W ----- ----- * ³	— RDR010/(TDR010)[R/W] B,H,W -----0 00000000 * ¹			
0018E8 _H	SACSR10[R/W] B,H,W 0---000 00000000	STMR10[R] B,H,W 00000000 00000000			
0018EC _H	STMCR10[R/W] B,H,W 00000000 00000000	— /(SCSCR10/SFUR10)[R/W] B,H,W ----- ----- * ³ * ⁴			

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
0018F0 _H	— /(SCSTR310)/ (LAMSR10) [R/W] B,H,W ----- *3	— /(SCSTR210)/ (LAMCR10) [R/W] B,H,W ----- *3	— /(SCSTR110)/ (SFLR110)[R/W] B,H,W ----- *3	— /(SCSTR010)/ (SFLR010)[R/W] B,H,W ----- *3	Multi-UART10	
0018F4 _H	—	— /(SCSFR210) [R/W] B,H,W ----- *3	— /(SCSFR110) [R/W] B,H,W ----- *3	— /(SCSFR010) [R/W] B,H,W ----- *3		
0018F8 _H	— /(TBYTE310)/ (LAMESR10) [R/W] B,H,W ----- *3	— /(TBYTE210)/ (LAMERT10) [R/W] B,H,W ----- *3	— /(TBYTE110)/ (LAMIER10) [R/W] B,H,W ----- *3	TBYTE010/(LAMRID10)/(LAMTID10) [R/W] B,H,W 00000000		
0018FC _H	BGR10[R/W] H, W 00000000 00000000		— /(ISMK10)[R/W] B,H,W ----- *2	— /(ISBA10)[R/W] B,H,W ----- *2		
001900 _H	FCR110[R/W] B,H,W ---00100	FCR010[R/W] B,H,W -0000000	FBYTE10[R/W] B,H,W 00000000 00000000			
001904 _H	FTICR10[R/W] B,H,W 00000000 00000000		—	—		
001908 _H	SCR11/(IBCR11) [R/W] B,H,W 0--00000	SMR11[R/W] B,H,W 000-00-0	SSR11[R/W] B,H,W 0-000011	ESCR11/(IBSR11) [R/W] B,H,W 00000000	Multi-UART11	
00190C _H	— /(RDR111/(TDR111))[R/W] B,H,W ----- *3		RDR011/(TDR011)[R/W] B,H,W -----0 00000000 *1			
001910 _H	SACSR11[R/W] B,H,W 0---000 00000000		STMR11[R] B,H,W 00000000 00000000			
001914 _H	STMCR11[R/W] B,H,W 00000000 00000000		— /(SCSCR11/SFUR11)[R/W] B,H,W ----- *3 *4			
001918 _H	— /(SCSTR311)/ (LAMSR11) [R/W] B,H,W ----- *3	— /(SCSTR211)/ (LAMCR11) [R/W] B,H,W ----- *3	— /(SCSTR111)/ (SFLR111)[R/W] B,H,W ----- *3	— /(SCSTR011)/ (SFLR011)[R/W] B,H,W ----- *3		
00191C _H	—	— /(SCSFR211) [R/W] B,H,W ----- *3	— /(SCSFR111) [R/W] B,H,W ----- *3	— /(SCSFR011) [R/W] B,H,W ----- *3		
001920 _H	— /(TBYTE311)/ (LAMESR11) [R/W] B,H,W ----- *3	— /(TBYTE211)/ (LAMERT11) [R/W] B,H,W ----- *3	— /(TBYTE111)/ (LAMIER11) [R/W] B,H,W ----- *3	TBYTE011/(LAMRID11)/(LAMTID11) [R/W] B,H,W 00000000		
001924 _H	BGR11[R/W] H, W 00000000 00000000		— /(ISMK11)[R/W] B,H,W ----- *2	— /(ISBA11)[R/W] B,H,W ----- *2	Multi-UART11	
001928 _H	FCR111[R/W] B,H,W ---00100	FCR011[R/W] B,H,W -0000000	FBYTE11[R/W] B,H,W 00000000 00000000			
00192C _H	FTICR11[R/W] B,H,W 00000000 00000000		—	—		
001930 _H to 0019D8 _H	—	—	—	—	Reserved	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0019DC _H	—	GATEC0 [R/W] B,H,W -----00	—	GATEC2 [R/W] B,H,W -----00	PPG GATE control
0019E0 _H	—	GATEC4 [R/W] B,H,W -----00	—	—	
0019E4 _H	—	—	—	—	
0019E8 _H	GTRS0 [R/W] B,H,W -0000000 -0000000		GTRS1 [R/W] B,H,W -0000000 -0000000		PPG controller
0019EC _H	GTRS2 [R/W] B,H,W -0000000 -0000000		GTRS3 [R/W] B,H,W -0000000 -0000000		
0019F0 _H	GTRS4 [R/W] B,H,W -0000000 -0000000		GTRS5 [R/W] B,H,W -0000000 -0000000		
0019F4 _H	GTRS6 [R/W] B,H,W -0000000 -0000000		GTRS7 [R/W] B,H,W -0000000 -0000000		
0019F8 _H	GTRS8 [R/W] B,H,W -0000000 -0000000		GTRS9 [R/W] B,H,W -0000000 -0000000		
0019FC _H	GTRS10 [R/W] B,H,W -0000000 -0000000		GTRS11 [R/W] B,H,W -0000000 -0000000		PPG controller
001A00 _H	GTRS12 [R/W] B,H,W -0000000 -0000000		GTRS13 [R/W] B,H,W -0000000 -0000000		
001A04 _H	GTRS14 [R/W] B,H,W -0000000 -0000000		GTRS15 [R/W] B,H,W -0000000 -0000000		
001A08 _H	GTRS16 [R/W] B,H,W -0000000 -0000000		GTRS17 [R/W] B,H,W -0000000 -0000000		
001A0C _H	GTRS18 [R/W] B,H,W -0000000 -0000000		GTRS19 [R/W] B,H,W -0000000 -0000000		
001A10 _H	GTRS20 [R/W] B,H,W -0000000 -0000000		GTRS21 [R/W] B,H,W -0000000 -0000000		
001A14 _H	GTRS22 [R/W] B,H,W -0000000 -0000000		GTRS23 [R/W] B,H,W -0000000 -0000000		PPG controller
001A18 _H to 001A2C _H	—	—	—	—	
001A30 _H	—	—	—	—	
001A34 _H	—	—	—	—	
001A38 _H	GTREN0 [R/W] H,W 00000000 00000000		GTREN1 [R/W] H,W 00000000 00000000		PPG controller
001A3C _H	GTREN2 [R/W] H,W 00000000 00000000		—	—	
001A40 _H	PCN0 [R/W] B,H,W 00000000 000000-0		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		PPG0 * for communication
001A44 _H	PDUTO [W] H,W XXXXXXXX XXXXXXXX		PTMR0 [R] H,W 11111111 11111111		
001A48 _H	PCN200 [R/W] B,H,W --000000 ----110		PSDR0 [R/W] H,W 00000000 00000000		
001A4C _H	PTPC0 [R/W] H,W 00000000 00000000		PCMDWD0 [R/W] B,H,W ----- -----0000		
001A50 _H	PHCSR0 [W] H,W XXXXXXXX XXXXXXXX		PLCSR0 [W] H,W XXXXXXXX XXXXXXXX		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001A54H	PHDUTO [W] H,W XXXXXXXX XXXXXXXX		PLDUTO0 [W] H,W XXXXXXXX XXXXXXXX		PPG0 * for communication
001A58H	PCMDDTO [R/W] H,W 00000000 00000000		—	—	
001A5CH	PCN1 [R/W] B,H,W 00000000 000000-0		PCSR1 [W] H,W XXXXXXXX XXXXXXXX		PPG1 * for communication
001A60H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PTMR1 [R] H,W 11111111 11111111		
001A64H	PCN201 [R/W] B,H,W --000000 ----110		PSDR1 [R/W] H,W 00000000 00000000		PPG1 * for communication
001A68H	PTPC1 [R/W] H,W 00000000 00000000		PCMDWD1 [R/W] B,H,W ----- ----0000		
001A6CH	PHCSR1 [W] H,W XXXXXXXX XXXXXXXX		PLCSR1 [W] H,W XXXXXXXX XXXXXXXX		
001A70H	PHDUT1 [W] H,W XXXXXXXX XXXXXXXX		PLDUT1 [W] H,W XXXXXXXX XXXXXXXX		
001A74H	PCMDDT1 [R/W] H,W 00000000 00000000	—	—	—	
001A78H	PCN2 [R/W] B,H,W 00000000 000000-0		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2 * for communication
001A7CH	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PTMR2 [R] H,W 11111111 11111111		
001A80H	PCN202 [R/W] B,H,W --000000 ----110		PSDR2 [R/W] H,W 00000000 00000000		PPG2 * for communication
001A84H	PTPC2 [R/W] H,W 00000000 00000000		PCMDWD2 [R/W] B,H,W ----- ----0000		
001A88H	PHCSR2 [W] H,W XXXXXXXX XXXXXXXX		PLCSR2 [W] H,W XXXXXXXX XXXXXXXX		
001A8CH	PHDUT2 [W] H,W XXXXXXXX XXXXXXXX		PLDUT2 [W] H,W XXXXXXXX XXXXXXXX		
001A90H	PCMDDT2 [R/W] H,W 00000000 00000000	—	—	—	
001A94H	PCN3 [R/W] B,H,W 00000000 000000-0		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3 * for communication
001A98H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PTMR3 [R] H,W 11111111 11111111		
001A9CH	PCN203 [R/W] B,H,W --000000 ----110		PSDR3 [R/W] H,W 00000000 00000000		
001AA0H	PTPC3 [R/W] H,W 00000000 00000000		PCMDWD3 [R/W] B,H,W ----- ----0000		
001AA4H	PHCSR3 [W] H,W XXXXXXXX XXXXXXXX		PLCSR3 [W] H,W XXXXXXXX XXXXXXXX		
001AA8H	PHDUT3 [W] H,W XXXXXXXX XXXXXXXX		PLDUT3 [W] H,W XXXXXXXX XXXXXXXX		PPG4
001AACH	PCMDDT3 [R/W] H,W 00000000 00000000	—	—	—	
001AB0H	PCN4 [R/W] B,H,W 00000000 000000-0		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		
001AB4H	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PTMR4 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001AB8 _H	PCN204 [R/W] B,H,W --000000 -----110		PSDR4 [R/W] H,W 00000000 00000000		PPG4
001ABC _H	PTPC4 [R/W] H,W 00000000 00000000		—	—	
001AC0 _H	PCN5 [R/W] B,H,W 00000000 0000000-0		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
001AC4 _H	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PTMR5 [R] H,W 11111111 11111111		
001AC8 _H	PCN205 [R/W] B,H,W --000000 -----110		PSDR5 [R/W] H,W 00000000 00000000		PPG5
001ACC _H	PTPC5 [R/W] H,W 00000000 00000000		—	—	
001AD0 _H	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
001AD4 _H	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
001AD8 _H	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		PPG6
001ADC _H	PTPC6 [R/W] H,W 00000000 00000000		—	—	
001AE0 _H	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
001AE4 _H	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
001AE8 _H	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		PPG7
001AEC _H	PTPC7 [R/W] H,W 00000000 00000000		—	—	
001AF0 _H	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
001AF4 _H	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
001AF8 _H	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		PPG8
001AFC _H	PTPC8 [R/W] H,W 00000000 00000000		—	—	
001B00 _H	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
001B04 _H	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
001B08 _H	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		PPG9
001B0C _H	PTPC9 [R/W] H,W 00000000 00000000		—	—	
001B10 _H	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
001B14 _H	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B18 _H	PCN210 [R/W] B,H,W --000000 ----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
001B1C _H	PTPC10 [R/W] H,W 00000000 00000000		—	—	
001B20 _H	PCN11 [R/W] B,H,W 00000000 0000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11
001B24 _H	PDUT11 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR11 [R] H,W 11111111 11111111		PPG11
001B28 _H	PCN211 [R/W] B,H,W --000000 ----110		PSDR11 [R/W] H,W 00000000 00000000		
001B2C _H	PTPC11 [R/W] H,W 00000000 00000000		—	—	
001B30 _H	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXXX XXXXXXXX		PPG12
001B34 _H	PDUT12 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
001B38 _H	PCN212 [R/W] B,H,W --000000 ----110		PSDR12 [R/W] H,W 00000000 00000000		PPG12
001B3C _H	PTPC12 [R/W] H,W 00000000 00000000		—	—	
001B40 _H	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXXX XXXXXXXX		PPG13
001B44 _H	PDUT13 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
001B48 _H	PCN213 [R/W] B,H,W --000000 ----110		PSDR13 [R/W] H,W 00000000 00000000		PPG13
001B4C _H	PTPC13 [R/W] H,W 00000000 00000000		—	—	
001B50 _H	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXXX XXXXXXXX		PPG14
001B54 _H	PDUT14 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
001B58 _H	PCN214 [R/W] B,H,W --000000 ----110		PSDR14 [R/W] H,W 00000000 00000000		PPG14
001B5C _H	PTPC14 [R/W] H,W 00000000 00000000		—	—	
001B60 _H	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXXX XXXXXXXX		PPG15
001B64 _H	PDUT15 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
001B68 _H	PCN215 [R/W] B,H,W --000000 ----110		PSDR15 [R/W] H,W 00000000 00000000		PPG15
001B6C _H	PTPC15 [R/W] H,W 00000000 00000000		—	—	
001B70 _H	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXXX XXXXXXXX		PPG16
001B74 _H	PDUT16 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR16 [R] H,W 11111111 11111111		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B78H	PCN216 [R/W] B,H,W --000000 ----110		PSDR16 [R/W] H,W 00000000 00000000		PPG16
001B7CH	PTPC16 [R/W] H,W 00000000 00000000		—	—	
001B80H	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
001B84H	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
001B88H	PCN217 [R/W] B,H,W --000000 ----110		PSDR17 [R/W] H,W 00000000 00000000		PPG18
001B8CH	PTPC17 [R/W] H,W 00000000 00000000		—	—	
001B90H	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
001B94H	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
001B98H	PCN218 [R/W] B,H,W --000000 ----110		PSDR18 [R/W] H,W 00000000 00000000		PPG19
001B9CH	PTPC18 [R/W] H,W 00000000 00000000		—	—	
001BA0H	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
001BA4H	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
001BA8H	PCN219 [R/W] B,H,W --000000 ----110		PSDR19 [R/W] H,W 00000000 00000000		PPG20
001BACH	PTPC19 [R/W] H,W 00000000 00000000		—	—	
001BB0H	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
001BB4H	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
001BB8H	PCN220 [R/W] B,H,W --000000 ----110		PSDR20 [R/W] H,W 00000000 00000000		PPG21
001BBCH	PTPC20 [R/W] H,W 00000000 00000000		—	—	
001BC0H	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
001BC4H	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
001BC8H	PCN221 [R/W] B,H,W --000000 ----110		PSDR21 [R/W] H,W 00000000 00000000		PPG21
001BCCH	PTPC21 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001BD0H	PCN22 [R/W] B,H,W 00000000 000000-0		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
001BD4H	PDUT22 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR22 [R] H,W 11111111 11111111		
001BD8H	PCN222 [R/W] B,H,W --000000 ----110		PSDR22 [R/W] H,W 00000000 00000000		
001BDCH	PTPC22 [R/W] H,W 00000000 00000000	—	—	—	
001BE0H	PCN23 [R/W] B,H,W 00000000 000000-0		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
001BE4H	PDUT23 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR23 [R] H,W 11111111 11111111		
001BE8H	PCN223 [R/W] B,H,W --000000 ----110		PSDR23 [R/W] H,W 00000000 00000000		
001BECH	PTPC23 [R/W] H,W 00000000 00000000	—	—	—	
001BF0H	PCN24 [R/W] B,H,W 00000000 000000-0		PCSR24 [W] H,W XXXXXXXX XXXXXXXX		PPG24
001BF4H	PDUT24 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR24 [R] H,W 11111111 11111111		
001BF8H	PCN224 [R/W] B,H,W --000000 ----110		PSDR24 [R/W] H,W 00000000 00000000		
001BFCH	PTPC24 [R/W] H,W 00000000 00000000	—	—	—	
001C00H	PCN25 [R/W] B,H,W 00000000 000000-0		PCSR25 [W] H,W XXXXXXXX XXXXXXXX		PPG25
001C04H	PDUT25 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR25 [R] H,W 11111111 11111111		
001C08H	PCN225 [R/W] B,H,W --000000 ----110		PSDR25 [R/W] H,W 00000000 00000000		
001C0CH	PTPC25 [R/W] H,W 00000000 00000000	—	—	—	
001C10H	PCN26 [R/W] B,H,W 00000000 000000-0		PCSR26 [W] H,W XXXXXXXX XXXXXXXX		PPG26
001C14H	PDUT26 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR26 [R] H,W 11111111 11111111		
001C18H	PCN226 [R/W] B,H,W --000000 ----110		PSDR26 [R/W] H,W 00000000 00000000		
001C1CH	PTPC26 [R/W] H,W 00000000 00000000	—	—	—	
001C20H	PCN27 [R/W] B,H,W 00000000 000000-0		PCSR27 [W] H,W XXXXXXXX XXXXXXXX		PPG27
001C24H	PDUT27 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR27 [R] H,W 11111111 11111111		PPG27
001C28H	PCN227 [R/W] B,H,W --000000 ----110		PSDR27 [R/W] H,W 00000000 00000000		
001C2CH	PTPC27 [R/W] H,W 00000000 00000000	—	—	—	PPG27

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C30 _H	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
001C34 _H	PDUT28 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
001C38 _H	PCN228 [R/W] B,H,W --000000 ----110		PSDR28 [R/W] H,W 00000000 00000000		
001C3C _H	PTPC28 [R/W] H,W 00000000 00000000	—	—	—	
001C40 _H	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
001C44 _H	PDUT29 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
001C48 _H	PCN229 [R/W] B,H,W --000000 ----110		PSDR29 [R/W] H,W 00000000 00000000		
001C4C _H	PTPC29 [R/W] H,W 00000000 00000000	—	—	—	
001C50 _H	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
001C54 _H	PDUT30 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
001C58 _H	PCN230 [R/W] B,H,W --000000 ----110		PSDR30 [R/W] H,W 00000000 00000000		
001C5C _H	PTPC30 [R/W] H,W 00000000 00000000	—	—	—	
001C60 _H	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
001C64 _H	PDUT31 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
001C68 _H	PCN231 [R/W] B,H,W --000000 ----110		PSDR31 [R/W] H,W 00000000 00000000		
001C6C _H	PTPC31 [R/W] H,W 00000000 00000000	—	—	—	
001C70 _H	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
001C74 _H	PDUT32 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR32 [R] H,W 11111111 11111111		
001C78 _H	PCN232 [R/W] B,H,W --000000 ----110		PSDR32 [R/W] H,W 00000000 00000000		PPG32
001C7C _H	PTPC32 [R/W] H,W 00000000 00000000	—	—	—	
001C80 _H	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXX XXXXXXXX		PPG33
001C84 _H	PDUT33 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
001C88 _H	PCN233 [R/W] B,H,W --000000 ----110		PSDR33 [R/W] H,W 00000000 00000000		PPG33
001C8C _H	PTPC33 [R/W] H,W 00000000 00000000	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C90 _H	PCN34 [R/W] B,H,W 00000000 000000-0		PCSR34 [W] H,W XXXXXXXX XXXXXXXX		PPG34
001C94 _H	PDUT34 [W] H,W XXXXXXXX XXXXXXXX		PTMR34 [R] H,W 11111111 11111111		
001C98 _H	PCN234 [R/W] B,H,W --000000 ----110		PSDR34 [R/W] H,W 00000000 00000000		
001C9C _H	PTPC34 [R/W] H,W 00000000 00000000	—	—	—	
001CA0 _H	PCN35 [R/W] B,H,W 00000000 000000-0		PCSR35 [W] H,W XXXXXXXX XXXXXXXX		PPG35
001CA4 _H	PDUT35 [W] H,W XXXXXXXX XXXXXXXX		PTMR35 [R] H,W 11111111 11111111		
001CA8 _H	PCN235 [R/W] B,H,W --000000 ----110		PSDR35 [R/W] H,W 00000000 00000000		
001CAC _H	PTPC35 [R/W] H,W 00000000 00000000	—	—	—	
001CB0 _H	PCN36 [R/W] B,H,W 00000000 000000-0		PCSR36 [W] H,W XXXXXXXX XXXXXXXX		PPG36
001CB4 _H	PDUT36 [W] H,W XXXXXXXX XXXXXXXX		PTMR36 [R] H,W 11111111 11111111		
001CB8 _H	PCN236 [R/W] B,H,W --000000 ----110		PSDR36 [R/W] H,W 00000000 00000000		
001CBC _H	PTPC36 [R/W] H,W 00000000 00000000	—	—	—	
001CC0 _H	PCN37 [R/W] B,H,W 00000000 000000-0		PCSR37 [W] H,W XXXXXXXX XXXXXXXX		PPG37
001CC4 _H	PDUT37 [W] H,W XXXXXXXX XXXXXXXX		PTMR37 [R] H,W 11111111 11111111		
001CC8 _H	PCN237 [R/W] B,H,W --000000 ----110		PSDR37 [R/W] H,W 00000000 00000000		
001CCC _H	PTPC37 [R/W] H,W 00000000 00000000	—	—	—	
001CD0 _H	PCN38 [R/W] B,H,W 00000000 000000-0		PCSR38 [W] H,W XXXXXXXX XXXXXXXX		PPG38
001CD4 _H	PDUT38 [W] H,W XXXXXXXX XXXXXXXX		PTMR38 [R] H,W 11111111 11111111		
001CD8 _H	PCN238 [R/W] B,H,W --000000 ----110		PSDR38 [R/W] H,W 00000000 00000000		
001CDC _H	PTPC38 [R/W] H,W 00000000 00000000	—	—	—	
001CE0 _H	PCN39 [R/W] B,H,W 00000000 000000-0		PCSR39 [W] H,W XXXXXXXX XXXXXXXX		PPG39
001CE4 _H	PDUT39 [W] H,W XXXXXXXX XXXXXXXX		PTMR39 [R] H,W 11111111 11111111		PPG39
001CE8 _H	PCN239 [R/W] B,H,W --000000 ----110		PSDR39 [R/W] H,W 00000000 00000000		
001CEC _H	PTPC39 [R/W] H,W 00000000 00000000	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001CF0 _H	PCN40 [R/W] B,H,W 00000000 000000-0		PCSR40 [W] H,W XXXXXXXX XXXXXXXX		PPG40
001CF4 _H	PDUT40 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR40 [R] H,W 11111111 11111111		
001CF8 _H	PCN240 [R/W] B,H,W --000000 ----110		PSDR40 [R/W] H,W 00000000 00000000		
001CFC _H	PTPC40 [R/W] H,W 00000000 00000000	—	—	—	
001D00 _H	PCN41 [R/W] B,H,W 00000000 000000-0		PCSR41 [W] H,W XXXXXXXX XXXXXXXX		PPG41
001D04 _H	PDUT41 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR41 [R] H,W 11111111 11111111		
001D08 _H	PCN241 [R/W] B,H,W --000000 ----110		PSDR41 [R/W] H,W 00000000 00000000		
001D0C _H	PTPC41 [R/W] H,W 00000000 00000000	—	—	—	
001D10 _H	PCN42 [R/W] B,H,W 00000000 000000-0		PCSR42 [W] H,W XXXXXXXX XXXXXXXX		PPG42
001D14 _H	PDUT42 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR42 [R] H,W 11111111 11111111		
001D18 _H	PCN242 [R/W] B,H,W --000000 ----110		PSDR42 [R/W] H,W 00000000 00000000		
001D1C _H	PTPC42 [R/W] H,W 00000000 00000000	—	—	—	
001D20 _H	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXX XXXXXXXX		PPG43
001D24 _H	PDUT43 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
001D28 _H	PCN243 [R/W] B,H,W --000000 ----110		PSDR43 [R/W] H,W 00000000 00000000		
001D2C _H	PTPC43 [R/W] H,W 00000000 00000000	—	—	—	
001D30 _H	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXX XXXXXXXX		PPG44
001D34 _H	PDUT44 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
001D38 _H	PCN244 [R/W] B,H,W --000000 ----110		PSDR44 [R/W] H,W 00000000 00000000		
001D3C _H	PTPC44 [R/W] H,W 00000000 00000000	—	—	—	
001D40 _H	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXX XXXXXXXX		PPG45
001D44 _H	PDUT45 [W] H,W XXXXXXXXX XXXXXXXXX		PTMR45 [R] H,W 11111111 11111111		
001D48 _H	PCN245 [R/W] B,H,W --000000 ----110		PSDR45 [R/W] H,W 00000000 00000000		
001D4C _H	PTPC45 [R/W] H,W 00000000 00000000	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D50 _H	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
001D54 _H	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
001D58 _H	PCN246 [R/W] B,H,W --000000 ----110		PSDR46 [R/W] H,W 00000000 00000000		
001D5C _H	PTPC46 [R/W] H,W 00000000 00000000	—	—	—	
001D60 _H	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
001D64 _H	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
001D68 _H	PCN247 [R/W] B,H,W --000000 ----110		PSDR47 [R/W] H,W 00000000 00000000		
001D6C _H	PTPC47 [R/W] H,W 00000000 00000000	—	—	—	
001D70 _H to 001FFC _H	—	—	—	—	Reserved
002000 _H	CTRLR0 [R/W] B,H,W ----- 000-0001		STATR0 [R/W] B,H,W ----- 00000000		CAN0 (128msb)
002004 _H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008 _H	INTRO [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W ----- X00000--		
00200C _H	BRPER0 [R/W] B,H,W ----- ----0000	—	—	—	
002010 _H	IF1CREQ0 [R/W] B,H,W 0----- 00000001		IF1CMSK0 [R/W] B,H,W ----- 00000000		
002014 _H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018 _H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201C _H	IF1MCTR0 [R/W] B,H,W 00000000 0---0000	—	—	—	
002020 _H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024 _H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028 _H	—	—	—	—	
00202C _H	—	—	—	—	
002030 _H , 002034 _H	Reserved(IF1 data mirror)				
002038 _H	—	—	—	—	
00203C _H	—	—	—	—	
002040 _H	IF2CREQ0 [R/W] B,H,W 0----- 00000001		IF2CMSK0 [R/W] B,H,W ----- 00000000		
002044 _H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048 _H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00204C _H	IF2MCTR0 [R/W] B,H,W 00000000 0---0000	—	—	—	
002050 _H	IF2DTA10 [R/W] B,H,W 00000000 00000000	IF2DTA20 [R/W] B,H,W 00000000 00000000	—	—	
002054 _H	IF2DTB10 [R/W] B,H,W 00000000 00000000	IF2DTB20 [R/W] B,H,W 00000000 00000000	—	—	
002058 _H	—	—	—	—	
00205C _H	—	—	—	—	
002060 _H , 002064 _H	Reserved(IF2 data mirror)				
002068 _H to 00207C _H	—				
002080 _H	TREQR20 [R] B,H,W 00000000 00000000	TREQR10 [R] B,H,W 00000000 00000000	—	—	CAN0 (128msb)
002084 _H	TREQR40 [R] B,H,W 00000000 00000000	TREQR30 [R] B,H,W 00000000 00000000	—	—	
002088 _H	TREQR60 [R] B,H,W 00000000 00000000	TREQR50 [R] B,H,W 00000000 00000000	—	—	
00208C _H	TREQR80 [R] B,H,W 00000000 00000000	TREQR70 [R] B,H,W 00000000 00000000	—	—	
002090 _H	NEWDT20 [R] B,H,W 00000000 00000000	NEWDT10 [R] B,H,W 00000000 00000000	—	—	
002094 _H	NEWDT40 [R] B,H,W 00000000 00000000	NEWDT30 [R] B,H,W 00000000 00000000	—	—	
002098 _H	NEWDT60 [R] B,H,W 00000000 00000000	NEWDT50 [R] B,H,W 00000000 00000000	—	—	
00209C _H	NEWDT80 [R] B,H,W 00000000 00000000	NEWDT70 [R] B,H,W 00000000 00000000	—	—	
0020A0 _H	INTPND20 [R] B,H,W 00000000 00000000	INTPND10 [R] B,H,W 00000000 00000000	—	—	
0020A4 _H	INTPND40 [R] B,H,W 00000000 00000000	INTPND30 [R] B,H,W 00000000 00000000	—	—	
0020A8 _H	INTPND60 [R] B,H,W 00000000 00000000	INTPND50 [R] B,H,W 00000000 00000000	—	—	
0020AC _H	INTPND80 [R] B,H,W 00000000 00000000	INTPND70 [R] B,H,W 00000000 00000000	—	—	
0020B0 _H	MSGVAL20 [R] B,H,W 00000000 00000000	MSGVAL10 [R] B,H,W 00000000 00000000	—	—	
0020B4 _H	MSGVAL40 [R] B,H,W 00000000 00000000	MSGVAL30 [R] B,H,W 00000000 00000000	—	—	
0020B8 _H	MSGVAL60 [R] B,H,W 00000000 00000000	MSGVAL50 [R] B,H,W 00000000 00000000	—	—	
0020BC _H	MSGVAL80 [R] B,H,W 00000000 00000000	MSGVAL70 [R] B,H,W 00000000 00000000	—	—	
0020C0 _H to 0020FC _H	—				CAN0 (128msb)

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
002100 _H	CTRLR1 [R/W] B,H,W ----- 000-0001		STATR1 [R/W] B,H,W ----- 00000000		CAN1 (64msb)	
002104 _H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001			
002108 _H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W ----- X00000--			
00210C _H	BRPER1 [R/W] B,H,W ----- ----0000		—	—		
002110 _H	IF1CREQ1 [R/W] B,H,W 0----- 00000001		IF1CMSK1 [R/W] B,H,W ----- 00000000			
002114 _H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111			
002118 _H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000			
00211C _H	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—		
002120 _H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000			
002124 _H	IF1DTB21 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000			
002128 _H	—	—	—	—		
00212C _H	—	—	—	—		
002130 _H , 002134 _H	Reserved (IF1 data mirror)					
002138 _H	—	—	—	—		
00213C _H	—	—	—	—		
002140 _H	IF2CREQ1 [R/W] B,H,W 0----- 00000001		IF2CMSK1 [R/W] B,H,W ----- 00000000		CAN1 (64msb)	
002144 _H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111			
002148 _H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000			
00214C _H	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—		
002150 _H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000			
002154 _H	IF2DTB21 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000			
002158 _H	—	—	—	—		
00215C _H	—	—	—	—		
002160 _H , 002164 _H	Reserved (IF2 data mirror)					
002168 _H to 00217C _H	—					
002180 _H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000			
002184 _H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000			
002188 _H	—	—	—	—		
00218C _H	—	—	—	—		

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
002190 _H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		CAN1 (64msb)	
002194 _H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000			
002198 _H	—	—	—	—		
00219C _H	—	—	—	—		
0021A0 _H	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000			
0021A4 _H	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000			
0021A8 _H	—	—	—	—		
0021AC _H	—	—	—	—		
0021B0 _H	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000			
0021B4 _H	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000			
0021B8 _H	—	—	—	—		
0021BC _H	—	—	—	—		
0021C0 _H to 0021FC _H	—	—	—	—		
002200 _H	CTRLR2 [R/W] B,H,W ----- 000-0001		STATR2 [R/W] B,H,W ----- 00000000		CAN2 (64msb)	
002204 _H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2 [R/W] B,H,W -0100011 00000001			
002208 _H	INTR2 [R] B,H,W 00000000 00000000		TESTR2 [R/W] B,H,W ----- X00000--			
00220C _H	BRPER2 [R/W] B,H,W ----- ----0000		—			
002210 _H	IF1CREQ2 [R/W] B,H,W 0----- 00000001		IF1CMSK2 [R/W] B,H,W ----- 00000000			
002214 _H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111			
002218 _H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000			
00221C _H	IF1MCTR2 [R/W] B,H,W 00000000 0---0000		—			
002220 _H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000			
002224 _H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000			
002228 _H	—	—	—	—		
00222C _H	—	—	—	—		
002230 _H , 002234 _H	Reserved (IF1 data mirror)					
002238 _H	—	—	—	—		
00223C _H	—	—	—	—		
002240 _H	IF2CREQ2 [R/W] B,H,W 0----- 00000001		IF2CMSK2 [R/W] B,H,W ----- 00000000			

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002244H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12 [R/W] B,H,W 11111111 11111111		
002248H	IF2ARB22 [R/W] B,H,W 00000000 00000000		IF2ARB12 [R/W] B,H,W 00000000 00000000		
00224CH	IF2MCTR2 [R/W] B,H,W 00000000 0---0000			—	
002250H	IF2DTA12 [R/W] B,H,W 00000000 00000000		IF2DTA22 [R/W] B,H,W 00000000 00000000		
002254H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		
002258H	—	—	—	—	
00225CH	—	—	—	—	
002260H, 002264H	Reserved (IF2 data mirror)				
002268H to 00227CH	—				
002280H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		CAN2 (64msb)
002284H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288H	—	—	—	—	
00228CH	—	—	—	—	
002290H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298H	—	—	—	—	
00229CH	—	—	—	—	
0022A0H	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
0022A4H	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
0022A8H	—	—	—	—	
0022ACH	—	—	—	—	
0022B0H	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
0022B4H	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
0022B8H	—	—	—	—	
0022BCH	—	—	—	—	
0022C0H to 0022FCH	—				
002300H	DFCTLR [R/W] B,H,W -0-----		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304H	—	—	—	—	
002308H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W -----	FLIFFER2 [R/W] B,H,W -----	Flash / WorkFlash

Address	Address offset value / Register name				Block	
	+0	+1	+2	+3		
00230C _H to 0023FC _H	—				Reserved	
002400 _H	SEEARX [R] B,H,W -0000000 00000000		DEEARX [R] B,H,W -0000000 00000000		XBS RAM ECC control	
002404 _H	EECSR _X [R/W] B,H,W ----00--	—	EFEARX [R/W] B,H,W -0000000 00000000			
002408 _H	—	EFECRX [R/W] B,H,W -----0 00000000 00000000				
00240C _H to 002FFC _H	—				Reserved	
003000 _H	SEEARA [R] B,H,W ----000 00000000		DEEARA [R] B,H,W ----000 00000000		Backup RAM ECC control	
003004 _H	EECSRA [R/W] B,H,W ----00--	—	EFEARA [R/W] B,H,W ----000 00000000			
003008 _H	—	EFECRA [R/W] B,H,W -----0 00000000 00000000				
00300C _H	TEAR0X[R] B,H,W 000----- -0000000 00000000				RAM/ diagnosis XBS RAM	
003010 _H	TEAR1X[R] B,H,W 000----- -0000000 00000000					
003014 _H	TEAR2X[R] B,H,W 000----- -0000000 00000000					
003018 _H	TAEARX [R/W] B,H,W -1111111 11111111		TASARX [R/W] B,H,W -0000000 00000000			
00301C _H	TFECRX [R/W] B,H,W ----0000	TICRX [R/W] B,H,W ----0000	TTCRX [R/W] B,H,W -----00 00001100			
003020 _H	TSRCRX [W] B,H,W 0-----	—	—	TKCCRX [R/W] B,H,W 00----00	RAM/ diagnosis Backup RAM	
003024 _H to 00302C _H	—				Reserved	
003030 _H	TEAR0A[R] B,H,W 000-----000 00000000					
003034 _H	TEAR1A[R] B,H,W 000-----000 00000000					
003038 _H	TEAR2A[R] B,H,W 000-----000 00000000					
00303C _H	TAEARA[R/W] B,H,W ----111 11111111		TASARA[R/W] B,H,W ----000 00000000			
003040 _H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W -----00 00001100		RAM/ diagnosis Backup RAM	
003044 _H	TSRCRA [R/W] B,H,W 0-----	—	—	TKCCRA [R/W] B,H,W 00----00		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003048 _H to 0030FC _H	—				Reserved
003100 _H	BUSDIGSR0[R/W] H,W 00000000 0----00		BUSDIGSR1[R/W] H,W 00000000 0----00		
003104 _H	BUSDIGSR2[R/W] H,W 00000000 0----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108 _H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
00310C _H	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110 _H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114 _H	—	—	BUSDIGSR3[R/W] H,W 00000000 0----00		
003118 _H	BUSDIGSR4[R/W] H,W 00000000 0----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
00311C _H	—	—	—	—	
003120 _H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124 _H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128 _H to 003FFC _H	—				Reserved
004000 _H to 005FFC _H	Backup-RAM				Backup RAM area
006000 _H to 00EFFC _H	—	—	—	—	Reserved
00F000 _H to 00FEFC _H	—	—	—	—	Reserved [S]
00FF00 _H	DSUCR [R/W] B,H,W -----0		—	—	OCDU [S]
00FF04 _H to 00FF0C _H	—				Reserved [S]
00FF10 _H	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14 _H	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF18 _H to 00FFF4 _H	—				Reserved [S]
00FFF8 _H	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FFFC _H	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt Vector 64 Pins

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFECH	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFDC _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFCCh	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFF8 _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFF4 _H	2* ²
Reload timer 3/6/7	19	13	ICR03	3B0 _H	000FFF0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
-	22	16	ICR06	3A4 _H	000FFFA4 _H	-* ⁶
-	23	17	ICR07	3A0 _H	000FFFA0 _H	-* ⁶
-	24	18	ICR08	39C _H	000FFF9C _H	-* ⁶
-	25	19	ICR09	398 _H	000FFF98 _H	-* ⁶
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8CH	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7CH	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78H	17
CAN0	34	22	ICR18	374 _H	000FFF74H	-
CAN1	35	23	ICR19	370 _H	000FFF70H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6CH	-
Up/down counter 0						
Up/down counter 1						
Real time clock						
-	38	26	ICR22	364 _H	000FFF64H	-* ⁶
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60H	23
PPG 1/10/11/20/30/31	40	28	ICR24	35C _H	000FFF5CH	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43						
16-bit Free-run timer 2 (0 detection) / (compare clear)	41	29	ICR25	358 _H	000FFF58H	25* ³
PPG 4/24/35	42	2A	ICR26	354 _H	000FFF54H	26* ³
PPG 7/16/17/27/37	43	2B	ICR27	350 _H	000FFF50H	27* ³
PPG 19	44	2C	ICR28	34C _H	000FFF4CH	28* ³
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48H	29
Main timer	46	2E	ICR30	344 _H	000FFF44H	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Clock calibration unit (sub oscillation)	47	2F	ICR31	340H	000FFF40H	31*1,*4
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/10/11/14/15/16/17/22/27/28/31	48	30	ICR32	33CH	000FFF3CH	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338H	000FFF38H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334H	000FFF34H	34*5
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330H	000FFF30H	35
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32CH	000FFF2CH	36*1
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328H	000FFF28H	37
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324H	000FFF24H	38*1
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320H	000FFF20H	39
WG dead timer underflow 0 / 1 / 2						
WG dead timer reload 0 / 1 / 2						
WG DTTI 0						
32-bit ICU4 (fetching/measurement)	56	38	ICR40	31CH	000FFF1CH	40
Multi-function serial interface ch.11 (transmission completed)						
32-bit ICU5 (fetching/measurement)	57	39	ICR41	318H	000FFF18H	41
A/D converter 32/34/35/37/38/40/41/42/43/44/45/46/47						
32-bit OCU7/11 (match)	58	3A	ICR42	314H	000FFF14H	42
32-bit OCU8/9 (match)	59	3B	ICR43	310H	000FFF10H	43
-	60	3C	ICR44	30CH	000FFF0CH	-*6
-	61	3D	ICR45	308H	000FFF08H	-
-						
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304H	000FFF04H	-
Delay interrupt	63	3F	ICR47	300H	000FFF00H	-
System reserved (Used for REALOS™*8)	64	40	-	2FCH	000FFEFCH	-
System reserved (Used for REALOS)	65	41	-	2F8H	000FFEF8H	-

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Used with the INT instruction	66 255	42 FF	-	2F4H 000H	000FFEF4H 000FFC00H	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.

80 Pins

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFEC _H	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFDC _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFCC _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0~7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8~15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
-	22	16	ICR06	3A4 _H	000FFFA4 _H	-* ⁶
-	23	17	ICR07	3A0 _H	000FFFA0 _H	-* ⁶
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
-	38	26	ICR22	364 _H	000FFF64 _H	-* ⁶
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
PPG 1/10/11/20/30/31	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/15/24/35	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 7/16/17/26/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/18/19/29	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Clock calibration unit (sub oscillation)	47	2F	ICR31	340H	000FFF40H	31*1,*4
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/10/11/12/14/15/16/17/19/22/26/27/28/31	48	30	ICR32	33CH	000FFF3CH	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338H	000FFF38H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334H	000FFF34H	34*5
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 5	51	33	ICR35	330H	000FFF30H	35*5
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32CH	000FFF2CH	36*1
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328H	000FFF28H	37
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324H	000FFF24H	38*1
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320H	000FFF20H	39
WG dead timer underflow 0 / 1 / 2						
WG dead timer reload 0 / 1 / 2						
WG DTTI 0	56	38	ICR40	31CH	000FFF1CH	40
32-bit ICU4 (fetching/measurement)						
Multi-function serial interface ch.11 (transmission completed)						
32-bit ICU5 (fetching/measurement)	57	39	ICR41	318H	000FFF18H	41
A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/ 47						
32-bit OCU7/11 (match)	58	3A	ICR42	314H	000FFF14H	42
32-bit OCU8/9 (match)	59	3B	ICR43	310H	000FFF10H	43
-	60	3C	ICR44	30CH	000FFF0CH	-*6
Base timer 1 IRQ0	61	3D	ICR45	308H	000FFF08H	45
Base timer 1 IRQ1						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304H	000FFF04H	-
Delay interrupt	63	3F	ICR47	300H	000FFF00H	-

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFCH	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFEF8H	-
Used with the INT instruction	66 255	42 FF	-	2F4 _H 000 _H	000FFEF4H 000FFC00H	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

100 Pins

Interrupt Factor	Interrupt number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3ECh	000FFFECh	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFDC _H	-
INTE instruction	9	9	-	3D8 _H	000FFF8D8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFF8D4 _H	-
System reserved	11	0B	-	3D0 _H	000FFF8D0 _H	-
System reserved	12	0C	-	3CC _H	000FFF8CCh	-
System reserved	13	0D	-	3C8 _H	000FFF8C8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFF8C4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFF8B8 _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFF8B4 _H	2* ²
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFF8B0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						

Interrupt Factor	Interrupt number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit Free-running timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 1/10/11/20/21/30/31	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/32/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/9/18/19/28/29	44	2C	ICR28	34C _H	000FFF4C _H	28* ³

Interrupt Factor	Interrupt number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348H	000FFF48H	29*1
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344H	000FFF44H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	47	2F	ICR31	340H	000FFF40H	31*1, *4
Clock calibration unit (sub oscillation)						
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/9/10/11/12/13/14/15/16 17/18/19/22/23/26/27/28/29/31						
Clock calibration unit (CR oscillation)	49	31	ICR33	338H	000FFF38H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334H	000FFF34H	34*5
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330H	000FFF30H	35*5
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32CH	000FFF2CH	36*1
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)	53	35	ICR37	328H	000FFF28H	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324H	000FFF24H	38*1
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320H	000FFF20H	39
WG dead timer underflow 0/1/2						
WG dead timer reload 0/1/2						
WG DTTI 0	56	38	ICR40	31CH	000FFF1CH	40
32-bit ICU4 (fetching/measurement)						
Multi-function serial interface ch.11 (transmission completed)						

Interrupt Factor	Interrupt number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
32-bit ICUS (fetching/measurement)						
A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/ 47	57	39	ICR41	318H	000FFF18H	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314H	000FFF14H	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310H	000FFF10H	43
-	60	3C	ICR44	30CH	000FFF0CH	44
-						
Base timer 1 IRQ0						
Base timer 1 IRQ1	61	3D	ICR45	308H	000FFF08H	45
-						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304H	000FFF04H	-
Delay interrupt	63	3F	ICR47	300H	000FFF00H	-
System reserved (Used for REALOS)	64	40	-	2FCH	000FFEFCH	-
System reserved (Used for REALOS)	65	41	-	2F8H	000FFEF8H	-
Used with the INT instruction	66	42	-	2F4H	000FFEF4H	-
	255	FF		000H	000FFC00H	

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

120 Pins

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFFE _H	-
FPU exception	5	5	-	3E8 _H	000FFFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFDC _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFDO _H	-
System reserved	12	0C	-	3CC _H	000FFFCC _H	-
System reserved	13	0D	-	3C8 _H	000FFFCC8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390H	000FFF90H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38CH	000FFF8CH	12*1
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388H	000FFF88H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384H	000FFF84H	14*1
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380H	000FFF80H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37CH	000FFF7CH	16*1
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378H	000FFF78H	17
CAN0	34	22	ICR18	374H	000FFF74H	-
CAN1	35	23	ICR19	370H	000FFF70H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36CH	000FFF6CH	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368H	000FFF68H	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364H	000FFF64H	22*1
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360H	000FFF60H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/20/21/30/31	40	28	ICR24	35CH	000FFF5CH	24*3
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358H	000FFF58H	25*3
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354H	000FFF54H	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350H	000FFF50H	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	34CH	000FFF4CH	28*3

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348H	000FFF48H	29*1
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344H	000FFF44H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)	47	2F	ICR31	340H	000FFF40H	31*1, *4
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)						
Multi-function serial interface ch.9 (reception completed)	48	30	ICR32	33CH	000FFF3CH	32
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/9/10/11/12/13/14/15/16/ 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31						
Clock calibration unit (CR oscillation)	49	31	ICR33	338H	000FFF38H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334H	000FFF34H	34*5
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5						
16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330H	000FFF30H	35*5
32-bit ICU6 (fetching/measurement)						
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)	52	34	ICR36	32CH	000FFF2CH	36*1
32-bit ICU7 (fetching/measurement)						
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)	53	35	ICR37	328H	000FFF28H	37
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	54	36	ICR38	324H	000FFF24H	38*1
WG dead timer underflow 0/1/2						
WG dead timer reload 0/1/2						
WG DTTI 0	55	37	ICR39	320H	000FFF20H	39
32-bit ICU4 (fetching/measurement)						
Multi-function serial interface ch.11 (transmission completed)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
32-bit ICUS (fetching/measurement)						
A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318H	000FFF18H	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314H	000FFF14H	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310H	000FFF10H	43
-	60	3C	ICR44	30CH	000FFF0CH	44
Base timer 1 IRQ0						
Base timer 1 IRQ1			ICR45	308H	000FFF08H	45
-	61	3D				
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304H	000FFF04H	-
Delay interrupt	63	3F	ICR47	300H	000FFF00H	-
System reserved (Used for REALOS)	64	40	-	2FCH	000FFEFCH	-
System reserved (Used for REALOS)	65	41	-	2F8H	000FFEF8H	-
Used with the INT instruction	66	42		2F4H	000FFEF4H	
			-			-
	255	FF		000H	000FFC00H	

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

144 Pins

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFECH	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFDC _H	-
INTE instruction	9	9	-	3D8 _H	000FFF8D8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFF8D4 _H	-
System reserved	11	0B	-	3D0 _H	000FFF8D0 _H	-
System reserved	12	0C	-	3CC _H	000FFF8C8 _H	-
System reserved	13	0D	-	3C8 _H	000FFF8C4 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFF8C0 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFF8B8 _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFF8B4 _H	2* ²
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFF8B0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis	36	24	ICR20	36C _H	000FFF6C _H	-
CAN2						
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/20/21/30/40/41	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 6/7/16/17/26/27/36/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	34C _H	000FFF4C _H	28* ³

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348H	000FFF48H	29* ¹
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344H	000FFF44H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	47	2F	ICR31	340H	000FFF40H	31* ^{1, *4}
Clock calibration unit (sub oscillation)						
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	33CH	000FFF3CH	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338H	000FFF38H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334H	000FFF34H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330H	000FFF30H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU 6 (fetching/measurement)	52	34	ICR36	32CH	000FFF2CH	36* ¹
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)	53	35	ICR37	328H	000FFF28H	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324H	000FFF24H	38* ¹
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320H	000FFF20H	39
WG dead timer underflow 0 / 1 / 2						
WG dead timer reload 0 / 1 / 2						
WG DTTI 0	56	38	ICR40	31CH	000FFF1CH	40
32-bit ICU4 (fetching/measurement)						
Multi-function serial interface ch.11 (transmission completed)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
32-bit ICU5 (fetching/measurement)						
A/D converter	57	39	ICR41	318H	000FFF18H	41
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47						
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314H	000FFF14H	42
32-bit OCU8/9 (match)	59	3B	ICR43	310H	000FFF10H	43
Base timer 0 IRQ0						
Base timer 0 IRQ1	60	3C	ICR44	30CH	000FFF0CH	44
Base timer 1 IRQ0						
Base timer 1 IRQ1						
-						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304H	000FFF04H	-
Delay interrupt	63	3F	ICR47	300H	000FFF00H	-
System reserved (Used for REALOS)	64	40	-	2FCH	000FFEFCH	-
System reserved (Used for REALOS)	65	41	-	2F8H	000FFEF8H	-
Used with the INT instruction	66	42	-	2F4H	000FFEF4H	-
			-			-
	255	FF		000H	000FFC00H	

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

176 Pins

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3ECh	000FFFECh	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFDC _H	-
INTE instruction	9	9	-	3D8 _H	000FFF8D8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFF8D4 _H	-
System reserved	11	0B	-	3D0 _H	000FFF8D0 _H	-
System reserved	12	0C	-	3CC _H	000FFF8C8 _H	-
System reserved	13	0D	-	3C8 _H	000FFF8C8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFF8C4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFF8B _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFF8B4 _H	2* ²
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFF8B0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44/45	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 6/7/16/17/26/27/36/37/46/47	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	34C _H	000FFF4C _H	28* ³

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ , * ⁴
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31						
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)						
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328 _H	000FFF28 _H	37
32-bit ICU8 (fetching/measurement)						
Multi-function serial interface ch.11 (reception completed)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)						
WG dead timer underflow 0/1/2	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer reload 0/1/2						
WG DTTI 0						
32-bit ICU4 (fetching/measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11 (transmission completed)						

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN
	Decimal	Hexa Decimal				
32-bit ICUS (fetching/measurement)						
A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/ 47	57	39	ICR41	318 _H	000FFF18 _H	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 0 IRQ1						
Base timer 1 IRQ0	61	3D	ICR45	308 _H	000FFF08 _H	45
Base timer 1 IRQ1						
-						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 _H	000FFF04 _H	-
Delay interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFCH	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFEF8H	-
Used with the INT instruction	66	42	-	2F4 _H	000FFEF4H	-
			-			-
	255	FF		000H	000FFC00H	

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

11. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1,*2	V _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	
Analog power supply voltage *1,*2	AV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	AV _{RH} ≤ AV _{CC} ≤ V _{CC}
Analog reference voltage *1	AV _{RH}	V _{SS} -0.3	V _{SS} +6.0	V	AV _{RH} ≤ AV _{CC}
Input voltage *1	V _I	V _{SS} -0.3	V _{CC} +0.3	V	
Analog pin input voltage *1	V _{IA5}	V _{SS} -0.3	V _{CC} +0.3	V	
Output voltage *1	V _O	V _{SS} -0.3	V _{CC} +0.3	V	
Maximum clamp current	I _{CLAMP}	-	4.0	mA	*6
Total maximum clamp current	Σ I _{CLAMP}	-	20	mA	*6
"L" level maximum output current *3	I _{OL1}	-	15	mA	
	I _{OL2}	-	30	mA	
"L" level average output current *4	I _{OLAV1}	-	4	mA	*9
	I _{OLAV2}	-	12	mA	*10
"L" level total output current *5	ΣI _{OL1}	-	100	mA	
	ΣI _{OL2}	-	120	mA	
"H" level maximum output current*3	I _{OH1}	-	-15	mA	
	I _{OH2}	-	-30	mA	
"H" level average output current*4	I _{OHAV1}	-	-4	mA	*9
	I _{OHAV2}	-	-12	mA	*10
"H" level total output current *5	ΣI _{OH1}	-	-100	mA	
	ΣI _{OH2}	-	-120	mA	
Power consumption	P _D	-	882	mW	*8
		-	675	mW	*8
Operating temperature	T _A	-40	+105	°C	
		-40	+125	°C	*7
Storage temperature	T _{STG}	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0 V

*2: Caution must be taken that AV_{CC}, AVR_H do not exceed V_{CC} upon power-on and under other circumstances.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

- *6:
- Corresponding pins: all general-purpose ports except P035, 041, 093, 122.
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
 - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
 - Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
 - Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
 - Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
 - Do not leave + B input pins open.

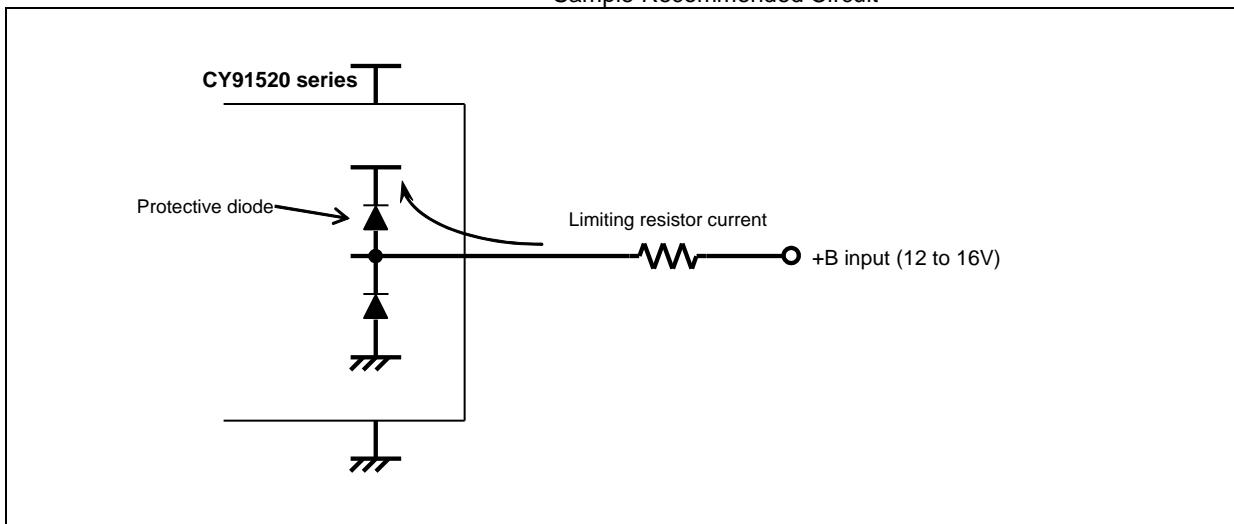
*7: When it is used under this condition, contact your sales representative.

*8: It is a standard when four-layer substrate is used.

*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.

*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample Recommended Circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} , AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0 V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3 V is used)
		2.7	5.5	V	Operation guarantee range ^{*1}
Smoothing capacitor ^{*2}	C_S	4.7 (tolerance within $\pm 50\%$)		μF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	$^{\circ}C$	
		-40	+125	$^{\circ}C$	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.

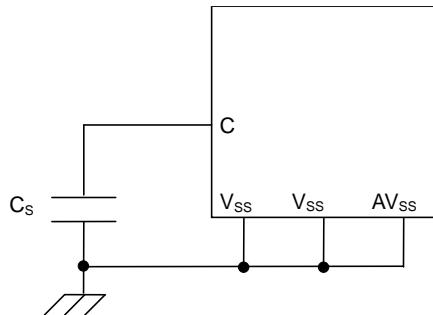
The initial detection voltage of the external low voltage detection is $2.8 V \pm 8\%$ ($2.576 V$ to $3.024 V$). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the

minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

*2: See the following diagram for details on the connection of smoothing capacitor Cs.

*3: When it is used under this condition, contact your sales representative.

· C Pin Connection Diagram



<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

DC Characteristics

(T_A: -40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CC5}	V _{CC}	Operating frequency F _{CP} = 80 MHz, F _{CPP} = 40 MHz, at normal operation	-	60	80	mA	
			Operating frequency F _{CP} = 80 MHz, F _{CPP} = 40 MHz, at Flash write	-	70	90	mA	
			Operating frequency F _{CP} = 80 MHz, F _{CPP} = 40 MHz, at Flash erase	-	70	90	mA	
			Operating frequency F _{CP} = 64 MHz, F _{CPP} = 32 MHz, at normal operation	-	54	71	mA	
			Operating frequency F _{CP} = 64 MHz, F _{CPP} = 32 MHz, at Flash write	-	64	81	mA	
			Operating frequency F _{CP} = 64 MHz, F _{CPP} = 32 MHz, at Flash erase	-	64	81	mA	
			Operating frequency F _{CP} = 48 MHz, F _{CPP} = 24 MHz, at normal operation	-	46	62	mA	
			Operating frequency F _{CP} = 48 MHz, F _{CPP} = 24 MHz, at Flash write	-	56	72	mA	
			Operating frequency F _{CP} = 48 MHz, F _{CPP} = 24 MHz, at Flash erase	-	56	72	mA	
	I _{CCS5}		Operating frequency F _{CP} = 80 MHz, F _{CPP} = 40 MHz, at CPU sleep mode	-	45	61	mA	
	I _{CCBS5}		Operating frequency F _{CP} = 80 MHz, F _{CPP} = 40 MHz, at bus sleep mode	-	23	51	mA	
I _{CC5}	I _{CC5}	Watch mode	When using crystal 4 MHz T _A = +25 °C*	-	1500	2610	μA	
			When using built-in CR clock 50 kHz T _A = +25 °C*	-	450	2000		
			When using sub clock 32 kHz T _A = +25 °C*	-	460	2000		
			Stop mode T _A = +25 °C*	-	450	2000	μA	
	I _{CC52}	Watch mode (power off)	When using crystal 4 MHz T _A = +25 °C*	-	1100	1300	μA	LVD/ RTC operation, Backup RAM 8 KB retention
			When using built-in CR clock 50 kHz, T _A = +25 °C*	-	77	267		
			When using sub clock 32 kHz T _A = +25 °C*	-	100	285		
	I _{CC52}	Stop mode (power off)	T _A = +25 °C*	-	74	265	μA	Backup RAM 8 KB retention

(T_A : -40 °C to +125 °C, $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\% / 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
Power supply current	Icc5	VCC	Operating frequency $F_{CP} = 80 \text{ MHz}$, $F_{CPP} = 40 \text{ MHz}$, at normal operation	-	60	102	mA		
			Operating frequency $F_{CP} = 80 \text{ MHz}$, $F_{CPP} = 40 \text{ MHz}$, at Flash write	-	70	115	mA		
			Operating frequency $F_{CP} = 80 \text{ MHz}$, $F_{CPP} = 40 \text{ MHz}$, at Flash erase	-	70	115	mA		
			Operating frequency $F_{CP} = 64 \text{ MHz}$, $F_{CPP} = 32 \text{ MHz}$, at normal operation	-	54	92	mA		
			Operating frequency $F_{CP} = 64 \text{ MHz}$, $F_{CPP} = 32 \text{ MHz}$, at Flash write	-	64	105	mA		
			Operating frequency $F_{CP} = 64 \text{ MHz}$, $F_{CPP} = 32 \text{ MHz}$, at Flash erase	-	64	105	mA		
			Operating frequency $F_{CP} = 48 \text{ MHz}$, $F_{CPP} = 24 \text{ MHz}$, at normal operation	-	46	82	mA		
			Operating frequency $F_{CP} = 48 \text{ MHz}$, $F_{CPP} = 24 \text{ MHz}$, at Flash write	-	56	95	mA		
			Operating frequency $F_{CP} = 48 \text{ MHz}$, $F_{CPP} = 24 \text{ MHz}$, at Flash erase	-	56	95	mA		
	Iccs5		Operating frequency $F_{CP} = 80 \text{ MHz}$, $F_{CPP} = 40 \text{ MHz}$, at CPU sleep mode	-	45	82	mA		
	Iccbs5		Operating frequency $F_{CP} = 80 \text{ MHz}$, $F_{CPP} = 40 \text{ MHz}$, at bus sleep mode	-	23	72	mA		
	Icct5		Watch mode	When using crystal 4 MHz $T_A = +25 \text{ }^\circ\text{C}^*$	-	1500	2610	μA	
	When using built-in CR clock 50 kHz $T_A = +25 \text{ }^\circ\text{C}^*$			-	450	2000			
	When using sub clock 32 kHz $T_A = +25 \text{ }^\circ\text{C}^*$			-	460	2000			
	Icc5		Stop mode	$T_A = +25 \text{ }^\circ\text{C}^*$	-	450	2000	μA	
	Icct52		Watch mode (power off)	When using crystal 4 MHz $T_A = +25 \text{ }^\circ\text{C}^*$	-	1100	1300	μA	
				When using built-in CR clock 50 kHz, $T_A = +25 \text{ }^\circ\text{C}^*$	-	77	267		
				When using sub clock 32 kHz $T_A = +25 \text{ }^\circ\text{C}^*$	-	100	285		
	Icc52		Stop mode (power off)	$T_A = +25 \text{ }^\circ\text{C}^*$	-	74	265	μA	
								Backup RAM 8 KB retention	

(T_A : -40 °C to +125 °C, $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\% / V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	All input pins	$V_{CC} = AV_{CC} = 5.5 \text{ V}$ $V_{SS} < V_I < V_{CC}$	-5	-	5	μA	
Input capacitance 1	C_{IN1}	Other than VCC,VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R_{UP1}	RSTX, NMIX	$V_{CC} = 5.0 \text{ V} \pm 10\%$	25	-	100	kΩ	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	45	-	140		
	R_{UP2}	P073,074 076,077	$V_{CC} = 5.0 \text{ V} \pm 10\%$	25	-	60		
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	33	-	90		
	R_{UP3}	Port pin other than P035, 041,073,074, 076,077,093, 122	$V_{CC} = 5.0 \text{ V} \pm 10\%$	25	-	100	kΩ	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	45	-	140		
"H" level output voltage	V_{OH1}	Normal output pin	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -4.0 \text{ mA}$	V_{CC} -0.5	-	V_{CC}	V	
			$V_{CC} = 3.0 \text{ V}$ $I_{OH} = -2.0 \text{ mA}$					
	V_{OH2}	P073,074,076, 077	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -3.0 \text{ mA}$	V_{CC} -0.5	-	V_{CC}	V	$I^2\text{C}$ pin output
	V_{OH3}	P103 to 106	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -12.0 \text{ mA}$	V_{CC} -0.5	-	V_{CC}	V	
			$V_{CC} = 3.0 \text{ V}$ $I_{OH} = -8.0 \text{ mA}$					
"L" level output voltage	V_{OL1}	Normal output pin	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 4.0 \text{ mA}$	0	-	0.4	V	
			$V_{CC} = 3.0 \text{ V}$ $I_{OL} = 2.0 \text{ mA}$					
	V_{OL2}	P073,074,076, 077	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 3.0 \text{ mA}$	0	-	0.4	V	$I^2\text{C}$ pin output
	V_{OL3}	P103 to 106	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 12.0 \text{ mA}$	0	-	0.4	V	
			$V_{CC} = 3.0 \text{ V}$ $I_{OL} = 8.0 \text{ mA}$					

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
"H" level input voltage	V _{IH1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	0.7× V _{cc}	-	V _{cc}	V		
		V _{IH3}	Port other than V _{IH1}	Automotive input level	0.8× V _{cc}	-	V _{cc}	V	
		V _{IH5}	RSTX,NMIX,MD 0,MD1	CMOS hysteresis input level	0.8× V _{cc}	-	V _{cc}	V	
		V _{IHT}	DEBUGIF	TTL input level	2	-	V _{cc}	V	
"L" level input voltage	V _{IL1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	V _{ss}	-	0.3× V _{cc}	V		
		V _{IL3}	Port other than V _{IH1}	Automotive input level	V _{ss}	-	0.5× V _{cc}	V	
		V _{IL5}	RSTX,NMIX,MD 0,MD1	CMOS hysteresis input level	V _{ss}	-	0.2× V _{cc}	V	
		V _{ILT}	DEBUGIF	TTL input level	V _{ss}	-	0.8	V	

*: It is a standard in BRAMSC (Backup RAM sleep control bit) = 1 (Enter the state of the sleep at the standby mode) condition.

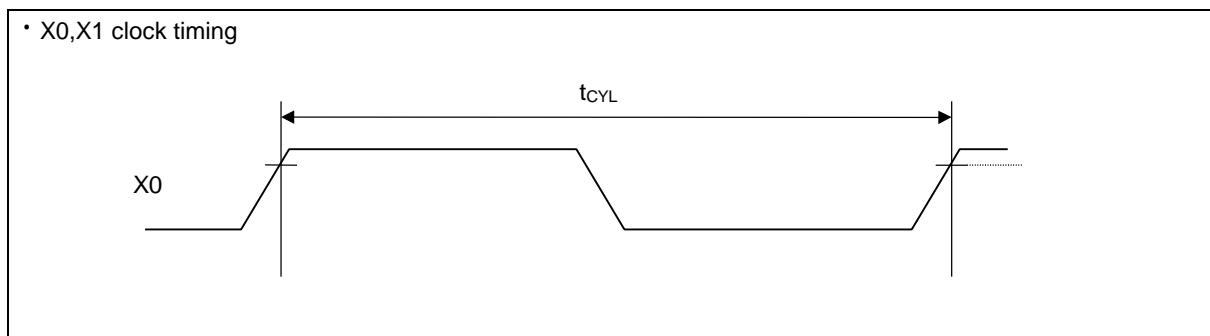
AC Characteristics
(1) Main Clock Timing

(TA: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 % / V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

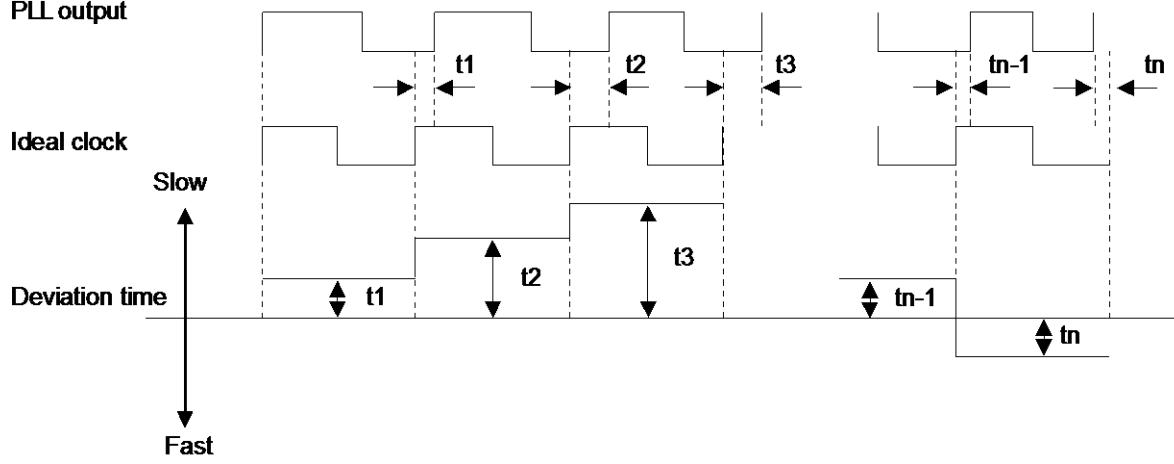
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _C	X0, X1		-	4	16	MHz	
Source oscillation clock cycle time	t _{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency* ¹	F _{CP}	-		2	-	80	MHz	CPU clock
	F _{CPP}			1		40		Peripheral bus clock
	F _{CPT}			1		40		External bus clock (When V _{CC} = 5.0 V is used)* ²
				1	-	32		External bus clock (When V _{CC} = 3.3 V is used)
Internal operating clock cycle time* ¹	t _{CP}	-		12.5	-	500	ns	CPU clock
	t _{CPP}			25		1000		Peripheral bus clock
	t _{CPT}			25		1000		External bus clock (When V _{CC} = 5.0 V is used)
				31.25	-	1000		External bus clock (When V _{CC} = 3.3 V is used)
CAN PLL jitter (during lock)	t _{PJ}	-		-10	-	10	ns	F _{CP} = 80 MHz (4 MHz multiplied by 20)
Built-in CR oscillation frequency	F _{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

*2: Please use it with external load capacity 12 pF or less for V_{CC} = 3.3 V ± 0.3 V (40 MHz operation).



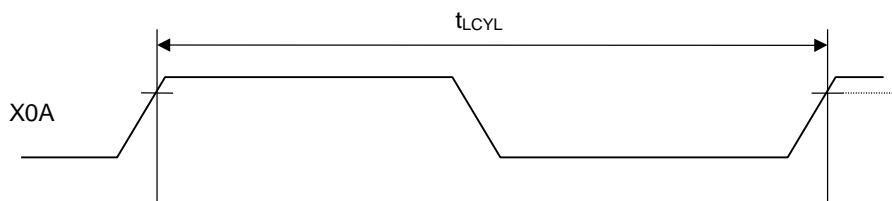
- CAN PLL jitter
Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.

PLL output


(1-2) Sub clock timing
 $(T_A: -40^\circ\text{C} \text{ to } +125^\circ\text{C}, V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%, V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V})$

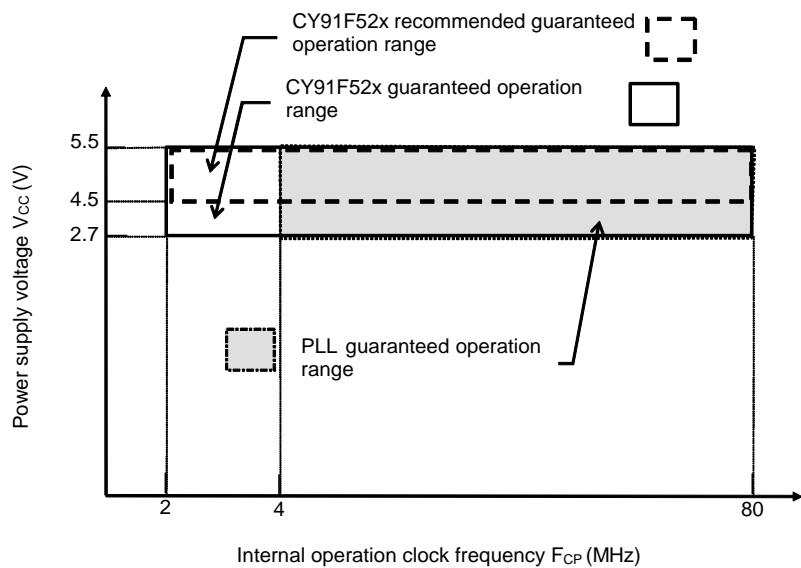
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A		-	30.52	-	μs	

- X0A,X1A clock timing



- Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

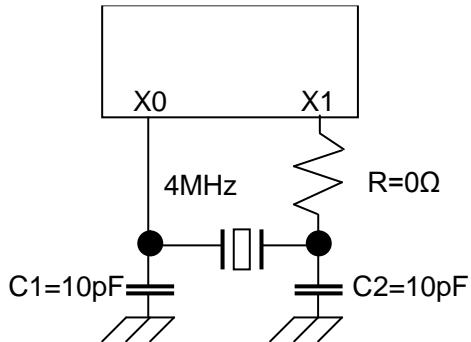


Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Oscillation clock frequency vs. Internal operation clock frequency

Main Clock	Internal operation clock frequency								
	PLL clock								
	Multipled by 1	Multipled by 2	Multipled by 3	Multipled by 4	...	Multipled by 19	Multipled by 20		
Oscillation clock frequency	4 MHz	2 MHz	4 MHz	8 MHz	12 MHz	16 MHz	...	76 MHz	80 MHz

- Example of oscillation circuit



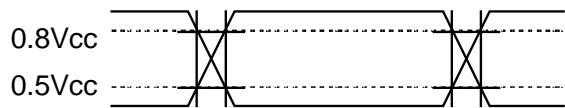
Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20 ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.

Design your print circuit board so that the oscillator can start oscillation within 20 ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

AC characteristics are specified by the following measurement reference voltage values.

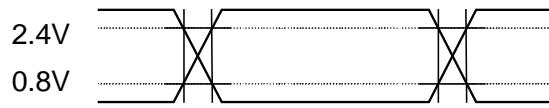
● Input Signal Waveform

Hysteresis Input Pin (Automotive)

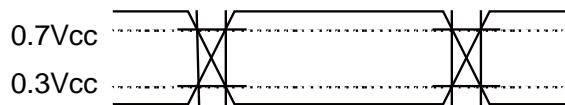


● Output Signal Waveform

Output Pin



Hysteresis Input Pin (CMOS schmitt)



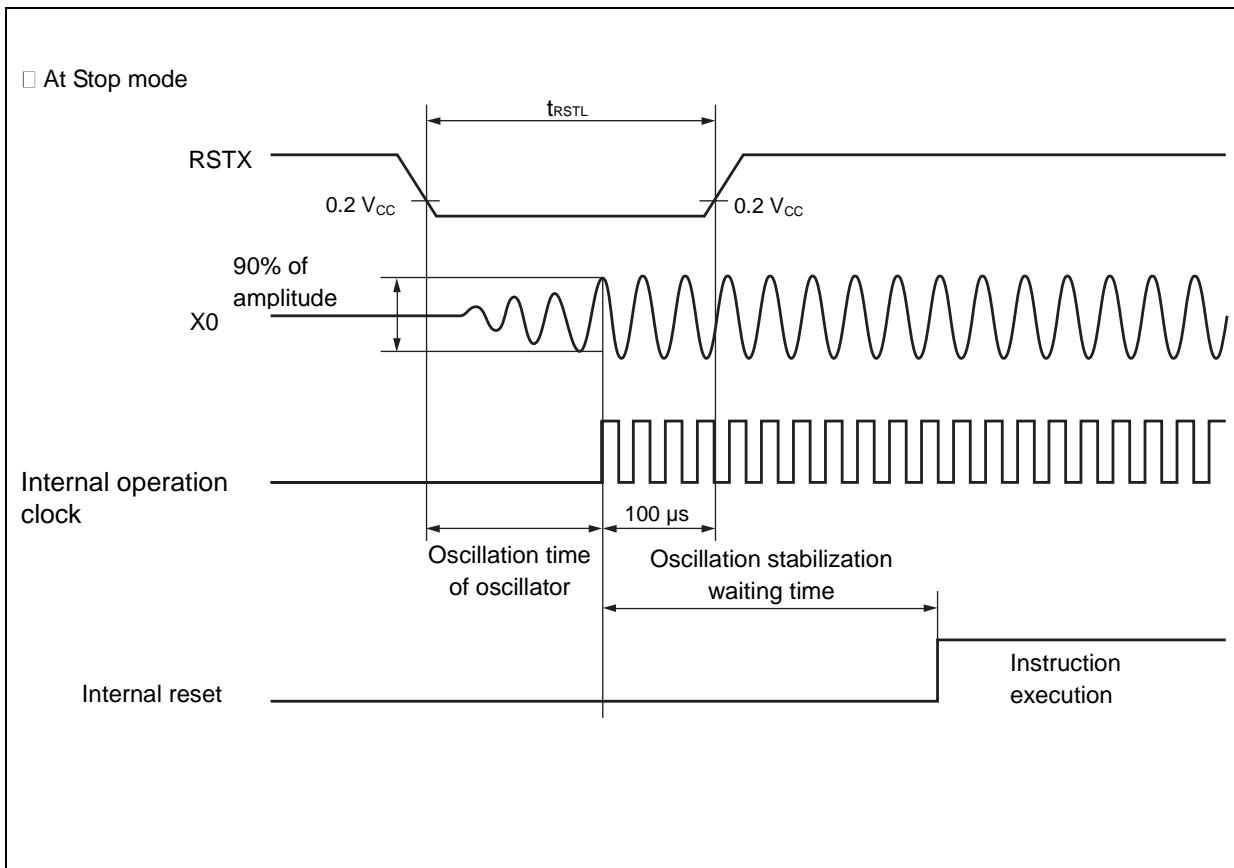
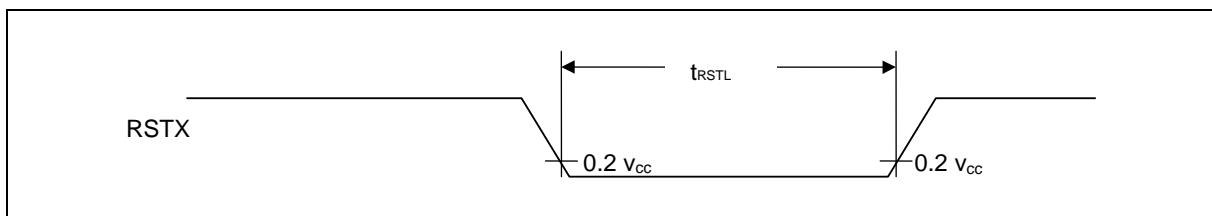
(2) Reset Input

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{RSTL}	RSTX	–	10	–	μs	When normal operation
				Oscillation time of oscillator* +100	–	μs	At Stop mode At Power-on ^{*2}
				100	–	μs	At Watch mode
				1	–	μs	
Width for reset input removal							

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90 %. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using CY91F52xxxD or CY91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.



(3) Power-on Conditions

(3-1) [CY9152xxxB/CY9152xxxC/CY9152xxxD]

(T_A : -40 °C to +125 °C, $V_{SS} = 0.0$ V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	—	V_{CC}	—	2.024	2.2	2.376	V	
Level detection hysteresis width	—	V_{CC}	—	—	100	—	mV	
Level detection time	—	—	—	—	—	30	μs	*1
Power off time	t_{OFF}	V_{CC}	—	50	—	—	ms	*2
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2 V to 2.376 V	—	—	4	mV/μs	*3
C pin voltage at Power-on	—	C	—	—	—	60	mV	*4

*1: This spec is at 4 mV/μs of power ramp rate. If the power ramp rate is faster than 4mV/μs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: V_{CC} must be held below 0.2 V for a minimum period of t_{OFF} .

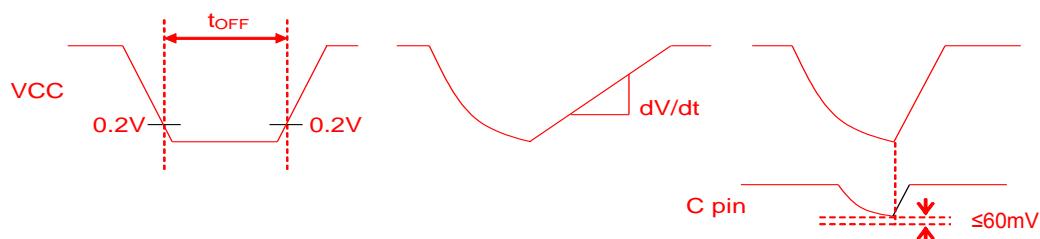
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when V_{CC} is turned on again.

Note:

When using CY91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use CY91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

- Power off time, Power ramp rate, C pin voltage at Power-on



(3-2) [CY9152xxxE]

(T_A : -40 °C to +125 °C, $V_{SS} = 0.0$ V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	V_{CC}	-	2.024	2.2	2.376	V	
Level detection hysteresis width	-	V_{CC}	-	-	100	-	mV	
Level detection time	-	-	-	-	-	30	μs	*1
Power off time	t_{OFF1}	V_{CC}	$V_{CC} \leq 0.2$ V	50	-	-	ms	*2
	t_{OFF2}	V_{CC}	$V_{CC} \leq 1.3$ V	100	-	-	μs	*4
Power ramp rate	dV/dt	V_{CC}	V_{CC} : 0.2 V to 2.376 V ($t_{OFF1} < 50$ ms)	-	-	50	mV/μs	*3
	dV/dt	V_{CC}	V_{CC} : 1.3 V to 2.376 V ($t_{OFF2} \geq 100$ μs)	-	-	1000	mV/μs	*4
C pin voltage at Power-on	-	C	-	-	-	60	mV	*5
Maximum ramp rate guaranteed to not generate power-on reset	$ dV/dt $	V_{CC}	V_{CC} : Between 2.4 V and 4.5 V	-	-	50	mV/μs	*6

*1: The specified level detection time applies only for power ramp rate of 1000 mV/μs or less.

*2: V_{CC} must be held below 0.2 V for a minimum period of t_{OFF1} .

*3: Power-on can detect by satisfying power ramp rate when t_{OFF1} is not satisfied.

*4: V_{CC} must be held below 1.3 V for a minimum period of t_{OFF2} .

Power ramp rate must be 1000 mV/μs or less from 1.3 V to 2.376 V.

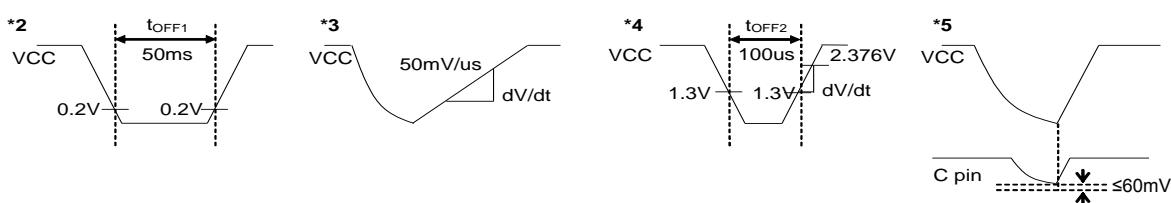
Power-on can detect by satisfying power ramp rate and power off time.

*5: C-pin voltage is below 60 mV when V_{CC} is turned on again.

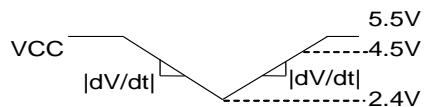
*6: This specification is specified the power supply fluctuation after power on detection. When V_{CC} voltage is between 2.4 V and 4.5 V, the power supply fluctuation is below 50 mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5 V and 5.5 V.

Note: When using CY91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

- Power off time, Power ramp rate, C pin voltage at Power-on



- Maximum ramp rate guaranteed to not generate power-on reset



(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR : MD0 = 0, SMR: SCINV = 0, SCR:SPI = 0

(TA: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V±0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	
				Min	Max			
Serial clock cycle time	t _{SCYC}	SCK0 to SCK11	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L = 50 pF	
SCK ↓ → SOT delay time	t _{SL0VI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns		
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns		
Valid SIN → SCK ↑ setup time	t _{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns		
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns		
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns		
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK11	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L = 50 pF	
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns		
SCK ↓ → SOT delay time	t _{SL0VE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns		
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns		
Valid SIN → SCK ↑ setup time	t _{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns		
SCK ↑ → Valid SIN hold time	t _{SHIXE}			20	-	ns		
SCK fall time	t _F	SCK0 to SCK11		-	5	ns		
SCK rise time	t _R	SCK0 to SCK11		-	5	ns		

Notes:

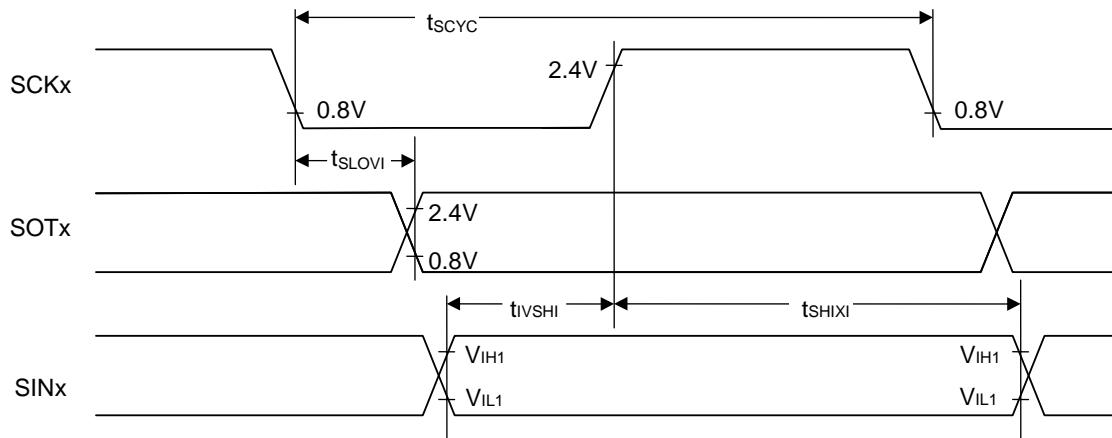
AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

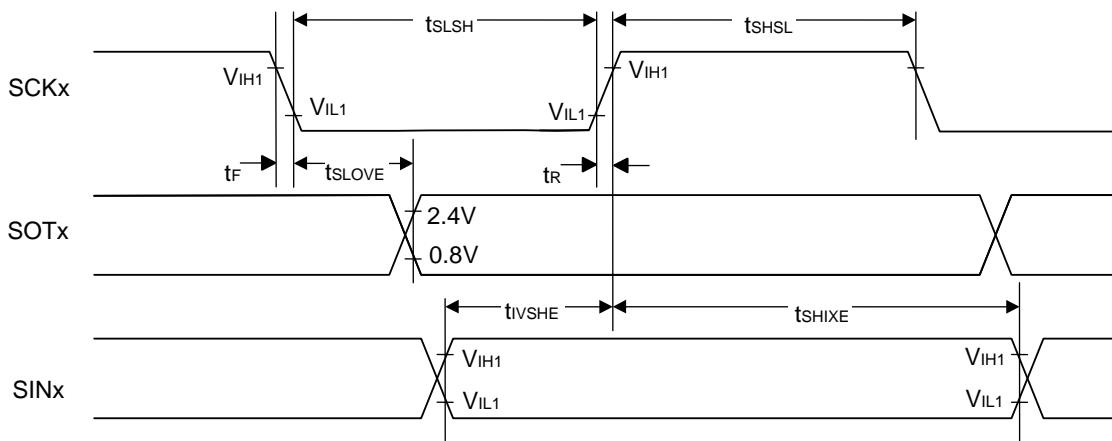
The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

See Hardware Manual for details.

- Internal shift clock mode



- External shift clock mode



(4-1-2) Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR : MD0 = 0, SMR: SCINV = 1, SCR:SPI = 0

(TA: -40 °C to +125 °C, V_{cc} = AV_{cc} = 5.0 V ± 10 %/V_{cc} = AV_{cc} = 3.3 V ± 0.3 V, V_{ss} = AV_{ss} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	
				Min	Max			
Serial clock cycle time	t _{SCYC}	SCK0 to SCK11	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L = 50 pF	
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns		
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns		
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns		
		SCK3 , SCK4 SIN3, SIN4		300	-	ns		
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns		
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK11	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L = 50 pF	
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns		
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns		
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns		
Valid SIN → SCK ↓ setup time	t _{IVSLE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns		
SCK ↓ → Valid SIN hold time	t _{SLIXE}			20	-	ns		
SCK fall time	t _F	SCK0 to SCK11	-	-	5	ns		
SCK rise time	t _R	SCK0 to SCK11		-	5	ns		

Notes:

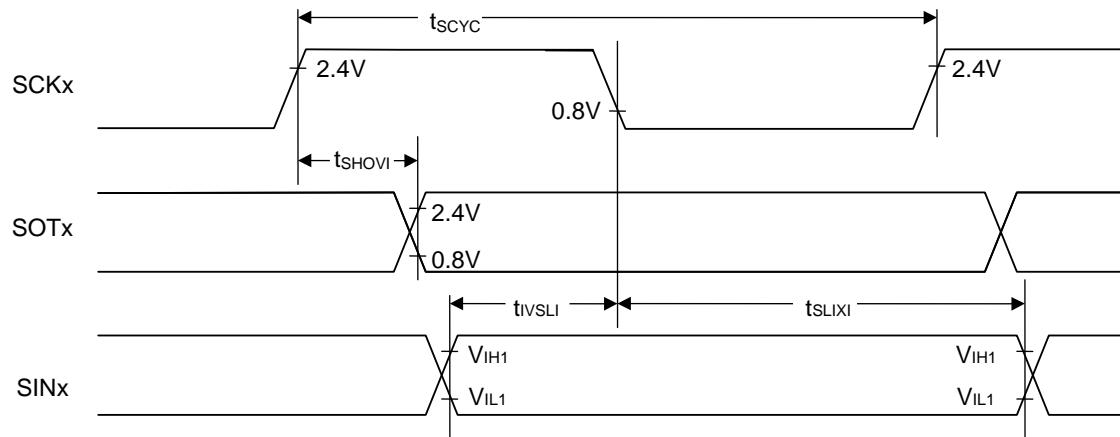
AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

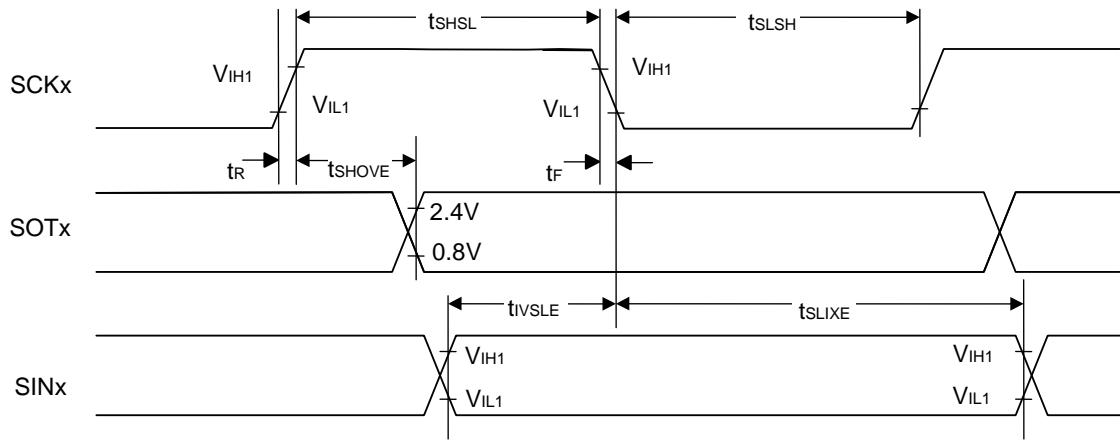
The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

See Hardware Manual for details.

□ Internal shift clock mode



• External shift clock mode



(4-1-3) Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 0, SMR:SCINV = 0, SCR:SPI = 1
(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	
				Min	Max			
Serial clock cycle time	t _{SCYC}	SCK0 to SCK11	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L = 50 pF	
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns		
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns		
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns		
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns		
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns		
SOT→SCK↓ delay time	t _{SOVLI}	SCK0 to SCK11 SOT0 to SOT11		2t _{CPP} -30	-	ns		
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK11	-	t _{CPP} + 10	-	ns	External shift clock mode output pin: C _L = 50 pF	
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns		
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns		
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns		
Valid SIN → SCK ↓ setup time	t _{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns		
SCK ↓ → Valid SIN hold time	t _{SLIXE}			20	-	ns		
SCK fall time	t _F	SCK0 to SCK11		-	5	ns		
SCK rise time	t _R	SCK0 to SCK11		-	5	ns		

Notes:

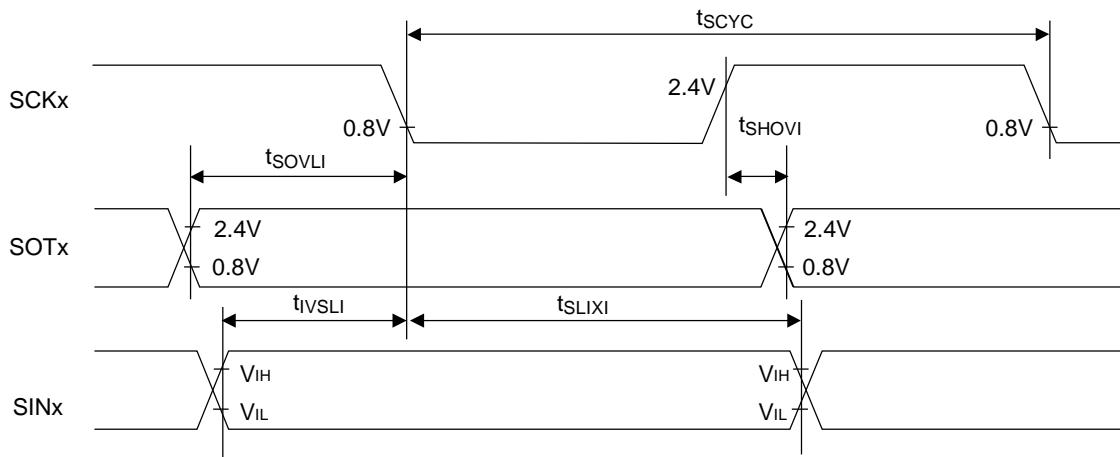
AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

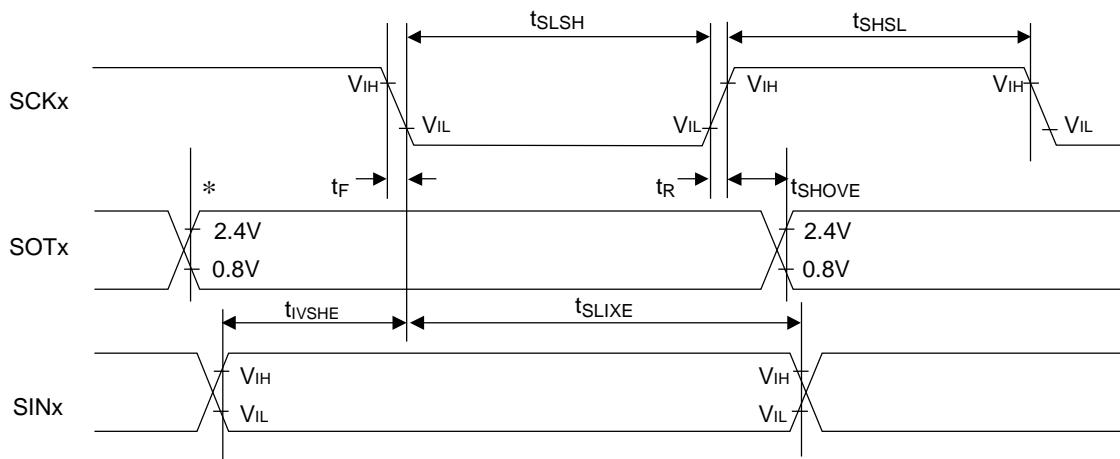
The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

See Hardware Manual for details.

□ Internal shift clock mode



• External shift clock mode



*: It writes in the TDR register and, then, it changes.

(4-1-4) Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 0, SMR:SCINV = 1, SCR:SPI = 1
(T_A: -40 °C to +125 °C, V_{CC} = A V_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	
				Min	Max			
Serial clock cycle time	t _{SCYC}	SCK0 to SCK11	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L = 50 pF	
SCK↓→ SOT delay time	t _{SLLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns		
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns		
Valid SIN → SCK↑setup time	t _{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns		
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns		
SCK↑→ Valid SIN hold time	t _{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns		
SOT→SCK↑ delay time	t _{SOVHI}	SCK0 to SCK11 SOT0 to SOT11		2t _{CPP} -30	-	ns		
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK11	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L = 50 pF	
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns		
SCK↓→ SOT delay time	t _{SLLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns		
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns		
Valid SIN → SCK↑setup time	t _{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns		
SCK↑→ Valid SIN hold time	t _{SHIXE}			20	-	ns		
SCK fall time	t _F	SCK0 to SCK11		-	5	ns		
SCK rise time	t _R	SCK0 to SCK11		-	5	ns		

Notes:

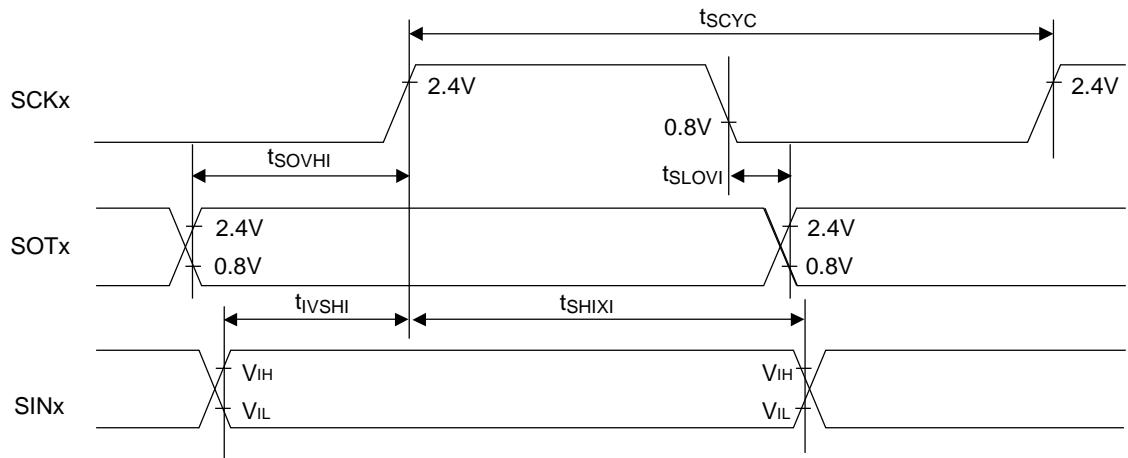
AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

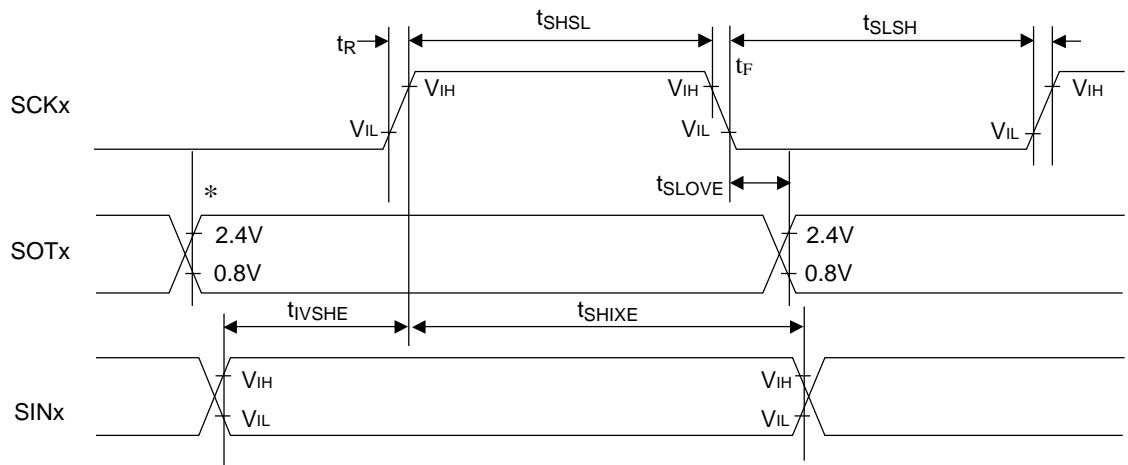
The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

See Hardware Manual for details.

- Internal shift clock mode



- External shift clock mode



*: It writes in the TDR register and, then, it changes.

(4-1-5) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,

When Serial chip select is used : SCSCR:CSEN = 1,

Serial clock output mark level "H" : SMR,SCSFR:SCINV = 0,

Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL = 1

(T_A : -40 °C to +125 °C, $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\% / V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	tcssi	SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	tcssu-50 *1	tcssu+0 *1	ns	Internal shift clock mode output pin : $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		tcssu-50 *1	tcssu+300 *1	ns	
SCK↑→SCS↑ hold time	tcsdi	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		tcsdi-10 *2	tcsdi+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		tcsdi-300 *2	tcsdi+50 *2	ns	
SCS deselect time	tcsdi	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		tcسد-50 *3	tcسد+50 *3	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t _{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK↑→SCS↑ hold time		SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		+0	-	ns	
SCS deselect time		SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		3t _{CPP} +30	-	ns	
SCS↓→SOT delay time		SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2 , SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↑→SOT delay time	t _{DSE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK↓→SCS↓ clock switch time	t _{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50	ns	

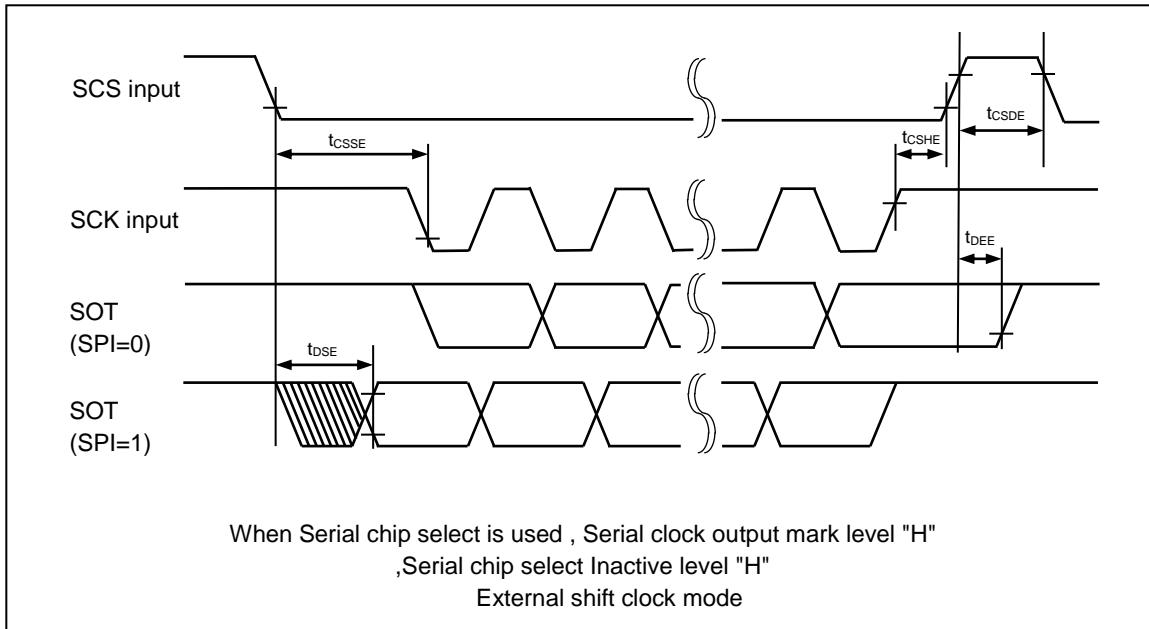
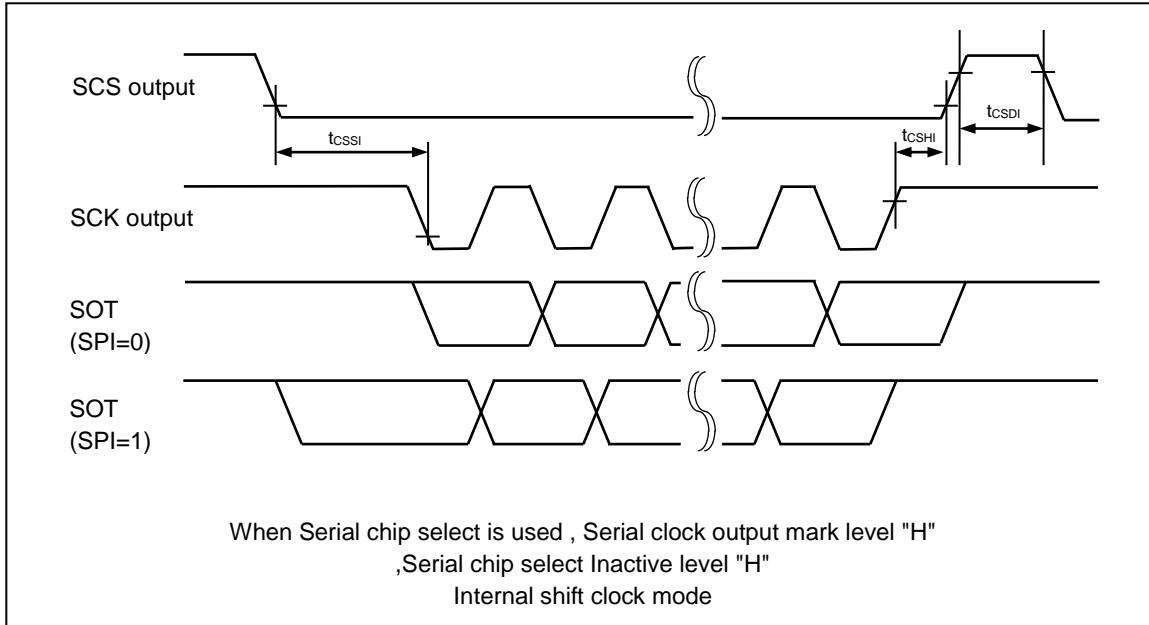
*1: t_{CSsu} = SCSTR:CSSU7-0xSerial chip select timing operating clock

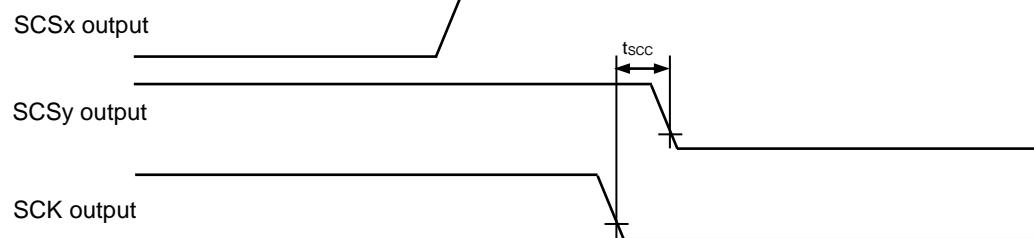
*2: t_{CSHD} = SCSTR:CSHD7-0xSerial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS15-0xSerial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.





When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-6) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,

When Serial chip select is used : SCSCR:CSEN = 1,

Serial clock output mark level "L" : SMR,SCSFR:SCINV = 1,

Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL = 1

(T_A : -40 °C to +125 °C, $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\% / V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t _{CSSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CSSSI-50} *1	t _{CSSSI+0} *1	ns	Internal shift clock mode output pin : $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSSSI-50} *1	t _{CSSSI+300} *1	ns	
SCK↓→SCS↑ hold time	t _{CSSH}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSSH-10} *2	t _{CSSH+50} *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSSH-300} *2	t _{CSSH+50} *2	ns	
SCS deselect time	t _{CSDS}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSDS-50} *3	t _{CSDS+50} *3	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t _{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK↓→SCS↑ hold time	t _{CSHE}	+0		-	ns		
SCS deselect time	t _{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		3t _{CPP} +30	-	ns	
SCS↓→SOT delay time	t _{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11	-	-	40	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↑→SOT delay time	t _{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK↑→SCS↓ clock switch time	t _{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50	ns	

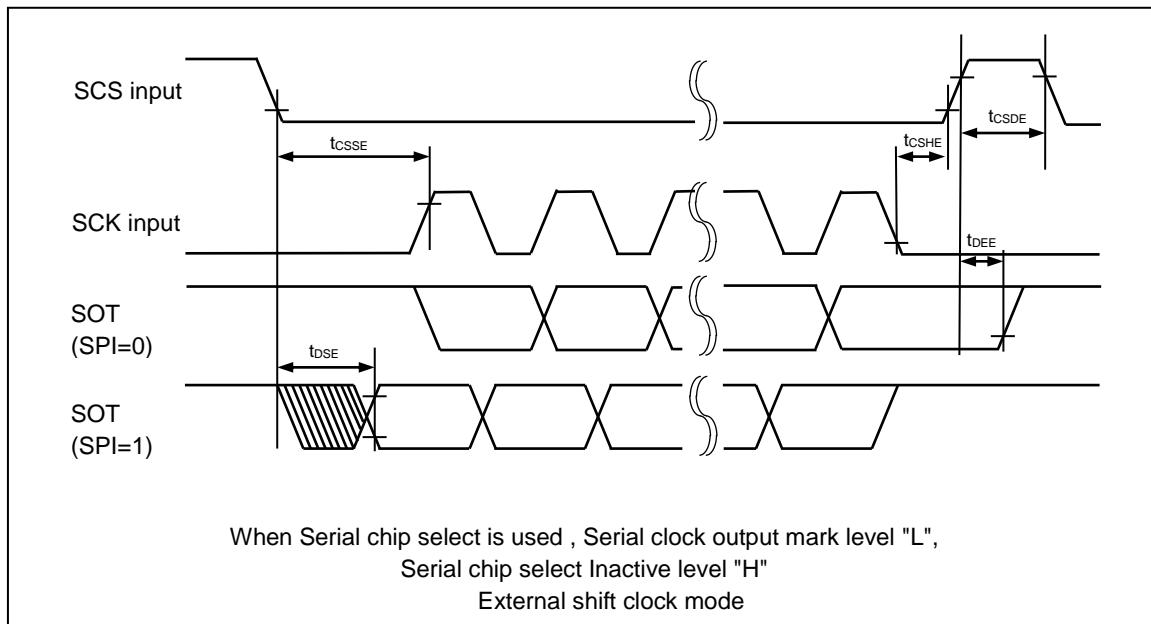
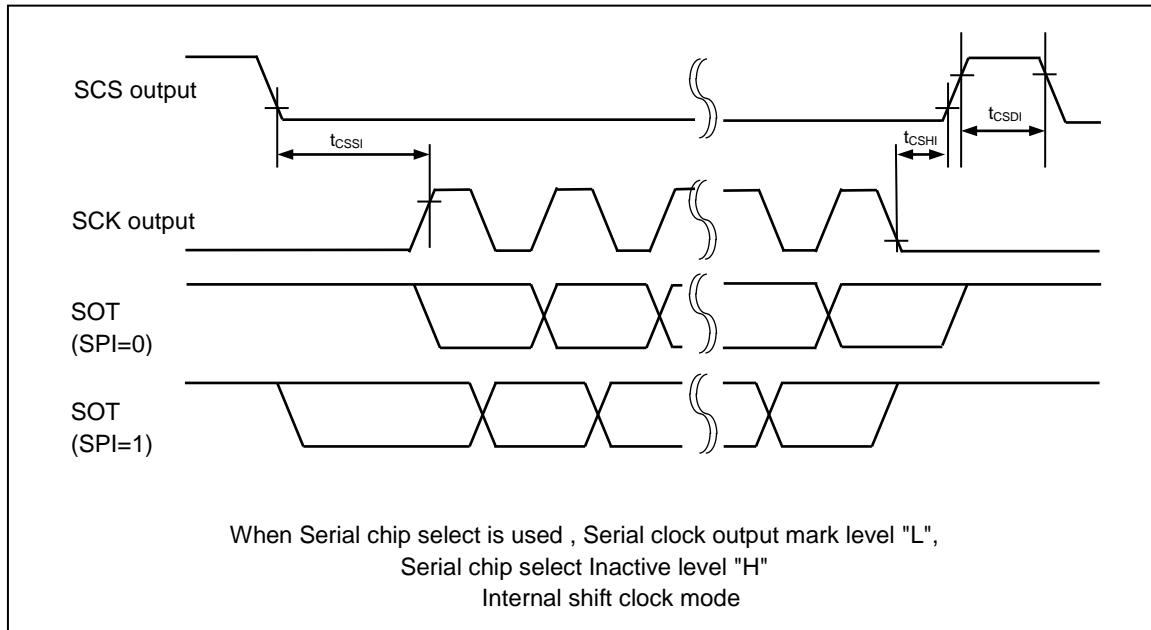
*1: tc_{SSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

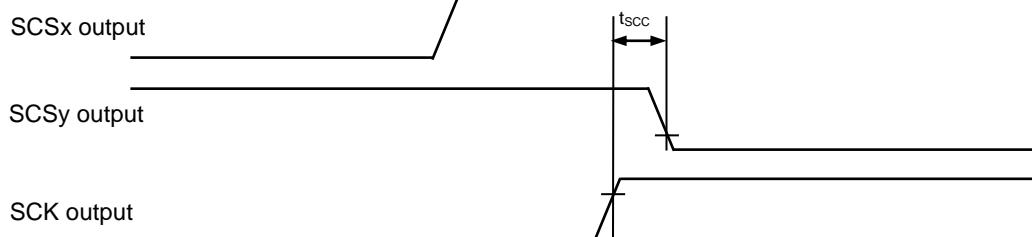
*2: tc_{SHD} = SCSTR:CSHD7-0 × Serial chip select timing operating clock

*3: tc_{SDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3





When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-7) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,

When Serial chip select is used : SCSCR:CSEN = 1,

Serial clock output mark level "H" : SMR,SCSFR:SCINV = 0,

Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL = 0

(TA: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3V±0.3V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t _{CSSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CSUU-50} *1	t _{CSUU+0} *1	ns	Internal shift clock mode output pin : C _L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSUU-50} *1	t _{CSUU+300} *1	ns	
SCK↑→SCS↓ hold time	t _{CSSH}	SCK1 to SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CSDH-10} *2	t _{CSDH+50} *2	ns	Internal shift clock mode output pin : C _L = 50 pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSDH-300} *2	t _{CSDH+50} *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSDS-50} *3	t _{CSDS+50} *3	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \uparrow →SCK \downarrow setup time	t _{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK \uparrow →SCS \downarrow hold time				+0	-	ns	
SCS deselect time				3t _{CPP} +30	-	ns	
SCS \uparrow →SOT delay time	t _{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11	-	-	40	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
		SCS3 , SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS \downarrow →SOT delay time	t _{DSE}	SCS1 to ~SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK \downarrow →SCS \uparrow clock switch time	t _{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50	ns	

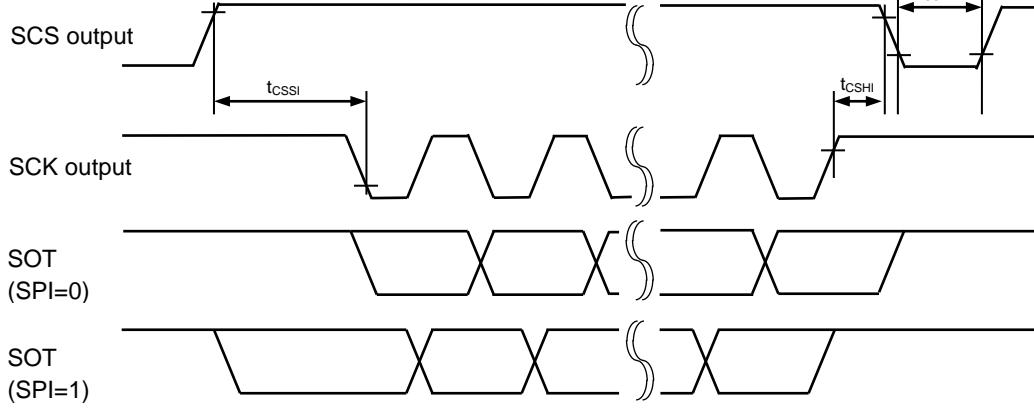
*1: t_{CSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD7-0 × Serial chip select timing operating clock

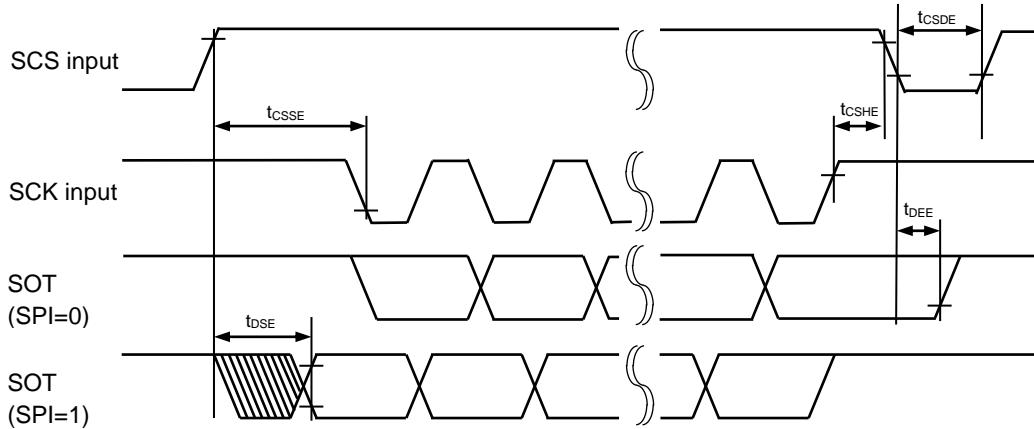
*3: t_{CSDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

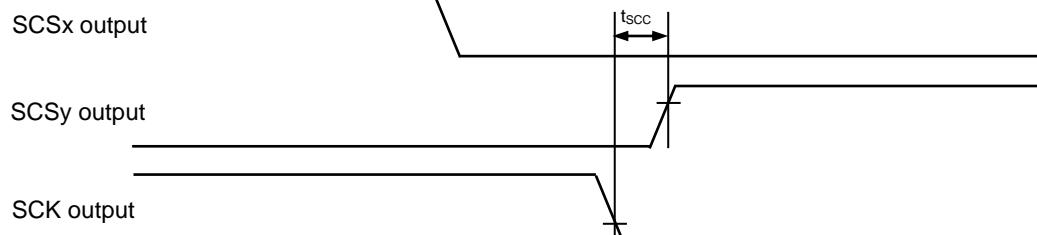
Please see the hardware manual for details of above-mentioned *1, *2, and *3.



When Serial chip select is used , Serial clock output mark level "H",
 Serial chip select Inactive level "L"
 Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
 Serial chip select Inactive level "L"
 External shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-8) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,

When Serial chip select is used: SCSCR:CSEN = 1,

Serial clock output mark level "L" : SMR,SCSFR:SCINV = 1,

Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL = 0

(T_A : -40 °C to +125 °C, $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\% / V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \uparrow →SCK \uparrow setup time	t _{CS\downarrowS\uparrow}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CS\downarrowS\uparrow-50} ^{*1}	t _{CS\downarrowS\uparrow+0} ^{*1}	ns	Internal shift clock mode output pin : $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CS\downarrowS\uparrow-50} ^{*1}	t _{CS\downarrowS\uparrow+300} ^{*1}	ns	
SCK \downarrow →SCS \downarrow hold time	t _{CS\downarrowH}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CS\downarrowH-10} ^{*2}	t _{CS\downarrowH+50} ^{*2}	ns	Internal shift clock mode output pin : $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CS\downarrowH-300} ^{*2}	t _{CS\downarrowH+50} ^{*2}	ns	
SCS deselect time	t _{CS\downarrowD}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CS\downarrowD-50} ^{*3}	t _{CS\downarrowD+50} ^{*3}	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \uparrow →SCK \uparrow setup time	t _{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK \downarrow →SCS \downarrow hold time		SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		+0	-	ns	
SCS deselect time		SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		3t _{CPP} +30	-	ns	
SCS \uparrow →SOT delay time	t _{DSE}	SCS1 , SCS2, SCS50~SCS53, SCS60~SCS63, SCS70~SCS73, SCS8~SCS11 SOT1 , SOT2, SOT5~SOT11	-	-	40	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
		SCS3 , SCS40~SCS43 SOT3 ,SOT4		-	300	ns	
SCS \downarrow →SOT delay time	t _{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: $C_L = 50 \text{ pF}$
SCK \uparrow →SCS \uparrow clock switch time	t _{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: $C_L = 50 \text{ pF}$
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50		

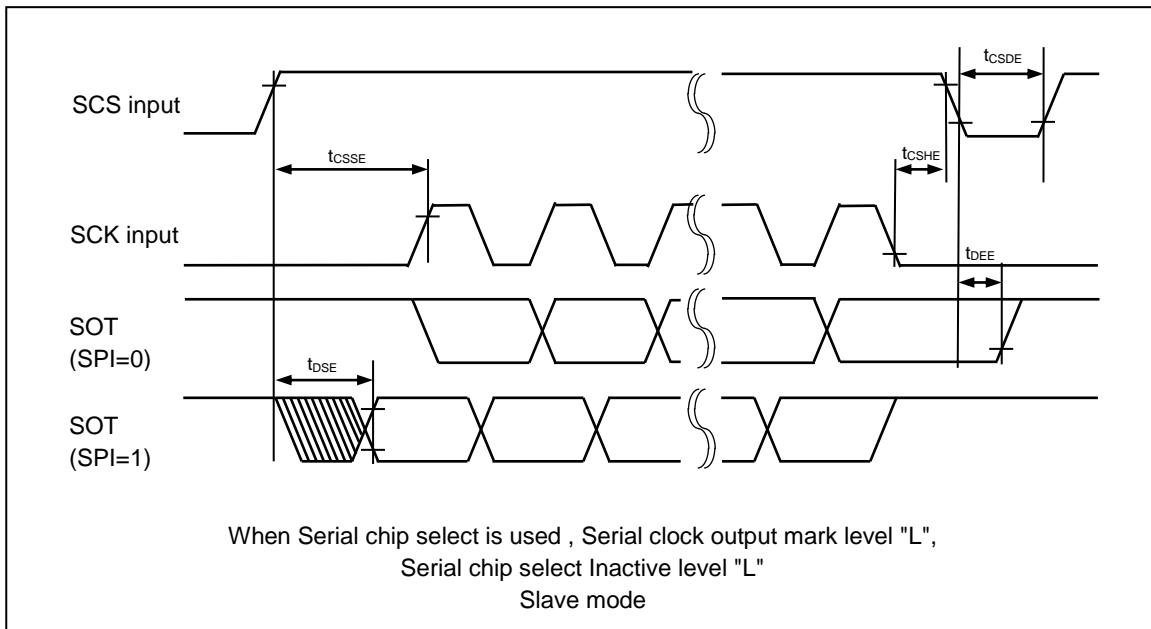
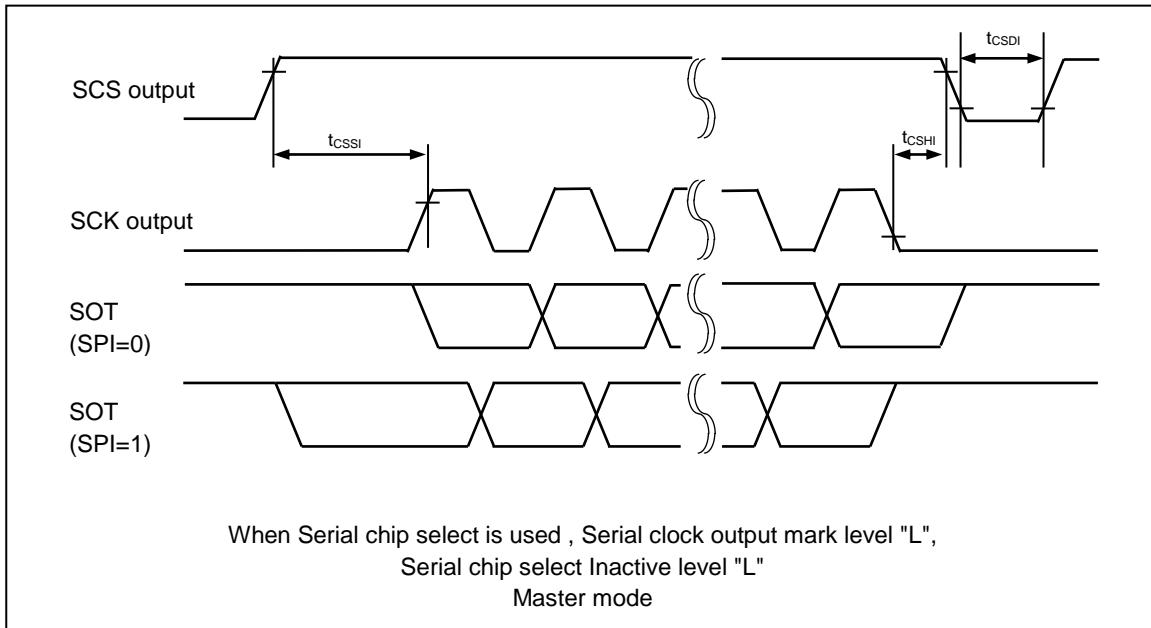
*1: tc_{SSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

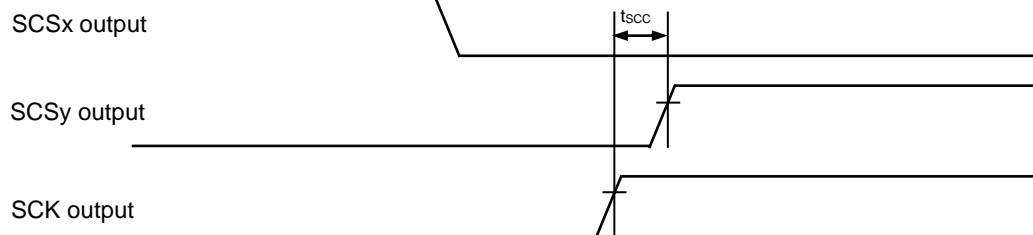
*2: tc_{SHD} = SCSTR:CSHD7-0 × Serial chip select timing operating clock

*3: tc_{SDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.





When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

(4-2) UART (Asynchronous serial interface) timing

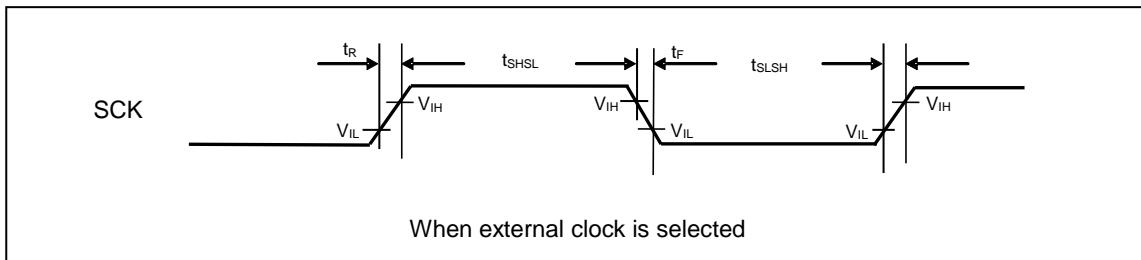
Bit setting: SMR : MD2 = 0, SMR:MD1 = 0, SMR : MD0 = 0

Bit setting: SMR : MD2 = 0, SMR:MD1 = 0, SMR : MD0 = 1

When external clock is selected (BGR:EXT = 1)

(TA: -40 °C to +125°C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK11	-	t _{CPP} +10	-	ns	output pin: C _L = 50 pF
Serial clock "H"pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	

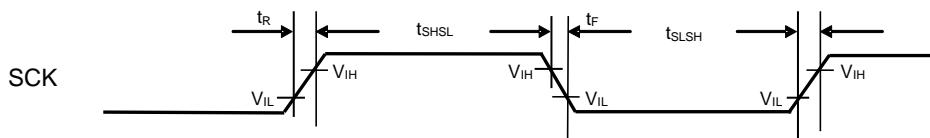


(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing

Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 1

(T_A : -40°C to +125°C, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{CC} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	$t_{CPP}+10$	-	ns	output pin: $C_L = 50\text{ pF}$
Serial clock "H" pulse width	t_{SHSL}			$t_{CPP}+10$	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

(4-4) I²C timing

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Fast Mode ^{*3}		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	SCK3 to SCK11	$C_L = 50 \text{ pF}$ $R = (V_P/I_{OL})^{*1}$	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t _{HDSTA}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		4.0	—	0.6	—	μs	
Period of "L" for SCL clock	t _{LOW}	SCK3 to SCK11, (SCL)		4.7	—	1.3	—	μs	
Period of "H" for SCL clock	t _{HIGH}	SCK3 to SCK11, (SCL)		4.0	—	0.6	—	μs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t _{SUSTA}	SCK3 to SCK11, (SCL)		4.7	—	0.6	—	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		0	3.45 ^{*2}	0	0.9 ^{*3}	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		250	—	100	—	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t _{SUSTO}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		4.0	—	0.6	—	μs	
Bus-free time between "stop" condition and "start" condition	t _{BUF}	—		4.7	—	1.3	—	μs	
Noise filter	t _{SP}	—	—	2t _{CPP} ^{*4}	—	2t _{CPP} ^{*4}	—	ns	

Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence. In ch.5-ch.8, ch.10, and ch.11, only a standard mode is correspondences.

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

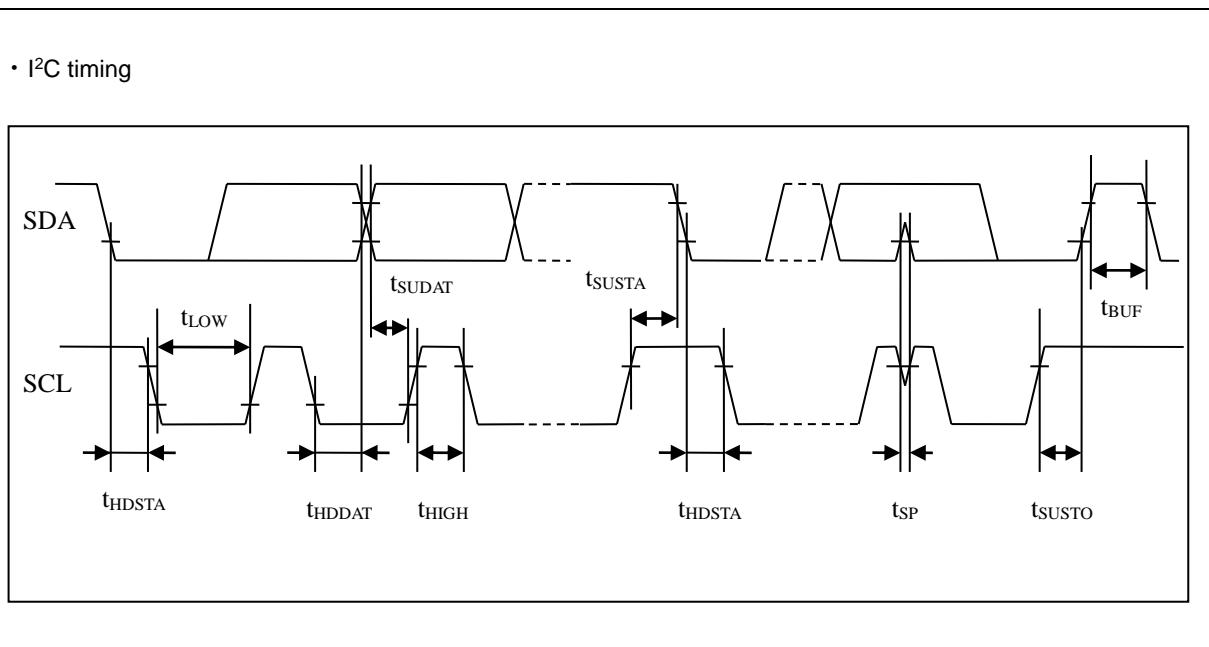
V_P shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A fast mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of

" $t_{SUDAT} \geq 250$ ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8 MHz or more when use I²C.

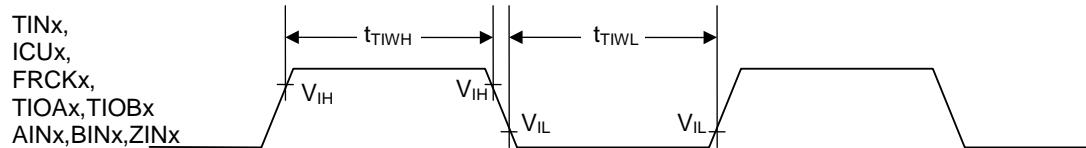


(5) Timer input timing

($T_A: -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{CC} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} , t_{TIWL}	TIN0 to TIN7 ICU0 to ICU9 FRCK0 to FRCK5 TIOA0, TIOA1, TIOB0, TIOB1, AIN0, AIN1, BIN0, BIN1, ZIN0, ZIN1	—	4t _{CPP}	—	ns	

- Timer input timing

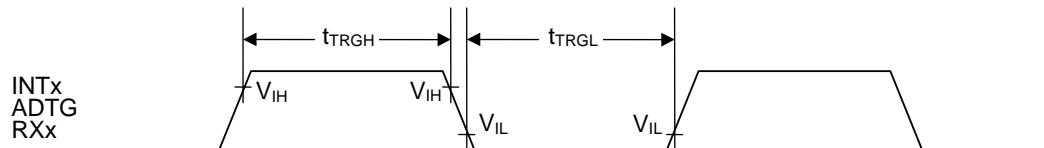


(6) Trigger input timing

($T_A: -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{CC} = AV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} , t_{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	—	5t _{CPP}	—	ns	
				1	—	μs	At stop mode

- Trigger input timing

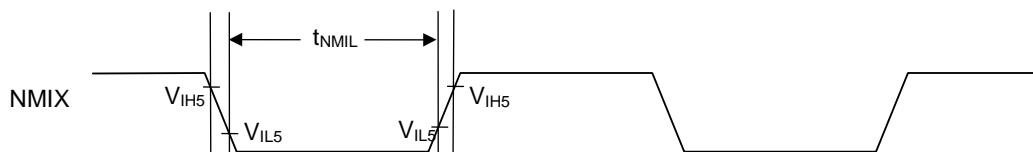


(7) NMI input timing

($T_A: -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{NMI\text{L}}$	NMIX	-	$4t_{CPP}$	-	ns	

- NMIX input timing



(8) Low voltage detection (External low-voltage detection)

($T_A: -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}		-	2.7	-	5.5	V	
Detection voltage ^{*3}	V_{DL}	VCC	^{*1}	-8%	$LVD5F_SEL[3:0]$	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Hysteresis width	V_{HYS}							
Low voltage detection time	T_d	-	-	-	0.1	-	V	When power-supply voltage rises
Power supply voltage regulation	-					30	μs	

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).

*3: The initial detection voltage of the external low voltage detection is $2.8 \text{ V} \pm 8\%$ (2.576 V to 3.024 V).

This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7 V).

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(9) Low voltage detection (Internal low-voltage detection)

(T_A: -40 °C to +125 °C, V_{ss} = AV_{ss} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage ^{*2}	V _{RDL}		^{*1}	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V _{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-		-	-	-	30	μs	

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: The detection voltage of the internal low voltage detection is 0.9 V ± 0.1 V.

This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(10) External bus I/F (synchronous mode) timing

(T_A: -40 °C to +105 °C, V_{cc} = AV_{cc} = 5.0 V ± 10 %/V_{cc} = AV_{cc} = 3.3 V ± 0.3 V, V_{ss} = AV_{ss} = 0.0 V)

(external load capacitance 50 pF)

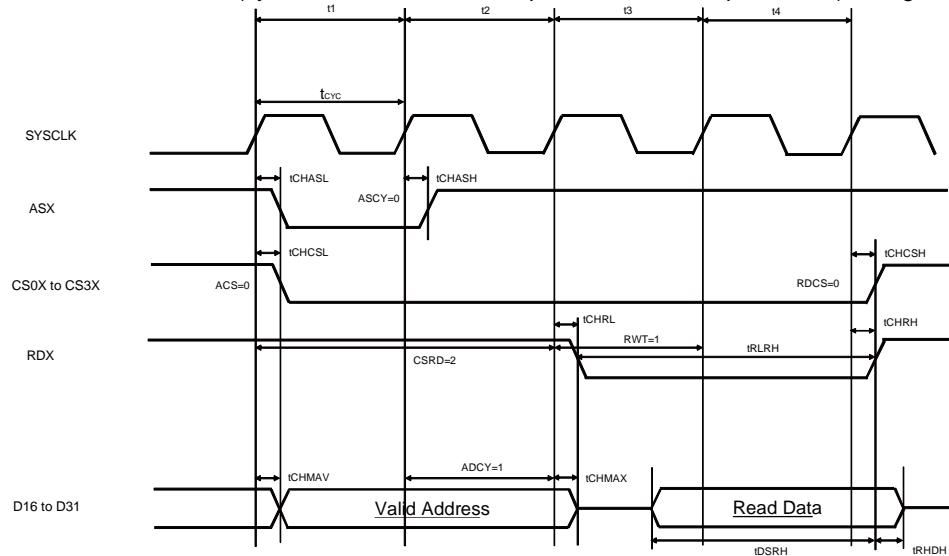
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	25	-	ns	V _{cc} = 5.0 V ± 10 % ^{*1}
			31.25			V _{cc} = 3.3 V ± 0.3 V
ASX delay time	t _{CHASL} , t _{CHASH}	SYSCLK ASX	0.5	18	ns	
CS0X to CS3X delay time	t _{CHCSL} , t _{CHCSH}	SYSCLK CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t _{CHAV} , t _{CHAX}	SYSCLK A00 to A21	0.5	18	ns	
RDX delay time	t _{CHRL} , t _{CHRH}	SYSCLK RDX	0.5	18	ns	
RDX minimum pulse	t _{RLRH}	RDX	t _{CYC} × 2 - 20	-	ns	RWT = 1, set RWT to 1 or more. ^{*2}
Data setup → RDX↑time	t _{DSRH}	RDX D16 to D31	18+t _{CYC}	-	ns	Same as above
RDX↑→ data hold	t _{RHDH}		0	-	ns	

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
WRnX delay time	t _{CHWL} , t _{CHWH}	SYSCLK WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t _{WLWH}	WR0X, WR1X	t _{CYC} - 10	-	ns	WWT = 0 ^{*2}
SYSCLK↑→ data output time	t _{CHDV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t _{CHDX}		-	18	ns	Set WRCS to 1 or more.
SYSCLK↑→ address output time	t _{CHMAV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t _{CHMAX}		-	18	ns	In multiplex mode, set as follows: <input type="checkbox"/> Set CSWR and CSRD to 2 or more. <input type="checkbox"/> ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

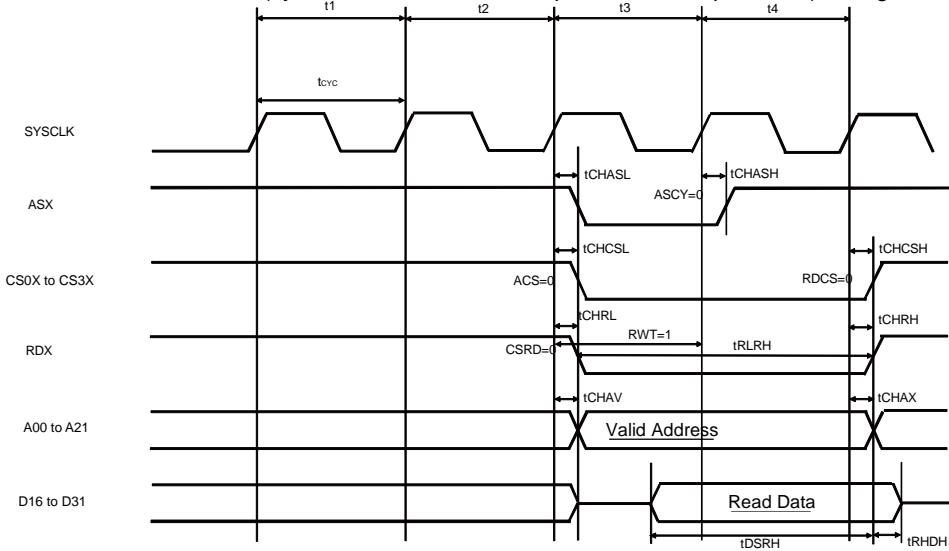
*1: Please use it with external load capacity 12 pF or less for VCC = 3.3 V ± 0.3 V (40 MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

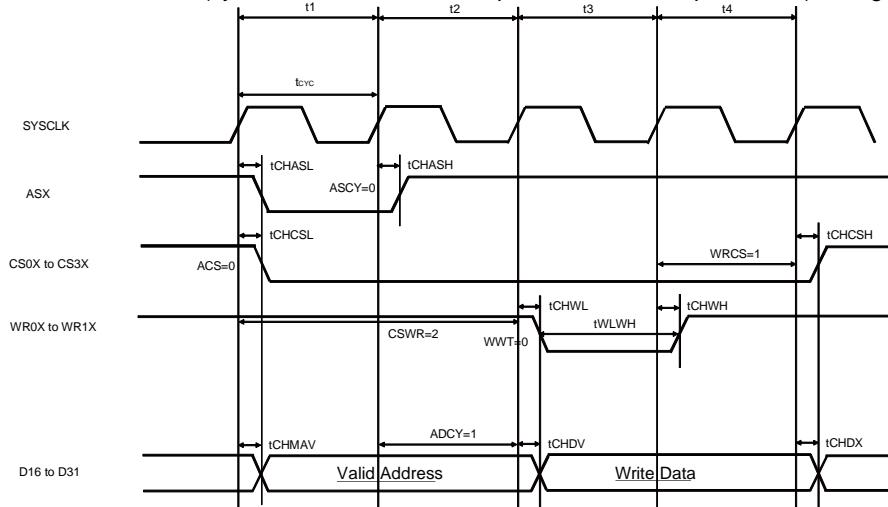
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



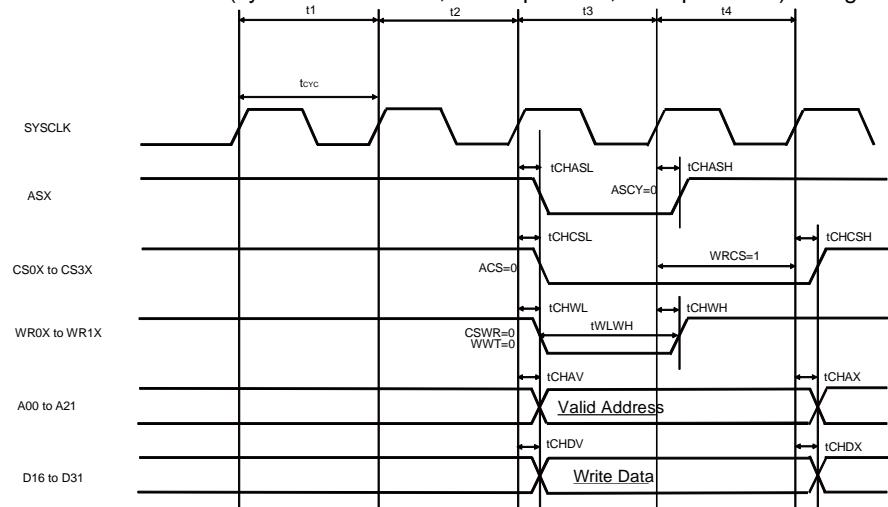
External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing



(11) External bus I/F (asynchronous mode) timing

(T_A: -40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

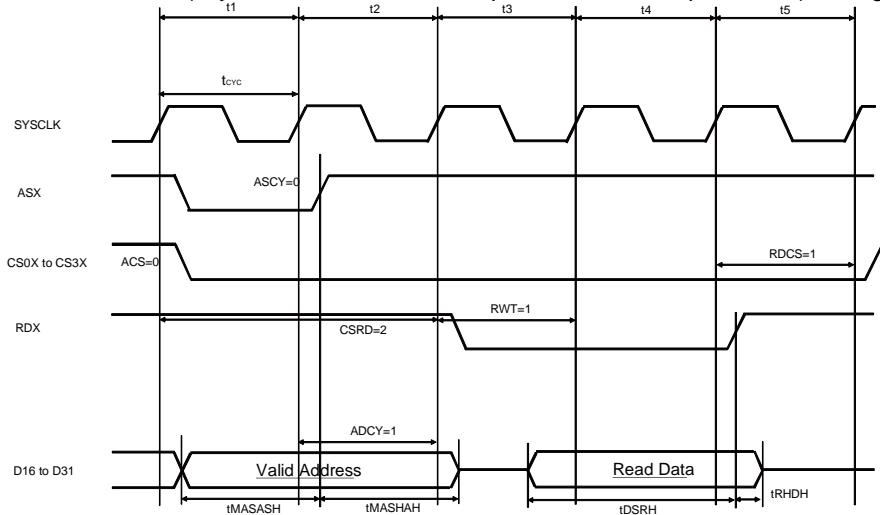
(external load capacitance 50pF)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	25	-	ns	V _{CC} = 5.0 V ± 10 % ^{*1}
			31.25			V _{CC} = 3.3 V ± 0.3 V
Address setup → RDX↑time	t _{ASRH}	RDX A00 to A21	2xt _{CYC} - 12	2xt _{CYC} + 12	ns	RWT = 1, set RWT to 1 or more. ^{*2}
RDX↑ → Address hold	t _{RHAH}		t _{CYC} - 12	t _{CYC} + 12	ns	Set RDCHS to 1 or more.
Data setup → RDX↑time	t _{DSRH}	RDX D16 to D31	18 + t _{CYC}	-	ns	RWT = 1, set RWT to 1 or more.
RDX↑ → Data hold	t _{RHDH}		0	-	ns	
Address setup → WRnX↑time	t _{ASWH}	WR0X to WR1X A00 to A21	t _{CYC} - 12	t _{CYC} + 12	ns	WWT = 0 ^{*2}
WRnX↑ → Address hold	t _{WHAH}		t _{CYC} - 12	t _{CYC} + 12	ns	Set WRCHS to 1 or more.
Data setup → WRnX↑time	t _{DSWH}	WR0X to WR1X D16 to D31	t _{CYC} - 16	t _{CYC} + 16	ns	WWT = 0 ^{*2}
WRnX↑ → Data hold	t _{WHDH}		t _{CYC} - 16	t _{CYC} + 16	ns	Set WRCHS to 1 or more.
Address setup → ASX↑time	t _{MASASH}	ASX D16 to D31	t _{CYC} - 16	t _{CYC} + 16	ns	ASCY = 0
ASX↑ → Address hold	t _{MASHAH}		t _{CYC} - 16	t _{CYC} + 16	ns	In multiplex mode, set as follows: <input type="checkbox"/> Set CSWR and CSRD to 2 or more. <input type="checkbox"/> ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

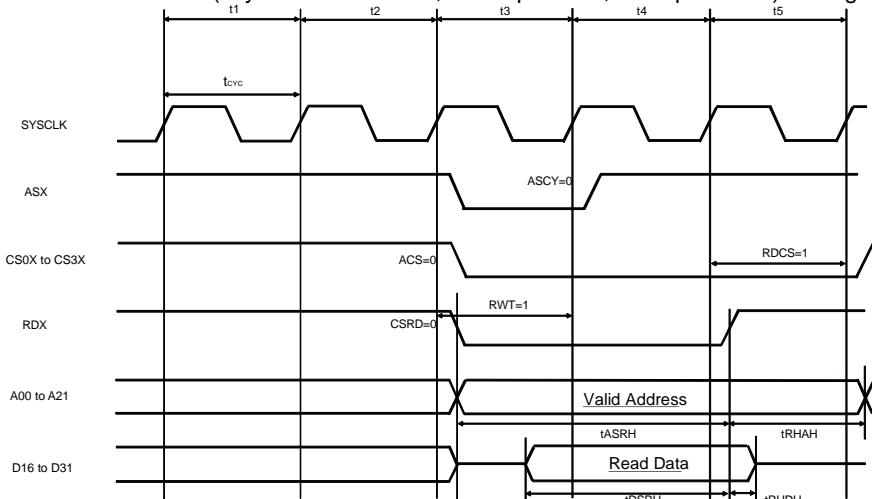
*1: Please use it with external load capacity 12 pF or less for V_{CC} = 3.3 V ± 0.3 V (40 MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

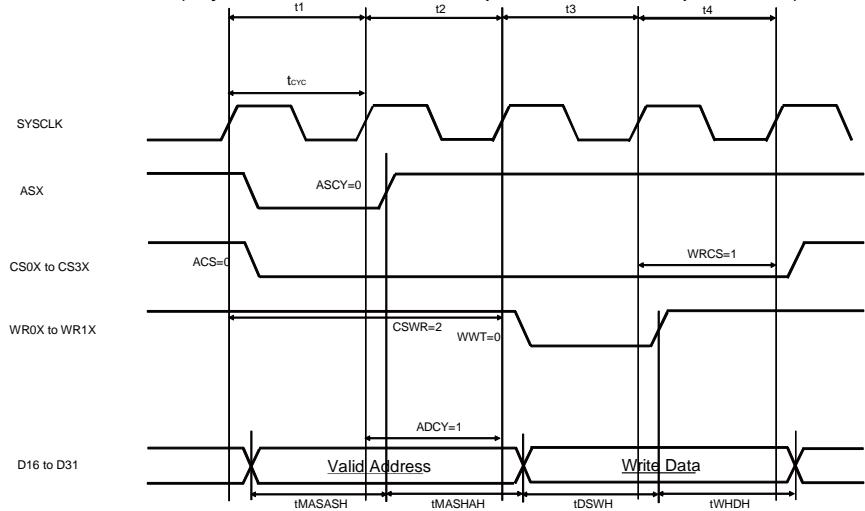
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



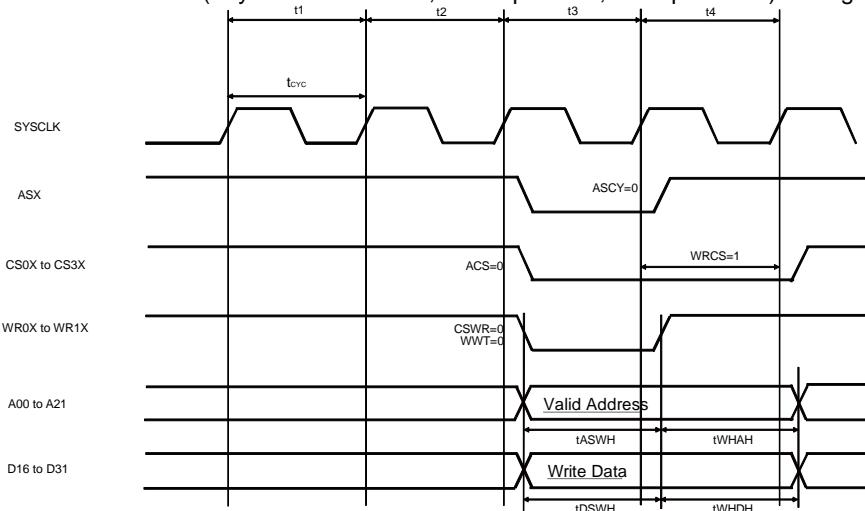
External bus I/F (asynchronous mode, read operation, and split mode) Timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing

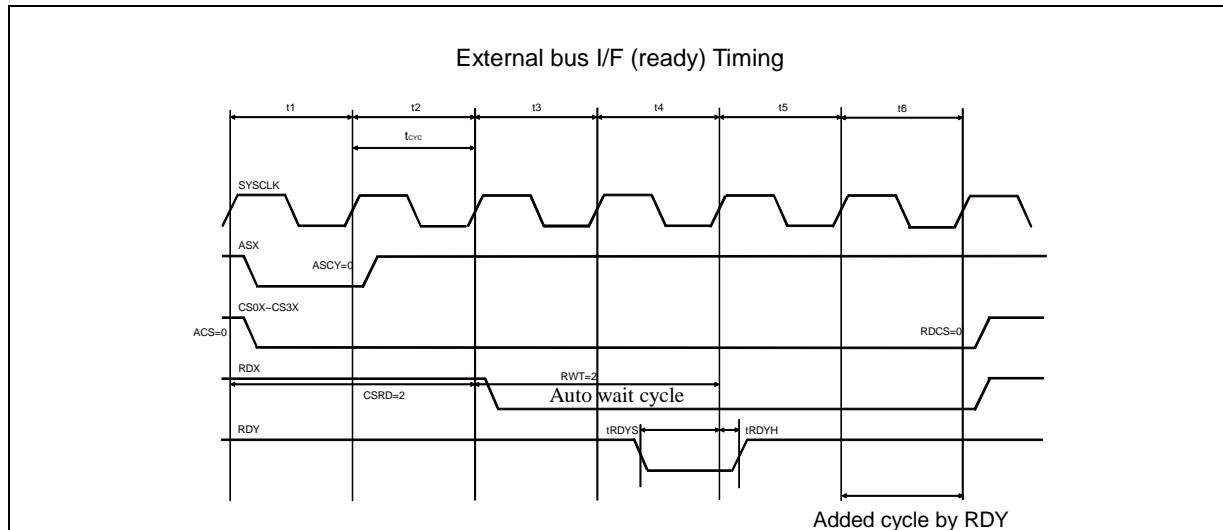


External bus I/F (Asynchronous mode, write operation, and split mode) Timing



(12) External bus I/F (ready) Timing
 $(T_A: -40^\circ\text{C} \text{ to } +105^\circ\text{C}, V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\% / V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V})$
 $(\text{external load capacitance } 50 \text{ pF})$

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t _{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t _{RDYH}	SYSCLK, RDY	0	-	ns	



A/D Converter
(1) 12-bit A/D Converter Electrical Characteristics

(TA: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %, V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V _{OT}	AN0 to AN47	AVRL- 11.5LSB	-	AVRL+ 12.5LSB	V	1LSB = (V _{FST} -V _{OT})/ 4094
Full-scale transition voltage	V _{FST}	AN0 to AN47	AVRH- 13.5LSB	-	AVRH+ 10.5LSB	V	
Sampling time	t _{SMP}	-	0.7	-	-	μs	*1
Compare time	t _{CMP}	-	0.7	-	-	μs	*1
A/D conversion time	t _{CNV}	-	1.4	-	-	μs	*1
Analog port input current	I _{AIN}	AN0 to AN47	-1.0	-	+1.0	μA	V _{AVSS} ≤ V _{AIN} ≤ V _{AVCC}
Analog input voltage	V _{AIN}	AN0 to AN47	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/ AVRL	-	0.0	-	V	
Power supply current	I _A	AVCC* ³	-	0.47	0.63	mA	Per unit T _A : +105 °C
			-	0.47	0.7	mA	Per unit T _A : +125 °C
	I _{AH}		-	-	2.5	μA	*2
	I _{IR}	AVRH	-	1	1.96	mA	Per unit
	I _{IRH}		-	-	1.6	μA	*2
Variation between channels	-	AN0 to AN47	-	-	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.

The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

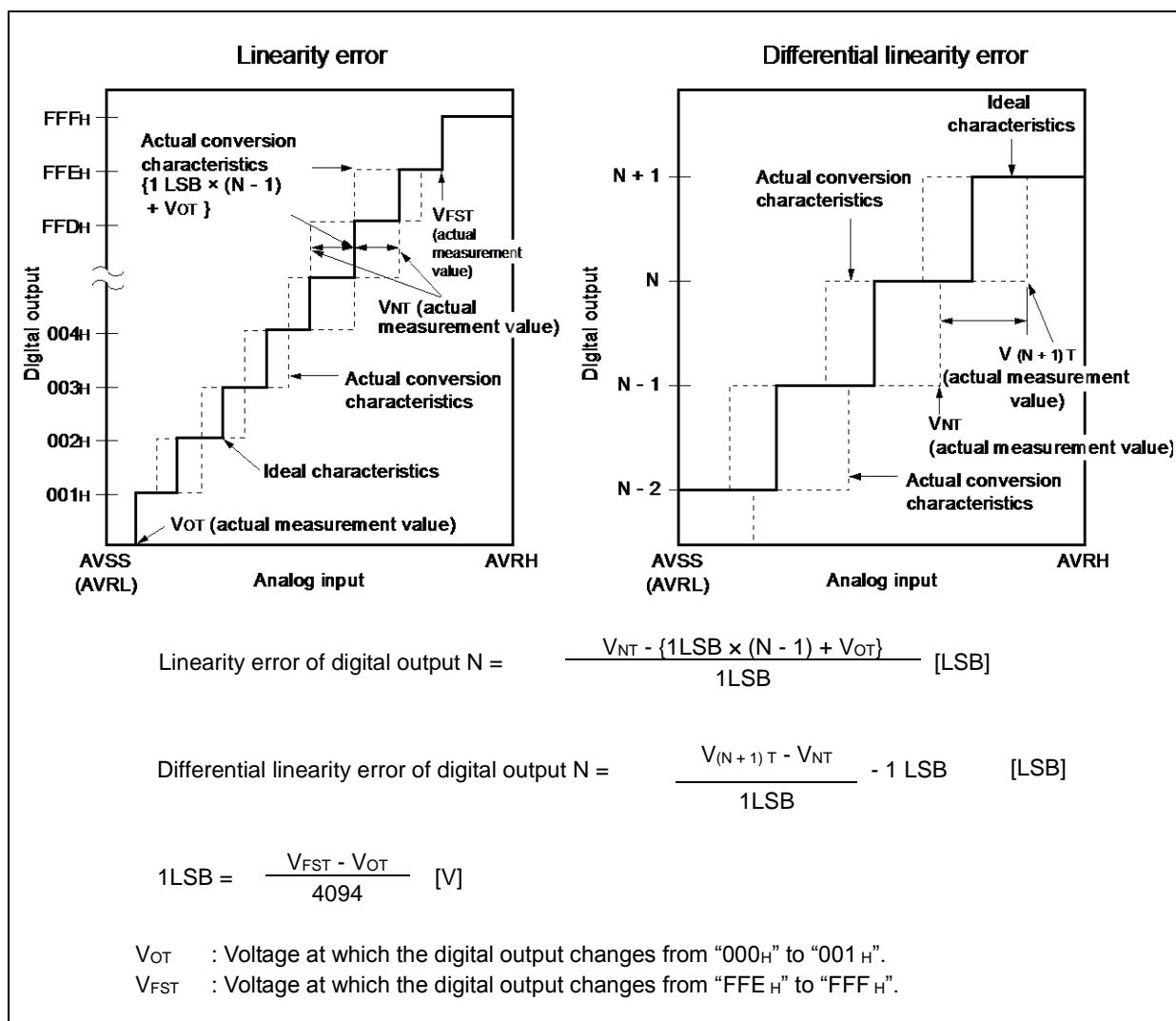
(Note) Please use the clock of 0.5 MHz-20 MHz for the output clock of A/D converter to guarantee accuracy.

(2) Definition of A/D Converter Terms

Resolution : Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000" $\leftarrow \rightarrow$ "0000 0000 0001") to the full-scale transition point ("1111 1111 1110" $\leftarrow \rightarrow$ "1111 1111 1111").

Differential linearity error : Deviation of the input voltage from the ideal value that is required to change the output code by LSB.

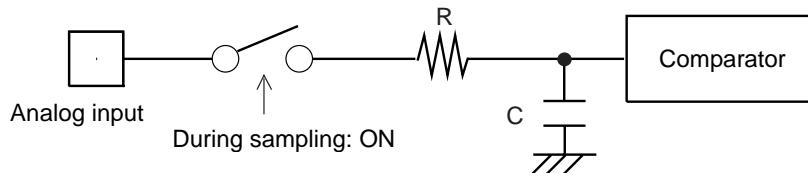


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μ F) to the analog input pin.

- Analog input circuit model



	R	C	
12-bit A/D	1.9 k Ω (Max)	8.30 pF (Max)	(4.5 V \leq AV _{cc} \leq 5.5 V)
	4.3 k Ω (Max)	8.30 pF (Max)	(3.0 V \leq AV _{cc} \leq 3.6 V)

Note: Listed values must be considered as reference values.

Flash Memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector ^{*1} , excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector ^{*1} , including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector ^{*1} , excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector ^{*1} , including internal preprogramming time
8-bit writing time	–	9	288	μs	Exclusive of overhead time at system level ^{*1}
16-bit writing time	–	12	384	μs	Exclusive of overhead time at system level ^{*1}
ECC writing time	–	9	288	μs	Exclusive of overhead time at system level ^{*1}
Erase cycle ^{*2} / Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average $T_A = +85^\circ\text{C}$ ^{*3}

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^\circ\text{C}$).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (V_{cc}) is prohibited.

In the application system where V_{cc} might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{cc} at 2.7 V or more within the duration calculated by the following expression:

$$T_d^* [\mu\text{s}] + (\text{period of PCLK } [\mu\text{s}] \times 257) + 50 [\mu\text{s}]$$

*: See "4.AC Characteristics (8) Low-voltage detection (External low-voltage detection)"

D/A Converter

(TA: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10 %/V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	-	-	-	8	bit	
Differential linearity error	-	-	-	-	-	± 3.0	LSB	
Conversion time	-	-	-	0.47	0.58	0.69	μs	C _L = 20
			-	2.37	2.90	3.43	μs	C _L = 100
Output impedance	R _O	DA0, DA1	-	3.1	3.8	4.5	kΩ	
Power supply current *1	I _A	AV _{CC}	-	-	475	580	μA	Each channel
	I _{AH}	AV _{CC}	-	-	-	7.5	μA	When powerdown Each channel

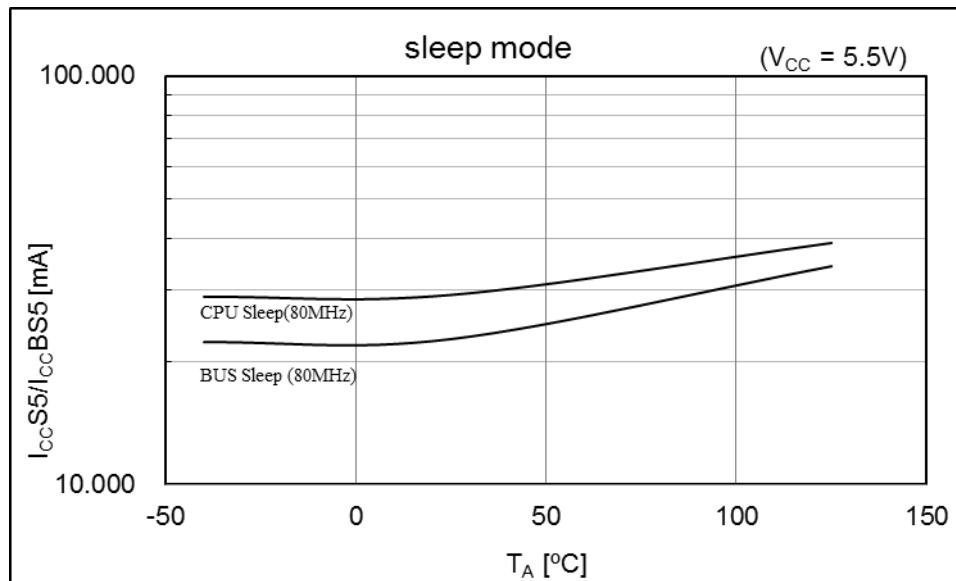
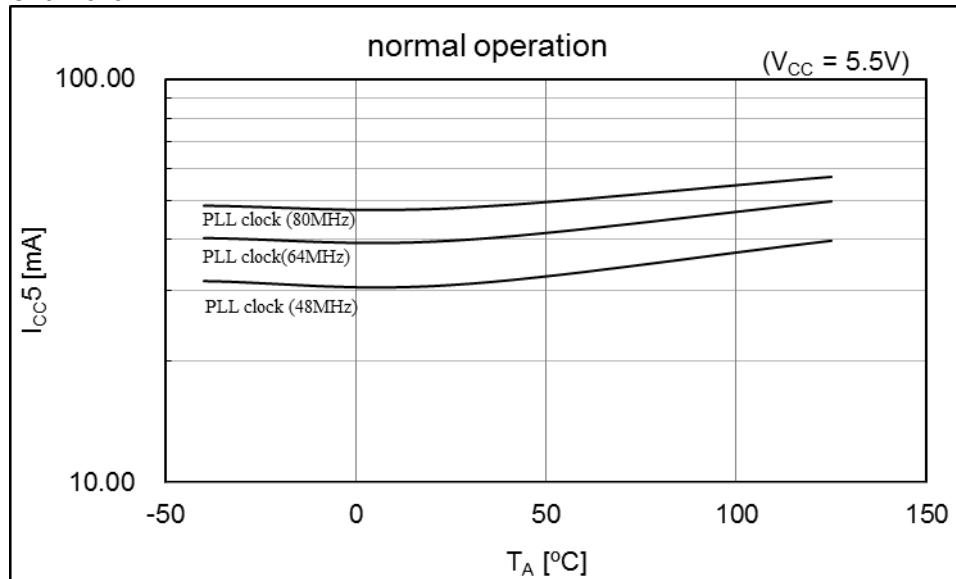
*1: The power supply current described only current value on D/A converter.

The total AV_{CC} current value must be calculated the power supply current for D/A converter and A/D converter.

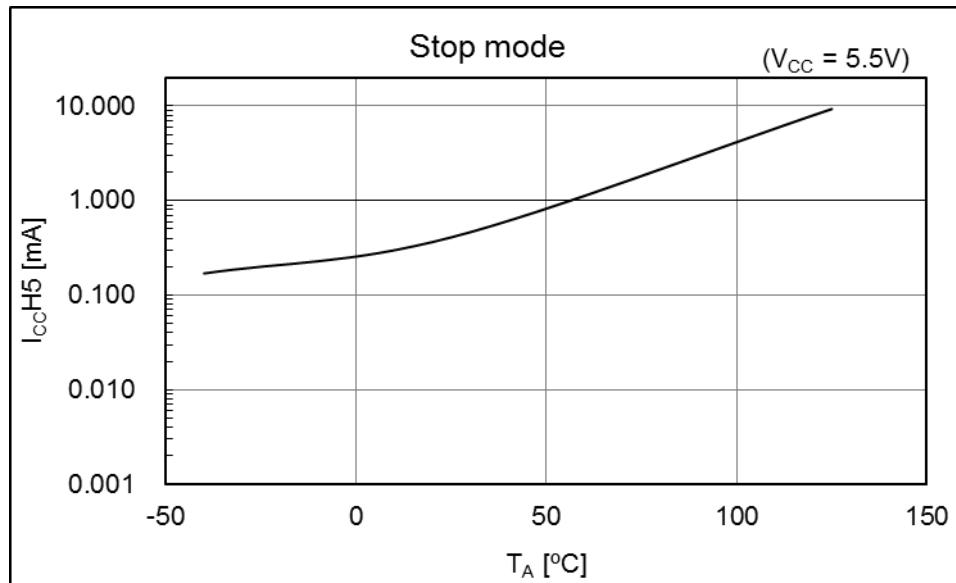
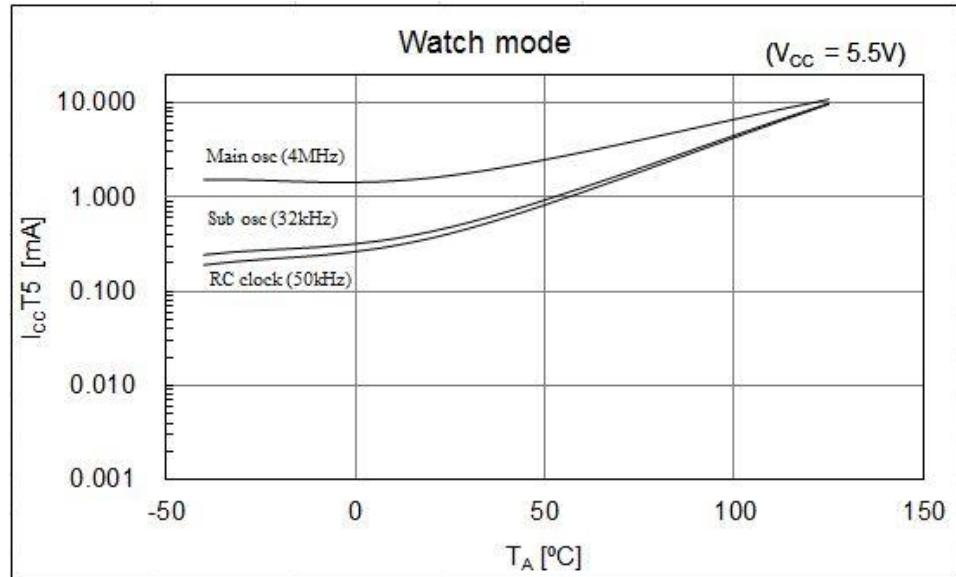
12. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

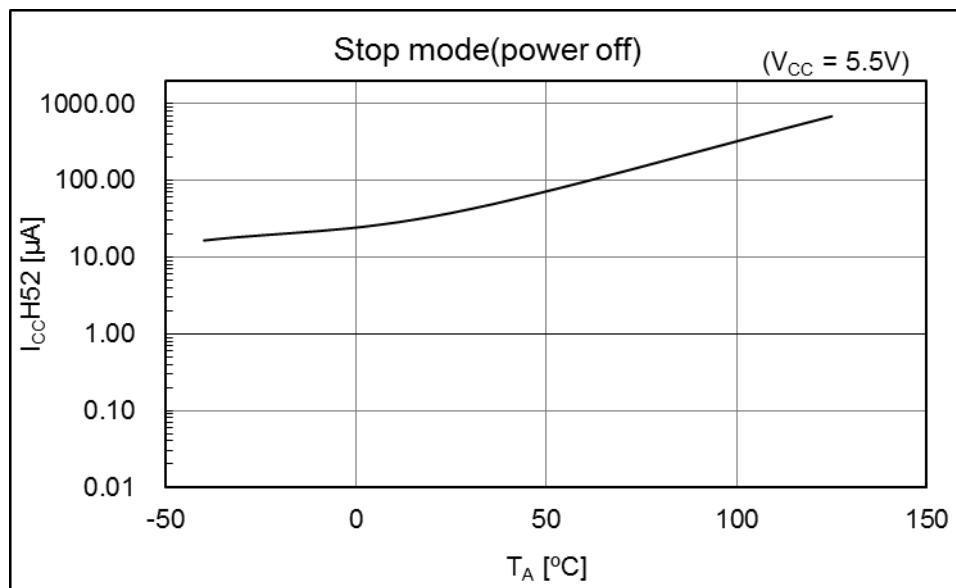
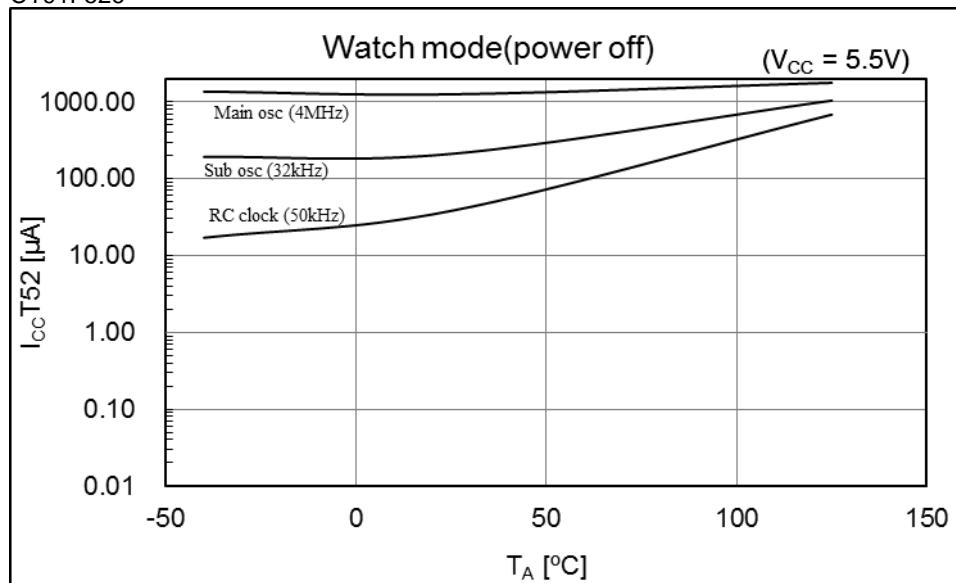
CY91F526



CY91F526



CY91F526



13. Ordering Information CY91F52xxxB^{*1}

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526LWPMC	Yes	ON	ON	LQP • 176 pin, Plastic
CY91F526LYPMC			OFF	
CY91F526LJPMC		OFF	ON	
CY91F526LLPMC			OFF	
CY91F525LWPMC		ON	ON	
CY91F525LYPMC			OFF	
CY91F525LJPMC		OFF	ON	
CY91F525LLPMC			OFF	
CY91F524LWPMC		ON	ON	
CY91F524LYPMC			OFF	
CY91F524LJPMC		OFF	ON	
CY91F524LLPMC			OFF	
CY91F523LWPMC		ON	ON	
CY91F523LYPMC			OFF	
CY91F523LJPMC		OFF	ON	
CY91F523LLPMC			OFF	
CY91F522LWPMC	None	ON	ON	
CY91F522LYPMC			OFF	
CY91F522LJPMC		OFF	ON	
CY91F522LLPMC			OFF	
CY91F526LSBPMC		ON	ON	
CY91F526LUBPMC			OFF	
CY91F526LHBPNC		OFF	ON	
CY91F526LKBPNC			OFF	
CY91F525LSBPMC		ON	ON	
CY91F525LUBPMC			OFF	
CY91F525LHBPNC		OFF	ON	
CY91F525LKBPNC			OFF	
CY91F524LSBPMC		ON	ON	
CY91F524LUBPMC			OFF	
CY91F524LHBPNC		OFF	ON	
CY91F524LKBPNC			OFF	
CY91F523LSBPMC		ON	ON	
CY91F523LUBPMC			OFF	
CY91F523LHBPNC		OFF	ON	
CY91F523LKBPNC			OFF	
CY91F522LSBPMC		ON	ON	
CY91F522LUBPMC			OFF	
CY91F522LHBPNC		OFF	ON	
CY91F522LKBPNC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
CY91F526KWBPMC	Yes	ON	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526KYBPMC			OFF	
CY91F526KJBP MC		OFF	ON	
CY91F526KLBP MC			OFF	
CY91F525KWBPMC		ON	ON	
CY91F525KYBPMC			OFF	
CY91F525KJBP MC		OFF	ON	
CY91F525KLBP MC			OFF	
CY91F524KWBPMC		ON	ON	
CY91F524KYBPMC			OFF	
CY91F524KJBP MC		OFF	ON	
CY91F524KLBP MC			OFF	
CY91F523KWBPMC		ON	ON	
CY91F523KYBPMC			OFF	
CY91F523KJBP MC		OFF	ON	
CY91F523KLBP MC			OFF	
CY91F522KWBPMC		ON	ON	
CY91F522KYBPMC			OFF	
CY91F522KJBP MC		OFF	ON	
CY91F522KLBP MC			OFF	
CY91F526KS BPMC	None	ON	ON	
CY91F526KU BPMC			OFF	
CY91F526KH BPMC		OFF	ON	
CY91F526KK BPMC			OFF	
CY91F525KS BPMC		ON	ON	
CY91F525KU BPMC			OFF	
CY91F525KH BPMC		OFF	ON	
CY91F525KK BPMC			OFF	
CY91F524KS BPMC		ON	ON	
CY91F524KU BPMC			OFF	
CY91F524KH BPMC		OFF	ON	
CY91F524KK BPMC			OFF	
CY91F523KS BPMC		ON	ON	
CY91F523KU BPMC			OFF	
CY91F523KH BPMC		OFF	ON	
CY91F523KK BPMC			OFF	
CY91F522KS BPMC		ON	ON	
CY91F522KU BPMC			OFF	
CY91F522KH BPMC		OFF	ON	
CY91F522KK BPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
CY91F526KWBPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4 mm) Plastic
CY91F526KYBPMC1			OFF	
CY91F526KJBP MC1		OFF	ON	
CY91F526KLBP MC1			OFF	
CY91F525KWBPMC1		ON	ON	
CY91F525KYBPMC1			OFF	
CY91F525KJBP MC1		OFF	ON	
CY91F525KLBP MC1			OFF	
CY91F524KWBPMC1		ON	ON	
CY91F524KYBPMC1			OFF	
CY91F524KJBP MC1		OFF	ON	
CY91F524KLBP MC1			OFF	
CY91F523KWBPMC1		ON	ON	
CY91F523KYBPMC1			OFF	
CY91F523KJBP MC1		OFF	ON	
CY91F523KLBP MC1			OFF	
CY91F522KWBPMC1		ON	ON	
CY91F522KYBPMC1			OFF	
CY91F522KJBP MC1		OFF	ON	
CY91F522KLBP MC1			OFF	
CY91F526KSBPMC1	None	ON	ON	
CY91F526KUBPMC1			OFF	
CY91F526KHBP MC1		OFF	ON	
CY91F526KKBP MC1			OFF	
CY91F525KSBPMC1		ON	ON	
CY91F525KUBPMC1			OFF	
CY91F525KHBP MC1		OFF	ON	
CY91F525KKBP MC1			OFF	
CY91F524KSBPMC1		ON	ON	
CY91F524KUBPMC1			OFF	
CY91F524KHBP MC1		OFF	ON	
CY91F524KKBP MC1			OFF	
CY91F523KSBPMC1		ON	ON	
CY91F523KUBPMC1			OFF	
CY91F523KHBP MC1		OFF	ON	
CY91F523KKBP MC1			OFF	
CY91F522KSBPMC1		ON	ON	
CY91F522KUBPMC1			OFF	
CY91F522KHBP MC1		OFF	ON	
CY91F522KKBP MC1			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
CY91F526JWPMC	Yes	ON	ON	LQM • 120 pin, Plastic
CY91F526JYBPMC			OFF	
CY91F526JJBPMC		OFF	ON	
CY91F526JLBPMC			OFF	
CY91F525JWPMC		ON	ON	
CY91F525JYBPMC			OFF	
CY91F525JJBPMC		OFF	ON	
CY91F525JLBPMC			OFF	
CY91F524JWPMC		ON	ON	
CY91F524JYBPMC			OFF	
CY91F524JJBPMC		OFF	ON	
CY91F524JLBPMC			OFF	
CY91F523JWPMC		ON	ON	
CY91F523JYBPMC			OFF	
CY91F523JJBPMC		OFF	ON	
CY91F523JLBPMC			OFF	
CY91F522JWPMC		ON	ON	
CY91F522JYBPMC			OFF	
CY91F522JJBPMC		OFF	ON	
CY91F522JLBPMC			OFF	
CY91F526JSBPMC	None	ON	ON	
CY91F526JUBPMC			OFF	
CY91F526JHBJPMC		OFF	ON	
CY91F526JKBPMC			OFF	
CY91F525JSBPMC		ON	ON	
CY91F525JUBPMC			OFF	
CY91F525JHBJPMC		OFF	ON	
CY91F525JKBPMC			OFF	
CY91F524JSBPMC		ON	ON	
CY91F524JUBPMC			OFF	
CY91F524JHBJPMC		OFF	ON	
CY91F524JKBPMC			OFF	
CY91F523JSBPMC		ON	ON	
CY91F523JUBPMC			OFF	
CY91F523JHBJPMC		OFF	ON	
CY91F523JKBPMC			OFF	
CY91F522JSBPMC		ON	ON	
CY91F522JUBPMC			OFF	
CY91F522JHBJPMC		OFF	ON	
CY91F522JKBPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
CY91F526FWBPMC	Yes	ON	ON	LQI • 100 pin, Plastic
CY91F526FYBPMC			OFF	
CY91F526FJBPMC		OFF	ON	
CY91F526FLBPMC			OFF	
CY91F525FWBPMC		ON	ON	
CY91F525FYBPMC			OFF	
CY91F525FJBPMC		OFF	ON	
CY91F525FLBPMC			OFF	
CY91F524FWBPMC		ON	ON	
CY91F524FYBPMC			OFF	
CY91F524FJBPMC		OFF	ON	
CY91F524FLBPMC			OFF	
CY91F523FWBPMC		ON	ON	
CY91F523FYBPMC			OFF	
CY91F523FJBPMC		OFF	ON	
CY91F523FLBPMC			OFF	
CY91F522FWBPMC		ON	ON	
CY91F522FYBPMC			OFF	
CY91F522FJBPMC		OFF	ON	
CY91F522FLBPMC			OFF	
CY91F526FSBPMC	None	ON	ON	LQI • 100 pin, Plastic
CY91F526FUBPMC			OFF	
CY91F526FHBPMC		OFF	ON	
CY91F526FKBPMC			OFF	
CY91F525FSBPMC		ON	ON	
CY91F525FUBPMC			OFF	
CY91F525FHBPMC		OFF	ON	
CY91F525FKBPMC			OFF	
CY91F524FSBPMC		ON	ON	
CY91F524FUBPMC			OFF	
CY91F524FHBPMC		OFF	ON	
CY91F524FKBPMC			OFF	
CY91F523FSBPMC		ON	ON	
CY91F523FUBPMC			OFF	
CY91F523FHBPMC		OFF	ON	
CY91F523FKBPMC			OFF	
CY91F522FSBPMC		ON	ON	
CY91F522FUBPMC			OFF	
CY91F522FHBPMC		OFF	ON	
CY91F522FKBPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*2
CY91F526DWBPMC	Yes	ON	ON	LQH • 80 pin, Plastic
CY91F526DYBPMC			OFF	
CY91F526DJBPMC		OFF	ON	
CY91F526DLBPMC			OFF	
CY91F525DWBPMC		ON	ON	
CY91F525DYBPMC			OFF	
CY91F525DJBPMC		OFF	ON	
CY91F525DLBPMC			OFF	
CY91F524DWBPMC		ON	ON	
CY91F524DYBPMC			OFF	
CY91F524DJBPMC		OFF	ON	
CY91F524DLBPMC			OFF	
CY91F523DWBPMC		ON	ON	
CY91F523DYBPMC			OFF	
CY91F523DJBPMC		OFF	ON	
CY91F523DLBPMC			OFF	
CY91F522DWBPMC		ON	ON	
CY91F522DYBPMC			OFF	
CY91F522DJBPMC		OFF	ON	
CY91F522DLBPMC			OFF	
CY91F526DSBPMC	None	ON	ON	LQH • 80 pin, Plastic
CY91F526DUBPMC			OFF	
CY91F526DHBPMC		OFF	ON	
CY91F526DKBPMC			OFF	
CY91F525DSBPMC		ON	ON	
CY91F525DUBPMC			OFF	
CY91F525DHBPMC		OFF	ON	
CY91F525DKBPMC			OFF	
CY91F524DSBPMC		ON	ON	
CY91F524DUBPMC			OFF	
CY91F524DHBPMC		OFF	ON	
CY91F524DKBPMC			OFF	
CY91F523DSBPMC		ON	ON	
CY91F523DUBPMC			OFF	
CY91F523DHBPMC		OFF	ON	
CY91F523DKBPMC			OFF	
CY91F522DSBPMC		ON	ON	
CY91F522DUBPMC			OFF	
CY91F522DHBPMC		OFF	ON	
CY91F522DKBPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526BWBPMC1	Yes	ON	ON	LQD • 64 pin, Plastic
CY91F526BYBPMC1			OFF	
CY91F526BJBPMC1		OFF	ON	
CY91F526BLBPMC1			OFF	
CY91F525BWBPMC1		ON	ON	
CY91F525BYBPMC1			OFF	
CY91F525BJBPMC1		OFF	ON	
CY91F525BLBPMC1			OFF	
CY91F524BWBPMC1		ON	ON	
CY91F524BYBPMC1			OFF	
CY91F524BJBPMC1		OFF	ON	
CY91F524BLBPMC1			OFF	
CY91F523BWBPMC1		ON	ON	
CY91F523BYBPMC1			OFF	
CY91F523BJBPMC1		OFF	ON	
CY91F523BLBPMC1			OFF	
CY91F522BWBPMC1		ON	ON	
CY91F522BYBPMC1			OFF	
CY91F522BJBPMC1		OFF	ON	
CY91F522BLBPMC1			OFF	
CY91F526BSBPMC1	None	ON	ON	LQD • 64 pin, Plastic
CY91F526BUBPMC1			OFF	
CY91F526BHBPMC1		OFF	ON	
CY91F526KKBPMC1			OFF	
CY91F525BSBPMC1		ON	ON	
CY91F525BUBPMC1			OFF	
CY91F525BHBPMC1		OFF	ON	
CY91F525KKBPMC1			OFF	
CY91F524BSBPMC1		ON	ON	
CY91F524BUBPMC1			OFF	
CY91F524BHBPMC1		OFF	ON	
CY91F524KKBPMC1			OFF	
CY91F523BSBPMC1		ON	ON	
CY91F523BUBPMC1			OFF	
CY91F523BHBPMC1		OFF	ON	
CY91F523KKBPMC1			OFF	
CY91F522BSBPMC1		ON	ON	
CY91F522BUBPMC1			OFF	
CY91F522BHBPMC1		OFF	ON	
CY91F522KKBPMC1			OFF	

^{*1}: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.

^{*2}: For details of the package, see [Package Dimensions](#).

14. Ordering Information CY91F52xxxC^{*1}

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526LWCPMC	Yes	ON	ON	LQP • 176 pin, Plastic
CY91F526LYCPMC			OFF	
CY91F526LJCPMC		OFF	ON	
CY91F526LLCPMC			OFF	
CY91F525LWCPMC		ON	ON	
CY91F525LYCPMC			OFF	
CY91F525LJCPMC		OFF	ON	
CY91F525LLCPMC			OFF	
CY91F524LWCPMC		ON	ON	
CY91F524LYCPMC			OFF	
CY91F524LJCPMC		OFF	ON	
CY91F524LLCPMC			OFF	
CY91F523LWCPMC		ON	ON	
CY91F523LYCPMC			OFF	
CY91F523LJCPMC		OFF	ON	
CY91F523LLCPMC			OFF	
CY91F522LWCPMC	None	ON	ON	
CY91F522LYCPMC			OFF	
CY91F522LJCPMC		OFF	ON	
CY91F522LLCPMC			OFF	
CY91F526LSCPML		ON	ON	
CY91F526LUCPMC			OFF	
CY91F526LHCPMC		OFF	ON	
CY91F526LKCPMC			OFF	
CY91F525LSCPML		ON	ON	
CY91F525LUCPMC			OFF	
CY91F525LHCPMC		OFF	ON	
CY91F525LKCPMC			OFF	
CY91F524LSCPML		ON	ON	
CY91F524LUCPMC			OFF	
CY91F524LHCPMC		OFF	ON	
CY91F524LKCPMC			OFF	
CY91F523LSCPML		ON	ON	
CY91F523LUCPMC			OFF	
CY91F523LHCPMC		OFF	ON	
CY91F523LKCPMC			OFF	
CY91F522LSCPML		ON	ON	
CY91F522LUCPMC			OFF	
CY91F522LHCPMC		OFF	ON	
CY91F522LKCPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526KCPMC	Yes	ON	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526KYCPMC			OFF	
CY91F526KJCPMC		OFF	ON	
CY91F526KLCPMC			OFF	
CY91F525KCPMC		ON	ON	
CY91F525KYCPMC			OFF	
CY91F525KJCPMC		OFF	ON	
CY91F525KLCPMC			OFF	
CY91F524KCPMC		ON	ON	
CY91F524KYCPMC			OFF	
CY91F524KJCPMC		OFF	ON	
CY91F524KLCPMC			OFF	
CY91F523KCPMC		ON	ON	
CY91F523KYCPMC			OFF	
CY91F523KJCPMC		OFF	ON	
CY91F523KLCPMC			OFF	
CY91F522KCPMC		ON	ON	
CY91F522KYCPMC			OFF	
CY91F522KJCPMC		OFF	ON	
CY91F522KLCPMC			OFF	
CY91F526KSCPMC	None	ON	ON	
CY91F526KUCPMC			OFF	
CY91F526KHCPMC		OFF	ON	
CY91F526KKCPMC			OFF	
CY91F525KSCPMC		ON	ON	
CY91F525KUCPMC			OFF	
CY91F525KHCPMC		OFF	ON	
CY91F525KKCPMC			OFF	
CY91F524KSCPMC		ON	ON	
CY91F524KUCPMC			OFF	
CY91F524KHCPMC		OFF	ON	
CY91F524KKCPMC			OFF	
CY91F523KSCPMC		ON	ON	
CY91F523KUCPMC			OFF	
CY91F523KHCPMC		OFF	ON	
CY91F523KKCPMC			OFF	
CY91F522KSCPMC		ON	ON	
CY91F522KUCPMC			OFF	
CY91F522KHCPMC		OFF	ON	
CY91F522KKCPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526KWCPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4 mm) Plastic
CY91F526KYCPMC1			OFF	
CY91F526KJCPMC1		OFF	ON	
CY91F526KLCPMC1			OFF	
CY91F525KWCPMC1		ON	ON	
CY91F525KYCPMC1			OFF	
CY91F525KJCPMC1		OFF	ON	
CY91F525KLCPMC1			OFF	
CY91F524KWCPMC1		ON	ON	
CY91F524KYCPMC1			OFF	
CY91F524KJCPMC1		OFF	ON	
CY91F524KLCPMC1			OFF	
CY91F523KWCPMC1		ON	ON	
CY91F523KYCPMC1			OFF	
CY91F523KJCPMC1		OFF	ON	
CY91F523KLCPMC1			OFF	
CY91F522KWCPMC1		ON	ON	
CY91F522KYCPMC1			OFF	
CY91F522KJCPMC1		OFF	ON	
CY91F522KLCPMC1			OFF	
CY91F526KSCPMC1	None	ON	ON	
CY91F526KUCPMC1			OFF	
CY91F526KHCPMC1		OFF	ON	
CY91F526KKCPMC1			OFF	
CY91F525KSCPMC1		ON	ON	
CY91F525KUCPMC1			OFF	
CY91F525KHCPMC1		OFF	ON	
CY91F525KKCPMC1			OFF	
CY91F524KSCPMC1		ON	ON	
CY91F524KUCPMC1			OFF	
CY91F524KHCPMC1		OFF	ON	
CY91F524KKCPMC1			OFF	
CY91F523KSCPMC1		ON	ON	
CY91F523KUCPMC1			OFF	
CY91F523KHCPMC1		OFF	ON	
CY91F523KKCPMC1			OFF	
CY91F522KSCPMC1		ON	ON	
CY91F522KUCPMC1			OFF	
CY91F522KHCPMC1		OFF	ON	
CY91F522KKCPMC1			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526JWCPMC	Yes	ON	ON	LQM • 120 pin, Plastic
CY91F526JYCPMC			OFF	
CY91F526JJCPMC		OFF	ON	
CY91F526JLCPMC			OFF	
CY91F525JWCPMC		ON	ON	
CY91F525JYCPMC			OFF	
CY91F525JJCPMC		OFF	ON	
CY91F525JLCPMC			OFF	
CY91F524JWCPMC		ON	ON	
CY91F524JYCPMC			OFF	
CY91F524JJCPMC		OFF	ON	
CY91F524JLCPMC			OFF	
CY91F523JWCPMC		ON	ON	
CY91F523JYCPMC			OFF	
CY91F523JJCPMC		OFF	ON	
CY91F523JLCPMC			OFF	
CY91F522JWCPMC		ON	ON	
CY91F522JYCPMC			OFF	
CY91F522JJCPMC		OFF	ON	
CY91F522JLCPMC			OFF	
CY91F526JSCPMC	None	ON	ON	
CY91F526JUCPMC			OFF	
CY91F526JHCPMC		OFF	ON	
CY91F526JKCPMC			OFF	
CY91F525JSCPMC		ON	ON	
CY91F525JUCPMC			OFF	
CY91F525JHCPMC		OFF	ON	
CY91F525JKCPMC			OFF	
CY91F524JSCPMC		ON	ON	
CY91F524JUCPMC			OFF	
CY91F524JHCPMC		OFF	ON	
CY91F524JKCPMC			OFF	
CY91F523JSCPMC		ON	ON	
CY91F523JUCPMC			OFF	
CY91F523JHCPMC		OFF	ON	
CY91F523JKCPMC			OFF	
CY91F522JSCPMC		ON	ON	
CY91F522JUCPMC			OFF	
CY91F522JHCPMC		OFF	ON	
CY91F522JKCPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526FWCPMC	Yes	ON	ON	LQI • 100 pin, Plastic
CY91F526FYCPMC			OFF	
CY91F526FJCPMC		OFF	ON	
CY91F526FLCPMC			OFF	
CY91F525FWCPMC		ON	ON	
CY91F525FYCPMC			OFF	
CY91F525FJCPMC		OFF	ON	
CY91F525FLCPMC			OFF	
CY91F524FWCPMC		ON	ON	
CY91F524FYCPMC			OFF	
CY91F524FJCPMC		OFF	ON	
CY91F524FLCPMC			OFF	
CY91F523FWCPMC		ON	ON	
CY91F523FYCPMC			OFF	
CY91F523FJCPMC		OFF	ON	
CY91F523FLCPMC			OFF	
CY91F522FWCPMC		ON	ON	
CY91F522FYCPMC			OFF	
CY91F522FJCPMC		OFF	ON	
CY91F522FLCPMC			OFF	
CY91F526FSCPMC	None	ON	ON	LQI • 100 pin, Plastic
CY91F526FUCPMC			OFF	
CY91F526FHCPMC		OFF	ON	
CY91F526FKCPMC			OFF	
CY91F525FSCPMC		ON	ON	
CY91F525FUCPMC			OFF	
CY91F525FHCPMC		OFF	ON	
CY91F525FKCPMC			OFF	
CY91F524FSCPMC		ON	ON	
CY91F524FUCPMC			OFF	
CY91F524FHCPMC		OFF	ON	
CY91F524FKCPMC			OFF	
CY91F523FSCPMC		ON	ON	
CY91F523FUCPMC			OFF	
CY91F523FHCPMC		OFF	ON	
CY91F523FKCPMC			OFF	
CY91F522FSCPMC		ON	ON	
CY91F522FUCPMC			OFF	
CY91F522FHCPMC		OFF	ON	
CY91F522FKCPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526DWCPMC	Yes	ON	ON	LQH • 80 pin, Plastic
CY91F526DYCPMC			OFF	
CY91F526DJCPMC		OFF	ON	
CY91F526DLCPMC			OFF	
CY91F525DWCPMC		ON	ON	
CY91F525DYCPMC			OFF	
CY91F525DJCPMC		OFF	ON	
CY91F525DLCPMC			OFF	
CY91F524DWCPMC		ON	ON	
CY91F524DYCPMC			OFF	
CY91F524DJCPMC		OFF	ON	
CY91F524DLCPMC			OFF	
CY91F523DWCPMC		ON	ON	
CY91F523DYCPMC			OFF	
CY91F523DJCPMC		OFF	ON	
CY91F523DLCPMC			OFF	
CY91F522DWCPMC		ON	ON	
CY91F522DYCPMC			OFF	
CY91F522DJCPMC		OFF	ON	
CY91F522DLCPMC			OFF	
CY91F526DSCPMC	None	ON	ON	
CY91F526DUCPMC			OFF	
CY91F526DHCPMC		OFF	ON	
CY91F526DKCPMC			OFF	
CY91F525DSCPMC		ON	ON	
CY91F525DUCPMC			OFF	
CY91F525DHCPMC		OFF	ON	
CY91F525DKCPMC			OFF	
CY91F524DSCPMC		ON	ON	
CY91F524DUCPMC			OFF	
CY91F524DHCPMC		OFF	ON	
CY91F524DKCPMC			OFF	
CY91F523DSCPMC		ON	ON	
CY91F523DUCPMC			OFF	
CY91F523DHCPMC		OFF	ON	
CY91F523DKCPMC			OFF	
CY91F522DSCPMC		ON	ON	
CY91F522DUCPMC			OFF	
CY91F522DHCPMC		OFF	ON	
CY91F522DKCPMC			OFF	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package ^{*2}
CY91F526BWCPMC1	Yes	ON	ON	LQD • 64 pin, Plastic
CY91F526BYCPMC1			OFF	
CY91F526BJCPMC1		OFF	ON	
CY91F526BLCPMC1			OFF	
CY91F525BWCPMC1		ON	ON	
CY91F525BYCPMC1			OFF	
CY91F525BJCPMC1		OFF	ON	
CY91F525BLCPMC1			OFF	
CY91F524BWCPMC1		ON	ON	
CY91F524BYCPMC1			OFF	
CY91F524BJCPMC1		OFF	ON	
CY91F524BLCPMC1			OFF	
CY91F523BWCPMC1		ON	ON	
CY91F523BYCPMC1			OFF	
CY91F523BJCPMC1		OFF	ON	
CY91F523BLCPMC1			OFF	
CY91F522BWCPMC1		ON	ON	
CY91F522BYCPMC1			OFF	
CY91F522BJCPMC1		OFF	ON	
CY91F522BLCPMC1			OFF	
CY91F526BSCPMC1	None	ON	ON	LQD • 64 pin, Plastic
CY91F526BUCPMC1			OFF	
CY91F526BHCPMC1		OFF	ON	
CY91F526BKCPMC1			OFF	
CY91F525BSCPMC1		ON	ON	
CY91F525BUCPMC1			OFF	
CY91F525BHCPMC1		OFF	ON	
CY91F525BKCPMC1			OFF	
CY91F524BSCPMC1		ON	ON	
CY91F524BUCPMC1			OFF	
CY91F524BHCPMC1		OFF	ON	
CY91F524BKCPMC1			OFF	
CY91F523BSCPMC1		ON	ON	
CY91F523BUCPMC1			OFF	
CY91F523BHCPMC1		OFF	ON	
CY91F523BKCPMC1			OFF	
CY91F522BSCPMC1		ON	ON	
CY91F522BUCPMC1			OFF	
CY91F522BHCPMC1		OFF	ON	
CY91F522BKCPMC1			OFF	

^{*1}: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.

^{*2}: For details of the package, see [Package Dimensions](#).

15. Ordering Information CY91F52xxxD

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526LWDPMC	Yes	ON	ON	LQP • 176 pin, Plastic
CY91F526LJDPMC		OFF	ON	
CY91F525LWDPMC		ON	ON	
CY91F525LJDPMC		OFF	ON	
CY91F524LWDPMC		ON	ON	
CY91F524LJDPMC		OFF	ON	
CY91F523LWDPMC		ON	ON	
CY91F523LJDPMC		OFF	ON	
CY91F522LWDPMC		ON	ON	
CY91F522LJDPMC		OFF	ON	
CY91F526LSDPMC	None	ON	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526LHDPMC		OFF	ON	
CY91F525LSDPMC		ON	ON	
CY91F525LHDPMC		OFF	ON	
CY91F524LSDPMC		ON	ON	
CY91F524LHDPMC		OFF	ON	
CY91F523LSDPMC		ON	ON	
CY91F523LHDPMC		OFF	ON	
CY91F522LSDPMC		ON	ON	
CY91F522LHDPMC		OFF	ON	
CY91F526KWDFPMC	Yes	ON	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526KJDFPMC		OFF	ON	
CY91F525KWDFPMC		ON	ON	
CY91F525KJDFPMC		OFF	ON	
CY91F524KWDFPMC		ON	ON	
CY91F524KJDFPMC		OFF	ON	
CY91F523KWDFPMC		ON	ON	
CY91F523KJDFPMC		OFF	ON	
CY91F522KWDFPMC		ON	ON	
CY91F522KJDFPMC		OFF	ON	
CY91F526KSDFPMC	None	ON	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526KHDFPMC		OFF	ON	
CY91F525KSDFPMC		ON	ON	
CY91F525KHDFPMC		OFF	ON	
CY91F524KSDFPMC		ON	ON	
CY91F524KHDFPMC		OFF	ON	
CY91F523KSDFPMC		ON	ON	
CY91F523KHDFPMC		OFF	ON	
CY91F522KSDFPMC		ON	ON	
CY91F522KHDFPMC		OFF	ON	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526KWDFMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4 mm) Plastic
CY91F526KJDPMC1		OFF	ON	
CY91F525KWDFMC1		ON	ON	
CY91F525KJDPMC1		OFF	ON	
CY91F524KWDFMC1		ON	ON	
CY91F524KJDPMC1		OFF	ON	
CY91F523KWDFMC1		ON	ON	
CY91F523KJDPMC1		OFF	ON	
CY91F522KWDFMC1		ON	ON	
CY91F522KJDPMC1		OFF	ON	
CY91F526KSDPMC1	None	ON	ON	LQM • 120 pin, Plastic
CY91F526KHDFMC1		OFF	ON	
CY91F525KSDPMC1		ON	ON	
CY91F525KHDFMC1		OFF	ON	
CY91F524KSDPMC1		ON	ON	
CY91F524KHDFMC1		OFF	ON	
CY91F523KSDPMC1		ON	ON	
CY91F523KHDFMC1		OFF	ON	
CY91F522KSDPMC1		ON	ON	
CY91F522KHDFMC1		OFF	ON	
CY91F526JWDPMC	Yes	ON	ON	LQM • 120 pin, Plastic
CY91F526JJDFMC		OFF	ON	
CY91F525JWDPMC		ON	ON	
CY91F525JJDFMC		OFF	ON	
CY91F524JWDPMC		ON	ON	
CY91F524JJDFMC		OFF	ON	
CY91F523JWDPMC		ON	ON	
CY91F523JJDFMC		OFF	ON	
CY91F522JWDPMC		ON	ON	
CY91F522JJDFMC		OFF	ON	
CY91F526JSDFMC	None	ON	ON	LQM • 120 pin, Plastic
CY91F526JHDFMC		OFF	ON	
CY91F525JSDFMC		ON	ON	
CY91F525JHDFMC		OFF	ON	
CY91F524JSDFMC		ON	ON	
CY91F524JHDFMC		OFF	ON	
CY91F523JSDFMC		ON	ON	
CY91F523JHDFMC		OFF	ON	
CY91F522JSDFMC		ON	ON	
CY91F522JHDFMC		OFF	ON	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526FWDPMC	Yes	ON	ON	LQI • 100 pin, Plastic
CY91F526FJDPMC		OFF	ON	
CY91F525FWDPMC		ON	ON	
CY91F525FJDPMC		OFF	ON	
CY91F524FWDPMC		ON	ON	
CY91F524FJDPMC		OFF	ON	
CY91F523FWDPMC		ON	ON	
CY91F523FJDPMC		OFF	ON	
CY91F522FWDPMC		ON	ON	
CY91F522FJDPMC		OFF	ON	
CY91F526FSDPMC	None	ON	ON	LQH • 80 pin, Plastic
CY91F526FHDFPMC		OFF	ON	
CY91F525FSDPMC		ON	ON	
CY91F525FHDFPMC		OFF	ON	
CY91F524FSDPMC		ON	ON	
CY91F524FHDFPMC		OFF	ON	
CY91F523FSDPMC		ON	ON	
CY91F523FHDFPMC		OFF	ON	
CY91F522FSDPMC		ON	ON	
CY91F522FHDFPMC		OFF	ON	
CY91F526DWDFPMC	Yes	ON	ON	LQH • 80 pin, Plastic
CY91F526DJDFPMC		OFF	ON	
CY91F525DWDFPMC		ON	ON	
CY91F525DJDFPMC		OFF	ON	
CY91F524DWDFPMC		ON	ON	
CY91F524DJDFPMC		OFF	ON	
CY91F523DWDFPMC		ON	ON	
CY91F523DJDFPMC		OFF	ON	
CY91F522DWDFPMC		ON	ON	
CY91F522DJDFPMC		OFF	ON	
CY91F526DSDFPMC	None	ON	ON	LQH • 80 pin, Plastic
CY91F526DHDFPMC		OFF	ON	
CY91F525DSDFPMC		ON	ON	
CY91F525DHDFPMC		OFF	ON	
CY91F524DSDFPMC		ON	ON	
CY91F524DHDFPMC		OFF	ON	
CY91F523DSDFPMC		ON	ON	
CY91F523DHDFPMC		OFF	ON	
CY91F522DSDFPMC		ON	ON	
CY91F522DHDFPMC		OFF	ON	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526BWDFMC1	Yes	ON	ON	LQD • 64 pin, Plastic
CY91F526BJDFMC1		OFF	ON	
CY91F525BWDFMC1		ON	ON	
CY91F525BJDFMC1		OFF	ON	
CY91F524BWDFMC1		ON	ON	
CY91F524BJDFMC1		OFF	ON	
CY91F523BWDFMC1		ON	ON	
CY91F523BJDFMC1		OFF	ON	
CY91F522BWDFMC1		ON	ON	
CY91F522BJDFMC1		OFF	ON	
CY91F526BSDDFMC1	None	ON	ON	LQD • 64 pin, Plastic
CY91F526BHDFMC1		OFF	ON	
CY91F525BSDDFMC1		ON	ON	
CY91F525BHDFMC1		OFF	ON	
CY91F524BSDDFMC1		ON	ON	
CY91F524BHDFMC1		OFF	ON	
CY91F523BSDDFMC1		ON	ON	
CY91F523BHDFMC1		OFF	ON	
CY91F522BSDDFMC1		ON	ON	
CY91F522BHDFMC1		OFF	ON	

*: For details of the package, see [Package Dimensions](#).

16. Ordering Information CY91F52xxxE

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526LWEPMC	Yes	ON	ON	LQP • 176 pin, Plastic
CY91F526LJEPMC		OFF	ON	
CY91F525LWEPMC		ON	ON	
CY91F525LJEPMC		OFF	ON	
CY91F524LWEPMC		ON	ON	
CY91F524LJEPMC		OFF	ON	
CY91F523LWEPMC		ON	ON	
CY91F523LJEPMC		OFF	ON	
CY91F522LWEPMC		ON	ON	
CY91F522LJEPMC		OFF	ON	
CY91F526LSEPMC	None	ON	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526LHEPMC		OFF	ON	
CY91F526LKEPMC		OFF	OFF	
CY91F525LSEPMC		ON	ON	
CY91F525LHEPMC		OFF	ON	
CY91F524LSEPMC		ON	ON	
CY91F524LHEPMC		OFF	ON	
CY91F523LSEPMC		ON	ON	
CY91F523LHEPMC		OFF	ON	
CY91F522LSEPMC		ON	ON	
CY91F522LHEPMC	Yes	OFF	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526KWEPMC		ON	ON	
CY91F526KJEPMC		OFF	ON	
CY91F525KWEPMC		ON	ON	
CY91F525KJEPMC		OFF	ON	
CY91F524KWEPMC		ON	ON	
CY91F524KJEPMC		OFF	ON	
CY91F523KWEPMC		ON	ON	
CY91F523KJEPMC		OFF	ON	
CY91F522KWEPMC		ON	ON	
CY91F522KJEPMC	None	OFF	ON	LQS • 144 pin, (Lead pitch 0.5 mm) Plastic
CY91F526KSEPMC		ON	ON	
CY91F526KHEPMC		OFF	ON	
CY91F525KSEPMC		ON	ON	
CY91F525KHEPMC		OFF	ON	
CY91F524KSEPMC		ON	ON	
CY91F524KHEPMC		OFF	ON	
CY91F523KSEPMC		ON	ON	
CY91F523KHEPMC		OFF	ON	
CY91F522KSEPMC		ON	ON	
CY91F522KHEPMC		OFF	ON	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526KWEPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4 mm) Plastic
CY91F526KJEPMC1		OFF	ON	
CY91F525KWEPMC1		ON	ON	
CY91F525KJEPMC1		OFF	ON	
CY91F524KWEPMC1		ON	ON	
CY91F524KJEPMC1		OFF	ON	
CY91F523KWEPMC1		ON	ON	
CY91F523KJEPMC1		OFF	ON	
CY91F522KWEPMC1		ON	ON	
CY91F522KJEPMC1		OFF	ON	
CY91F526KSEPMC1	None	ON	ON	LQM • 120 pin, Plastic
CY91F526KHEPMC1		OFF	ON	
CY91F525KSEPMC1		ON	ON	
CY91F525KHEPMC1		OFF	ON	
CY91F524KSEPMC1		ON	ON	
CY91F524KHEPMC1		OFF	ON	
CY91F523KSEPMC1		ON	ON	
CY91F523KHEPMC1		OFF	ON	
CY91F522KSEPMC1		ON	ON	
CY91F522KHEPMC1		OFF	ON	
CY91F526JWEPMC	Yes	ON	ON	LQM • 120 pin, Plastic
CY91F526JJEPMC		OFF	ON	
CY91F525JWEPMC		ON	ON	
CY91F525JJEPMC		OFF	ON	
CY91F524JWEPMC		ON	ON	
CY91F524JJEPMC		OFF	ON	
CY91F523JWEPMC		ON	ON	
CY91F523JJEPMC		OFF	ON	
CY91F522JWEPMC		ON	ON	
CY91F522JJEPMC		OFF	ON	
CY91F526JSEPMC	None	ON	ON	LQM • 120 pin, Plastic
CY91F526JHEPMC		OFF	ON	
CY91F525JSEPMC		ON	ON	
CY91F525JHEPMC		OFF	ON	
CY91F524JSEPMC		ON	ON	
CY91F524JHEPMC		OFF	ON	
CY91F523JSEPMC		ON	ON	
CY91F523JHEPMC		OFF	ON	
CY91F522JSEPMC		ON	ON	
CY91F522JHEPMC		OFF	ON	

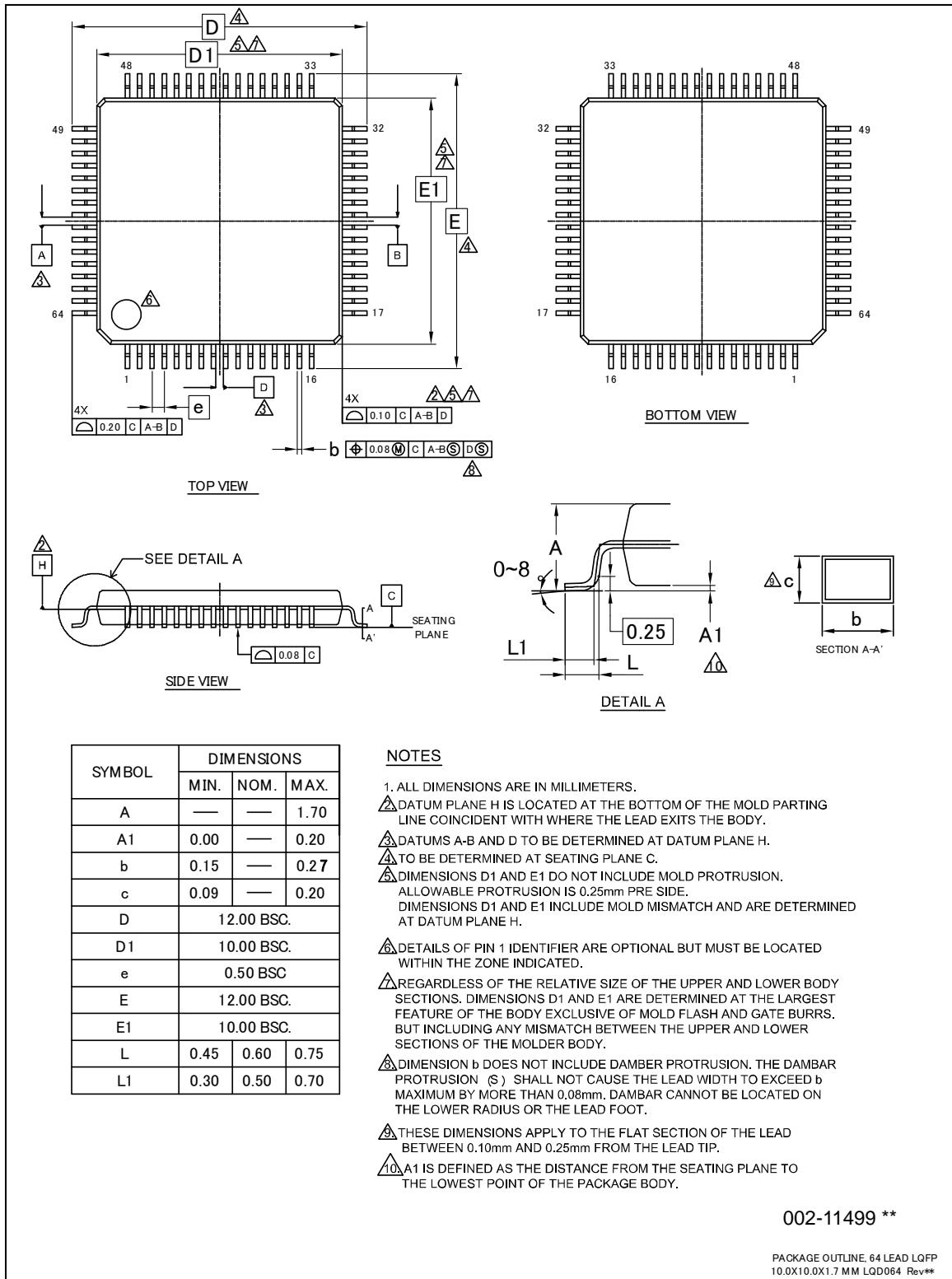
Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526FWEPMC	Yes	ON	ON	LQI • 100 pin, Plastic
CY91F526FJEPMC		OFF	ON	
CY91F525FWEPMC		ON	ON	
CY91F525FJEPMC		OFF	ON	
CY91F524FWEPMC		ON	ON	
CY91F524FJEPMC		OFF	ON	
CY91F523FWEPMC		ON	ON	
CY91F523FJEPMC		OFF	ON	
CY91F522FWEPMC		ON	ON	
CY91F522FJEPMC		OFF	ON	
CY91F526FSEPMC	None	ON	ON	LQH • 80 pin, Plastic
CY91F526FHEPMC		OFF	ON	
CY91F525FSEPMC		ON	ON	
CY91F525FHEPMC		OFF	ON	
CY91F524FSEPMC		ON	ON	
CY91F524FHEPMC		OFF	ON	
CY91F523FSEPMC		ON	ON	
CY91F523FHEPMC		OFF	ON	
CY91F522FSEPMC		ON	ON	
CY91F522FHEPMC		OFF	ON	
CY91F526DWEPMC	Yes	ON	ON	LQH • 80 pin, Plastic
CY91F526DJEPMC		OFF	ON	
CY91F525DWEPMC		ON	ON	
CY91F525DJEPMC		OFF	ON	
CY91F524DWEPMC		ON	ON	
CY91F524DJEPMC		OFF	ON	
CY91F523DWEPMC		ON	ON	
CY91F523DJEPMC		OFF	ON	
CY91F522DWEPMC		ON	ON	
CY91F522DJEPMC		OFF	ON	
CY91F526DSEPMC	None	ON	ON	LQH • 80 pin, Plastic
CY91F526DHEPMC		OFF	ON	
CY91F525DSEPMC		ON	ON	
CY91F525DHEPMC		OFF	ON	
CY91F524DSEPMC		ON	ON	
CY91F524DHEPMC		OFF	ON	
CY91F523DSEPMC		ON	ON	
CY91F523DHEPMC		OFF	ON	
CY91F522DSEPMC		ON	ON	
CY91F522DHEPMC		OFF	ON	

Part Number	Sub Clock	CSV Initial Value	LVD Initial Value	Package*
CY91F526BWEPMC1	Yes	ON	ON	LQD • 64 pin, Plastic
CY91F526BJEPMC1		OFF	ON	
CY91F525BWEPMC1		ON	ON	
CY91F525BJEPMC1		OFF	ON	
CY91F524BWEPMC1		ON	ON	
CY91F524BJEPMC1		OFF	ON	
CY91F523BWEPMC1		ON	ON	
CY91F523BJEPMC1		OFF	ON	
CY91F522BWEPMC1		ON	ON	
CY91F522BJEPMC1		OFF	ON	
CY91F526BSEPMC1	None	ON	ON	LQD • 64 pin, Plastic
CY91F526BHEPMC1		OFF	ON	
CY91F525BSEPMC1		ON	ON	
CY91F525BHEPMC1		OFF	ON	
CY91F524BSEPMC1		ON	ON	
CY91F524BHEPMC1		OFF	ON	
CY91F523BSEPMC1		ON	ON	
CY91F523BHEPMC1		OFF	ON	
CY91F522BSEPMC1		ON	ON	
CY91F522BHEPMC1		OFF	ON	

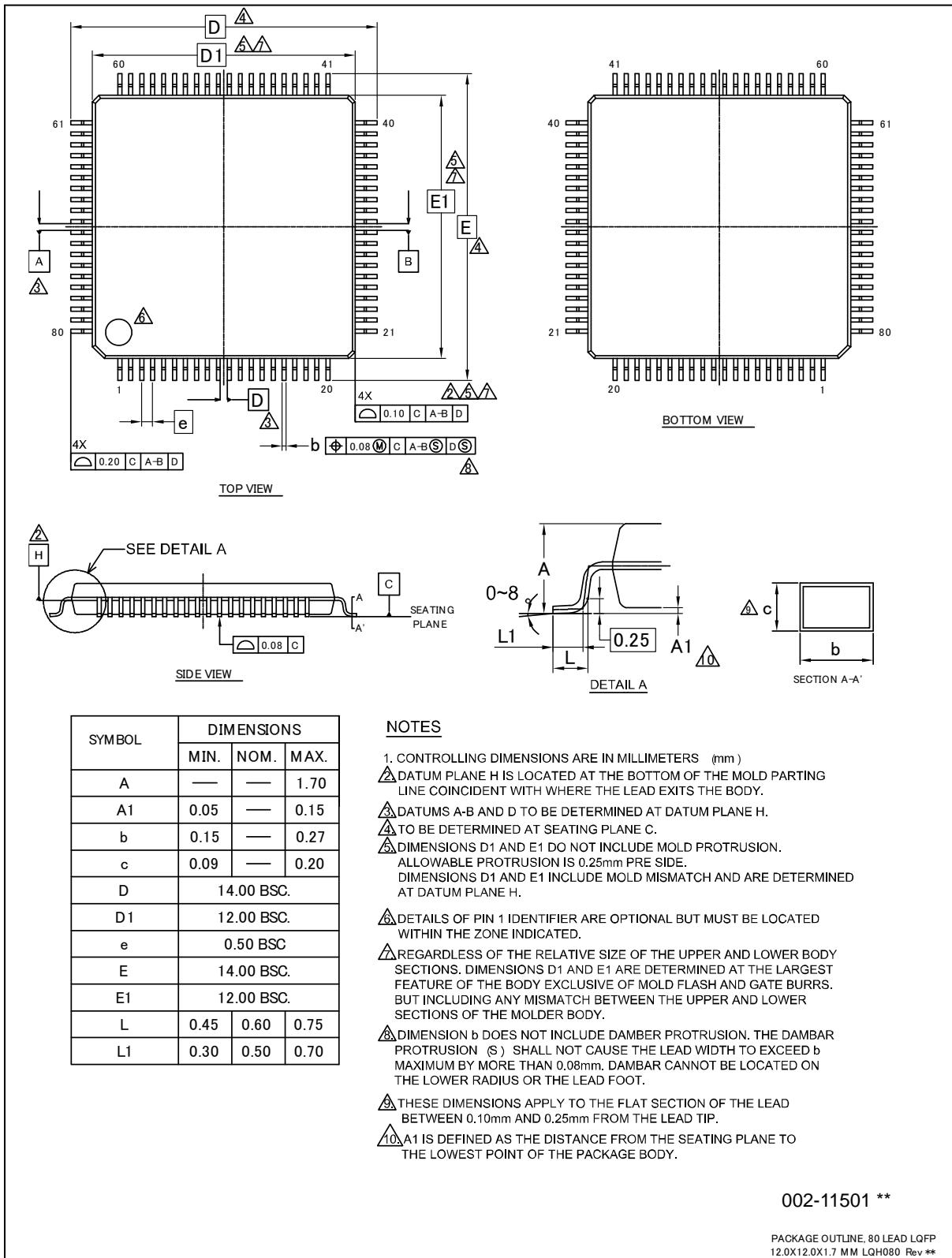
*: For details of the package, see [Package Dimensions](#).

17. Package Dimensions

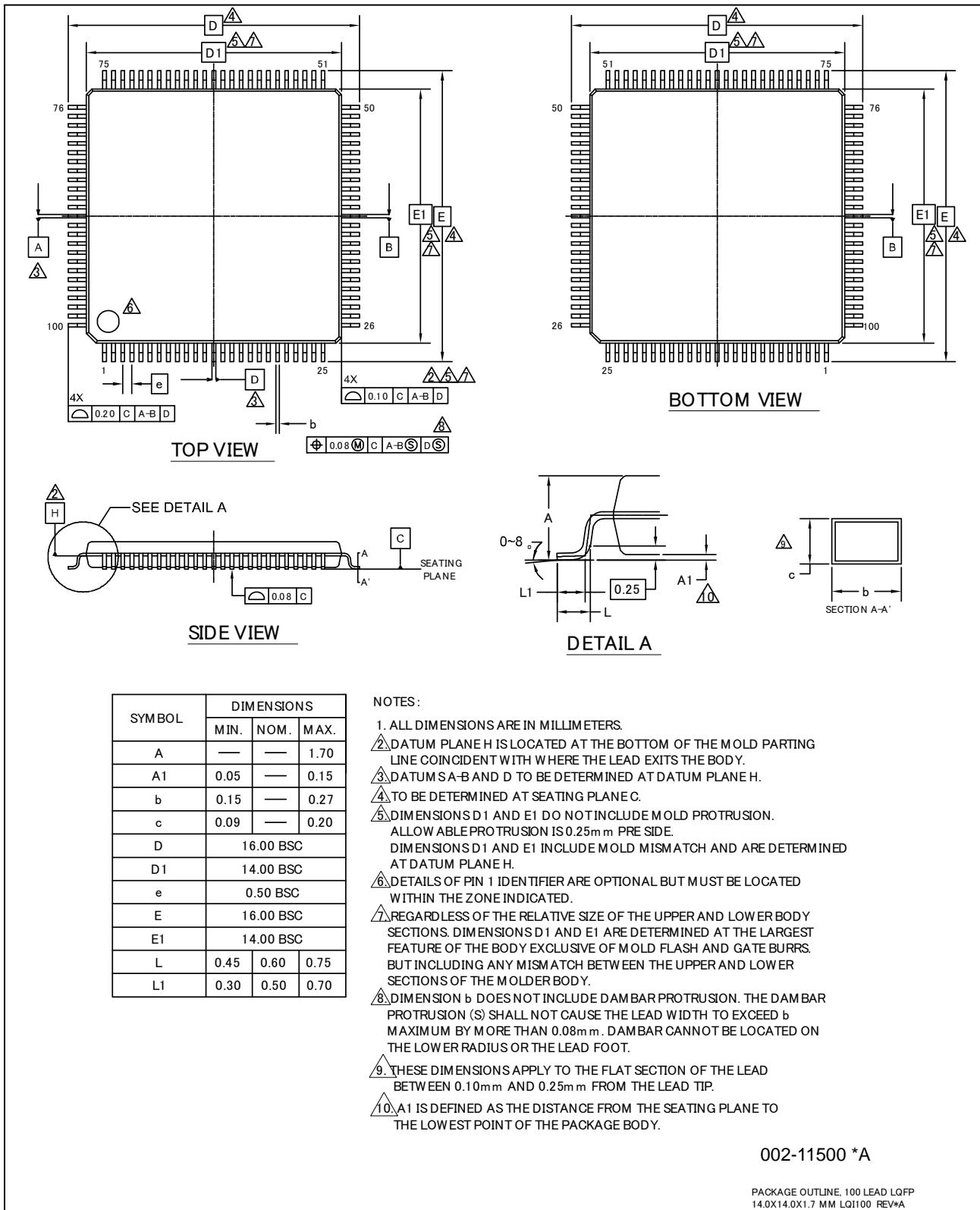
Package Type	Package Code
LQFP 64pin	LQD064



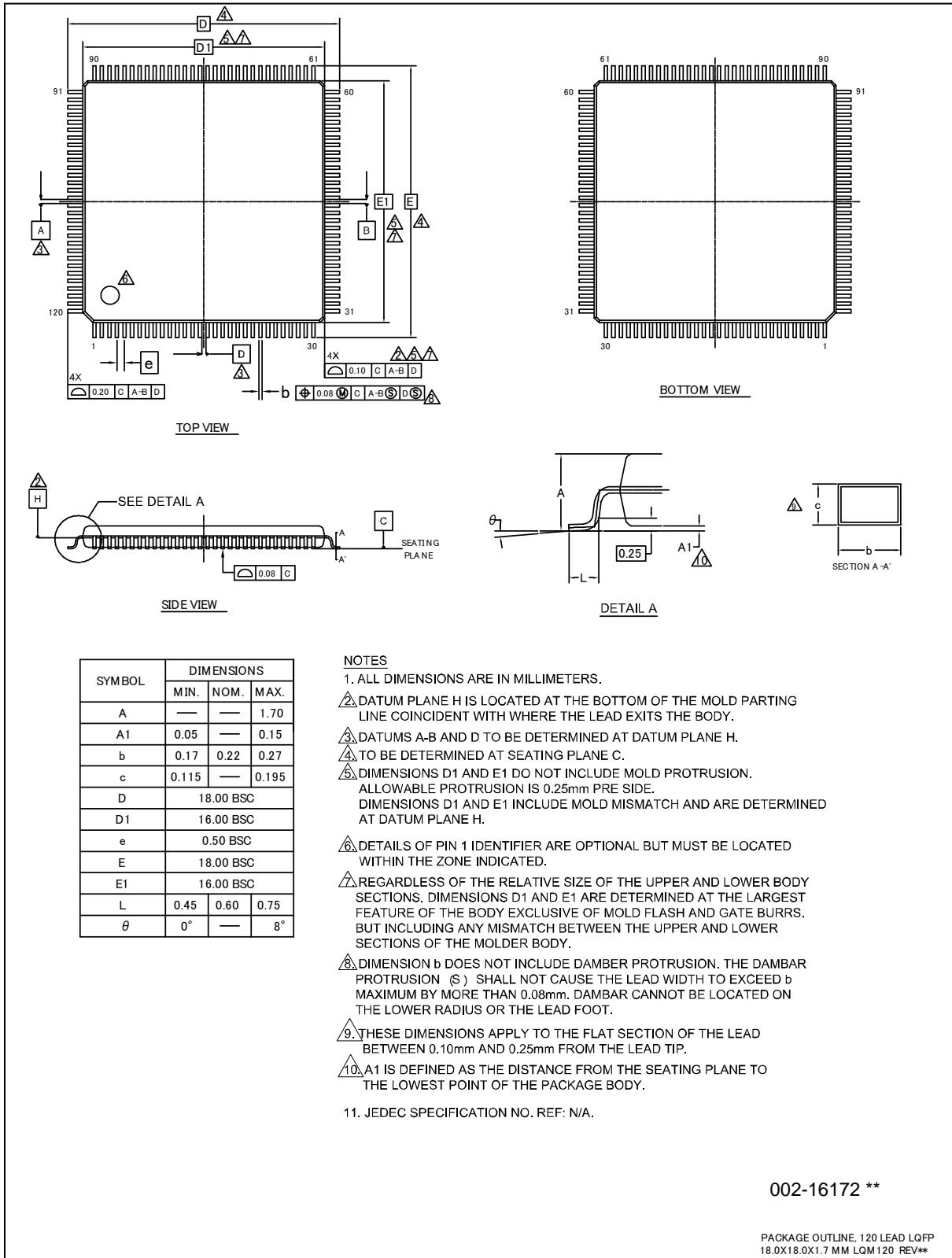
Package Type	Package Code
LQFP 80pin	LQH080



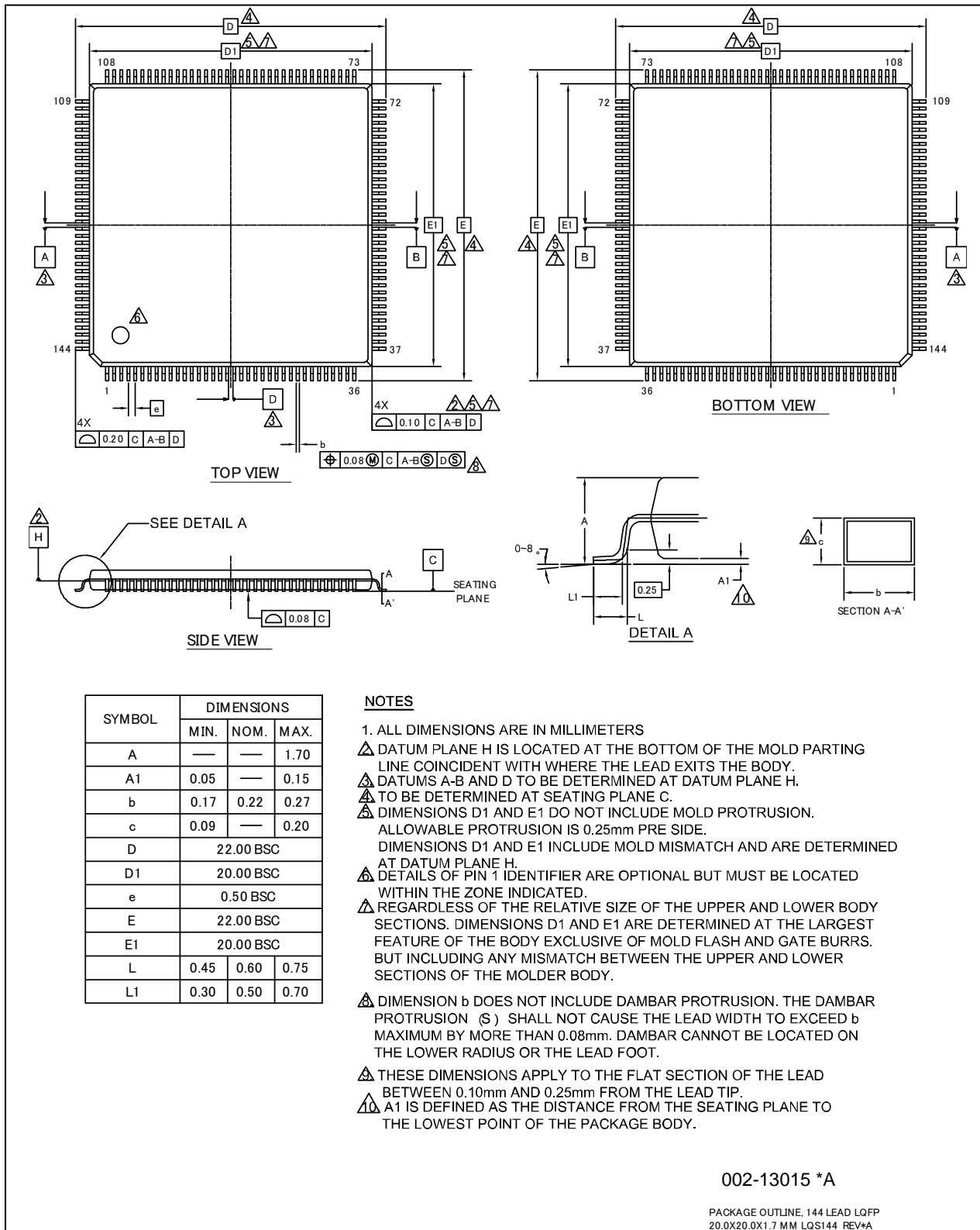
Package Type	Package Code
LQFP 100pin	LQI100



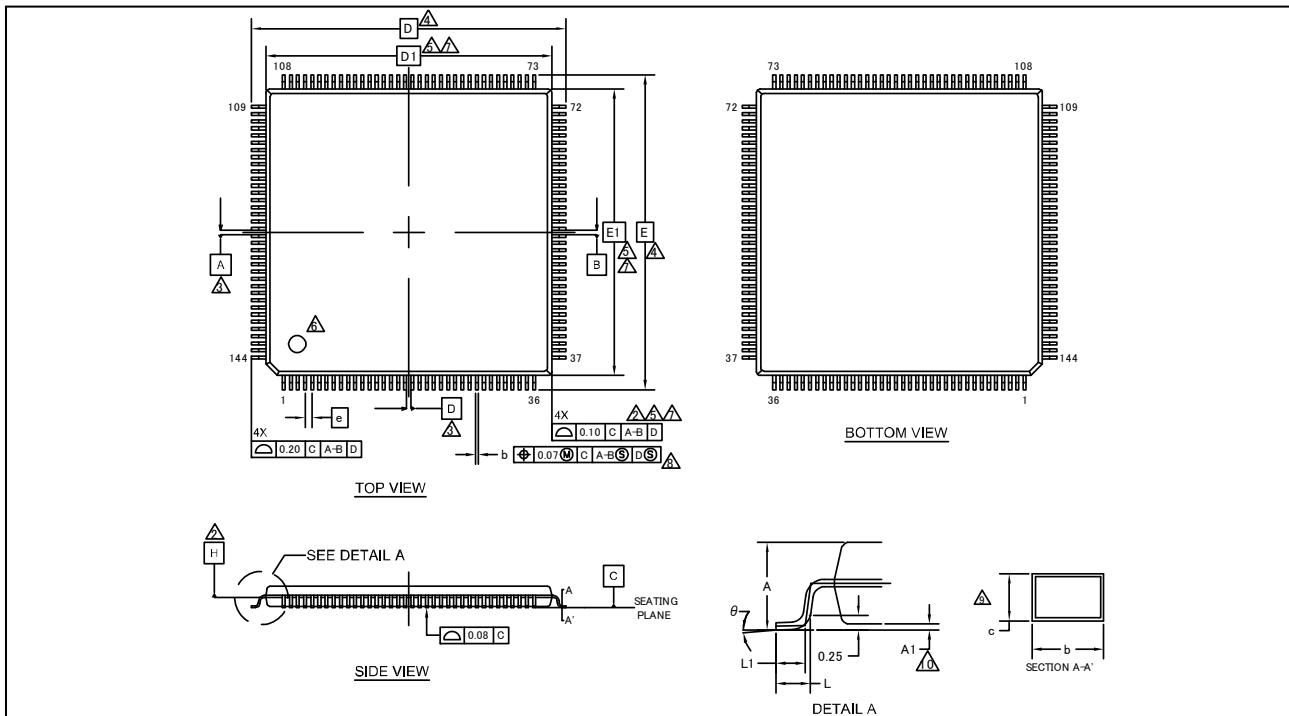
Package Type	Package Code
LQFP 120pin	LQM120



Package Type	Package Code
LQFP 144pin	LQS144



Package Type	Package Code
LQFP 144pin	LQN144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.145	0.18	0.215
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.40 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

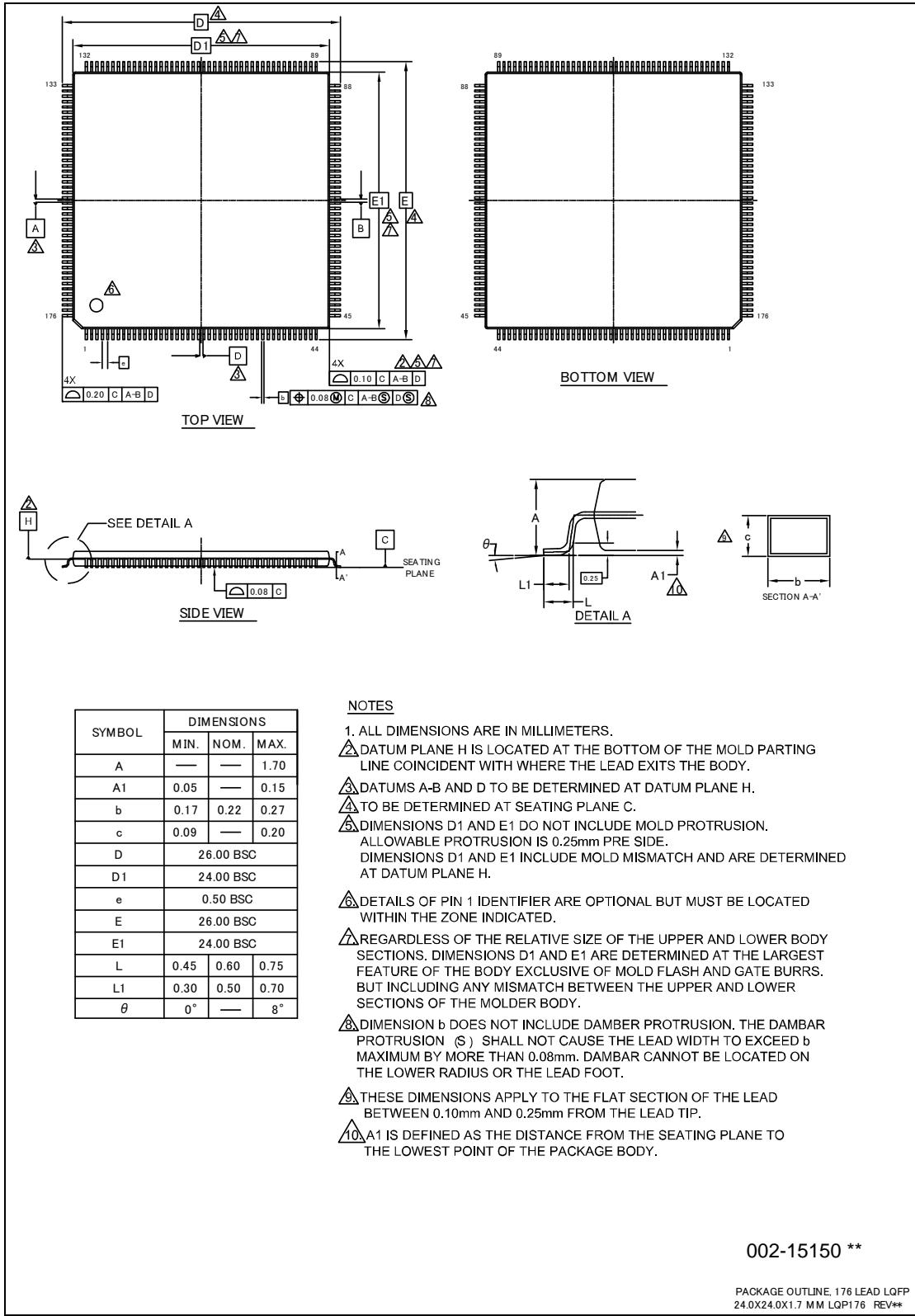
NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-14045 **

PACKAGE OUTLINE, 144 LEAD LQFP
16.0X16.0X1.7 MM LQN144 REV**

Package Type	Package Code
LQFP 176pin	LQP176



18. Errata

This section describes the errata for the CY91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
CY91F522B/D/F/J/K/L
CY91F523B/D/F/J/K/L
CY91F524B/D/F/J/K/L
CY91F525B/D/F/J/K/L
CY91F526B/D/F/J/K/L

CY91F522/3/4/5/6 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available CY91520 Series devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Power-on Conditions is not enough in the Datasheet Specification	CY91F522B/D/F/J/K/L CY91F523B/D/F/J/K/L CY91F524B/D/F/J/K/L	B, C	Will be fixed in production silicon version D, E
[2]. Limitation for Watch mode (power off)	CY91F525B/D/F/J/K/L CY91F526B/D/F/J/K/L		

1. Power-on Conditions is not enough in the Datasheet Specification

■ Problem Definition

If the Power-On-Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

■ Parameters Affected

t_{OFF} for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

■ Trigger Condition

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

- (1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})
- (2) VCC Power ramp rate less than 4 mV/ μ s (dV/dt) until a voltage level for a safe Power-On detection is reached
- (3) C-pin voltage is below 60 mV when VCC is turned on again

■ Scope of Impact

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

■ Workaround

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

- (1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})
- (2) VCC Power ramp rate is less than 4 mV/ μ s (dV/dt) until a voltage level for a safe Power-On detection is reached
- (3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will releases new version D, so Cypress recommends the version D for CY91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

■ Fix Status

Will be fixed in production silicon version D, E

2. Limitation for Watch mode (power off)**■ Problem Definition**

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

■ Trigger Conditions

- (1) Using the watch mode (power off)
- (2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '16' to '30', or using NMIX pin as source for recovering from the watch mode (power off)
- (3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
(*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 μ s to 100 μ s

■ Scope of Impact

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

WTCRH, WTCRM, WTCRL

CSELR.SCEN

CMONR.SCRDY

CCRTSELR.CST

CCRTSELR.CSC

■ Workaround

It is necessary to satisfy the below both conditions of (1) and (2).

- (1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '31', before CPU state changes to the watch mode (power off)
- (2) Don't use NMIX pin as source for recovering from the watch mode (power off)

■ Fix Status

Will not be planned

19. Major Changes

Spansion Publication Number: MB91F526L_DS705-00011

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
3	■FEATURES	<p>Corrected the following description. 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input ↓ 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input</p>
33 to 36	■I/O CIRCUIT TYPE	<p>Corrected the following description to "Type F, G, I, J, K, M". Schmitt input → CMOS hysteresis input Corrected the following description to "Type D, E". I²C Schmitt input → I²C hysteresis input</p>
44 to 49	■BLOCK DIAGRAM	<p>Corrected the following description.</p> <ul style="list-style-type: none"> •MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B •MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D •MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F •MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J •MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K •MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L
138	■ELECTRICAL CHARACTERISTICS 2. Recommended operating conditions	<p>Added the following description.</p> <p>*1 : When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset</p>
139,140	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C ". Max 1420µA → Max 2000µA
139	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	<p>Corrected the value of "Power supply voltage range". (TA:-40°C to +105°C, Vcc=AVcc=2.7V to 5.5V, VSS=AVSS=0.0V) ↓ (TA:-40°C to +105°C, Vcc=AVcc=5.0V±10%/3.3V±0.3V, Vss=AVss=0.0V)</p>
140,141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	<p>Corrected the value of "Power supply voltage range". (TA:-40°C to +125°C, Vcc=AVcc=2.7V to 5.5V, VSS=AVSS=0.0V) ↓ (TA:-40°C to +125°C, Vcc=AVcc=5.0V±10%/3.3V±0.3V, Vss=AVss=0.0V)</p>
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of " Pull-up resistance R _{UP1} ". Vcc=3.3V±0.3V Min 49 Max 140 → Min 45 Max 140
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the following description. Pull-up resistance R _{UP2} Port pin other than P035,041,093,122 → P073,074,076,077
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of " Pull-up resistance R _{UP2} ". VCC=5.0V±10% Min 25 Max 100 → Min 25 Max 60 VCC=3.3V±0.3V Min 49 Max 140 → Min 33 Max 90
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	<p>Added the value of " Pull-up resistance R_{UP3}". Pin name : Port pin other than P035,041,073,074,076,077,093,122 VCC=5.0V±10% Min 25 Max 100 VCC=3.3V±0.3V Min 45 Max 140</p>

Page	Section	Change Results
150,152, 154,156	ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4) $SCK \downarrow \Rightarrow SOT$ delay time t_{SLOVI} (4-1-2),(4-1-3) $SCK \uparrow \Rightarrow SOT$ delay time t_{SHOVI} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300
150,152, 154,156	ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4)Valid SIN $\Rightarrow SCK \uparrow$ setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN $\Rightarrow SCK \downarrow$ setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max -
150,152, 154,156	ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-4) $SCK \downarrow \Rightarrow SOT$ delay time t_{SLOVE} (4-1-2),(4-1-3) $SCK \uparrow \Rightarrow SOT$ delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300
150,152, 154,156	ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4)	(4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_F Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11 Value: Min - Max 5

Page	Section	Change Results
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	<p>(4-1-5)$SCS \downarrow \Rightarrow SCK \downarrow$ setup time t_{CS51} (4-1-6)$SCS \downarrow \Rightarrow SCK \uparrow$ setup time t_{CS51} (4-1-7)$SCS \uparrow \Rightarrow SCK \downarrow$ setup time t_{CS51} (4-1-8)$SCS \uparrow \Rightarrow SCK \uparrow$ setup time t_{CS51}</p> <p>Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CS5U}+0$ Max $t_{CS5U}+50$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CS5U}-50$ Max $t_{CS5U}+0$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $t_{CS5U}-50$ Max $t_{CS5U}+300$</p>
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	<p>(4-1-5)$SCK \uparrow \Rightarrow SCS \uparrow$hold time t_{CSH1} (4-1-6)$SCK \downarrow \Rightarrow SCS \uparrow$hold time t_{CSH1} (4-1-7)$SCK \uparrow \Rightarrow SCS \downarrow$hold time t_{CSH1} (4-1-8)$SCK \downarrow \Rightarrow SCS \downarrow$hold time t_{CSH1}</p> <p>Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSHD}-50$ Max $t_{CSHD}+0$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSHD}-10$ Max $t_{CSHD}+50$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $t_{CSHD}-300$ Max $t_{CSHD}+50$</p>
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	<p>(4-1-5),(4-1-6)$SCS \downarrow \Rightarrow SOT$ delay time t_{DSE} (4-1-7),(4-1-8)$SCS \uparrow \Rightarrow SOT$ delay time t_{DSE}</p> <p>Corrected the following description. Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1 to SOT11 Value: Min - Max 40 ↓ Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1,SOT2,SOT5 to SOT11 Value: Min - Max 40 Pin name: SCS3,SCS40 to SCS43 SOT3,SOT4 Value: Min - Max 300</p>

Page	Section	Change Results
159,162, 165,168	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5)SCK \downarrow ⇒SCS \downarrow clock switch time tscs (4-1-6)SCK \uparrow ⇒SCS \downarrow clock switch time tscs (4-1-7)SCK \downarrow ⇒SCS \uparrow clock switch time tscs (4-1-8)SCK \uparrow ⇒SCS \uparrow clock switch time tscs Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min 3t _{CPP} +0 Max 3t _{CPP} +50 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min 3t _{CPP} -10 Max 3t _{CPP} +50 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min 3t _{CPP} -300 Max 3t _{CPP} +50
159,162, 165,168	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	Added the following description. Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Added the value of "Total error". Total error value Min – Typ – Max ±12 LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Added the following description. Parameter : Power supply current I _A AVCC*3 *3: The power supply current described only current value on A/D converter. The total Avcc current value must be calculated the power supply current for A/D converter and D/A converter.
188	■ELECTRICAL CHARACTERISTICS 7.D/A Converter	Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter.
187	■ELECTRICAL CHARACTERISTICS 6.Flash memory	Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing Tj<+105°C"

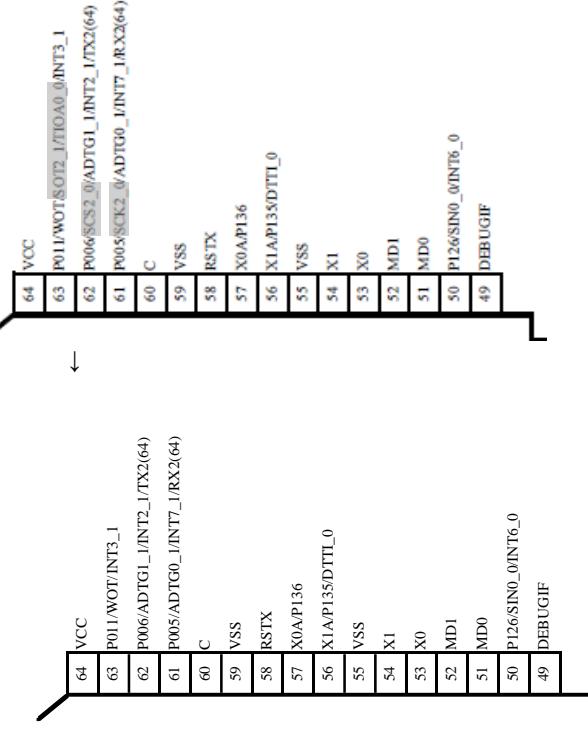
Page	Section	Change Results
188	■ELECTRICAL CHARACTERISTICS 7.D/A Converter	Corrected the following description. Parameter : Power supply current Symbol IA Pin name AV _{cc} Symbol IAH Pin name AV _{cc} ↓ Symbol IA Pin name AVCC Symbol IAH Pin name AVCC
190	■EXAMPLE CHARACTERISTICS	Corrected the following description. Watch mode
192	■ORDERING INFORMATION	Corrected the following description. ■ORDERING INFORMATION ↓ ■ORDERING INFORMATION MB91F52xxxB ^{*1} Package ↓ Package ^{*2}
198	■ORDERING INFORMATION	Added the following description. * ¹ : It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
198	■ORDERING INFORMATION	Corrected the following description. For details of the package, see "■ PACKAGE DIMENSIONS ". ↓ * ² : For details of the package, see "■ PACKAGE DIMENSIONS ".
199 to 205	■ORDERING INFORMATION	Added the following description. ■ORDERING INFORMATION MB91F52xxxC
-	-	Company name and layout design change

Page	Section	Change Results				
Cypress Document Number: 002-04662						
Rev *B						
1	■Features	<p>Corrected the following description.</p> <ul style="list-style-type: none"> · Clock generation (equipped with SSCG function) <ul style="list-style-type: none"> · Main oscillation (4MHz to 16MHz) · Sub oscillation (32kHz to 100kHz) or none sub oscillation · PLL multiplication rate : 1 to 20 times <p style="text-align: center;">↓</p> <ul style="list-style-type: none"> · Clock generation (equipped with SSCG function) <ul style="list-style-type: none"> · Main oscillation (4MHz to 16MHz) · Sub oscillation (32kHz) or no sub oscillation · PLL multiplication rate : 1 to 20 times <p style="background-color: #e0e0e0; padding: 2px;">• Equipped with a 100kHz CR oscillator</p>				
2	■Features	<p>Corrected the following description.</p> <ul style="list-style-type: none"> · Base timer : Max. 2 channels <ul style="list-style-type: none"> · 16-bit timer · Any of four PWM/PPG/PWC/reload timer functions can be selected and used · A 32-bit timer can be used in 2 channels of cascade mode <p style="text-align: center;">↓</p> <ul style="list-style-type: none"> · Base timer : Max. 2 channels <ul style="list-style-type: none"> · 16-bit timer · Any of four PWM/PPG/PWC/reload timer functions can be selected and used · As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascaded mode 				
6	■Product Lineup	<p>Corrected the following description for Product lineup comparison(64 pin).</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Multi-Function Serial Interface</td> <td style="padding: 2px; text-align: center;">8ch</td> </tr> </table> <p style="text-align: center;">↓</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Multi-Function Serial Interface</td> <td style="padding: 2px; text-align: center;">8ch^{*1}</td> </tr> </table>	Multi-Function Serial Interface	8ch	Multi-Function Serial Interface	8ch ^{*1}
Multi-Function Serial Interface	8ch					
Multi-Function Serial Interface	8ch ^{*1}					
6	■Product Lineup	<p>Added the following sentences under Product lineup comparison(64 pin)</p> <p style="background-color: #e0e0e0; padding: 2px;">*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).</p>				
7	■Product Lineup	<p>Corrected the following description for Product lineup comparison(80 pin).</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Multi-Function Serial Interface</td> <td style="padding: 2px; text-align: center;">9ch</td> </tr> </table> <p style="text-align: center;">↓</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Multi-Function Serial Interface</td> <td style="padding: 2px; text-align: center;">9ch^{*1}</td> </tr> </table>	Multi-Function Serial Interface	9ch	Multi-Function Serial Interface	9ch ^{*1}
Multi-Function Serial Interface	9ch					
Multi-Function Serial Interface	9ch ^{*1}					
7	■Product Lineup	<p>Added the following sentences under Product lineup comparison(80 pin)</p> <p style="background-color: #e0e0e0; padding: 2px;">*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).</p>				
8	■Product Lineup	<p>Corrected the following description for Product lineup comparison(100 pin).</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Multi-Function Serial Interface</td> <td style="padding: 2px; text-align: center;">12ch</td> </tr> </table> <p style="text-align: center;">↓</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Multi-Function Serial Interface</td> <td style="padding: 2px; text-align: center;">12ch^{*1}</td> </tr> </table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch ^{*1}
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch ^{*1}					
8	■Product Lineup	<p>Added the following sentences under Product lineup comparison(100 pin)</p> <p style="background-color: #e0e0e0; padding: 2px;">*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).</p>				

Page	Section	Change Results				
9	■Product Lineup	<p>Corrected the following description for Product lineup comparison(120 pin).</p> <table border="1"> <tr> <td>Multi-Function Serial Interface</td> <td>12ch</td> </tr> </table> <p style="text-align: center;">↓</p> <table border="1"> <tr> <td>Multi-Function Serial Interface</td> <td>12ch*1</td> </tr> </table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
9	■Product Lineup	<p>Added the following sentences under Product lineup comparison(120 pin)</p> <p>*1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).</p> <p>Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).</p>				
10	■Product Lineup	<p>Corrected the following description for Product lineup comparison(144 pin).</p> <table border="1"> <tr> <td>Multi-Function Serial Interface</td> <td>12ch</td> </tr> </table> <p style="text-align: center;">↓</p> <table border="1"> <tr> <td>Multi-Function Serial Interface</td> <td>12ch*1</td> </tr> </table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
10	■Product Lineup	<p>Added the following sentences under Product lineup comparison(144 pin)</p> <p>*1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).</p> <p>Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).</p>				
11	■Product Lineup	<p>Corrected the following description for Product lineup comparison(176 pin).</p> <table border="1"> <tr> <td>Multi-Function Serial Interface</td> <td>12ch</td> </tr> </table> <p style="text-align: center;">↓</p> <table border="1"> <tr> <td>Multi-Function Serial Interface</td> <td>12ch*1</td> </tr> </table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
11	■Product Lineup	<p>Added the following sentences under Product lineup comparison(176 pin)</p> <p>*1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).</p> <p>Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).</p>				

Page	Section	Change Results																																																																
13	■Pin Assignment MB91F52xB	<p>Signals indicated by the shading below deleted in Figure. - Left side</p> <p style="text-align: center;">↓</p> <table style="margin-left: auto; margin-right: auto;"> <tr><td>VSS</td><td>1</td></tr> <tr><td>P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1</td><td>2</td></tr> <tr><td>P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0</td><td>3</td></tr> <tr><td>P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1</td><td>4</td></tr> <tr><td>P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1</td><td>5</td></tr> <tr><td>P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2</td><td>6</td></tr> <tr><td>P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2</td><td>7</td></tr> <tr><td>P151/SCK8_0/SCL8/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTT1_1</td><td>8</td></tr> <tr><td>P035/SIN8_0/OCU8_1/TOT4_0/AIN0_0/INT11_0</td><td>9</td></tr> <tr><td>P036/SCK8_0/OCU7_1/TOT5_0/BIN0_0</td><td>10</td></tr> <tr><td>P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1</td><td>11</td></tr> <tr><td>P041/SIN9_0/ICU9_1/BIN1_0/INT12_0</td><td>12</td></tr> <tr><td>P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0</td><td>13</td></tr> <tr><td>P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2</td><td>14</td></tr> <tr><td>P047/AN45/TRG8_0/TIN3_2/SOT0_1</td><td>15</td></tr> <tr><td>P053/AN44/PPG35_0/INT14_1/SCK0_1</td><td>16</td></tr> </table> <table style="margin-left: auto; margin-right: auto;"> <tr><td>VSS</td><td>1</td></tr> <tr><td>P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1</td><td>2</td></tr> <tr><td>P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0</td><td>3</td></tr> <tr><td>P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1</td><td>4</td></tr> <tr><td>P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1</td><td>5</td></tr> <tr><td>P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2</td><td>6</td></tr> <tr><td>P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2</td><td>7</td></tr> <tr><td>P151/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTT1_1</td><td>8</td></tr> <tr><td>P035/OCU8_1/TOT4_0/AIN0_0/INT11_0</td><td>9</td></tr> <tr><td>P036/OCU7_1/TOT5_0/BIN0_0</td><td>10</td></tr> <tr><td>P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1</td><td>11</td></tr> <tr><td>P041/SIN9_0/ICU9_1/BIN1_0/INT12_0</td><td>12</td></tr> <tr><td>P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0</td><td>13</td></tr> <tr><td>P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2</td><td>14</td></tr> <tr><td>P047/AN45/TRG8_0/TIN3_2/SOT0_1</td><td>15</td></tr> <tr><td>P053/AN44/PPG35_0/INT14_1/SCK0_1</td><td>16</td></tr> </table>	VSS	1	P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2	P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3	P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	4	P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	5	P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	6	P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	7	P151/SCK8_0/SCL8 /OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTT1_1	8	P035/SIN8_0/OCU8_1/TOT4_0/AIN0_0/INT11_0	9	P036/SCK8_0/OCU7_1/TOT5_0/BIN0_0	10	P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	11	P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	12	P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	13	P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	14	P047/AN45/TRG8_0/TIN3_2/SOT0_1	15	P053/AN44/PPG35_0/INT14_1/SCK0_1	16	VSS	1	P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2	P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3	P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	4	P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	5	P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	6	P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	7	P151/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTT1_1	8	P035/OCU8_1/TOT4_0/AIN0_0/INT11_0	9	P036/OCU7_1/TOT5_0/BIN0_0	10	P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	11	P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	12	P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	13	P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	14	P047/AN45/TRG8_0/TIN3_2/SOT0_1	15	P053/AN44/PPG35_0/INT14_1/SCK0_1	16
VSS	1																																																																	
P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2																																																																	
P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3																																																																	
P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	4																																																																	
P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	5																																																																	
P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	6																																																																	
P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	7																																																																	
P151/SCK8_0/SCL8 /OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTT1_1	8																																																																	
P035/SIN8_0/OCU8_1/TOT4_0/AIN0_0/INT11_0	9																																																																	
P036/SCK8_0/OCU7_1/TOT5_0/BIN0_0	10																																																																	
P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	11																																																																	
P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	12																																																																	
P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	13																																																																	
P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	14																																																																	
P047/AN45/TRG8_0/TIN3_2/SOT0_1	15																																																																	
P053/AN44/PPG35_0/INT14_1/SCK0_1	16																																																																	
VSS	1																																																																	
P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2																																																																	
P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3																																																																	
P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	4																																																																	
P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	5																																																																	
P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	6																																																																	
P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	7																																																																	
P151/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTT1_1	8																																																																	
P035/OCU8_1/TOT4_0/AIN0_0/INT11_0	9																																																																	
P036/OCU7_1/TOT5_0/BIN0_0	10																																																																	
P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	11																																																																	
P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	12																																																																	
P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	13																																																																	
P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	14																																																																	
P047/AN45/TRG8_0/TIN3_2/SOT0_1	15																																																																	
P053/AN44/PPG35_0/INT14_1/SCK0_1	16																																																																	

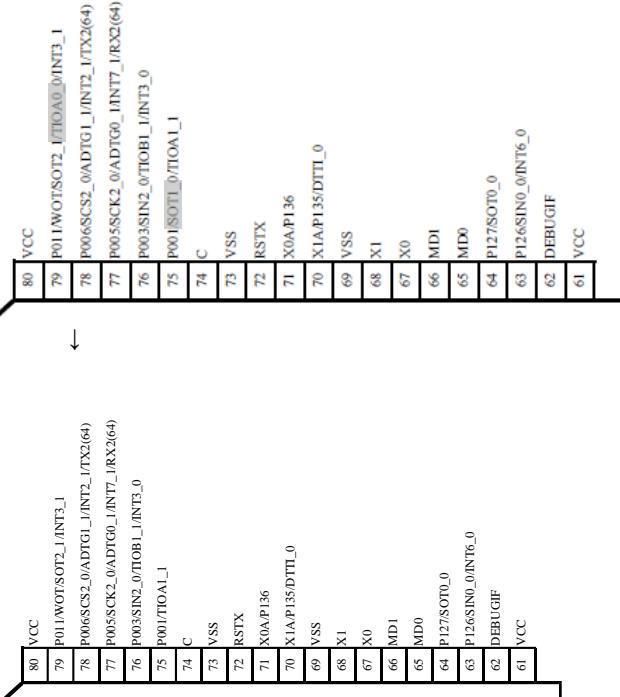
Page	Section	Change Results																																																																
13	■Pin Assignment MB91F52xB	<p>- Right side</p> <p style="text-align: center;">↓</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>48</td><td>P122/SIN6_0/AN31/OCU8_0/INT9_1</td></tr> <tr><td>47</td><td>P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0</td></tr> <tr><td>46</td><td>P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1</td></tr> <tr><td>45</td><td>P110/TX1(64)/SCS63_0/AN22</td></tr> <tr><td>44</td><td>NMIX</td></tr> <tr><td>43</td><td>P105/SCS71_0/AN17/PPG13_0</td></tr> <tr><td>42</td><td>P104/SCS72_0/AN16/PPG12_0</td></tr> <tr><td>41</td><td>P103/SCS73_0/AN15/PPG11_0</td></tr> <tr><td>40</td><td>P102/SIN7_0/AN14/PPG10_0/INT10_0</td></tr> <tr><td>39</td><td>AVCC0</td></tr> <tr><td>38</td><td>AVRH0</td></tr> <tr><td>37</td><td>AVSS0/AVRL0</td></tr> <tr><td>36</td><td>P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1</td></tr> <tr><td>35</td><td>P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0</td></tr> <tr><td>34</td><td>P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1</td></tr> <tr><td>33</td><td>VSS</td></tr> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>48</td><td>P122/SIN6_0/AN31/OCU8_0/INT9_1</td></tr> <tr><td>47</td><td>P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0</td></tr> <tr><td>46</td><td>P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1</td></tr> <tr><td>45</td><td>P110/TX1(64)/SCS63_0/AN22</td></tr> <tr><td>44</td><td>NMIX</td></tr> <tr><td>43</td><td>P105/AN17/PPG13_0</td></tr> <tr><td>42</td><td>P104/AN16/PPG12_0</td></tr> <tr><td>41</td><td>P103/AN15/PPG11_0</td></tr> <tr><td>40</td><td>P102/AN14/PPG10_0/INT10_0</td></tr> <tr><td>39</td><td>AVCC0</td></tr> <tr><td>38</td><td>AVRH0</td></tr> <tr><td>37</td><td>AVSS0/AVRL0</td></tr> <tr><td>36</td><td>P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1</td></tr> <tr><td>35</td><td>P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0</td></tr> <tr><td>34</td><td>P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0</td></tr> <tr><td>33</td><td>VSS</td></tr> </table>	48	P122/SIN6_0/AN31/OCU8_0/INT9_1	47	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0	46	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1	45	P110/TX1(64)/SCS63_0/AN22	44	NMIX	43	P105/SCS71_0/AN17/PPG13_0	42	P104/SCS72_0/AN16/PPG12_0	41	P103/SCS73_0/AN15/PPG11_0	40	P102/SIN7_0/AN14/PPG10_0/INT10_0	39	AVCC0	38	AVRH0	37	AVSS0/AVRL0	36	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1	35	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0	34	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1	33	VSS	48	P122/SIN6_0/AN31/OCU8_0/INT9_1	47	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0	46	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1	45	P110/TX1(64)/SCS63_0/AN22	44	NMIX	43	P105/AN17/PPG13_0	42	P104/AN16/PPG12_0	41	P103/AN15/PPG11_0	40	P102/AN14/PPG10_0/INT10_0	39	AVCC0	38	AVRH0	37	AVSS0/AVRL0	36	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1	35	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0	34	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0	33	VSS
48	P122/SIN6_0/AN31/OCU8_0/INT9_1																																																																	
47	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0																																																																	
46	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1																																																																	
45	P110/TX1(64)/SCS63_0/AN22																																																																	
44	NMIX																																																																	
43	P105/SCS71_0/AN17/PPG13_0																																																																	
42	P104/SCS72_0/AN16/PPG12_0																																																																	
41	P103/SCS73_0/AN15/PPG11_0																																																																	
40	P102/SIN7_0/AN14/PPG10_0/INT10_0																																																																	
39	AVCC0																																																																	
38	AVRH0																																																																	
37	AVSS0/AVRL0																																																																	
36	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1																																																																	
35	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0																																																																	
34	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1																																																																	
33	VSS																																																																	
48	P122/SIN6_0/AN31/OCU8_0/INT9_1																																																																	
47	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0																																																																	
46	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1																																																																	
45	P110/TX1(64)/SCS63_0/AN22																																																																	
44	NMIX																																																																	
43	P105/AN17/PPG13_0																																																																	
42	P104/AN16/PPG12_0																																																																	
41	P103/AN15/PPG11_0																																																																	
40	P102/AN14/PPG10_0/INT10_0																																																																	
39	AVCC0																																																																	
38	AVRH0																																																																	
37	AVSS0/AVRL0																																																																	
36	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1																																																																	
35	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0																																																																	
34	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0																																																																	
33	VSS																																																																	

Page	Section	Change Results
13	■Pin Assignment MB91F52xB	<p>- Top</p>  <p>* In a single clock product, pin 56 and pin 57 are the general-purpose ports.</p>
13	■Pin Assignment MB91F52xB	<p>The following note added on the bottom left of Figure. * In a single clock product, pin 56 and pin 57 are the general-purpose ports.</p>

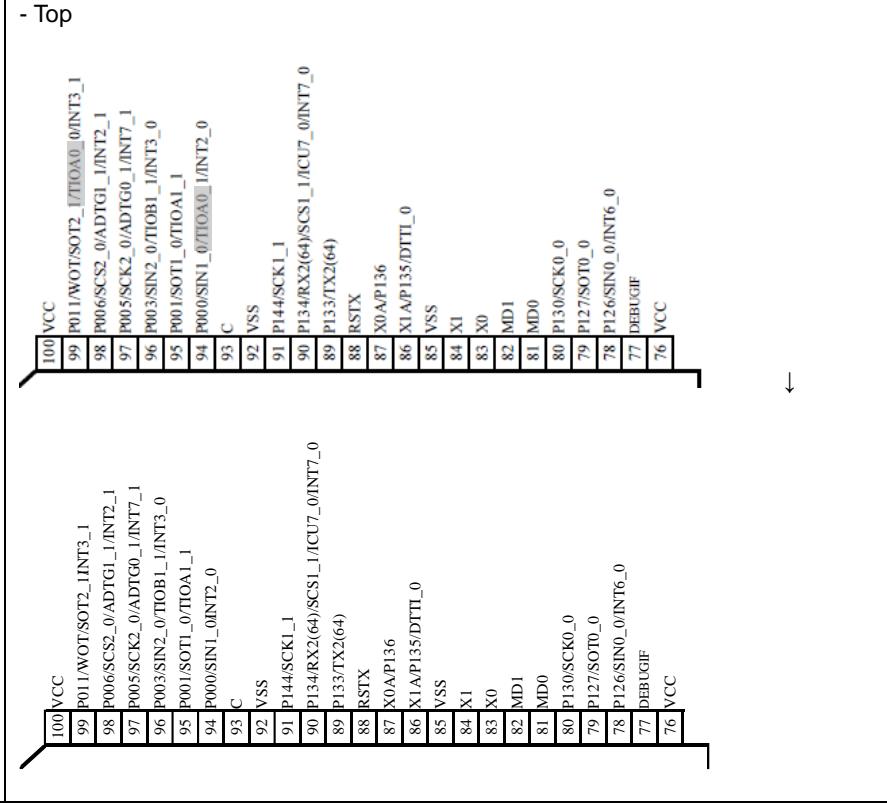
Page	Section	Change Results																																																																																
14	■Pin Assignment MB91F52xD	<p>Signals indicated by the shading below deleted in Figure. - Left side</p> <p style="text-align: center;">↓</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>VSS</td><td>1</td></tr> <tr><td>P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1</td><td>2</td></tr> <tr><td>P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0</td><td>3</td></tr> <tr><td>P026/SCK4_1/PPG26_0/TIN3_0</td><td>4</td></tr> <tr><td>P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1</td><td>5</td></tr> <tr><td>P031/SCS42_1/PPG29_0/TOT2_0</td><td>6</td></tr> <tr><td>P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1</td><td>7</td></tr> <tr><td>P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2</td><td>8</td></tr> <tr><td>P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2</td><td>9</td></tr> <tr><td>P151/SCK8_0/SCL8/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTTL1</td><td>10</td></tr> <tr><td>P035/SIN8_0/OCU8_1/TOT4_0/AIN0_0/INT11_0</td><td>11</td></tr> <tr><td>P036/SCS8_0/OCU7_1/TOT5_0/BIN0_0</td><td>12</td></tr> <tr><td>P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1</td><td>13</td></tr> <tr><td>P041/SIN9_0/ICU9_1/BIN1_0/INT12_0</td><td>14</td></tr> <tr><td>P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0</td><td>15</td></tr> <tr><td>P044/SCS9_0/ICU6_1/TRG2_1</td><td>16</td></tr> <tr><td>P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2</td><td>17</td></tr> <tr><td>P047/AN45/TRG8_0/TIN3_2/SOT0_1</td><td>18</td></tr> <tr><td>P053/AN44/PPG35_0/INT14_1/SCK0_1</td><td>19</td></tr> <tr><td>VCC</td><td>20</td></tr> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>VSS</td><td>1</td></tr> <tr><td>P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1</td><td>2</td></tr> <tr><td>P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0</td><td>3</td></tr> <tr><td>P026/SCK4_1/PPG26_0/TIN3_0</td><td>4</td></tr> <tr><td>P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1</td><td>5</td></tr> <tr><td>P031/SCS42_1/PPG29_0</td><td>6</td></tr> <tr><td>P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1</td><td>7</td></tr> <tr><td>P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2</td><td>8</td></tr> <tr><td>P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2</td><td>9</td></tr> <tr><td>P151/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTTL1</td><td>10</td></tr> <tr><td>P035/OCU8_1/TOT4_0/AIN0_0/INT11_0</td><td>11</td></tr> <tr><td>P036/OCU7_1/TOT5_0/BIN0_0</td><td>12</td></tr> <tr><td>P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1</td><td>13</td></tr> <tr><td>P041/SIN9_0/ICU9_1/BIN1_0/INT12_0</td><td>14</td></tr> <tr><td>P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0</td><td>15</td></tr> <tr><td>P044/SCS9_0/ICU6_1/TRG2_1</td><td>16</td></tr> <tr><td>P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2</td><td>17</td></tr> <tr><td>P047/AN45/TRG8_0/TIN3_2/SOT0_1</td><td>18</td></tr> <tr><td>P053/AN44/PPG35_0/INT14_1/SCK0_1</td><td>19</td></tr> <tr><td>VCC</td><td>20</td></tr> </table>	VSS	1	P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2	P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3	P026/SCK4_1/PPG26_0/TIN3_0	4	P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	5	P031/SCS42_1/PPG29_0/TOT2_0	6	P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	7	P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	8	P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	9	P151/SCK8_0/SCL8/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTTL1	10	P035/SIN8_0/OCU8_1/TOT4_0/AIN0_0/INT11_0	11	P036/SCS8_0/OCU7_1/TOT5_0/BIN0_0	12	P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	13	P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	14	P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	15	P044/SCS9_0/ICU6_1/TRG2_1	16	P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	17	P047/AN45/TRG8_0/TIN3_2/SOT0_1	18	P053/AN44/PPG35_0/INT14_1/SCK0_1	19	VCC	20	VSS	1	P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2	P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3	P026/SCK4_1/PPG26_0/TIN3_0	4	P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	5	P031/SCS42_1/PPG29_0	6	P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	7	P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	8	P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	9	P151/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTTL1	10	P035/OCU8_1/TOT4_0/AIN0_0/INT11_0	11	P036/OCU7_1/TOT5_0/BIN0_0	12	P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	13	P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	14	P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	15	P044/SCS9_0/ICU6_1/TRG2_1	16	P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	17	P047/AN45/TRG8_0/TIN3_2/SOT0_1	18	P053/AN44/PPG35_0/INT14_1/SCK0_1	19	VCC	20
VSS	1																																																																																	
P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2																																																																																	
P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3																																																																																	
P026/SCK4_1/PPG26_0/TIN3_0	4																																																																																	
P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	5																																																																																	
P031/SCS42_1/PPG29_0/TOT2_0	6																																																																																	
P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	7																																																																																	
P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	8																																																																																	
P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	9																																																																																	
P151/SCK8_0/SCL8/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTTL1	10																																																																																	
P035/SIN8_0/OCU8_1/TOT4_0/AIN0_0/INT11_0	11																																																																																	
P036/SCS8_0/OCU7_1/TOT5_0/BIN0_0	12																																																																																	
P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	13																																																																																	
P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	14																																																																																	
P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	15																																																																																	
P044/SCS9_0/ICU6_1/TRG2_1	16																																																																																	
P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	17																																																																																	
P047/AN45/TRG8_0/TIN3_2/SOT0_1	18																																																																																	
P053/AN44/PPG35_0/INT14_1/SCK0_1	19																																																																																	
VCC	20																																																																																	
VSS	1																																																																																	
P020/SIN3_1/TRG3_0/TIN0_2/RTO5_1	2																																																																																	
P024/SIN4_1/PPG24_0/TIN1_0/RTO4_1/INT15_0	3																																																																																	
P026/SCK4_1/PPG26_0/TIN3_0	4																																																																																	
P027/SCS40_1/PPG27_0/TOT0_0/RTO3_1	5																																																																																	
P031/SCS42_1/PPG29_0	6																																																																																	
P032/SCS43_1/PPG30_0/TOT3_0/RTO2_1	7																																																																																	
P033/PPG31_0/ICU3_3/TIN4_0/RTO1_1/SCK3_2	8																																																																																	
P034/OCU11_1/ICU2_3/TIN5_0/RTO0_1/SOT3_2	9																																																																																	
P151/OCU9_1/TRG7_0/ICU0_3/TIN7_0/ZIN0_2/DTTL1	10																																																																																	
P035/OCU8_1/TOT4_0/AIN0_0/INT11_0	11																																																																																	
P036/OCU7_1/TOT5_0/BIN0_0	12																																																																																	
P040/PPG23_1/TOT7_0/AIN1_0/SIN0_1	13																																																																																	
P041/SIN9_0/ICU9_1/BIN1_0/INT12_0	14																																																																																	
P042/SOT9_0/AN47/ICU8_1/TRG0_1/ZIN1_0	15																																																																																	
P044/SCS9_0/ICU6_1/TRG2_1	16																																																																																	
P045/SCK9_0/AN46/ICU5_1/TRG3_1/TOT1_2	17																																																																																	
P047/AN45/TRG8_0/TIN3_2/SOT0_1	18																																																																																	
P053/AN44/PPG35_0/INT14_1/SCK0_1	19																																																																																	
VCC	20																																																																																	

Page	Section	Change Results			
14	■Pin Assignment MB91F52xD	<p>- Bottom</p> <table border="0"> <tr> <td style="vertical-align: top;"> 40 VCC P087/D/A0/0/PPG3/7_0/INT8_0 P082/SINS_0/AN1/PPG2_0 P081/SOTS_0/SDA/5/AN2/PPG1_0 P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1 P073/SOT4_0/SDA/4/AN33/ICU3_2 P077/SIN4_0/AN34/ICU2_2/INT5_0 P071/SCK4_2/AN35/ICU1_2/MONCLK P067/AN36/FRCK5_0/AIN0_1 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 P061/SOT10_1/AN41/ICU3_1/TOT6_1/INT13_1 AVSS/AVRLI AVRHI P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 AVCC1 P055/SIN10_0/AN43/PPG3/7_0/TIN4_1 VSS </td> <td style="vertical-align: top; text-align: center;"> ↓ ↓ </td> <td style="vertical-align: top;"> 40 VCC P087/D/A0/0/PPG3/7_0/INT8_0 P082/SINS_0/AN1/PPG2_0 P081/SOTS_0/SDA/5/AN2/PPG1_0 P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1 P073/SIN4_0/AN34/ICU2_2/INT5_0 P072/SIN4_0/AN34/ICU2_2/INT5_0 P071/SCK4_2/AN35/ICU1_2/MONCLK P067/AN36/FRCK5_0/AIN0_1 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 P061/SOT10_1/AN41/ICU3_1/TOT6_1/INT13_1 AVSS/AVRLI AVRHI P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 AVCC1 P055/SIN10_0/AN43/PPG3/7_0/TIN4_1 VSS </td> </tr> </table>	40 VCC P087/D/A0/0/PPG3/7_0/INT8_0 P082/SINS_0/AN1/PPG2_0 P081/SOTS_0/SDA/5/AN2/PPG1_0 P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1 P073/SOT4_0/SDA/4/AN33/ICU3_2 P077/SIN4_0/AN34/ICU2_2/INT5_0 P071/SCK4_2/AN35/ICU1_2/MONCLK P067/AN36/FRCK5_0/AIN0_1 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 P061/SOT10_1/AN41/ICU3_1/TOT6_1/INT13_1 AVSS/AVRLI AVRHI P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 AVCC1 P055/SIN10_0/AN43/PPG3/7_0/TIN4_1 VSS	↓ ↓	40 VCC P087/D/A0/0/PPG3/7_0/INT8_0 P082/SINS_0/AN1/PPG2_0 P081/SOTS_0/SDA/5/AN2/PPG1_0 P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1 P073/SIN4_0/AN34/ICU2_2/INT5_0 P072/SIN4_0/AN34/ICU2_2/INT5_0 P071/SCK4_2/AN35/ICU1_2/MONCLK P067/AN36/FRCK5_0/AIN0_1 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 P061/SOT10_1/AN41/ICU3_1/TOT6_1/INT13_1 AVSS/AVRLI AVRHI P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 AVCC1 P055/SIN10_0/AN43/PPG3/7_0/TIN4_1 VSS
40 VCC P087/D/A0/0/PPG3/7_0/INT8_0 P082/SINS_0/AN1/PPG2_0 P081/SOTS_0/SDA/5/AN2/PPG1_0 P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1 P073/SOT4_0/SDA/4/AN33/ICU3_2 P077/SIN4_0/AN34/ICU2_2/INT5_0 P071/SCK4_2/AN35/ICU1_2/MONCLK P067/AN36/FRCK5_0/AIN0_1 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 P061/SOT10_1/AN41/ICU3_1/TOT6_1/INT13_1 AVSS/AVRLI AVRHI P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 AVCC1 P055/SIN10_0/AN43/PPG3/7_0/TIN4_1 VSS	↓ ↓	40 VCC P087/D/A0/0/PPG3/7_0/INT8_0 P082/SINS_0/AN1/PPG2_0 P081/SOTS_0/SDA/5/AN2/PPG1_0 P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1 P073/SIN4_0/AN34/ICU2_2/INT5_0 P072/SIN4_0/AN34/ICU2_2/INT5_0 P071/SCK4_2/AN35/ICU1_2/MONCLK P067/AN36/FRCK5_0/AIN0_1 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TOT7_1/ZIN1_1 P061/SOT10_1/AN41/ICU3_1/TOT6_1/INT13_1 AVSS/AVRLI AVRHI P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 AVCC1 P055/SIN10_0/AN43/PPG3/7_0/TIN4_1 VSS			

Page	Section	Change Results																																																																																
14	■Pin Assignment MB91F52xD	<p>- Right side</p> <p>↓</p> <table border="1" data-bbox="605 382 1030 889"> <tr><td>60</td><td>VSS</td></tr> <tr><td>59</td><td>P122/SIN6_0/AN31/OCU8_0/INT9_1</td></tr> <tr><td>58</td><td>P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0</td></tr> <tr><td>57</td><td>P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1</td></tr> <tr><td>56</td><td>P114/SCS61_0/AN26/PPG18_0/RTO2_0</td></tr> <tr><td>55</td><td>P110/TX1(64)/SCS63_0/AN22</td></tr> <tr><td>54</td><td>NMIX</td></tr> <tr><td>53</td><td>P107/AN19/PPG15_0</td></tr> <tr><td>52</td><td>P105/SCS71_0/AN17/PPG13_0</td></tr> <tr><td>51</td><td>P104/SCS72_0/AN16/PPG12_0</td></tr> <tr><td>50</td><td>P103/SCS73_0/AN15/PPG11_0</td></tr> <tr><td>49</td><td>P102/SIN7_0/AN14/PPG10_0/INT10_0</td></tr> <tr><td>48</td><td>P100/SCK7_0/SCL7/AN12/PPG8_0</td></tr> <tr><td>47</td><td>AVCC0</td></tr> <tr><td>46</td><td>AVRH0</td></tr> <tr><td>45</td><td>AVSS0/AVRL0</td></tr> <tr><td>44</td><td>P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1</td></tr> <tr><td>43</td><td>P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0</td></tr> <tr><td>42</td><td>P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1</td></tr> <tr><td>41</td><td>VSS</td></tr> </table> <table border="1" data-bbox="605 974 997 1481"> <tr><td>60</td><td>VSS</td></tr> <tr><td>59</td><td>P122/SIN6_0/AN31/OCU8_0/INT9_1</td></tr> <tr><td>58</td><td>P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0</td></tr> <tr><td>57</td><td>P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1</td></tr> <tr><td>56</td><td>P114/SCS61_0/AN26/PPG18_0/RTO2_0</td></tr> <tr><td>55</td><td>P110/TX1(64)/SCS63_0/AN22</td></tr> <tr><td>54</td><td>NMIX</td></tr> <tr><td>53</td><td>P107/AN19/PPG15_0</td></tr> <tr><td>52</td><td>P105/AN17/PPG13_0</td></tr> <tr><td>51</td><td>P104/AN16/PPG12_0</td></tr> <tr><td>50</td><td>P103/AN15/PPG11_0</td></tr> <tr><td>49</td><td>P102/AN14/PPG10_0/INT10_0</td></tr> <tr><td>48</td><td>P100/AN12/PPG8_0</td></tr> <tr><td>47</td><td>AVCC0</td></tr> <tr><td>46</td><td>AVRH0</td></tr> <tr><td>45</td><td>AVSS0/AVRL0</td></tr> <tr><td>44</td><td>P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1</td></tr> <tr><td>43</td><td>P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0</td></tr> <tr><td>42</td><td>P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1</td></tr> <tr><td>41</td><td>VSS</td></tr> </table>	60	VSS	59	P122/SIN6_0/AN31/OCU8_0/INT9_1	58	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0	57	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1	56	P114/SCS61_0/AN26/PPG18_0/RTO2_0	55	P110/TX1(64)/SCS63_0/AN22	54	NMIX	53	P107/AN19/PPG15_0	52	P105/SCS71_0/AN17/PPG13_0	51	P104/SCS72_0/AN16/PPG12_0	50	P103/SCS73_0/AN15/PPG11_0	49	P102/SIN7_0/AN14/PPG10_0/INT10_0	48	P100/SCK7_0/SCL7/AN12/PPG8_0	47	AVCC0	46	AVRH0	45	AVSS0/AVRL0	44	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1	43	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0	42	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1	41	VSS	60	VSS	59	P122/SIN6_0/AN31/OCU8_0/INT9_1	58	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0	57	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1	56	P114/SCS61_0/AN26/PPG18_0/RTO2_0	55	P110/TX1(64)/SCS63_0/AN22	54	NMIX	53	P107/AN19/PPG15_0	52	P105/AN17/PPG13_0	51	P104/AN16/PPG12_0	50	P103/AN15/PPG11_0	49	P102/AN14/PPG10_0/INT10_0	48	P100/AN12/PPG8_0	47	AVCC0	46	AVRH0	45	AVSS0/AVRL0	44	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1	43	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0	42	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1	41	VSS
60	VSS																																																																																	
59	P122/SIN6_0/AN31/OCU8_0/INT9_1																																																																																	
58	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0																																																																																	
57	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1																																																																																	
56	P114/SCS61_0/AN26/PPG18_0/RTO2_0																																																																																	
55	P110/TX1(64)/SCS63_0/AN22																																																																																	
54	NMIX																																																																																	
53	P107/AN19/PPG15_0																																																																																	
52	P105/SCS71_0/AN17/PPG13_0																																																																																	
51	P104/SCS72_0/AN16/PPG12_0																																																																																	
50	P103/SCS73_0/AN15/PPG11_0																																																																																	
49	P102/SIN7_0/AN14/PPG10_0/INT10_0																																																																																	
48	P100/SCK7_0/SCL7/AN12/PPG8_0																																																																																	
47	AVCC0																																																																																	
46	AVRH0																																																																																	
45	AVSS0/AVRL0																																																																																	
44	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1																																																																																	
43	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0																																																																																	
42	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1																																																																																	
41	VSS																																																																																	
60	VSS																																																																																	
59	P122/SIN6_0/AN31/OCU8_0/INT9_1																																																																																	
58	P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0																																																																																	
57	P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1																																																																																	
56	P114/SCS61_0/AN26/PPG18_0/RTO2_0																																																																																	
55	P110/TX1(64)/SCS63_0/AN22																																																																																	
54	NMIX																																																																																	
53	P107/AN19/PPG15_0																																																																																	
52	P105/AN17/PPG13_0																																																																																	
51	P104/AN16/PPG12_0																																																																																	
50	P103/AN15/PPG11_0																																																																																	
49	P102/AN14/PPG10_0/INT10_0																																																																																	
48	P100/AN12/PPG8_0																																																																																	
47	AVCC0																																																																																	
46	AVRH0																																																																																	
45	AVSS0/AVRL0																																																																																	
44	P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1																																																																																	
43	P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0																																																																																	
42	P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT1_1																																																																																	
41	VSS																																																																																	

Page	Section	Change Results																																								
14	■Pin Assignment MB91F52xD	<p>- Top</p>  <table border="1"> <tr><td>80</td><td>VCC</td></tr> <tr><td>79</td><td>P011WOT/SOT2_1/INT3_1</td></tr> <tr><td>78</td><td>P006SCK2_0/ADTG1_1/INT2_1/TX2(64)</td></tr> <tr><td>77</td><td>P005SCK2_0/ADTG0_1/INT7_1/RX2(64)</td></tr> <tr><td>76</td><td>P003SIN2_0/TIOB1_1/INT3_0</td></tr> <tr><td>75</td><td>P001SOT1_0/TIOA1_1</td></tr> <tr><td>74</td><td>C</td></tr> <tr><td>73</td><td>VSS</td></tr> <tr><td>72</td><td>RSTX</td></tr> <tr><td>71</td><td>XAP136</td></tr> <tr><td>70</td><td>XAP135DTTL_0</td></tr> <tr><td>69</td><td>VSS</td></tr> <tr><td>68</td><td>X1</td></tr> <tr><td>67</td><td>X0</td></tr> <tr><td>66</td><td>MD1</td></tr> <tr><td>65</td><td>MD0</td></tr> <tr><td>64</td><td>P27SOT0_0</td></tr> <tr><td>63</td><td>P26SIN0_0/INT6_0</td></tr> <tr><td>62</td><td>DEBUGIF</td></tr> <tr><td>61</td><td>VCC</td></tr> </table>	80	VCC	79	P011WOT/SOT2_1/INT3_1	78	P006SCK2_0/ADTG1_1/INT2_1/TX2(64)	77	P005SCK2_0/ADTG0_1/INT7_1/RX2(64)	76	P003SIN2_0/TIOB1_1/INT3_0	75	P001SOT1_0/TIOA1_1	74	C	73	VSS	72	RSTX	71	XAP136	70	XAP135DTTL_0	69	VSS	68	X1	67	X0	66	MD1	65	MD0	64	P27SOT0_0	63	P26SIN0_0/INT6_0	62	DEBUGIF	61	VCC
80	VCC																																									
79	P011WOT/SOT2_1/INT3_1																																									
78	P006SCK2_0/ADTG1_1/INT2_1/TX2(64)																																									
77	P005SCK2_0/ADTG0_1/INT7_1/RX2(64)																																									
76	P003SIN2_0/TIOB1_1/INT3_0																																									
75	P001SOT1_0/TIOA1_1																																									
74	C																																									
73	VSS																																									
72	RSTX																																									
71	XAP136																																									
70	XAP135DTTL_0																																									
69	VSS																																									
68	X1																																									
67	X0																																									
66	MD1																																									
65	MD0																																									
64	P27SOT0_0																																									
63	P26SIN0_0/INT6_0																																									
62	DEBUGIF																																									
61	VCC																																									
14	■Pin Assignment MB91F52xD	<p>The following note added on the bottom left of Figure.</p> <p>* In a single clock product, pin 71 and pin 72 are the general-purpose ports.</p>																																								

Page	Section	Change Results
15	■Pin Assignment MB91F52xF	<p>Signals indicated by the shading below deleted in Figure.</p> <p>(Error) - Bottom</p> <p>50 VCC 49 P087/DA0/PPG7_0/INT8_0 48 P086/DA0/PPG6_0 47 P082/SIN5_0/AN1/PPG2_0 46 P081/SOT5_0/SDA5/AN0/PPG1_0 45 PI53/SCS5_0/SCS5/AN32/FRCK1_1/INT4_1 44 PI52/SCS5_0/SCS5/AN32/FRCK1_1/INT4_1 43 P073/SOT4_0/SDA4/AN33/ICU3_2 42 P072/SIN4_0/AN34/ICU2_2/INT5_0 41 P071/SCK4_2/AN35/ICU1_2/MONCLK 40 P070/ICU1_2 39 P067/AN36/FRCK5_0/AIN0_1 38 P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1 37 P065/SCS43_0/FRCK3_0/ZIN0_1/PPG44_1 36 P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PPG43_1 35 P063/SCS41_0/AN39/PPG5_1/FRCK1_0/BIN1_1 34 P062/SCS10_1/SCS40_0/AN40/PPG4_1/FRCK0_0/TO17_1/ZIN1_1 33 P061/SOT10_1/AN41/ICU6_0/PPG3_1/ICU3_1/TO16_1/INT13_1 32 P060/SCS10_0/PPG2_1/ICU2_1/TO15_1/INT13_0 31 AVSS1/AVRL1 30 AVRHI 29 P057/SCK10_1/AN42/ICU8_0/TRG0_2/PPG1_1/ICU1_1/TIN6_1 28 AVCC1 27 P055/SIN10_0/AN43/PPG37_0/TIN4_1 26 VSS</p>

Page	Section	Change Results				
15	■Pin Assignment MB91F52xF	<p>- Top</p>  <p>↓</p>				
15	■Pin Assignment MB91F52xF	<p>The following note added on the bottom left of Figure.</p> <p>* In a single clock product, pin 86 and pin 87 are the general-purpose ports.</p>				
16	■Pin Assignment MB91F52xJ	<p>The following note added on the bottom left of Figure.</p> <p>* In a single clock product, pin 102 and pin 103 are the general-purpose ports.</p>				
17	■Pin Assignment MB91F52xK	<p>The following note added on the bottom left of Figure.</p> <p>* In a single clock product, pin 121 and pin 122 are the general-purpose ports.</p>				
18	■Pin Assignment MB91F52xL	<p>The following note added on the bottom left of Figure.</p> <p>* In a single clock product, pin 149 and pin 150 are the general-purpose ports.</p>				
19 to 35	■PIN Description	<p>A List of "Pin Description" modified.</p> <table border="1" data-bbox="589 1457 996 1553"> <tr> <td data-bbox="589 1457 792 1553">I/O Circuit types^{*1}</td><td data-bbox="792 1457 996 1553">Function^{*2}</td></tr> </table> <p>↓</p> <table border="1" data-bbox="589 1574 996 1698"> <tr> <td data-bbox="589 1574 792 1698">I/O Circuit types^{*8}</td><td data-bbox="792 1574 996 1698">Function^{*9}</td></tr> </table>	I/O Circuit types ^{*1}	Function ^{*2}	I/O Circuit types ^{*8}	Function ^{*9}
I/O Circuit types ^{*1}	Function ^{*2}					
I/O Circuit types ^{*8}	Function ^{*9}					

Page	Section	Change Results																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
19	■PIN Description	A List of "Pin Description" modified. (Errors) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>2</td> <td>2</td> <td>P015</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>3</td> <td>3</td> <td>D29</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>TRG0_0</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>P016</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>3</td> <td>3</td> <td>D30</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>TRG1_0</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>4</td> <td>P170</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>PPG36_1</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>4</td> <td>5</td> <td>P017</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>D31</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>TRG2_0</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>6</td> <td>P171</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>PPG37_1</td> </tr> <tr> <td colspan="6" style="text-align: center;">2</td><td>P020</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">2</td><td>ASX</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">2</td><td>SIN3_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">2</td><td>TRG3_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">2</td><td>TIN0_2</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">2</td><td>RTO5_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">3</td><td>P021</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">3</td><td>CS0X</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">3</td><td>SOT3_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">3</td><td>TRG6_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">3</td><td>TRG4_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">4</td><td>P022</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">4</td><td>CS1X</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">4</td><td>SCK3_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">4</td><td>TRG7_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">4</td><td>TRG5_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">5</td><td>P023</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">5</td><td>RDX</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">5</td><td>SCS3_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">5</td><td>PPG32_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">5</td><td>TIN0_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>P024</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>WR0X</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>SIN4_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>PPG24_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>TIN1_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>RTO4_1</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">6</td><td>INT15_0</td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">7</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">7</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">7</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">8</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">8</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">8</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">9</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">9</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">9</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">10</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">10</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">10</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">11</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">11</td><td></td> <td></td> </tr> <tr> <td colspan="6" style="text-align: center;">11</td><td></td> <td></td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176	-	-	-	-	2	2	P015	-	-	-	-	3	3	D29	-	-	-	-	-	-	TRG0_0	-	-	-	-	-	-	P016	-	-	-	-	3	3	D30	-	-	-	-	-	-	TRG1_0	-	-	-	-	-	4	P170	-	-	-	-	-	-	PPG36_1	-	-	-	-	4	5	P017	-	-	-	-	-	-	D31	-	-	-	-	-	-	TRG2_0	-	-	-	-	-	6	P171	-	-	-	-	-	-	PPG37_1	2						P020		2						ASX		2						SIN3_1		2						TRG3_0		2						TIN0_2		2						RTO5_1		3						P021		3						CS0X		3						SOT3_1		3						TRG6_1		3						TRG4_0		4						P022		4						CS1X		4						SCK3_1		4						TRG7_1		4						TRG5_0		5						P023		5						RDX		5						SCS3_1		5						PPG32_0		5						TIN0_0		6						P024		6						WR0X		6						SIN4_1		6						PPG24_0		6						TIN1_0		6						RTO4_1		6						INT15_0		7								7								7								8								8								8								9								9								9								10								10								10								11								11								11														
Pin no.						Pin Name																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
64	80	100	120	144	176																																																																																																																																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	2	2	P015																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	3	3	D29																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	TRG0_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	P016																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	3	3	D30																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	TRG1_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	4	P170																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	PPG36_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	4	5	P017																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	D31																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	TRG2_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	6	P171																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
-	-	-	-	-	-	PPG37_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
2						P020																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
2						ASX																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
2						SIN3_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
2						TRG3_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
2						TIN0_2																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
2						RTO5_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
3						P021																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
3						CS0X																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
3						SOT3_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
3						TRG6_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
3						TRG4_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
4						P022																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
4						CS1X																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
4						SCK3_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
4						TRG7_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
4						TRG5_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
5						P023																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
5						RDX																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
5						SCS3_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
5						PPG32_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
5						TIN0_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						P024																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						WR0X																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						SIN4_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						PPG24_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						TIN1_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						RTO4_1																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6						INT15_0																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
7																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
7																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
7																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
8																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
8																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
8																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
9																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
9																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
9																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
10																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
10																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
10																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
11																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
11																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
11																																																																																																																																																																																																																																																																																																																																																																																																																																																																									

Page	Section	Change Results																																																																																																																																																																																																																																																																																																																																																								
19	■PIN Description	(Continued) (Correct) <table border="1" data-bbox="600 390 1242 1745"> <thead> <tr> <th colspan="6" data-bbox="605 397 1067 439">Pin no.</th><th colspan="2" data-bbox="1072 397 1242 439">Pin Name</th></tr> <tr> <th data-bbox="605 439 638 471">64</th><th data-bbox="646 439 679 471">80</th><th data-bbox="687 439 720 471">100</th><th data-bbox="728 439 760 471">120</th><th data-bbox="769 439 801 471">144</th><th data-bbox="809 439 842 471">176</th><th colspan="2" data-bbox="1072 439 1242 471"></th></tr> </thead> <tbody> <tr> <td data-bbox="605 481 638 513">-</td><td data-bbox="646 481 679 513">-</td><td data-bbox="687 481 720 513">-</td><td data-bbox="728 481 760 513">-</td><td data-bbox="769 481 801 513">2</td><td data-bbox="809 481 842 513">2</td><td colspan="2" data-bbox="1072 481 1242 513">P015</td></tr> <tr> <td data-bbox="605 524 638 555">-</td><td data-bbox="646 524 679 555">-</td><td data-bbox="687 524 720 555">-</td><td data-bbox="728 524 760 555">-</td><td data-bbox="769 524 801 555">3</td><td data-bbox="809 524 842 555">3</td><td colspan="2" data-bbox="1072 524 1242 555">D29</td></tr> <tr> <td data-bbox="605 566 638 597">-</td><td data-bbox="646 566 679 597">-</td><td data-bbox="687 566 720 597">-</td><td data-bbox="728 566 760 597">-</td><td data-bbox="769 566 801 597">-</td><td data-bbox="809 566 842 597">-</td><td colspan="2" data-bbox="1072 566 1242 597">TRG0_0</td></tr> <tr> <td data-bbox="605 608 638 640">-</td><td data-bbox="646 608 679 640">-</td><td data-bbox="687 608 720 640">-</td><td data-bbox="728 608 760 640">-</td><td data-bbox="769 608 801 640">-</td><td data-bbox="809 608 842 640">-</td><td colspan="2" data-bbox="1072 608 1242 640">P016</td></tr> <tr> <td data-bbox="605 650 638 682">-</td><td data-bbox="646 650 679 682">-</td><td data-bbox="687 650 720 682">-</td><td data-bbox="728 650 760 682">-</td><td data-bbox="769 650 801 682">3</td><td data-bbox="809 650 842 682">3</td><td colspan="2" data-bbox="1072 650 1242 682">D30</td></tr> <tr> <td data-bbox="605 693 638 724">-</td><td data-bbox="646 693 679 724">-</td><td data-bbox="687 693 720 724">-</td><td data-bbox="728 693 760 724">-</td><td data-bbox="769 693 801 724">-</td><td data-bbox="809 693 842 724">-</td><td colspan="2" data-bbox="1072 693 1242 724">TRG1_0</td></tr> <tr> <td data-bbox="605 735 638 767">-</td><td data-bbox="646 735 679 767">-</td><td data-bbox="687 735 720 767">-</td><td data-bbox="728 735 760 767">-</td><td data-bbox="769 735 801 767">-</td><td data-bbox="809 735 842 767">-</td><td colspan="2" data-bbox="1072 735 1242 767">P170</td></tr> <tr> <td data-bbox="605 777 638 809">-</td><td data-bbox="646 777 679 809">-</td><td data-bbox="687 777 720 809">-</td><td data-bbox="728 777 760 809">-</td><td data-bbox="769 777 801 809">-</td><td data-bbox="809 777 842 809">-</td><td colspan="2" data-bbox="1072 777 1242 809">PPG36_1</td></tr> <tr> <td data-bbox="605 819 638 851">-</td><td data-bbox="646 819 679 851">-</td><td data-bbox="687 819 720 851">-</td><td data-bbox="728 819 760 851">-</td><td data-bbox="769 819 801 851">-</td><td data-bbox="809 819 842 851">-</td><td colspan="2" data-bbox="1072 819 1242 851">P017</td></tr> <tr> <td data-bbox="605 862 638 893">-</td><td data-bbox="646 862 679 893">-</td><td data-bbox="687 862 720 893">-</td><td data-bbox="728 862 760 893">-</td><td data-bbox="769 862 801 893">4</td><td data-bbox="809 862 842 893">5</td><td colspan="2" data-bbox="1072 862 1242 893">D31</td></tr> <tr> <td data-bbox="605 904 638 936">-</td><td data-bbox="646 904 679 936">-</td><td data-bbox="687 904 720 936">-</td><td data-bbox="728 904 760 936">-</td><td data-bbox="769 904 801 936">-</td><td data-bbox="809 904 842 936">-</td><td colspan="2" data-bbox="1072 904 1242 936">TRG2_0</td></tr> <tr> <td data-bbox="605 946 638 978">-</td><td data-bbox="646 946 679 978">-</td><td data-bbox="687 946 720 978">-</td><td data-bbox="728 946 760 978">-</td><td data-bbox="769 946 801 978">-</td><td data-bbox="809 946 842 978">-</td><td colspan="2" data-bbox="1072 946 1242 978">P171</td></tr> <tr> <td data-bbox="605 988 638 1020">-</td><td data-bbox="646 988 679 1020">-</td><td data-bbox="687 988 720 1020">-</td><td data-bbox="728 988 760 1020">-</td><td data-bbox="769 988 801 1020">-</td><td data-bbox="809 988 842 1020">-</td><td colspan="2" data-bbox="1072 988 1242 1020">PPG37_1</td></tr> <tr> <td data-bbox="605 1031 638 1062">-</td><td data-bbox="646 1031 679 1062">-</td><td data-bbox="687 1031 720 1062">-</td><td data-bbox="728 1031 760 1062">-</td><td data-bbox="769 1031 801 1062">-</td><td data-bbox="809 1031 842 1062">-</td><td colspan="2" data-bbox="1072 1031 1242 1062">P020</td></tr> <tr> <td data-bbox="605 1073 638 1105">-</td><td data-bbox="646 1073 679 1105">-</td><td data-bbox="687 1073 720 1105">-</td><td data-bbox="728 1073 760 1105">-</td><td data-bbox="769 1073 801 1105">-</td><td data-bbox="809 1073 842 1105">-</td><td colspan="2" data-bbox="1072 1073 1242 1105">ASX *2, *3, *4, *5</td></tr> <tr> <td data-bbox="605 1115 638 1147">2 *1</td><td data-bbox="646 1115 679 1147">2 *1</td><td data-bbox="687 1115 720 1147">2 *1</td><td data-bbox="728 1115 760 1147">2 *1</td><td data-bbox="769 1115 801 1147">5</td><td data-bbox="809 1115 842 1147">7</td><td colspan="2" data-bbox="1072 1115 1242 1147">SIN3_1</td></tr> <tr> <td data-bbox="605 1157 638 1189">-</td><td data-bbox="646 1157 679 1189">-</td><td data-bbox="687 1157 720 1189">-</td><td data-bbox="728 1157 760 1189">-</td><td data-bbox="769 1157 801 1189">-</td><td data-bbox="809 1157 842 1189">-</td><td colspan="2" data-bbox="1072 1157 1242 1189">TRG3_0</td></tr> <tr> <td data-bbox="605 1200 638 1231">-</td><td data-bbox="646 1200 679 1231">-</td><td data-bbox="687 1200 720 1231">-</td><td data-bbox="728 1200 760 1231">-</td><td data-bbox="769 1200 801 1231">-</td><td data-bbox="809 1200 842 1231">-</td><td colspan="2" data-bbox="1072 1200 1242 1231">TIN0_2</td></tr> <tr> <td data-bbox="605 1242 638 1274">-</td><td data-bbox="646 1242 679 1274">-</td><td data-bbox="687 1242 720 1274">-</td><td data-bbox="728 1242 760 1274">-</td><td data-bbox="769 1242 801 1274">-</td><td data-bbox="809 1242 842 1274">-</td><td colspan="2" data-bbox="1072 1242 1242 1274">RTO5_1</td></tr> <tr> <td data-bbox="605 1284 638 1316">-</td><td data-bbox="646 1284 679 1316">-</td><td data-bbox="687 1284 720 1316">-</td><td data-bbox="728 1284 760 1316">-</td><td data-bbox="769 1284 801 1316">-</td><td data-bbox="809 1284 842 1316">-</td><td colspan="2" data-bbox="1072 1284 1242 1316">P021</td></tr> <tr> <td data-bbox="605 1326 638 1358">-</td><td data-bbox="646 1326 679 1358">-</td><td data-bbox="687 1326 720 1358">-</td><td data-bbox="728 1326 760 1358">-</td><td data-bbox="769 1326 801 1358">-</td><td data-bbox="809 1326 842 1358">-</td><td colspan="2" data-bbox="1072 1326 1242 1358">CS0X *5</td></tr> <tr> <td data-bbox="605 1369 638 1400">-</td><td data-bbox="646 1369 679 1400">-</td><td data-bbox="687 1369 720 1400">-</td><td data-bbox="728 1369 760 1400">-</td><td data-bbox="769 1369 801 1400">-</td><td data-bbox="809 1369 842 1400">-</td><td colspan="2" data-bbox="1072 1369 1242 1400">SOT3_1</td></tr> <tr> <td data-bbox="605 1411 638 1443">-</td><td data-bbox="646 1411 679 1443">-</td><td data-bbox="687 1411 720 1443">-</td><td data-bbox="728 1411 760 1443">-</td><td data-bbox="769 1411 801 1443">-</td><td data-bbox="809 1411 842 1443">-</td><td colspan="2" data-bbox="1072 1411 1242 1443">TRG6_1</td></tr> <tr> <td data-bbox="605 1453 638 1485">-</td><td data-bbox="646 1453 679 1485">-</td><td data-bbox="687 1453 720 1485">-</td><td data-bbox="728 1453 760 1485">-</td><td data-bbox="769 1453 801 1485">-</td><td data-bbox="809 1453 842 1485">-</td><td colspan="2" data-bbox="1072 1453 1242 1485">TRG4_0</td></tr> <tr> <td data-bbox="605 1496 638 1527">-</td><td data-bbox="646 1496 679 1527">-</td><td data-bbox="687 1496 720 1527">-</td><td data-bbox="728 1496 760 1527">-</td><td data-bbox="769 1496 801 1527">-</td><td data-bbox="809 1496 842 1527">-</td><td colspan="2" data-bbox="1072 1496 1242 1527">P022</td></tr> <tr> <td data-bbox="605 1538 638 1569">-</td><td data-bbox="646 1538 679 1569">-</td><td data-bbox="687 1538 720 1569">-</td><td data-bbox="728 1538 760 1569">-</td><td data-bbox="769 1538 801 1569">-</td><td data-bbox="809 1538 842 1569">-</td><td colspan="2" data-bbox="1072 1538 1242 1569">CS1X *5</td></tr> <tr> <td data-bbox="605 1580 638 1612">-</td><td data-bbox="646 1580 679 1612">-</td><td data-bbox="687 1580 720 1612">-</td><td data-bbox="728 1580 760 1612">-</td><td data-bbox="769 1580 801 1612">-</td><td data-bbox="809 1580 842 1612">-</td><td colspan="2" data-bbox="1072 1580 1242 1612">SCK3_1</td></tr> <tr> <td data-bbox="605 1622 638 1654">-</td><td data-bbox="646 1622 679 1654">-</td><td data-bbox="687 1622 720 1654">-</td><td data-bbox="728 1622 760 1654">-</td><td data-bbox="769 1622 801 1654">-</td><td data-bbox="809 1622 842 1654">-</td><td colspan="2" data-bbox="1072 1622 1242 1654">TRG7_1</td></tr> <tr> <td data-bbox="605 1665 638 1696">-</td><td data-bbox="646 1665 679 1696">-</td><td data-bbox="687 1665 720 1696">-</td><td data-bbox="728 1665 760 1696">-</td><td data-bbox="769 1665 801 1696">-</td><td data-bbox="809 1665 842 1696">-</td><td colspan="2" data-bbox="1072 1665 1242 1696">TRG5_0</td></tr> <tr> <td data-bbox="605 1707 638 1738">-</td><td data-bbox="646 1707 679 1738">-</td><td data-bbox="687 1707 720 1738">-</td><td data-bbox="728 1707 760 1738">-</td><td data-bbox="769 1707 801 1738">-</td><td data-bbox="809 1707 842 1738">-</td><td colspan="2" data-bbox="1072 1707 1242 1738">P023</td></tr> <tr> <td data-bbox="605 1749 638 1781">-</td><td data-bbox="646 1749 679 1781">-</td><td data-bbox="687 1749 720 1781">-</td><td data-bbox="728 1749 760 1781">-</td><td data-bbox="769 1749 801 1781">-</td><td data-bbox="809 1749 842 1781">-</td><td colspan="2" data-bbox="1072 1749 1242 1781">RDX *5</td></tr> <tr> <td data-bbox="605 1791 638 1823">-</td><td data-bbox="646 1791 679 1823">-</td><td data-bbox="687 1791 720 1823">-</td><td data-bbox="728 1791 760 1823">-</td><td data-bbox="769 1791 801 1823">-</td><td data-bbox="809 1791 842 1823">-</td><td colspan="2" data-bbox="1072 1791 1242 1823">SCS3_1</td></tr> <tr> <td data-bbox="605 1834 638 1865">-</td><td data-bbox="646 1834 679 1865">-</td><td data-bbox="687 1834 720 1865">-</td><td data-bbox="728 1834 760 1865">-</td><td data-bbox="769 1834 801 1865">-</td><td data-bbox="809 1834 842 1865">-</td><td colspan="2" data-bbox="1072 1834 1242 1865">PPG32_0</td></tr> <tr> <td data-bbox="605 1876 638 1908">-</td><td data-bbox="646 1876 679 1908">-</td><td data-bbox="687 1876 720 1908">-</td><td data-bbox="728 1876 760 1908">-</td><td data-bbox="769 1876 801 1908">-</td><td data-bbox="809 1876 842 1908">-</td><td colspan="2" data-bbox="1072 1876 1242 1908">TIN0_0</td></tr> <tr> <td data-bbox="605 1918 638 1950">-</td><td data-bbox="646 1918 679 1950">-</td><td data-bbox="687 1918 720 1950">-</td><td data-bbox="728 1918 760 1950">-</td><td data-bbox="769 1918 801 1950">-</td><td data-bbox="809 1918 842 1950">-</td><td colspan="2" data-bbox="1072 1918 1242 1950">P024</td></tr> <tr> <td data-bbox="605 1960 638 1992">-</td><td data-bbox="646 1960 679 1992">-</td><td data-bbox="687 1960 720 1992">-</td><td data-bbox="728 1960 760 1992">-</td><td data-bbox="769 1960 801 1992">-</td><td data-bbox="809 1960 842 1992">-</td><td colspan="2" data-bbox="1072 1960 1242 1992">WR0X *2, *3, *4, *5</td></tr> <tr> <td data-bbox="605 2003 638 2034">-</td><td data-bbox="646 2003 679 2034">-</td><td data-bbox="687 2003 720 2034">-</td><td data-bbox="728 2003 760 2034">-</td><td data-bbox="769 2003 801 2034">-</td><td data-bbox="809 2003 842 2034">-</td><td colspan="2" data-bbox="1072 2003 1242 2034">SIN4_1</td></tr> <tr> <td data-bbox="605 2045 638 2077">-</td><td data-bbox="646 2045 679 2077">-</td><td data-bbox="687 2045 720 2077">-</td><td data-bbox="728 2045 760 2077">-</td><td data-bbox="769 2045 801 2077">-</td><td data-bbox="809 2045 842 2077">-</td><td colspan="2" data-bbox="1072 2045 1242 2077">PPG24_0</td></tr> <tr> <td data-bbox="605 2087 638 2113">-</td><td data-bbox="646 2087 679 2113">-</td><td data-bbox="687 2087 720 2113">-</td><td data-bbox="728 2087 760 2113">-</td><td data-bbox="769 2087 801 2113">-</td><td data-bbox="809 2087 842 2113">-</td><td colspan="2" data-bbox="1072 2087 1242 2113">TIN1_0</td></tr> <tr> <td data-bbox="605 2129 638 2113">-</td><td data-bbox="646 2129 679 2113">-</td><td data-bbox="687 2129 720 2113">-</td><td data-bbox="728 2129 760 2113">-</td><td data-bbox="769 2129 801 2113">-</td><td data-bbox="809 2129 842 2113">-</td><td colspan="2" data-bbox="1072 2129 1242 2113">RTO4_1</td></tr> <tr> <td data-bbox="605 2172 638 2113">-</td><td data-bbox="646 2172 679 2113">-</td><td data-bbox="687 2172 720 2113">-</td><td data-bbox="728 2172 760 2113">-</td><td data-bbox="769 2172 801 2113">-</td><td data-bbox="809 2172 842 2113">-</td><td colspan="2" data-bbox="1072 2172 1242 2113">INT15_0</td></tr> </tbody> </table>	Pin no.						Pin Name		64	80	100	120	144	176			-	-	-	-	2	2	P015		-	-	-	-	3	3	D29		-	-	-	-	-	-	TRG0_0		-	-	-	-	-	-	P016		-	-	-	-	3	3	D30		-	-	-	-	-	-	TRG1_0		-	-	-	-	-	-	P170		-	-	-	-	-	-	PPG36_1		-	-	-	-	-	-	P017		-	-	-	-	4	5	D31		-	-	-	-	-	-	TRG2_0		-	-	-	-	-	-	P171		-	-	-	-	-	-	PPG37_1		-	-	-	-	-	-	P020		-	-	-	-	-	-	ASX *2, *3, *4, *5		2 *1	2 *1	2 *1	2 *1	5	7	SIN3_1		-	-	-	-	-	-	TRG3_0		-	-	-	-	-	-	TIN0_2		-	-	-	-	-	-	RTO5_1		-	-	-	-	-	-	P021		-	-	-	-	-	-	CS0X *5		-	-	-	-	-	-	SOT3_1		-	-	-	-	-	-	TRG6_1		-	-	-	-	-	-	TRG4_0		-	-	-	-	-	-	P022		-	-	-	-	-	-	CS1X *5		-	-	-	-	-	-	SCK3_1		-	-	-	-	-	-	TRG7_1		-	-	-	-	-	-	TRG5_0		-	-	-	-	-	-	P023		-	-	-	-	-	-	RDX *5		-	-	-	-	-	-	SCS3_1		-	-	-	-	-	-	PPG32_0		-	-	-	-	-	-	TIN0_0		-	-	-	-	-	-	P024		-	-	-	-	-	-	WR0X *2, *3, *4, *5		-	-	-	-	-	-	SIN4_1		-	-	-	-	-	-	PPG24_0		-	-	-	-	-	-	TIN1_0		-	-	-	-	-	-	RTO4_1		-	-	-	-	-	-	INT15_0	
Pin no.						Pin Name																																																																																																																																																																																																																																																																																																																																																				
64	80	100	120	144	176																																																																																																																																																																																																																																																																																																																																																					
-	-	-	-	2	2	P015																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	3	3	D29																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG0_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P016																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	3	3	D30																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG1_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P170																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	PPG36_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P017																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	4	5	D31																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG2_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P171																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	PPG37_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P020																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	ASX *2, *3, *4, *5																																																																																																																																																																																																																																																																																																																																																				
2 *1	2 *1	2 *1	2 *1	5	7	SIN3_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG3_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TIN0_2																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	RTO5_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P021																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	CS0X *5																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	SOT3_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG6_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG4_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P022																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	CS1X *5																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	SCK3_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG7_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TRG5_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P023																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	RDX *5																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	SCS3_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	PPG32_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TIN0_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	P024																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	WR0X *2, *3, *4, *5																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	SIN4_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	PPG24_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	TIN1_0																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	RTO4_1																																																																																																																																																																																																																																																																																																																																																				
-	-	-	-	-	-	INT15_0																																																																																																																																																																																																																																																																																																																																																				

Page	Section	Change Results																																																																																																																																																																																																																																																																																																																																		
20	■PIN Description	A List of "Pin Description" modified. (Error) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th>Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> <th></th> </tr> </thead> <tbody> <tr> <td>-</td> <td>-</td> <td>4</td> <td>7</td> <td>10</td> <td>12</td> <td>P025</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>13</td> <td>WR1X</td> </tr> <tr> <td>-</td> <td>4</td> <td>5</td> <td>8</td> <td>11</td> <td>14</td> <td>SOT4_1</td> </tr> <tr> <td>-</td> <td>5</td> <td>6</td> <td>9</td> <td>12</td> <td>15</td> <td>PPG25_0</td> </tr> <tr> <td>-</td> <td>6</td> <td>8</td> <td>11</td> <td>14</td> <td>18</td> <td>TIN2_0</td> </tr> <tr> <td>-</td> <td>7</td> <td>10</td> <td>13</td> <td>15</td> <td>19</td> <td>P172</td> </tr> <tr> <td>-</td> <td>8</td> <td>12</td> <td>16</td> <td>18</td> <td>20</td> <td>PPG38_1</td> </tr> <tr> <td>-</td> <td>9</td> <td>11</td> <td>14</td> <td>17</td> <td></td> <td>P026</td> </tr> <tr> <td>-</td> <td>10</td> <td>13</td> <td>15</td> <td>18</td> <td></td> <td>A00</td> </tr> <tr> <td>-</td> <td>11</td> <td>14</td> <td>17</td> <td>19</td> <td></td> <td>SCK4_1</td> </tr> <tr> <td>-</td> <td>12</td> <td>15</td> <td>18</td> <td>20</td> <td></td> <td>PPG26_0</td> </tr> <tr> <td>-</td> <td>13</td> <td>16</td> <td>19</td> <td></td> <td></td> <td>TIN3_0</td> </tr> <tr> <td>-</td> <td>14</td> <td>17</td> <td>19</td> <td></td> <td></td> <td>P027</td> </tr> <tr> <td>-</td> <td>15</td> <td>18</td> <td></td> <td></td> <td></td> <td>A01</td> </tr> <tr> <td>-</td> <td>16</td> <td>19</td> <td></td> <td></td> <td></td> <td>SCS40_1</td> </tr> <tr> <td>-</td> <td>17</td> <td>20</td> <td></td> <td></td> <td></td> <td>PPG27_0</td> </tr> <tr> <td>-</td> <td>18</td> <td></td> <td></td> <td></td> <td></td> <td>TOT0_0</td> </tr> <tr> <td>-</td> <td>19</td> <td></td> <td></td> <td></td> <td></td> <td>RTO3_1</td> </tr> <tr> <td>-</td> <td>20</td> <td></td> <td></td> <td></td> <td></td> <td>P173</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG39_1</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P030</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A02</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS41_1</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG28_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT1_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P031</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A03</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS42_1</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG29_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT2_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P032</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A04</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS43_1</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG30_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT3_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>RTO2_1</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P033</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A05</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG31_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU3_3</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIN4_0</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>RTO1_1</td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCK3_2</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176		-	-	4	7	10	12	P025	-	-	-	-	-	13	WR1X	-	4	5	8	11	14	SOT4_1	-	5	6	9	12	15	PPG25_0	-	6	8	11	14	18	TIN2_0	-	7	10	13	15	19	P172	-	8	12	16	18	20	PPG38_1	-	9	11	14	17		P026	-	10	13	15	18		A00	-	11	14	17	19		SCK4_1	-	12	15	18	20		PPG26_0	-	13	16	19			TIN3_0	-	14	17	19			P027	-	15	18				A01	-	16	19				SCS40_1	-	17	20				PPG27_0	-	18					TOT0_0	-	19					RTO3_1	-	20					P173	-						PPG39_1	-						P030	-						A02	-						SCS41_1	-						PPG28_0	-						TOT1_0	-						P031	-						A03	-						SCS42_1	-						PPG29_0	-						TOT2_0	-						P032	-						A04	-						SCS43_1	-						PPG30_0	-						TOT3_0	-						RTO2_1	-						P033	-						A05	-						PPG31_0	-						ICU3_3	-						TIN4_0	-						RTO1_1	-						SCK3_2							
Pin no.						Pin Name																																																																																																																																																																																																																																																																																																																														
64	80	100	120	144	176																																																																																																																																																																																																																																																																																																																															
-	-	4	7	10	12	P025																																																																																																																																																																																																																																																																																																																														
-	-	-	-	-	13	WR1X																																																																																																																																																																																																																																																																																																																														
-	4	5	8	11	14	SOT4_1																																																																																																																																																																																																																																																																																																																														
-	5	6	9	12	15	PPG25_0																																																																																																																																																																																																																																																																																																																														
-	6	8	11	14	18	TIN2_0																																																																																																																																																																																																																																																																																																																														
-	7	10	13	15	19	P172																																																																																																																																																																																																																																																																																																																														
-	8	12	16	18	20	PPG38_1																																																																																																																																																																																																																																																																																																																														
-	9	11	14	17		P026																																																																																																																																																																																																																																																																																																																														
-	10	13	15	18		A00																																																																																																																																																																																																																																																																																																																														
-	11	14	17	19		SCK4_1																																																																																																																																																																																																																																																																																																																														
-	12	15	18	20		PPG26_0																																																																																																																																																																																																																																																																																																																														
-	13	16	19			TIN3_0																																																																																																																																																																																																																																																																																																																														
-	14	17	19			P027																																																																																																																																																																																																																																																																																																																														
-	15	18				A01																																																																																																																																																																																																																																																																																																																														
-	16	19				SCS40_1																																																																																																																																																																																																																																																																																																																														
-	17	20				PPG27_0																																																																																																																																																																																																																																																																																																																														
-	18					TOT0_0																																																																																																																																																																																																																																																																																																																														
-	19					RTO3_1																																																																																																																																																																																																																																																																																																																														
-	20					P173																																																																																																																																																																																																																																																																																																																														
-						PPG39_1																																																																																																																																																																																																																																																																																																																														
-						P030																																																																																																																																																																																																																																																																																																																														
-						A02																																																																																																																																																																																																																																																																																																																														
-						SCS41_1																																																																																																																																																																																																																																																																																																																														
-						PPG28_0																																																																																																																																																																																																																																																																																																																														
-						TOT1_0																																																																																																																																																																																																																																																																																																																														
-						P031																																																																																																																																																																																																																																																																																																																														
-						A03																																																																																																																																																																																																																																																																																																																														
-						SCS42_1																																																																																																																																																																																																																																																																																																																														
-						PPG29_0																																																																																																																																																																																																																																																																																																																														
-						TOT2_0																																																																																																																																																																																																																																																																																																																														
-						P032																																																																																																																																																																																																																																																																																																																														
-						A04																																																																																																																																																																																																																																																																																																																														
-						SCS43_1																																																																																																																																																																																																																																																																																																																														
-						PPG30_0																																																																																																																																																																																																																																																																																																																														
-						TOT3_0																																																																																																																																																																																																																																																																																																																														
-						RTO2_1																																																																																																																																																																																																																																																																																																																														
-						P033																																																																																																																																																																																																																																																																																																																														
-						A05																																																																																																																																																																																																																																																																																																																														
-						PPG31_0																																																																																																																																																																																																																																																																																																																														
-						ICU3_3																																																																																																																																																																																																																																																																																																																														
-						TIN4_0																																																																																																																																																																																																																																																																																																																														
-						RTO1_1																																																																																																																																																																																																																																																																																																																														
-						SCK3_2																																																																																																																																																																																																																																																																																																																														

Page	Section	Change Results							
		(Continued) (Correct)							
20	■PIN Description	Pin no.						Pin Name	
		64	80	100	120	144	176	P025	
		-	-	4 ^{*1}	7 ^{*1}	10	12	WR1X ^{*4, *5}	
		-	-	-	-	-	13	SOT4_1	
		-	-	-	-	-	14	PPG25_0	
		-	4 ^{*1}	5 ^{*1}	8 ^{*1}	11	14	TIN2_0	
		-	4 ^{*1}	5 ^{*1}	6 ^{*1}	9 ^{*1}	12	15	P172
		-	4 ^{*1}	5 ^{*1}	6 ^{*1}	9 ^{*1}	12	15	PPG38_1
		-	-	-	-	-	16	P026	
		-	-	7 ^{*1}	10 ^{*1}	13	17	A00 ^{*3, *4, *5}	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	SCK4_1	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	PPG26_0	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	TIN3_0	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	P027	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	A01 ^{*2, *3, *4, *5}	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	SCS40_1	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	PPG27_0	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	TOT0_0	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	RTO3_1	
		-	-	-	-	-	16	P173	
		-	-	-	-	-	16	PPG39_1	
		-	-	7 ^{*1}	10 ^{*1}	13	17	P030	
		-	-	7 ^{*1}	10 ^{*1}	13	17	A02 ^{*4, *5}	
		-	-	7 ^{*1}	10 ^{*1}	13	17	SCS41_1	
		-	-	7 ^{*1}	10 ^{*1}	13	17	PPG28_0	
		-	-	7 ^{*1}	10 ^{*1}	13	17	TOT1_0	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	P031	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	A03 ^{*3, *4, *5}	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	SCS42_1	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	PPG29_0	
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	TOT2_0 ^{*3}	
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	P032
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	A04 ^{*2, *3, *4, *5}
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	SCS43_1
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	PPG30_0
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	TOT3_0
		-	5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	RTO2_1
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	P033
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	A05 ^{*2, *3, *4, *5}
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	PPG31_0
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	ICU3_3
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	TIN4_0
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	RTO1_1
		-	6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	SCK3_2

Page	Section	Change Results																																																																																																																																																																																																																																																																																					
21, 22	■PIN Description	A List of "Pin Description" modified. (Errors) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th>Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> <th></th> </tr> </thead> <tbody> <tr> <td>7</td> <td>9</td> <td>11</td> <td>14</td> <td>17</td> <td>21</td> <td>P034</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A06</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>OCU11_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU2_3</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIN5_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>RTO0_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SOT3_2</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P151</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCK8_0/</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCL8</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>OCU9_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG7_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU0_3</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIN7_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ZIN0_2</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>DTT1_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P035</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A07</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SIN8_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>OCU8_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT4_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AIN0_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT11_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P036</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A08</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS8_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>OCU7_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT5_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>BIN0_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P037</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A09</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>OCU6_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT6_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ZIN0_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P174</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG8_1</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176		7	9	11	14	17	21	P034							A06							OCU11_1							ICU2_3							TIN5_0							RTO0_1							SOT3_2														P151							SCK8_0/							SCL8							OCU9_1							TRG7_0							ICU0_3							TIN7_0							ZIN0_2							DTT1_1							P035							A07							SIN8_0							OCU8_1							TOT4_0							AIN0_0							INT11_0							P036							A08							SCS8_0							OCU7_1							TOT5_0							BIN0_0							P037							A09							OCU6_1							TOT6_0							ZIN0_0							P174							TRG8_1				
Pin no.						Pin Name																																																																																																																																																																																																																																																																																	
64	80	100	120	144	176																																																																																																																																																																																																																																																																																		
7	9	11	14	17	21	P034																																																																																																																																																																																																																																																																																	
						A06																																																																																																																																																																																																																																																																																	
						OCU11_1																																																																																																																																																																																																																																																																																	
						ICU2_3																																																																																																																																																																																																																																																																																	
						TIN5_0																																																																																																																																																																																																																																																																																	
						RTO0_1																																																																																																																																																																																																																																																																																	
						SOT3_2																																																																																																																																																																																																																																																																																	
						P151																																																																																																																																																																																																																																																																																	
						SCK8_0/																																																																																																																																																																																																																																																																																	
						SCL8																																																																																																																																																																																																																																																																																	
						OCU9_1																																																																																																																																																																																																																																																																																	
						TRG7_0																																																																																																																																																																																																																																																																																	
						ICU0_3																																																																																																																																																																																																																																																																																	
						TIN7_0																																																																																																																																																																																																																																																																																	
						ZIN0_2																																																																																																																																																																																																																																																																																	
						DTT1_1																																																																																																																																																																																																																																																																																	
						P035																																																																																																																																																																																																																																																																																	
						A07																																																																																																																																																																																																																																																																																	
						SIN8_0																																																																																																																																																																																																																																																																																	
						OCU8_1																																																																																																																																																																																																																																																																																	
						TOT4_0																																																																																																																																																																																																																																																																																	
						AIN0_0																																																																																																																																																																																																																																																																																	
						INT11_0																																																																																																																																																																																																																																																																																	
						P036																																																																																																																																																																																																																																																																																	
						A08																																																																																																																																																																																																																																																																																	
						SCS8_0																																																																																																																																																																																																																																																																																	
						OCU7_1																																																																																																																																																																																																																																																																																	
						TOT5_0																																																																																																																																																																																																																																																																																	
						BIN0_0																																																																																																																																																																																																																																																																																	
						P037																																																																																																																																																																																																																																																																																	
						A09																																																																																																																																																																																																																																																																																	
						OCU6_1																																																																																																																																																																																																																																																																																	
						TOT6_0																																																																																																																																																																																																																																																																																	
						ZIN0_0																																																																																																																																																																																																																																																																																	
						P174																																																																																																																																																																																																																																																																																	
						TRG8_1																																																																																																																																																																																																																																																																																	

Page	Section	Change Results						
		(Continued) (Correct)						
Page	Section	Pin no.	Pin Name					
21, 22	■PIN Description	64 80 100 120 144 176	P034 A06 *2, *3, *4, *5 OCU11_1 ICU2_3 TIN5_0 RTO0_1 SOT3_2		7 *1 9 *1 11 *1 14 *1 17 21			
			P151 SCK8_0/ SCL8 *2, *3 OCU9_1 TRG7_0 ICU0_3 TIN7_0 ZIN0_2 DTTI_1		8 *1 10 *1 13 16 19 23			
			P035 A07 *2, *3, *4, *5 SIN8_0 *2, *3 OCU8_1 TOT4_0 AIN0_0 INT11_0		9 *1 11 *1 14 *1 17 *1 20 24			
			P036 A08 *2, *3, *4, *5 SCS8_0 *2, *3 OCU7_1 TOT5_0 BIN0_0		10 *1 12 *1 15 *1 18 *1 21 25			
			P037 A09 *4, *5 OCU6_1 TOT6_0 ZIN0_0		- - 16 *1 19 *1 22 26			
			P174 TRG8_1		- - - - - 27			

Page	Section	Change Results																																																																																																																																																																																																																																																																																																																																		
22, 23	■PIN Description	A List of "Pin Description" modified. (Error) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th>Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> <th></th> </tr> </thead> <tbody> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>28</td> <td>P175</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG9_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P040</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A10</td> </tr> <tr> <td>11</td> <td>13</td> <td>17</td> <td>20</td> <td>23</td> <td>29</td> <td>PPG23_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT7_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AIN1_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SIN0_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P041</td> </tr> <tr> <td>12</td> <td>14</td> <td>18</td> <td>21</td> <td>24</td> <td>30</td> <td>A11</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SIN9_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU9_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>BIN1_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT12_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P042</td> </tr> <tr> <td>13</td> <td>15</td> <td>19</td> <td>22</td> <td>25</td> <td>31</td> <td>A12</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SOT9_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN47</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU8_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG0_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ZIN1_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P043</td> </tr> <tr> <td>-</td> <td>-</td> <td>20</td> <td>23</td> <td>26</td> <td>32</td> <td>A13</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU7_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG1_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P044</td> </tr> <tr> <td>-</td> <td>16</td> <td>21</td> <td>24</td> <td>27</td> <td>33</td> <td>A14</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS9_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU6_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG2_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P045</td> </tr> <tr> <td>14</td> <td>17</td> <td>22</td> <td>25</td> <td>28</td> <td>34</td> <td>A15</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCK9_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN46</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU5_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG3_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TOT1_2</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P046</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>26</td> <td>29</td> <td>35</td> <td>A16</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU4_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG4_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P176</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>36</td> <td>TRG10_0</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176		-	-	-	-	-	28	P175							TRG9_1							P040							A10	11	13	17	20	23	29	PPG23_1							TOT7_0							AIN1_0							SIN0_1							P041	12	14	18	21	24	30	A11							SIN9_0							ICU9_1							BIN1_0							INT12_0							P042	13	15	19	22	25	31	A12							SOT9_0							AN47							ICU8_1							TRG0_1							ZIN1_0							P043	-	-	20	23	26	32	A13							ICU7_1							TRG1_1							P044	-	16	21	24	27	33	A14							SCS9_0							ICU6_1							TRG2_1							P045	14	17	22	25	28	34	A15							SCK9_0							AN46							ICU5_1							TRG3_1							TOT1_2							P046	-	-	-	26	29	35	A16							ICU4_1							TRG4_1							P176	-	-	-	-	-	36	TRG10_0							
Pin no.						Pin Name																																																																																																																																																																																																																																																																																																																														
64	80	100	120	144	176																																																																																																																																																																																																																																																																																																																															
-	-	-	-	-	28	P175																																																																																																																																																																																																																																																																																																																														
						TRG9_1																																																																																																																																																																																																																																																																																																																														
						P040																																																																																																																																																																																																																																																																																																																														
						A10																																																																																																																																																																																																																																																																																																																														
11	13	17	20	23	29	PPG23_1																																																																																																																																																																																																																																																																																																																														
						TOT7_0																																																																																																																																																																																																																																																																																																																														
						AIN1_0																																																																																																																																																																																																																																																																																																																														
						SIN0_1																																																																																																																																																																																																																																																																																																																														
						P041																																																																																																																																																																																																																																																																																																																														
12	14	18	21	24	30	A11																																																																																																																																																																																																																																																																																																																														
						SIN9_0																																																																																																																																																																																																																																																																																																																														
						ICU9_1																																																																																																																																																																																																																																																																																																																														
						BIN1_0																																																																																																																																																																																																																																																																																																																														
						INT12_0																																																																																																																																																																																																																																																																																																																														
						P042																																																																																																																																																																																																																																																																																																																														
13	15	19	22	25	31	A12																																																																																																																																																																																																																																																																																																																														
						SOT9_0																																																																																																																																																																																																																																																																																																																														
						AN47																																																																																																																																																																																																																																																																																																																														
						ICU8_1																																																																																																																																																																																																																																																																																																																														
						TRG0_1																																																																																																																																																																																																																																																																																																																														
						ZIN1_0																																																																																																																																																																																																																																																																																																																														
						P043																																																																																																																																																																																																																																																																																																																														
-	-	20	23	26	32	A13																																																																																																																																																																																																																																																																																																																														
						ICU7_1																																																																																																																																																																																																																																																																																																																														
						TRG1_1																																																																																																																																																																																																																																																																																																																														
						P044																																																																																																																																																																																																																																																																																																																														
-	16	21	24	27	33	A14																																																																																																																																																																																																																																																																																																																														
						SCS9_0																																																																																																																																																																																																																																																																																																																														
						ICU6_1																																																																																																																																																																																																																																																																																																																														
						TRG2_1																																																																																																																																																																																																																																																																																																																														
						P045																																																																																																																																																																																																																																																																																																																														
14	17	22	25	28	34	A15																																																																																																																																																																																																																																																																																																																														
						SCK9_0																																																																																																																																																																																																																																																																																																																														
						AN46																																																																																																																																																																																																																																																																																																																														
						ICU5_1																																																																																																																																																																																																																																																																																																																														
						TRG3_1																																																																																																																																																																																																																																																																																																																														
						TOT1_2																																																																																																																																																																																																																																																																																																																														
						P046																																																																																																																																																																																																																																																																																																																														
-	-	-	26	29	35	A16																																																																																																																																																																																																																																																																																																																														
						ICU4_1																																																																																																																																																																																																																																																																																																																														
						TRG4_1																																																																																																																																																																																																																																																																																																																														
						P176																																																																																																																																																																																																																																																																																																																														
-	-	-	-	-	36	TRG10_0																																																																																																																																																																																																																																																																																																																														

Page	Section	Change Results										
		(Continued) (Correct)										
22, 23	■PIN Description	64	80	100	120	144	176	Pin no.				Pin Name
		-	-	-	-	-	28					P175
		11 ^{*1}	13 ^{*1}	17 ^{*1}	20 ^{*1}	23	29					TRG9_1
												P040
												A10 ^{*2, *3, *4, *5}
												PPG23_1
												TOT7_0
												AIN1_0
												SIN0_1
		12 ^{*1}	14 ^{*1}	18 ^{*1}	21 ^{*1}	24	30					P041
												A11 ^{*2, *3, *4, *5}
												SIN9_0
												ICU9_1
												BIN1_0
												INT12_0
		13 ^{*1}	15 ^{*1}	19 ^{*1}	22 ^{*1}	25	31					P042
												A12 ^{*2, *3, *4, *5}
												SOT9_0
												AN47
												ICU8_1
												TRG0_1
												ZIN1_0
												P043
22, 23	■PIN Description	-	-	20 ^{*1}	23 ^{*1}	26	32					A13 ^{*4, *5}
		-	16 ^{*1}	21 ^{*1}	24 ^{*1}	27	33					ICU7_1
												TRG1_1
												P044
												A14 ^{*3, *4, *5}
												SCS9_0
												ICU6_1
												TRG2_1
		14 ^{*1}	17 ^{*1}	22 ^{*1}	25 ^{*1}	28	34					P045
												A15 ^{*2, *3, *4, *5}
												SCK9_0
												AN46
												ICU5_1
												TRG3_1
												TOT1_2
												P046
22, 23	■PIN Description	-	-	-	26 ^{*1}	29	35					A16 ^{*5}
		-	-	-	-	-	36					ICU4_1
		-	-	-	-	-	-					TRG4_1
		-	-	-	-	-	-					P176
		-	-	-	-	-	-					TRG10_0

Page	Section	Change Results																																																																																																																																																																																																																																																																																																																				
23, 24	■PIN Description	A List of "Pin Description" modified. (Errors) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th>Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> <th></th> </tr> </thead> <tbody> <tr> <td>15</td> <td>18</td> <td>23</td> <td>27</td> <td>30</td> <td>37</td> <td>P047</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A17</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN45</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG8_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIN3_2</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SOT0_1</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>38</td> <td>P177</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG11_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td>28</td> <td>31</td> <td>39</td> <td>P050</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A18</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG5_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG33_0</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>32</td> <td>40</td> <td>P051</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A19</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TRG9_0</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>33</td> <td>41</td> <td>P052</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A20</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG34_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT14_0</td> </tr> <tr> <td>16</td> <td>19</td> <td>24</td> <td>29</td> <td>34</td> <td>42</td> <td>P053</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A21</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN44</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG35_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT14_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCK0_1</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>35</td> <td>43</td> <td>P054</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SYSCLK</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG36_0</td> </tr> <tr> <td>17</td> <td>22</td> <td>27</td> <td>32</td> <td>38</td> <td>46</td> <td>P055</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>CS2X</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SIN10_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN43</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG37_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIN4_1</td> </tr> <tr> <td>-</td> <td>-</td> <td>-</td> <td>33</td> <td>39</td> <td>49</td> <td>P056</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>CS3X</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU9_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG0_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ICU0_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIN5_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>DTT1_2</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176		15	18	23	27	30	37	P047							A17							AN45							TRG8_0							TIN3_2							SOT0_1	-	-	-	-	-	38	P177							TRG11_0				28	31	39	P050							A18							TRG5_1							PPG33_0	-	-	-	-	32	40	P051							A19							TRG9_0	-	-	-	-	33	41	P052							A20							PPG34_0							INT14_0	16	19	24	29	34	42	P053							A21							AN44							PPG35_0							INT14_1							SCK0_1	-	-	-	-	35	43	P054							SYSCLK							PPG36_0	17	22	27	32	38	46	P055							CS2X							SIN10_0							AN43							PPG37_0							TIN4_1	-	-	-	33	39	49	P056							CS3X							ICU9_0							PPG0_1							ICU0_1							TIN5_1							DTT1_2							
Pin no.						Pin Name																																																																																																																																																																																																																																																																																																																
64	80	100	120	144	176																																																																																																																																																																																																																																																																																																																	
15	18	23	27	30	37	P047																																																																																																																																																																																																																																																																																																																
						A17																																																																																																																																																																																																																																																																																																																
						AN45																																																																																																																																																																																																																																																																																																																
						TRG8_0																																																																																																																																																																																																																																																																																																																
						TIN3_2																																																																																																																																																																																																																																																																																																																
						SOT0_1																																																																																																																																																																																																																																																																																																																
-	-	-	-	-	38	P177																																																																																																																																																																																																																																																																																																																
						TRG11_0																																																																																																																																																																																																																																																																																																																
			28	31	39	P050																																																																																																																																																																																																																																																																																																																
						A18																																																																																																																																																																																																																																																																																																																
						TRG5_1																																																																																																																																																																																																																																																																																																																
						PPG33_0																																																																																																																																																																																																																																																																																																																
-	-	-	-	32	40	P051																																																																																																																																																																																																																																																																																																																
						A19																																																																																																																																																																																																																																																																																																																
						TRG9_0																																																																																																																																																																																																																																																																																																																
-	-	-	-	33	41	P052																																																																																																																																																																																																																																																																																																																
						A20																																																																																																																																																																																																																																																																																																																
						PPG34_0																																																																																																																																																																																																																																																																																																																
						INT14_0																																																																																																																																																																																																																																																																																																																
16	19	24	29	34	42	P053																																																																																																																																																																																																																																																																																																																
						A21																																																																																																																																																																																																																																																																																																																
						AN44																																																																																																																																																																																																																																																																																																																
						PPG35_0																																																																																																																																																																																																																																																																																																																
						INT14_1																																																																																																																																																																																																																																																																																																																
						SCK0_1																																																																																																																																																																																																																																																																																																																
-	-	-	-	35	43	P054																																																																																																																																																																																																																																																																																																																
						SYSCLK																																																																																																																																																																																																																																																																																																																
						PPG36_0																																																																																																																																																																																																																																																																																																																
17	22	27	32	38	46	P055																																																																																																																																																																																																																																																																																																																
						CS2X																																																																																																																																																																																																																																																																																																																
						SIN10_0																																																																																																																																																																																																																																																																																																																
						AN43																																																																																																																																																																																																																																																																																																																
						PPG37_0																																																																																																																																																																																																																																																																																																																
						TIN4_1																																																																																																																																																																																																																																																																																																																
-	-	-	33	39	49	P056																																																																																																																																																																																																																																																																																																																
						CS3X																																																																																																																																																																																																																																																																																																																
						ICU9_0																																																																																																																																																																																																																																																																																																																
						PPG0_1																																																																																																																																																																																																																																																																																																																
						ICU0_1																																																																																																																																																																																																																																																																																																																
						TIN5_1																																																																																																																																																																																																																																																																																																																
						DTT1_2																																																																																																																																																																																																																																																																																																																

Page	Section	Change Results						
		(Continued) (Correct)						
Pin no.								Pin Name
23, 24	■PIN Description	64	80	100	120	144	176	
		15 ^{*1}	18 ^{*1}	23 ^{*1}	27 ^{*1}	30	37	P047
		-	-	-	-	-	38	A17 ^{*2, *3, *4, *5}
		-	-	-	28 ^{*1}	31	39	AN45
		-	-	-	-	32	40	TRG8_0
		-	-	-	-	33	41	TIN3_2
		-	-	-	-	34	42	SOT0_1
		16 ^{*1}	19 ^{*1}	24 ^{*1}	29 ^{*1}	35	43	P177
		17 ^{*1}	22 ^{*1}	27 ^{*1}	32 ^{*1}	38	46	TRG11_0
		-	-	-	-	39	49	P050
		-	-	-	-	40		A18 ^{*5}
		-	-	-	-	41		TRG5_1
		-	-	-	-	42		PPG33_0
		-	-	-	-	43		P051
		-	-	-	-	44		A19
		-	-	-	-	45		TRG9_0
		-	-	-	-	46		P052
		-	-	-	-	47		A20
		-	-	-	-	48		PPG34_0
		-	-	-	-	49		INT14_0
		-	-	-	-	50		P053
		-	-	-	-	51		A21 ^{*2, *3, *4, *5}
		-	-	-	-	52		AN44
		-	-	-	-	53		PPG35_0
		-	-	-	-	54		INT14_1
		-	-	-	-	55		SCK0_1
		-	-	-	-	56		P054
		-	-	-	-	57		SYSCLK
		-	-	-	-	58		PPG36_0
		-	-	-	-	59		P055
		-	-	-	-	60		CS2X ^{*2, *3, *4, *5}
		-	-	-	-	61		SIN10_0
		-	-	-	-	62		AN43
		-	-	-	-	63		PPG37_0
		-	-	-	-	64		TIN4_1
		-	-	-	-	65		P056
		-	-	-	-	66		CS3X ^{*5}
		-	-	-	-	67		ICU9_0
		-	-	-	-	68		PPG0_1
		-	-	-	-	69		ICU0_1
		-	-	-	-	70		TIN5_1
		-	-	-	-	71		DTI1_2

Page	Section	Change Results														
24	■PIN Description	<p>A List of "Pin Description" modified.</p> <p>(Error)</p> <table border="1"> <tr><td>Function^{*2}</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External Bus chip select 2 output pin(0)</td></tr> <tr><td>Multi-function serial ch.10 serial data input pin(0)</td></tr> <tr><td>ADC analog 43 input pin</td></tr> <tr><td>PPG ch.37 output pin(0)</td></tr> <tr><td>Reload timer ch.4 event input pin(1)</td></tr> </table> <p>(Correct)</p> <table border="1"> <tr><td>Function^{*9}</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External Bus chip select 2 output pin</td></tr> <tr><td>Multi-function serial ch.10 serial data input pin(0)</td></tr> <tr><td>ADC analog 43 input pin</td></tr> <tr><td>PPG ch.37 output pin(0)</td></tr> <tr><td>Reload timer ch.4 event input pin(1)</td></tr> </table>	Function ^{*2}	General-purpose I/O port	External Bus chip select 2 output pin(0)	Multi-function serial ch.10 serial data input pin(0)	ADC analog 43 input pin	PPG ch.37 output pin(0)	Reload timer ch.4 event input pin(1)	Function ^{*9}	General-purpose I/O port	External Bus chip select 2 output pin	Multi-function serial ch.10 serial data input pin(0)	ADC analog 43 input pin	PPG ch.37 output pin(0)	Reload timer ch.4 event input pin(1)
Function ^{*2}																
General-purpose I/O port																
External Bus chip select 2 output pin(0)																
Multi-function serial ch.10 serial data input pin(0)																
ADC analog 43 input pin																
PPG ch.37 output pin(0)																
Reload timer ch.4 event input pin(1)																
Function ^{*9}																
General-purpose I/O port																
External Bus chip select 2 output pin																
Multi-function serial ch.10 serial data input pin(0)																
ADC analog 43 input pin																
PPG ch.37 output pin(0)																
Reload timer ch.4 event input pin(1)																

Page	Section	Change Results																
24	■PIN Description	<p>A List of "Pin Description" modified.</p> <p>(Error)</p> <table border="1" data-bbox="605 418 1149 762"> <tr><td>Function^{*2}</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External Bus chip select 3 output pin(0)</td></tr> <tr><td>Input capture ch.9 input pin(0)</td></tr> <tr><td>PPG ch.0 output pin(1)</td></tr> <tr><td>Input capture ch.0 input pin(1)</td></tr> <tr><td>Reload timer ch.5 event input pin(1)</td></tr> <tr><td>Waveform generator ch.0 to ch.5 input pin(2)</td></tr> </table> <p>(Correct)</p> <table border="1" data-bbox="605 826 1149 1174"> <tr><td>Function^{*9}</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External Bus chip select 3 output pin</td></tr> <tr><td>Input capture ch.9 input pin(0)</td></tr> <tr><td>PPG ch.0 output pin(1)</td></tr> <tr><td>Input capture ch.0 input pin(1)</td></tr> <tr><td>Reload timer ch.5 event input pin(1)</td></tr> <tr><td>Waveform generator ch.0 to ch.5 input pin(2)</td></tr> </table>	Function ^{*2}	General-purpose I/O port	External Bus chip select 3 output pin(0)	Input capture ch.9 input pin(0)	PPG ch.0 output pin(1)	Input capture ch.0 input pin(1)	Reload timer ch.5 event input pin(1)	Waveform generator ch.0 to ch.5 input pin(2)	Function ^{*9}	General-purpose I/O port	External Bus chip select 3 output pin	Input capture ch.9 input pin(0)	PPG ch.0 output pin(1)	Input capture ch.0 input pin(1)	Reload timer ch.5 event input pin(1)	Waveform generator ch.0 to ch.5 input pin(2)
Function ^{*2}																		
General-purpose I/O port																		
External Bus chip select 3 output pin(0)																		
Input capture ch.9 input pin(0)																		
PPG ch.0 output pin(1)																		
Input capture ch.0 input pin(1)																		
Reload timer ch.5 event input pin(1)																		
Waveform generator ch.0 to ch.5 input pin(2)																		
Function ^{*9}																		
General-purpose I/O port																		
External Bus chip select 3 output pin																		
Input capture ch.9 input pin(0)																		
PPG ch.0 output pin(1)																		
Input capture ch.0 input pin(1)																		
Reload timer ch.5 event input pin(1)																		
Waveform generator ch.0 to ch.5 input pin(2)																		

Page	Section	Change Results																																								
25	■PIN Description	<p>A List of "Pin Description" modified.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>19</td> <td>24</td> <td>29</td> <td>35</td> <td>41</td> <td>51</td> <td>P057 RDY SCK10_1 AN42 ICU8_0 TRG0_2 PPG1_1 ICU1_1 TIN6_1</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>19^{*1}</td> <td>24^{*1}</td> <td>29^{*1}</td> <td>35^{*1}</td> <td>41</td> <td>51</td> <td>P057 RDY^{*2, *3, *4, *5} SCK10_1 AN42 ICU8_0 TRG0_2 PPG1_1 ICU1_1 TIN6_1</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176	19	24	29	35	41	51	P057 RDY SCK10_1 AN42 ICU8_0 TRG0_2 PPG1_1 ICU1_1 TIN6_1	Pin no.						Pin Name	64	80	100	120	144	176	19 ^{*1}	24 ^{*1}	29 ^{*1}	35 ^{*1}	41	51	P057 RDY ^{*2, *3, *4, *5} SCK10_1 AN42 ICU8_0 TRG0_2 PPG1_1 ICU1_1 TIN6_1
Pin no.						Pin Name																																				
64	80	100	120	144	176																																					
19	24	29	35	41	51	P057 RDY SCK10_1 AN42 ICU8_0 TRG0_2 PPG1_1 ICU1_1 TIN6_1																																				
Pin no.						Pin Name																																				
64	80	100	120	144	176																																					
19 ^{*1}	24 ^{*1}	29 ^{*1}	35 ^{*1}	41	51	P057 RDY ^{*2, *3, *4, *5} SCK10_1 AN42 ICU8_0 TRG0_2 PPG1_1 ICU1_1 TIN6_1																																				
27	■PIN Description	<p>A List of "Pin Description" modified.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>35</td> <td>43</td> <td>49</td> <td>57</td> <td>71</td> <td>P073 SOT4_0/ SDA4 AN33 ICU3_2</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>35^{*3}</td> <td>43^{*4}</td> <td>49</td> <td>57</td> <td>71</td> <td>P073 SOT4_0/ SDA4^{*3, *4} AN33 ICU3_2</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176	-	35	43	49	57	71	P073 SOT4_0/ SDA4 AN33 ICU3_2	Pin no.						Pin Name	64	80	100	120	144	176	-	35 ^{*3}	43 ^{*4}	49	57	71	P073 SOT4_0/ SDA4 ^{*3, *4} AN33 ICU3_2
Pin no.						Pin Name																																				
64	80	100	120	144	176																																					
-	35	43	49	57	71	P073 SOT4_0/ SDA4 AN33 ICU3_2																																				
Pin no.						Pin Name																																				
64	80	100	120	144	176																																					
-	35 ^{*3}	43 ^{*4}	49	57	71	P073 SOT4_0/ SDA4 ^{*3, *4} AN33 ICU3_2																																				

Page	Section	Change Results																																													
29	■PIN Description	A List of "Pin Description" modified. (Error) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>34</td> <td>42</td> <td>52</td> <td>62</td> <td>77</td> <td>96</td> <td>P093 TX0_1 SIN11_0 AN7 ICU4_2 PPG16_1 ICU3_0 TOT2_1</td> </tr> </tbody> </table> (Correct) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>34^{*1}</td> <td>42^{*1}</td> <td>52</td> <td>62</td> <td>77</td> <td>96</td> <td>P093 TX0_1 SIN11_0 AN7 ICU4_2 PPG16_1 ICU3_0 TOT2_1^{*2, *3}</td> </tr> </tbody> </table>						Pin no.						Pin Name	64	80	100	120	144	176	34	42	52	62	77	96	P093 TX0_1 SIN11_0 AN7 ICU4_2 PPG16_1 ICU3_0 TOT2_1	Pin no.						Pin Name	64	80	100	120	144	176	34 ^{*1}	42 ^{*1}	52	62	77	96	P093 TX0_1 SIN11_0 AN7 ICU4_2 PPG16_1 ICU3_0 TOT2_1 ^{*2, *3}
Pin no.						Pin Name																																									
64	80	100	120	144	176																																										
34	42	52	62	77	96	P093 TX0_1 SIN11_0 AN7 ICU4_2 PPG16_1 ICU3_0 TOT2_1																																									
Pin no.						Pin Name																																									
64	80	100	120	144	176																																										
34 ^{*1}	42 ^{*1}	52	62	77	96	P093 TX0_1 SIN11_0 AN7 ICU4_2 PPG16_1 ICU3_0 TOT2_1 ^{*2, *3}																																									

Page	Section	Change Results																																																																																																																																																																																					
30	■PIN Description	A List of "Pin Description" modified.																																																																																																																																																																																					
(Error)																																																																																																																																																																																							
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="6" style="text-align: center;">Pin no.</th> <th rowspan="2" style="text-align: center; vertical-align: middle;">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>48</td> <td>59</td> <td>69</td> <td>85</td> <td>104</td> <td>P100</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCK7_0/ SCL7</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN12</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG8_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P102</td> </tr> <tr> <td></td> <td>40</td> <td>49</td> <td>61</td> <td>71</td> <td>87</td> <td>106</td> <td>SIN7_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN14</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG10_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT10_0</td> </tr> <tr> <td></td> <td>41</td> <td>50</td> <td>62</td> <td>72</td> <td>88</td> <td>107</td> <td>P103</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS73_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN15</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG11_0</td> </tr> <tr> <td></td> <td>42</td> <td>51</td> <td>63</td> <td>73</td> <td>89</td> <td>108</td> <td>P104</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS72_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN16</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG12_0</td> </tr> <tr> <td></td> <td>43</td> <td>52</td> <td>64</td> <td>74</td> <td>90</td> <td>109</td> <td>P105</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS71_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN17</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG13_0</td> </tr> </tbody> </table>								Pin no.						Pin Name	64	80	100	120	144	176	-	48	59	69	85	104	P100							SCK7_0/ SCL7							AN12							PPG8_0							P102		40	49	61	71	87	106	SIN7_0								AN14								PPG10_0								INT10_0		41	50	62	72	88	107	P103								SCS73_0								AN15								PPG11_0		42	51	63	73	89	108	P104								SCS72_0								AN16								PPG12_0		43	52	64	74	90	109	P105								SCS71_0								AN17								PPG13_0
Pin no.						Pin Name																																																																																																																																																																																	
64	80	100	120	144	176																																																																																																																																																																																		
-	48	59	69	85	104	P100																																																																																																																																																																																	
						SCK7_0/ SCL7																																																																																																																																																																																	
						AN12																																																																																																																																																																																	
						PPG8_0																																																																																																																																																																																	
						P102																																																																																																																																																																																	
	40	49	61	71	87	106	SIN7_0																																																																																																																																																																																
							AN14																																																																																																																																																																																
							PPG10_0																																																																																																																																																																																
							INT10_0																																																																																																																																																																																
	41	50	62	72	88	107	P103																																																																																																																																																																																
							SCS73_0																																																																																																																																																																																
							AN15																																																																																																																																																																																
							PPG11_0																																																																																																																																																																																
	42	51	63	73	89	108	P104																																																																																																																																																																																
							SCS72_0																																																																																																																																																																																
							AN16																																																																																																																																																																																
							PPG12_0																																																																																																																																																																																
	43	52	64	74	90	109	P105																																																																																																																																																																																
							SCS71_0																																																																																																																																																																																
							AN17																																																																																																																																																																																
							PPG13_0																																																																																																																																																																																
(Correct)																																																																																																																																																																																							
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="6" style="text-align: center;">Pin no.</th> <th rowspan="2" style="text-align: center; vertical-align: middle;">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>48^{*1}</td> <td>59</td> <td>69</td> <td>85</td> <td>104</td> <td>P100</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCK7_0/ SCL7^{*3}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN12</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG8_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P102</td> </tr> <tr> <td></td> <td>40^{*1}</td> <td>49^{*1}</td> <td>61</td> <td>71</td> <td>87</td> <td>106</td> <td>SIN7_0^{*2, *3}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN14</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG10_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT10_0</td> </tr> <tr> <td></td> <td>41^{*1}</td> <td>50^{*1}</td> <td>62</td> <td>72</td> <td>88</td> <td>107</td> <td>P103</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS73_0^{*2, *3}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN15</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG11_0</td> </tr> <tr> <td></td> <td>42^{*1}</td> <td>51^{*1}</td> <td>63</td> <td>73</td> <td>89</td> <td>108</td> <td>P104</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS72_0^{*2, *3}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN16</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG12_0</td> </tr> <tr> <td></td> <td>43^{*1}</td> <td>52^{*1}</td> <td>64</td> <td>74</td> <td>90</td> <td>109</td> <td>P105</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SCS71_0^{*2, *3}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>AN17</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PPG13_0</td> </tr> </tbody> </table>								Pin no.						Pin Name	64	80	100	120	144	176	-	48 ^{*1}	59	69	85	104	P100							SCK7_0/ SCL7 ^{*3}							AN12							PPG8_0							P102		40 ^{*1}	49 ^{*1}	61	71	87	106	SIN7_0 ^{*2, *3}								AN14								PPG10_0								INT10_0		41 ^{*1}	50 ^{*1}	62	72	88	107	P103								SCS73_0 ^{*2, *3}								AN15								PPG11_0		42 ^{*1}	51 ^{*1}	63	73	89	108	P104								SCS72_0 ^{*2, *3}								AN16								PPG12_0		43 ^{*1}	52 ^{*1}	64	74	90	109	P105								SCS71_0 ^{*2, *3}								AN17								PPG13_0
Pin no.						Pin Name																																																																																																																																																																																	
64	80	100	120	144	176																																																																																																																																																																																		
-	48 ^{*1}	59	69	85	104	P100																																																																																																																																																																																	
						SCK7_0/ SCL7 ^{*3}																																																																																																																																																																																	
						AN12																																																																																																																																																																																	
						PPG8_0																																																																																																																																																																																	
						P102																																																																																																																																																																																	
	40 ^{*1}	49 ^{*1}	61	71	87	106	SIN7_0 ^{*2, *3}																																																																																																																																																																																
							AN14																																																																																																																																																																																
							PPG10_0																																																																																																																																																																																
							INT10_0																																																																																																																																																																																
	41 ^{*1}	50 ^{*1}	62	72	88	107	P103																																																																																																																																																																																
							SCS73_0 ^{*2, *3}																																																																																																																																																																																
							AN15																																																																																																																																																																																
							PPG11_0																																																																																																																																																																																
	42 ^{*1}	51 ^{*1}	63	73	89	108	P104																																																																																																																																																																																
							SCS72_0 ^{*2, *3}																																																																																																																																																																																
							AN16																																																																																																																																																																																
							PPG12_0																																																																																																																																																																																
	43 ^{*1}	52 ^{*1}	64	74	90	109	P105																																																																																																																																																																																
							SCS71_0 ^{*2, *3}																																																																																																																																																																																
							AN17																																																																																																																																																																																
							PPG13_0																																																																																																																																																																																

Page	Section	Change Results																																																																																																																																																																		
33	■PIN Description	A List of "Pin Description" modified. (Error) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>-</td> <td>94</td> <td>111</td> <td>131</td> <td>159</td> <td>P000</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>D16</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SIN1_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIOA0_1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT2_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>P001</td> </tr> <tr> <td></td> <td></td> <td>75</td> <td>95</td> <td>112</td> <td>132</td> <td>160</td> <td>D17</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SOT1_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIOA1_1</td> </tr> </tbody> </table> (Correct) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th rowspan="2">Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>-</td> <td>94^{*1}</td> <td>111^{*1}</td> <td>131</td> <td>159</td> <td>P000</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>D16^{*4, *5}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SIN1_0</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIOA0_1^{*4}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>INT2_0</td> </tr> <tr> <td></td> <td></td> <td>75^{*1}</td> <td>95^{*1}</td> <td>112^{*1}</td> <td>132</td> <td>160</td> <td>P001</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>D17^{*3, *4, *5}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SOT1_0^{*3}</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>TIOA1_1</td> </tr> </tbody> </table>							Pin no.						Pin Name	64	80	100	120	144	176	-	-	94	111	131	159	P000							D16							SIN1_0							TIOA0_1							INT2_0							P001			75	95	112	132	160	D17								SOT1_0								TIOA1_1	Pin no.						Pin Name	64	80	100	120	144	176	-	-	94 ^{*1}	111 ^{*1}	131	159	P000							D16 ^{*4, *5}							SIN1_0							TIOA0_1 ^{*4}							INT2_0			75 ^{*1}	95 ^{*1}	112 ^{*1}	132	160	P001							D17 ^{*3, *4, *5}							SOT1_0 ^{*3}							TIOA1_1
Pin no.						Pin Name																																																																																																																																																														
64	80	100	120	144	176																																																																																																																																																															
-	-	94	111	131	159	P000																																																																																																																																																														
						D16																																																																																																																																																														
						SIN1_0																																																																																																																																																														
						TIOA0_1																																																																																																																																																														
						INT2_0																																																																																																																																																														
						P001																																																																																																																																																														
		75	95	112	132	160	D17																																																																																																																																																													
							SOT1_0																																																																																																																																																													
							TIOA1_1																																																																																																																																																													
Pin no.						Pin Name																																																																																																																																																														
64	80	100	120	144	176																																																																																																																																																															
-	-	94 ^{*1}	111 ^{*1}	131	159	P000																																																																																																																																																														
						D16 ^{*4, *5}																																																																																																																																																														
						SIN1_0																																																																																																																																																														
						TIOA0_1 ^{*4}																																																																																																																																																														
						INT2_0																																																																																																																																																														
		75 ^{*1}	95 ^{*1}	112 ^{*1}	132	160	P001																																																																																																																																																													
						D17 ^{*3, *4, *5}																																																																																																																																																														
						SOT1_0 ^{*3}																																																																																																																																																														
						TIOA1_1																																																																																																																																																														

Page	Section	Change Results																																																																																																																																																																																																																																																																																																													
34, 35	■PIN Description	A List of "Pin Description" modified. (Error) <table border="1"> <thead> <tr> <th colspan="6">Pin no.</th> <th>Pin Name</th> </tr> <tr> <th>64</th> <th>80</th> <th>100</th> <th>120</th> <th>144</th> <th>176</th> <th></th> </tr> </thead> <tbody> <tr> <td>-</td> <td>-</td> <td>-</td> <td>113</td> <td>133</td> <td>161</td> <td>P002</td> </tr> <tr> <td>-</td> <td>76</td> <td>96</td> <td>114</td> <td>134</td> <td>162</td> <td>D18</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>SCK1_0</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>TIOB0_1</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>P003</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>D19</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>SIN2_0</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>TIOB1_1</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>INT3_0</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>P004</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>D20</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>SOT2_0</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>P164</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>PPG32_1</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>P005</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>D21</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>SCK2_0</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>ADTG0_1</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>INT7_1</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>(RX2(64))</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>P165</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>PPG33_1</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>P006</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>D22</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>SCS2_0</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>ADTG1_1</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>INT2_1</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>(TX2(64))</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>P007</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>D23</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>P166</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>PPG34_1</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>P010</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>D24</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>P011</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>WOT</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>D25</td> </tr> <tr> <td>-</td> <td>63</td> <td>79</td> <td>99</td> <td>119</td> <td>140</td> <td>SOT2_1</td> </tr> <tr> <td>-</td> <td>61</td> <td>77</td> <td>97</td> <td>115</td> <td>136</td> <td>TIOA0_0</td> </tr> <tr> <td>-</td> <td>62</td> <td>78</td> <td>98</td> <td>116</td> <td>137</td> <td>INT3_1</td> </tr> </tbody> </table>	Pin no.						Pin Name	64	80	100	120	144	176		-	-	-	113	133	161	P002	-	76	96	114	134	162	D18	-	61	77	97	115	136	SCK1_0	-	62	78	98	116	137	TIOB0_1	-	63	79	99	119	140	P003	-	61	77	97	115	136	D19	-	62	78	98	116	137	SIN2_0	-	63	79	99	119	140	TIOB1_1	-	61	77	97	115	136	INT3_0	-	62	78	98	116	137	P004	-	63	79	99	119	140	D20	-	61	77	97	115	136	SOT2_0	-	62	78	98	116	137	P164	-	63	79	99	119	140	PPG32_1	-	61	77	97	115	136	P005	-	62	78	98	116	137	D21	-	63	79	99	119	140	SCK2_0	-	61	77	97	115	136	ADTG0_1	-	62	78	98	116	137	INT7_1	-	63	79	99	119	140	(RX2(64))	-	61	77	97	115	136	P165	-	62	78	98	116	137	PPG33_1	-	63	79	99	119	140	P006	-	61	77	97	115	136	D22	-	62	78	98	116	137	SCS2_0	-	63	79	99	119	140	ADTG1_1	-	61	77	97	115	136	INT2_1	-	62	78	98	116	137	(TX2(64))	-	63	79	99	119	140	P007	-	61	77	97	115	136	D23	-	62	78	98	116	137	P166	-	63	79	99	119	140	PPG34_1	-	61	77	97	115	136	P010	-	62	78	98	116	137	D24	-	63	79	99	119	140	P011	-	61	77	97	115	136	WOT	-	62	78	98	116	137	D25	-	63	79	99	119	140	SOT2_1	-	61	77	97	115	136	TIOA0_0	-	62	78	98	116	137	INT3_1							
Pin no.						Pin Name																																																																																																																																																																																																																																																																																																									
64	80	100	120	144	176																																																																																																																																																																																																																																																																																																										
-	-	-	113	133	161	P002																																																																																																																																																																																																																																																																																																									
-	76	96	114	134	162	D18																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	SCK1_0																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	TIOB0_1																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	P003																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	D19																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	SIN2_0																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	TIOB1_1																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	INT3_0																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	P004																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	D20																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	SOT2_0																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	P164																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	PPG32_1																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	P005																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	D21																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	SCK2_0																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	ADTG0_1																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	INT7_1																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	(RX2(64))																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	P165																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	PPG33_1																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	P006																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	D22																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	SCS2_0																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	ADTG1_1																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	INT2_1																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	(TX2(64))																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	P007																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	D23																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	P166																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	PPG34_1																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	P010																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	D24																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	P011																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	WOT																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	D25																																																																																																																																																																																																																																																																																																									
-	63	79	99	119	140	SOT2_1																																																																																																																																																																																																																																																																																																									
-	61	77	97	115	136	TIOA0_0																																																																																																																																																																																																																																																																																																									
-	62	78	98	116	137	INT3_1																																																																																																																																																																																																																																																																																																									

Page	Section	Change Results						
		(Continued) (Correct)						
		Pin no.						Pin Name
34, 35	■PIN Description	64	80	100	120	144	176	P002
		-	-	-	113 ^{*1}	133	161	D18 ^{*5}
							SCK1_0	
							TIOB0_1	
							P003	
			76 ^{*1}	96 ^{*1}	114 ^{*1}	134	162	D19 ^{*3, *4, *5}
							SIN2_0	
							TIOB1_1	
							INT3_0	
							P004	
			-	-	-	135	163	D20
							SOT2_0	
			-	-	-	-	164	P164
								PPG32_1
								P005
		61 ^{*1}	77 ^{*1}	97 ^{*1}	115 ^{*1}	136 ^{*1}	165 ^{*1}	D21 ^{*2, *3, *4, *5}
								SCK2_0 ^{*2}
								ADTG0_1
								INT7_1
								RX2(64) ^{*4, *5, *6, *7}
								P165
			-	-	-	-	166	PPG33_1
								P006
		62 ^{*1}	78 ^{*1}	98 ^{*1}	116 ^{*1}	137 ^{*1}	167 ^{*1}	D22 ^{*2, *3, *4, *5}
								SCS2_0 ^{*2}
								ADTG1_1
								INT2_1
								TX2(64) ^{*4, *5, *6, *7}
			-	-	117 ^{*1}	138	168	P007
								D23 ^{*5}
			-	-	-	-	169	P166
								PPG34_1
			-	-	118 ^{*1}	139	170	P010
								D24 ^{*5}
		63 ^{*1}	79 ^{*1}	99 ^{*1}	119 ^{*1}	140	171	P011
								WOT
								D25 ^{*2, *3, *4, *5}
								SOT2_1 ^{*2}
								TIOAO_0 ^{*2, *3, *4}
								INT3_1

Page	Section	Change Results																										
34	■PIN Description	<p>A List of "Pin Description" modified.</p> <p>(Error)</p> <table border="1" data-bbox="605 418 1149 1031"> <tr><td>Function^{*2}</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External bus data bit21 I/O (0)</td></tr> <tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr> <tr><td>A/D converter external trigger input 0 (1)</td></tr> <tr><td>INT7 External interrupt input (1)</td></tr> <tr><td>(CAN reception data 2 input MB91F52xB ,MB91F52xD only)</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External bus data bit22 I/O (0)</td></tr> <tr><td>Serial chip select 2 I/O (0)</td></tr> <tr><td>A/D converter external trigger input 1 (1)</td></tr> <tr><td>INT2 External interrupt input (1)</td></tr> <tr><td>(CAN transmission data 2 output MB91F52xB ,MB91F52xD only)</td></tr> </table> <p>(Correct)</p> <table border="1" data-bbox="605 1079 1149 1635"> <tr><td>Function^{*9}</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External bus data bit21 I/O (0)</td></tr> <tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr> <tr><td>A/D converter external trigger input 0 (1)</td></tr> <tr><td>INT7 External interrupt input (1)</td></tr> <tr><td>CAN reception data 2 input</td></tr> <tr><td>General-purpose I/O port</td></tr> <tr><td>External bus data bit22 I/O (0)</td></tr> <tr><td>Serial chip select 2 I/O (0)</td></tr> <tr><td>A/D converter external trigger input 1 (1)</td></tr> <tr><td>INT2 External interrupt input (1)</td></tr> <tr><td>CAN transmission data 2 output</td></tr> </table>	Function ^{*2}	General-purpose I/O port	External bus data bit21 I/O (0)	Multi-function serial ch.2 clock I/O (0)	A/D converter external trigger input 0 (1)	INT7 External interrupt input (1)	(CAN reception data 2 input MB91F52xB ,MB91F52xD only)	General-purpose I/O port	External bus data bit22 I/O (0)	Serial chip select 2 I/O (0)	A/D converter external trigger input 1 (1)	INT2 External interrupt input (1)	(CAN transmission data 2 output MB91F52xB ,MB91F52xD only)	Function ^{*9}	General-purpose I/O port	External bus data bit21 I/O (0)	Multi-function serial ch.2 clock I/O (0)	A/D converter external trigger input 0 (1)	INT7 External interrupt input (1)	CAN reception data 2 input	General-purpose I/O port	External bus data bit22 I/O (0)	Serial chip select 2 I/O (0)	A/D converter external trigger input 1 (1)	INT2 External interrupt input (1)	CAN transmission data 2 output
Function ^{*2}																												
General-purpose I/O port																												
External bus data bit21 I/O (0)																												
Multi-function serial ch.2 clock I/O (0)																												
A/D converter external trigger input 0 (1)																												
INT7 External interrupt input (1)																												
(CAN reception data 2 input MB91F52xB ,MB91F52xD only)																												
General-purpose I/O port																												
External bus data bit22 I/O (0)																												
Serial chip select 2 I/O (0)																												
A/D converter external trigger input 1 (1)																												
INT2 External interrupt input (1)																												
(CAN transmission data 2 output MB91F52xB ,MB91F52xD only)																												
Function ^{*9}																												
General-purpose I/O port																												
External bus data bit21 I/O (0)																												
Multi-function serial ch.2 clock I/O (0)																												
A/D converter external trigger input 0 (1)																												
INT7 External interrupt input (1)																												
CAN reception data 2 input																												
General-purpose I/O port																												
External bus data bit22 I/O (0)																												
Serial chip select 2 I/O (0)																												
A/D converter external trigger input 1 (1)																												
INT2 External interrupt input (1)																												
CAN transmission data 2 output																												

Page	Section	Change Results
36	■PIN Description	<p>The following sentences modified under the Table of Pin description.</p> <p>(Error) *1: For the I/O circuit types, see "■I/O CIRCUIT TYPE". *2: For switching, see "I/O Port" in HARDWARE MANUAL.</p> <p>(Correct) *1: There is a restriction of pin functions. See "Pin Name" of this table. *2: not supported in 64pin *3: not supported in 80pin *4: not supported in 100pin *5: not supported in 120pin *6: not supported in 144pin *7: not supported in 176pin *8: For the I/O circuit types, see "■I/O CIRCUIT TYPE". *9: For switching, see "I/O Port" in HARDWARE MANUAL.</p>
39	■I/O Circuit Type	<p>Remarks for Type I in "I/O Circuit Types" modified as follows:</p> <p>(Error) - 3V pad power supply (5V tolerant), General-purpose I/O port - Output 4mA - CMOS hysteresis input</p> <p>(Correct) - General-purpose I/O port (5V tolerant) - Output 4mA - CMOS hysteresis input</p>
40	■I/O Circuit Type	<p>Remarks for Type J in "I/O Circuit Types" modified as follows:</p> <p>(Error) - 3V pad power supply (5V tolerant), Analog input,General-purpose I/O port - Output 4mA - CMOS hysteresis input</p> <p>(Correct) - Analog input, General-purpose I/O port (5V tolerant) - Output 4mA - CMOS hysteresis input</p>

Page	Section	Change Results																																																																
40	■I/O Circuit Type	<p>Remarks for Type L in "I/O Circuit Types" modified as follows:</p> <p>(Error) - Open-drain I/O - Output 25mA (NOD) - TTL input</p> <p>(Correct) - Open-drain I/O - Output 25mA (Nch open-drain) - TTL input</p>																																																																
40	■I/O Circuit Type	<p>Remarks for Type M in "I/O Circuit Types" modified as follows:</p> <p>(Error) - CMOS hysteresis input - Pull-up resistor 50kΩ (5V cont)</p> <p>(Correct) - CMOS hysteresis input - Pull-up resistor 50kΩ</p>																																																																
121	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 64pins.</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																																																																
124	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 80pin modified as follows:</p> <table border="1"> <tr> <td>(Error)</td> <td>Base timer 1 IRQ0</td> <td>61</td> <td>3D</td> <td>ICR 45</td> <td>308H</td> <td>000F FF08 H</td> <td>45⁵</td> </tr> <tr> <td></td> <td>Base timer 1 IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <table border="1"> <tr> <td>(Correct)</td> <td>Base timer 1 IRQ0</td> <td>61</td> <td>3D</td> <td>ICR 45</td> <td>308H</td> <td>000F FF08 H</td> <td>45</td> </tr> <tr> <td></td> <td>Base timer 1 IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table>	(Error)	Base timer 1 IRQ0	61	3D	ICR 45	308H	000F FF08 H	45 ⁵		Base timer 1 IRQ1								-								-							(Correct)	Base timer 1 IRQ0	61	3D	ICR 45	308H	000F FF08 H	45		Base timer 1 IRQ1								-								-						
(Error)	Base timer 1 IRQ0	61	3D	ICR 45	308H	000F FF08 H	45 ⁵																																																											
	Base timer 1 IRQ1																																																																	
	-																																																																	
	-																																																																	
(Correct)	Base timer 1 IRQ0	61	3D	ICR 45	308H	000F FF08 H	45																																																											
	Base timer 1 IRQ1																																																																	
	-																																																																	
	-																																																																	
125	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 80pins.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																																																																

Page	Section	Change Results																																																																																				
129	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 100pin modified as follows:</p> <p>(Error)</p> <table border="1" data-bbox="605 418 1242 551"> <tr> <td>Base timer 0</td> <td></td> <td></td> <td></td> <td></td> <td>000F</td> <td></td> </tr> <tr> <td>IRQ0</td> <td>60</td> <td>3</td> <td>ICR</td> <td>30C_H</td> <td>FF0C</td> <td>44</td> </tr> <tr> <td>Base timer 0</td> <td></td> <td>C</td> <td>44</td> <td></td> <td>H</td> <td></td> </tr> <tr> <td>IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>(Correct)</p> <table border="1" data-bbox="605 608 1242 720"> <tr> <td>-</td> <td>60</td> <td>3</td> <td>ICR</td> <td>30C_H</td> <td>000F</td> <td></td> </tr> <tr> <td>-</td> <td>C</td> <td>44</td> <td></td> <td>FF0C</td> <td>FF</td> <td>44</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td>H</td> <td></td> <td></td> </tr> </table>	Base timer 0					000F		IRQ0	60	3	ICR	30C _H	FF0C	44	Base timer 0		C	44		H		IRQ1							-	60	3	ICR	30C _H	000F		-	C	44		FF0C	FF	44					H																																					
Base timer 0					000F																																																																																	
IRQ0	60	3	ICR	30C _H	FF0C	44																																																																																
Base timer 0		C	44		H																																																																																	
IRQ1																																																																																						
-	60	3	ICR	30C _H	000F																																																																																	
-	C	44		FF0C	FF	44																																																																																
				H																																																																																		
129	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 100pin modified as follows:</p> <p>(Error)</p> <table border="1" data-bbox="605 840 1242 1037"> <tr> <td>Base timer 1</td> <td></td> <td></td> <td></td> <td></td> <td>000F</td> <td></td> </tr> <tr> <td>IRQ0</td> <td>61</td> <td>3D</td> <td>ICR</td> <td>308_H</td> <td>FF08_H</td> <td>45</td> </tr> <tr> <td>Base timer 1</td> <td></td> <td></td> <td>45</td> <td></td> <td></td> <td>*5</td> </tr> <tr> <td>IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>(Correct)</p> <table border="1" data-bbox="605 1115 1242 1312"> <tr> <td>Base timer 1</td> <td></td> <td></td> <td></td> <td></td> <td>000F</td> <td></td> </tr> <tr> <td>IRQ0</td> <td>61</td> <td>3D</td> <td>ICR</td> <td>308_H</td> <td>FF08</td> <td>45</td> </tr> <tr> <td>Base timer 1</td> <td></td> <td></td> <td>45</td> <td></td> <td>H</td> <td></td> </tr> <tr> <td>IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table>	Base timer 1					000F		IRQ0	61	3D	ICR	308 _H	FF08 _H	45	Base timer 1			45			*5	IRQ1							-							-							Base timer 1					000F		IRQ0	61	3D	ICR	308 _H	FF08	45	Base timer 1			45		H		IRQ1							-							-						
Base timer 1					000F																																																																																	
IRQ0	61	3D	ICR	308 _H	FF08 _H	45																																																																																
Base timer 1			45			*5																																																																																
IRQ1																																																																																						
-																																																																																						
-																																																																																						
Base timer 1					000F																																																																																	
IRQ0	61	3D	ICR	308 _H	FF08	45																																																																																
Base timer 1			45		H																																																																																	
IRQ1																																																																																						
-																																																																																						
-																																																																																						
129	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 100pins.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																																																																																				

Page	Section	Change Results																																																		
131	■Interrupt Vector Table	<p>"42" is deleted as shown below from the interrupt factor in Interrupt vector 120pin.</p> <p>(Error)</p> <table border="1" data-bbox="600 460 1249 650"> <tr> <td>PPG2/3/12/13/22 /23/32/33/42/43</td> <td>41</td> <td>29</td> <td>ICR 25</td> <td>358 H</td> <td>000F FF58 H</td> <td>25 *3</td> </tr> <tr> <td>16-bit free-run timer 2 (0 detection) / (compare clear)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>(Correct)</p> <table border="1" data-bbox="600 714 1249 904"> <tr> <td>PPG2/3/12/13/22 /23/32/33/43</td> <td>41</td> <td>29</td> <td>ICR 25</td> <td>358 H</td> <td>000F FF58 H</td> <td>25 *3</td> </tr> <tr> <td>16-bit free-run timer 2 (0 detection) / (compare clear)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table>	PPG2/3/12/13/22 /23/32/33/42/43	41	29	ICR 25	358 H	000F FF58 H	25 *3	16-bit free-run timer 2 (0 detection) / (compare clear)							PPG2/3/12/13/22 /23/32/33/43	41	29	ICR 25	358 H	000F FF58 H	25 *3	16-bit free-run timer 2 (0 detection) / (compare clear)																												
PPG2/3/12/13/22 /23/32/33/42/43	41	29	ICR 25	358 H	000F FF58 H	25 *3																																														
16-bit free-run timer 2 (0 detection) / (compare clear)																																																				
PPG2/3/12/13/22 /23/32/33/43	41	29	ICR 25	358 H	000F FF58 H	25 *3																																														
16-bit free-run timer 2 (0 detection) / (compare clear)																																																				
133	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 120pin modified as follows:</p> <p>(Error)</p> <table border="1" data-bbox="600 1052 1249 1242"> <tr> <td>Base timer 1 IRQ0</td> <td rowspan="4">61</td> <td rowspan="4">3D</td> <td rowspan="4">ICR 45</td> <td rowspan="4">308 H</td> <td rowspan="4">000F FF08 H</td> <td rowspan="4">45 *5</td> </tr> <tr> <td>Base timer 1 IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>(Correct)</p> <table border="1" data-bbox="600 1305 1249 1496"> <tr> <td>Base timer 1 IRQ0</td> <td rowspan="4">61</td> <td rowspan="4">3D</td> <td rowspan="4">ICR 45</td> <td rowspan="4">308 H</td> <td rowspan="4">000F FF08 H</td> <td rowspan="4">45</td> </tr> <tr> <td>Base timer 1 IRQ1</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table>	Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45 *5	Base timer 1 IRQ1						-						-						Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45	Base timer 1 IRQ1						-						-					
Base timer 1 IRQ0	61	3D	ICR 45							308 H	000F FF08 H	45 *5																																								
Base timer 1 IRQ1																																																				
-																																																				
-																																																				
Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45																																														
Base timer 1 IRQ1																																																				
-																																																				
-																																																				
133	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 120pins.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																																																		

Page	Section	Change Results																																																		
135	■Interrupt Vector Table	<p>"42" is deleted as shown below from the interrupt factor in Interrupt vector 144pin.</p> <p>(Error)</p> <table border="1" data-bbox="600 460 1259 650"> <tr> <td>PPG2/3/12/13/22/ 23/32/33/42/43</td> <td>41</td> <td>29</td> <td>ICR 25</td> <td>358 _H</td> <td>000F FF58 _H</td> <td>25* ₃</td> </tr> <tr> <td>16-bit free-run timer 2 (0 detection) / (compare clear)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>(Correct)</p> <table border="1" data-bbox="600 714 1259 904"> <tr> <td>PPG2/3/12/13/22/ 23/32/33/43</td> <td>41</td> <td>29</td> <td>ICR 25</td> <td>358 _H</td> <td>000F FF58 _H</td> <td>25* ₃</td> </tr> <tr> <td>16-bit free-run timer 2 (0 detection) / (compare clear)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table>							PPG2/3/12/13/22/ 23/32/33/42/43	41	29	ICR 25	358 _H	000F FF58 _H	25* ₃	16-bit free-run timer 2 (0 detection) / (compare clear)							PPG2/3/12/13/22/ 23/32/33/43	41	29	ICR 25	358 _H	000F FF58 _H	25* ₃	16-bit free-run timer 2 (0 detection) / (compare clear)																						
PPG2/3/12/13/22/ 23/32/33/42/43	41	29	ICR 25	358 _H	000F FF58 _H	25* ₃																																														
16-bit free-run timer 2 (0 detection) / (compare clear)																																																				
PPG2/3/12/13/22/ 23/32/33/43	41	29	ICR 25	358 _H	000F FF58 _H	25* ₃																																														
16-bit free-run timer 2 (0 detection) / (compare clear)																																																				
137	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 144pin modified as follows:</p> <p>(Error)</p> <table border="1" data-bbox="600 1039 1259 1229"> <tr> <td>Base timer 1 IRQ0</td> <td rowspan="4">61</td> <td rowspan="4">3D</td> <td rowspan="4">ICR 45</td> <td rowspan="4">308 _H</td> <td rowspan="4">000F FF08 _H</td> <td rowspan="4">45 _{*5}</td> </tr> <tr> <td>Base timer 1 IRQ1</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>(Correct)</p> <table border="1" data-bbox="600 1293 1259 1483"> <tr> <td>Base timer 1 IRQ0</td> <td rowspan="4">61</td> <td rowspan="4">3D</td> <td rowspan="4">ICR 45</td> <td rowspan="4">308 _H</td> <td rowspan="4">000F FF08 _H</td> <td rowspan="4">45</td> </tr> <tr> <td>Base timer 1 IRQ1</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>-</td> <td></td> <td></td> <td></td> <td></td> </tr> </table>							Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45 _{*5}	Base timer 1 IRQ1					-					-					Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45	Base timer 1 IRQ1					-					-				
Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45 _{*5}																																														
Base timer 1 IRQ1																																																				
-																																																				
-																																																				
Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45																																														
Base timer 1 IRQ1																																																				
-																																																				
-																																																				
137	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 144pins.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																																																		

Page	Section	Change Results																																																																																				
141	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 176pin modified as follows:</p> <p>(Error)</p> <table border="1"> <tr><td>Base timer 1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>IRQ0</td><td>61</td><td>3D</td><td>ICR 45</td><td>308 H</td><td>000F FF08 H</td><td>45 *5</td></tr> <tr><td>Base timer 1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>IRQ1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> </table> <p>(Correct)</p> <table border="1"> <tr><td>Base timer 1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>IRQ0</td><td>61</td><td>3D</td><td>ICR 45</td><td>308 H</td><td>000F FF08 H</td><td>45</td></tr> <tr><td>Base timer 1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>IRQ1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> </table>	Base timer 1							IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45 *5	Base timer 1							IRQ1							-							-							Base timer 1							IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45	Base timer 1							IRQ1							-							-						
Base timer 1																																																																																						
IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45 *5																																																																																
Base timer 1																																																																																						
IRQ1																																																																																						
-																																																																																						
-																																																																																						
Base timer 1																																																																																						
IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45																																																																																
Base timer 1																																																																																						
IRQ1																																																																																						
-																																																																																						
-																																																																																						
141	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 176pins.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																																																																																				
142	■Electrical Characteristics 1. Absolute Maximum Ratings	<p>The remarks of "L" level average output current" and "H" level average output current" modified as follows.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th rowspan="2">Parameter</th> <th rowspan="2">Sym bol</th> <th colspan="2">Rating</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Max</th> </tr> </thead> <tbody> <tr><td>"L" level average output current *4</td><td>I_{OLAV1}</td><td>-</td><td>4</td><td>mA</td><td></td></tr> <tr><td></td><td>I_{OLAV2}</td><td>-</td><td>12</td><td>mA</td><td></td></tr> <tr><td>"H" level average output current *4</td><td>I_{OHAV1}</td><td>-</td><td>-4</td><td>mA</td><td></td></tr> <tr><td></td><td>I_{OHAV2}</td><td>-</td><td>-12</td><td>mA</td><td></td></tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th rowspan="2">Parameter</th> <th rowspan="2">Sym bol</th> <th colspan="2">Rating</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Max</th> </tr> </thead> <tbody> <tr><td>"L" level average output current *4</td><td>I_{OLAV1}</td><td>-</td><td>4</td><td>mA</td><td>*9</td></tr> <tr><td></td><td>I_{OLAV2}</td><td>-</td><td>12</td><td>mA</td><td>*10</td></tr> <tr><td>"H" level average output current *4</td><td>I_{OHAV1}</td><td>-</td><td>-4</td><td>mA</td><td>*9</td></tr> <tr><td></td><td>I_{OHAV2}</td><td>-</td><td>-12</td><td>mA</td><td>*10</td></tr> </tbody> </table>	Parameter	Sym bol	Rating		Unit	Remarks	Min	Max	"L" level average output current *4	I _{OLAV1}	-	4	mA			I _{OLAV2}	-	12	mA		"H" level average output current *4	I _{OHAV1}	-	-4	mA			I _{OHAV2}	-	-12	mA		Parameter	Sym bol	Rating		Unit	Remarks	Min	Max	"L" level average output current *4	I _{OLAV1}	-	4	mA	*9		I _{OLAV2}	-	12	mA	*10	"H" level average output current *4	I _{OHAV1}	-	-4	mA	*9		I _{OHAV2}	-	-12	mA	*10																				
Parameter	Sym bol	Rating			Unit	Remarks																																																																																
		Min	Max																																																																																			
"L" level average output current *4	I _{OLAV1}	-	4	mA																																																																																		
	I _{OLAV2}	-	12	mA																																																																																		
"H" level average output current *4	I _{OHAV1}	-	-4	mA																																																																																		
	I _{OHAV2}	-	-12	mA																																																																																		
Parameter	Sym bol	Rating		Unit	Remarks																																																																																	
		Min	Max																																																																																			
"L" level average output current *4	I _{OLAV1}	-	4	mA	*9																																																																																	
	I _{OLAV2}	-	12	mA	*10																																																																																	
"H" level average output current *4	I _{OHAV1}	-	-4	mA	*9																																																																																	
	I _{OHAV2}	-	-12	mA	*10																																																																																	
143	■Electrical Characteristics 1. Absolute Maximum Ratings	<p>The following note added.</p> <p>(Correct)</p> <p>*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.</p> <p>*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.</p>																																																																																				

Page	Section	Change Results
155	■Electrical Characteristics AC Characteristics (2) Reset Input	Added the At power-on ^{*2} condition to the remarks in Reset input time.
156	■Electrical Characteristics AC Characteristics (3) Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and C pin voltage at Power-on. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on.
6 to 11, 203 to 216	■Product lineup ■Ordering information	Package description modified to JEDEC description.
47	■During Power-on	The following sentence modified as deleted from Interrupt (Error) To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.
49, 50	■Block Diagram	The following Block diagram modified as follows: ●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B ●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D (Error) CAN (2ch). (Correct) CAN (3ch)
217 to 220	■Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxD
221 to 227	■Package Dimensions	Package Dimensions modified to JEDEC description.

Page	Section	Change Results				
Rev *C						
2	Features Peripheral Functions	<p>The following sentence modified in I2C as following:</p> <p>(Error) < I2C > 2 channels ch.3 , ch.4 Standard mode/high-speed mode supported.</p> <p>Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported</p> <p>(Correct) < I2C > 2 channels ch.3 , ch.4 Standard mode/fast mode supported.</p> <p>Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported</p>				
5,6,7,8,9 ,10	1. Product Lineup	<p>The following *2 added as follows:</p> <p>(Error) <table border="1"><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table></p> <p>(Correct) <table border="1"><tr><td>Power supply</td><td>2.7 V to 5.5 V *2</td></tr></table></p>	Power supply	2.7 V to 5.5 V	Power supply	2.7 V to 5.5 V *2
Power supply	2.7 V to 5.5 V					
Power supply	2.7 V to 5.5 V *2					
5,6,7,8,9 ,10	1. Product Lineup	<p>The following sentence added as follows:</p> <p>(Correct) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p>				
8, 9, 10,	1. Product Lineup	<p>The following sentence modified in the bottom of Product lineup comparison table as following:</p> <p>(Error) *1: Only channel 3 and channel 4 support the I2C (high-speed mode/standard mode).</p> <p>(Correct) *1: Only channel 3 and channel 4 support the I2C (fast mode/standard mode).</p>				
11	1. Product Lineup	Added silicon version E				

Page	Section	Change Results																
46	■During Power-on	<p>The following sentence modified as following:</p> <p>(Error) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.</p> <p>(Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.</p>																
142,143	11. Electrical Characteristics Recommended operating conditions	<p>The following sentence modified as following:</p> <p>(Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset.</p> <p>(Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is $2.8V \pm 8\%$ ($2.576V$ to $3.024V$). This detection voltage ($2.576V$) is below the minimum operation guarantee voltage ($2.7V$). Between this detection voltage and the minimum operation guarantee voltage, [redacted] MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, [redacted] the LVD reset factor flag is set as the voltage drops below the detection level.</p>																
156, 157	11. Electrical Characteristics AC Characteristics	Added (3-2) Power-on Conditions for MB91F52xxxE																
184	11. Electrical Characteristics AC Characteristics (4-4) I ² C timing	<p>The following sentence modified as following:</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th colspan="2">High-speed mode^{*3}</th> <th>Unit</th> <th>Remarks</th> </tr> <tr> <th>Min</th> <th>Max</th> <td></td> <td></td> </tr> </thead> </table> <p>Notes: Only ch.3 and ch.4 are standard mode/high-speed mode correspondence.</p> <p>*3: A high-speed mode I²C bus device can be used</p> <p>(Correct)</p> <table border="1"> <thead> <tr> <th colspan="2">Fast mode^{*3}</th> <th>Unit</th> <th>Remarks</th> </tr> <tr> <th>Min</th> <th>Max</th> <td></td> <td></td> </tr> </thead> </table> <p>Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence.</p> <p>*3: A fast mode I²C bus device can be used</p>	High-speed mode ^{*3}		Unit	Remarks	Min	Max			Fast mode ^{*3}		Unit	Remarks	Min	Max		
High-speed mode ^{*3}		Unit	Remarks															
Min	Max																	
Fast mode ^{*3}		Unit	Remarks															
Min	Max																	

Page	Section	Change Results																																				
187	11. Electrical Characteristics (8) Low voltage detection (External low-voltage detection)	<p>The following sentence modified in the Detection voltage as following:</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th colspan="3">Value</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Typ</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>2.7</td> <td>-</td> <td>5.5</td> <td>V</td> <td></td> </tr> <tr> <td>-8%</td> <td>2.8</td> <td>+8%</td> <td>V</td> <td>When power-supply voltage falls and detection level is set initially</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th colspan="3">Value</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Typ</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>2.7</td> <td>-</td> <td>5.5</td> <td>V</td> <td></td> </tr> <tr> <td>-8%</td> <td>LVD5F SEL [3:0]</td> <td>+8%</td> <td>V</td> <td>LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.</td> </tr> </tbody> </table>	Value			Unit	Remarks	Min	Typ	Max	2.7	-	5.5	V		-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially	Value			Unit	Remarks	Min	Typ	Max	2.7	-	5.5	V		-8%	LVD5F SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Value			Unit	Remarks																																		
Min	Typ	Max																																				
2.7	-	5.5	V																																			
-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially																																		
Value			Unit	Remarks																																		
Min	Typ	Max																																				
2.7	-	5.5	V																																			
-8%	LVD5F SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.																																		
188	11. Electrical Characteristics (9) Low voltage detection (RAM retention low-voltage detection)	<p>The following sentence modified as following:</p> <p>(Error)</p> <p>(9) Low voltage detection (Internal low-voltage detection)</p> <p>(Correct)</p> <p>(9) Low voltage detection (RAM retention low-voltage detection)</p>																																				
220 to 223	16. Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxE																																				
Rev *D																																						
1	Features	<p>The following sentence should be modified as follows:</p> <p>(Error) Conversion time : 1μs</p> <p>(Correct) Conversion time : 1.4μs</p>																																				

Page	Section	Change Results
5,6,7,8,9, ,10	1. Product Lineup	<p>The following sentence should be modified as follows:</p> <p>(Error) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p> <p>(Correct) *2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>
142,143	11. Electrical Characteristics Recommended operating conditions	<p>The following sentence should be modified as follows:</p> <p>(Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p> <p>(Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>
146	11. Electrical Characteristics DC Characteristics	<p>Pin name of R_{UP3} should be modified as follows:</p> <p>(Error) Port pin other than P035,041,093,122</p> <p>(Correct) Port pin other than P035,041,073,074,076,077,093,122</p>

Page	Section	Change Results																
187	11. Electrical Characteristics (8) Low voltage detection (External low-voltage detection)	<p>Note of Detection voltage should be added as follows:</p> <p>(Correct) Detection voltage ^{*3}</p> <p>^{*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V). Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.}</p>																
188	11. Electrical Characteristics (9) Low voltage detection (Internal low-voltage detection)	<p>The following sentence modified as following:</p> <p>(Error) (9) Low voltage detection (RAM retention low-voltage detection)</p> <p>(Correct) (9) Low voltage detection (Internal low-voltage detection)</p>																
		<p>The following symbol should be modified as follows:</p> <p>(Error) *</p> <p>(Correct) ^{*1}</p>																
		<p>Note of Detection voltage should be added as follows:</p> <p>(Correct) Detection voltage ^{*2}</p> <p>^{*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V. This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.}</p>																
233 to 235	18. Errata	Limitation for Watch mode (power off) should be added in Errata.																
Rev *F																		
222	16. Ordering Information MB91F526xxxE	<p>The shading part added as below.</p> <table border="1"> <thead> <tr> <th>Part number</th> <th>Sub clock</th> <th>CSV Initial value</th> <th>LVD Initial value</th> <th>Package*</th> </tr> </thead> <tbody> <tr> <td>MB91F526LSEPMC</td> <td rowspan="3">None</td> <td>ON</td> <td>ON</td> <td rowspan="3">LQP • 176 pin, Plastic</td> </tr> <tr> <td>MB91F526LHEPMC</td> <td>OFF</td> <td>ON</td> </tr> <tr> <td>MB91F526LKEPMC</td> <td>OFF</td> <td>OFF</td> </tr> </tbody> </table>	Part number	Sub clock	CSV Initial value	LVD Initial value	Package*	MB91F526LSEPMC	None	ON	ON	LQP • 176 pin, Plastic	MB91F526LHEPMC	OFF	ON	MB91F526LKEPMC	OFF	OFF
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*														
MB91F526LSEPMC	None	ON	ON	LQP • 176 pin, Plastic														
MB91F526LHEPMC		OFF	ON															
MB91F526LKEPMC		OFF	OFF															

Page	Section	Change Results						
Rev *G								
-		Marketing Part Numbers changed from an MB prefix to a CY prefix.						
Rev *H								
13	2. Pin Assignment	The shading part added for LQH080 as below. <table border="1"> <tr> <td>36</td> <td>P153/SCK5_0/SCL5/AN32/FRCK1_1/INT4_1</td> </tr> <tr> <td>35</td> <td>P073/SOT4_0/AN33/ICU3_2</td> </tr> <tr> <td>34</td> <td>P072/SIN4_0/AN34/ICU2_2/INT5_0</td> </tr> </table>	36	P153/SCK5_0/SCL5/AN32/FRCK1_1/INT4_1	35	P073/SOT4_0/AN33/ICU3_2	34	P072/SIN4_0/AN34/ICU2_2/INT5_0
36	P153/SCK5_0/SCL5/AN32/FRCK1_1/INT4_1							
35	P073/SOT4_0/AN33/ICU3_2							
34	P072/SIN4_0/AN34/ICU2_2/INT5_0							
14	2. Pin Assignment	The shading part added for LQI100 as below. <table border="1"> <tr> <td>44</td> <td>P152/SCS53_0</td> </tr> <tr> <td>43</td> <td>P073/SOT4_0/AN33/ICU3_2</td> </tr> <tr> <td>42</td> <td>P072/SIN4_0/AN34/ICU2_2/INT5_0</td> </tr> </table>	44	P152/SCS53_0	43	P073/SOT4_0/AN33/ICU3_2	42	P072/SIN4_0/AN34/ICU2_2/INT5_0
44	P152/SCS53_0							
43	P073/SOT4_0/AN33/ICU3_2							
42	P072/SIN4_0/AN34/ICU2_2/INT5_0							
217	16. Ordering Information CY91F52xxxE	The shading part modified as below. Error) LQE • 64 pin, Plastic Correct) LQD • 64 pin, Plastic						

Document History

Document Title: CY91520 Series 32-bit FR81S Microcontroller

Document Number: 002-04662

Revision	ECN	Orig. of Change	Submission Date	Description of Change
	–	–	–	Initial release
**	–	–	2/20/2014	<p>Features: Corrected the following description. 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input ↓ 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input</p> <p>I/O CIRCUIT TYPE: Corrected the following description to "Type F, G, I, J, K, M". Schmitt input → CMOS hysteresis input Corrected the following description to "Type D, E". I²C Schmitt input → I²C hysteresis input</p> <p>Block Diagram Corrected the following description.</p> <ul style="list-style-type: none"> • MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B • MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D • MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F • MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J • MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K • MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L <p>Electrical Characteristics 2. Recommended operating conditions: *1 : When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset</p> <p>Electrical Characteristics 3.DC characteristics Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C ". Max 1420µA → Max 2000µA Corrected the value of "Power supply voltage range". (TA:-40°C to +105°C, Vcc=AVcc=2.7V to 5.5V, VSS=AVSS=0.0V) ↓ (TA:-40°C to +105°C, Vcc=AVcc=5.0V±10%/3.3V±0.3V, Vss=AVss=0.0V) Corrected the value of "Power supply voltage range". (TA:-40°C to +125°C, Vcc=AVcc=2.7V to 5.5V, VSS=AVSS=0.0V) ↓ (TA:-40°C to +125°C, Vcc=AVcc=5.0V±10%/3.3V±0.3V, Vss=AVss=0.0V) Corrected the value of " Pull-up resistance R_{UP1}". Vcc=3.3V±0.3V Min 49 Max 140 →Min 45 Max 140 Corrected the following description. Pull-up resistance R_{UP2} Port pin other than P035,041,093,122 → P073,074,076,077 Corrected the value of " Pull-up resistance R_{UP2}".</p>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				<p>VCC=5.0V±10% Min 25 Max 100 →Min 25 Max 60 VCC=3.3V±0.3V Min 49 Max 140 →Min 33 Max 90</p> <p>Added the value of " Pull-up resistance R_{UP3}". Pin name : Port pin other than P035,041,073,074,076,077,093,122 VCC=5.0V±10% Min 25 Max 100 VCC=3.3V±0.3V Min 45 Max 140</p> <p>Electrical Characteristics 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4) (4-1-1),(4-1-4)SCK\downarrow⇒SOT delay time t_{SLOVI} (4-1-2),(4-1-3)SCK\uparrow⇒SOT delay time t_{SHOVI} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300 (4-1-1),(4-1-4)Valid SIN⇒SCK\uparrow setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN⇒SCK\downarrow setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max - (4-1-1),(4-1-4)SCK\downarrow⇒SOT delay time t_{SLOVE} (4-1-2),(4-1-3)SCK\uparrow⇒SOT delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300 (4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_F Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11</p>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				<p>Value: Min - Max 5 (4-1-5)SCS\downarrow⇒SCK\downarrow setup time t_{CS51} (4-1-6)SCS\downarrow⇒SCK\uparrow setup time t_{CS51} (4-1-7)SCS\uparrow⇒SCK\downarrow setup time t_{CS51} (4-1-8)SCS\uparrow⇒SCK\uparrow setup time t_{CS51} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CS51+0} Max $t_{CS51+50}$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CS51-50}$ Max t_{CS51+0} Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $t_{CS51-50}$ Max $t_{CS51+300}$ (4-1-5)SCK\uparrow⇒SCS\uparrowhold time t_{CSH1} (4-1-6)SCK\downarrow⇒SCS\uparrowhold time t_{CSH1} (4-1-7)SCK\uparrow⇒SCS\downarrowhold time t_{CSH1} (4-1-8)SCK\downarrow⇒SCS\downarrowhold time t_{CSH1} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSH1-50}$ Max t_{CSH1+0} ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSH1-10}$ Max $t_{CSH1+50}$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $t_{CSH1-300}$ Max $t_{CSH1+50}$ (4-1-5),(4-1-6)SCS\downarrow⇒SOT delay time t_{DSE} (4-1-7),(4-1-8)SCS\uparrow⇒SOT delay time t_{DSE} Corrected the following description. Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1 to SOT11 Value: Min - Max 40 ↓ Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73, SCS8 to SCS11 SOT1,SOT2,SOT5 to SOT11 Value: Min - Max 40 Pin name: SCS3,SCS40 to SCS43 SOT3,SOT4 Value: Min - Max 300 (4-1-5)SCK\downarrow⇒SCS\downarrow clock switch time t_{SCC} (4-1-6)SCK\uparrow⇒SCS\downarrow clock switch time t_{SCC} (4-1-7)SCK\downarrow⇒SCS\uparrow clock switch time t_{SCC} (4-1-8)SCK\uparrow⇒SCS\uparrow clock switch time t_{SCC} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 </p>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				<p>Value: Min $3t_{CPP}+0$ Max $3t_{CPP}+50$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}-10$ Max $3t_{CPP}+50$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $3t_{CPP}-300$ Max $3t_{CPP}+50$ Added the following description. Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again</p> <p>Electrical Characteristics 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics: Added the value of "Total error". Total error value Min – Typ – Max ± 12 LSB Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB Added the following description. Parameter : Power supply current $I_A AVCC^*3$ *3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.</p> <p>Electrical Characteristics 7.D/A Converter: Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter.</p> <p>Electrical Characteristics 6.Flash memory: Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing $T_j < +105^\circ C$"</p> <p>Electrical Characteristics 7.D/A Converter: Corrected the following description. Parameter : Power supply current Symbol IA Pin name AV_{cc} Symbol IAH Pin name AV_{cc} ↓ Symbol IA Pin name AVCC</p>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				<p>Symbol IAH Pin name AVCC</p> <p>Example Characteristics</p> <p>Corrected the following description. Watch mode</p> <p>Ordering Information</p> <p>Corrected the following description.</p> <ul style="list-style-type: none"> • ORDERING INFORMATION <li style="text-align: center;">↓ • ORDERING INFORMATION MB91F52xxxB^{*1} <p>Package</p> <p style="text-align: center;">↓</p> <p>Package^{*2}</p> <p>Added the following description.</p> <p>^{*1:} It is only supported for customers who have already adopted it now. We do not recommend adopting new products.</p> <p>Corrected the following description.</p> <p>For details of the package, see "■ PACKAGE DIMENSIONS".</p> <p style="text-align: center;">↓</p> <p>^{*2:} For details of the package, see "■ PACKAGE DIMENSIONS".</p> <p>Added the following description.</p> <ul style="list-style-type: none"> • ORDERING INFORMATION MB91F52xxxC <p>Company name and layout design change</p>
*A	4999456	JHMU	11/13/2015	<p>Updated to Cypress template.</p> <p>Added the following note to the remarks of "'L' level average output current" and "'H' level average output current" in "Absolute Maximum Ratings" of "ELECTRICAL CHARACTERISTICS".</p> <p style="padding-left: 2em;">*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.</p> <p style="padding-left: 2em;">*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.</p> <p>Added Errata section.</p>
*B	5112138	KUME	01/28/2016	<p>Fixed some clerical errors.</p> <p>For details, please see the chapter 18. Major Changes.</p>
*C	5196285	KUME	04/28/2016	<p>For details, please see the chapter 19. Major Changes.</p>
*D	5318862	KUME	06/23/2016	<p>For details, please see the chapter 19. Major Changes.</p>
*E	5711679	AESATMP7	04/25/2017	<p>Updated Cypress Logo and Copyright.</p>
*F	5984090	KUME	12/05/2017	<p>For details, please see the chapter 19. Major Changes.</p>
*G	5990912	KUME	12/12/2017	<p>Marketing Part Numbers changed from an MB prefix to a CY prefix.</p>
*H	6216567	KUME	06/25/2018	<p>Fixed LQD064 package for Ordering Information CY91F52xxxE.</p> <p>For details, please see the chapter 19. Major Changes.</p>

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

© Cypress Semiconductor Corporation, 2014-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помошь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помошь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.