



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV8746V — Bi-CMOS LSI PWM Constant-Current Control Stepping Motor Driver

Overview

The LV8746V is a stepping motor driver corresponding to the W1-2 aspect excitation drive that the selection of CLK-IN input and a parallel input is possible. It is ideally suited for driving brushed DC motors and stepping motors used in office equipment and amusement applications.

Features

- PWM current control stepping motor driver incorporated.
- BiCDMOS process IC
- Low on resistance (upper side : 0.84Ω ; lower side : 0.7Ω ; total of upper and lower : 1.54Ω ; Ta = 25°C, IO = 1A)
- Excitation mode can be set to 2-phase, 1-2 phase Full torque, 1-2 phase, or W1-2 phase
- CLK-IN input and a parallel input can be selected.
- Motor current selectable in four steps
- Output short-circuit protection circuit (selectable from latch-type or auto-reset-type) incorporated
- Unusual condition warning output pins
- No control power supply required

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------|---------|---------------------|------------|------|
| Supply voltage | VM max | | 38 | V |
| Output peak current | IO peak | tw ≤ 10ms, duty 20% | 1.2 | A |
| Output current | IO max | | 1 | A |
| Logic input voltage | VIN | | -0.3 to +6 | V |
| EMO input voltage | Vemo | | -0.3 to +6 | V |

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| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------|-------------|-------------|------|
| Allowable power dissipation | Pd max | Ta ≤ 85°C * | 3.1 | W |
| Operating temperature | Topr | | -20 to +85 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* Specified circuit board : 90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting.

Allowable Operating Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------|-----------------|------------|----------|------|
| Supply voltage range | VM | | 9 to 35 | V |
| Logic input voltage | V _{IN} | | 0 to 5.5 | V |
| VREF input voltage range | VREF | | 0 to 3 | V |

Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

| Parameter | Symbol | Conditions | Ratings | | | Unit | |
|---|--------------------------------|---|--|-------|-------|-------|---|
| | | | min | typ | max | | |
| Standby mode current drain | IMst | ST = "L" | | 190 | 300 | μA | |
| Current drain | IM | ST = "H", OE = "L", with no load | | 3.3 | 5 | mA | |
| VREG5 output voltage | Vreg5 | I _O = -1mA | 4.5 | 5 | 5.5 | V | |
| Thermal shutdown temperature | TSD | Design guarantee | 150 | 180 | 210 | °C | |
| Thermal hysteresis width | ΔTSD | Design guarantee | | 40 | | °C | |
| Motor driver | | | | | | | |
| Output on resistance | Ron _u | I _O = 1A, Upper-side on resistance | | 0.84 | 1.1 | Ω | |
| | Ron _d | I _O = 1A, Lower-side on resistance | | 0.7 | 0.9 | Ω | |
| Output leakage current | I _O leak | | | | 50 | μA | |
| Diode forward voltage | VD | ID = -1A | | 1.0 | 1.3 | V | |
| Logic pin input current(ST) | I _{INL} | V _{IN} = 0.8V | 3 | 8 | 15 | μA | |
| | I _{INH} | V _{IN} = 5V | 50 | 78 | 110 | μA | |
| Logic pin input current(other ST) | I _{INL} | V _{IN} = 0.8V | 3 | 8 | 15 | μA | |
| | I _{INH} | V _{IN} = 5V | 30 | 50 | 70 | μA | |
| Logic high-level input voltage | V _{INH} | | 2.0 | | | V | |
| Logic low-level input voltage | V _{INL} | | | | 0.8 | V | |
| Current setting comparator threshold voltage (CLK-IN input) | W1-2-phase drive | Vtdac0_W | Step 0 (When initialized : channel 1 comparator level) | 0.29 | 0.3 | 0.31 | V |
| | | Vtdac1_W | Step 1 (Initial state+1) | 0.29 | 0.3 | 0.31 | V |
| | | Vtdac2_W | Step 2 (Initial state+2) | 0.185 | 0.2 | 0.215 | V |
| | | Vtdac3_W | Step 3 (Initial state+3) | 0.09 | 0.1 | 0.11 | V |
| | 1-2 phase drive | Vtdac0_M | Step 0 (When initialized : channel 1 comparator level) | 0.29 | 0.3 | 0.31 | V |
| | | Vtdac2_M | Step 2 (Initial state+1) | 0.185 | 0.2 | 0.215 | V |
| | 1-2 phase drive (Full torque) | Vtdac0_H | Step 0 (When initialized : channel 1 comparator level) | 0.29 | 0.3 | 0.31 | V |
| | | Vtdac2_H | Step 2 (Initial state+1) | 0.29 | 0.3 | 0.31 | V |
| | 2 phase drive | Vtdac2_F | Step 2 | 0.29 | 0.3 | 0.31 | V |
| | | | | | | | |
| Current setting comparator threshold voltage (parallel input) | Vtdac11 | I01 = H , I11 = H | 0.29 | 0.3 | 0.31 | V | |
| | Vtdac01 | I01 = L , I11 = H | 0.185 | 0.2 | 0.215 | V | |
| | Vtdac10 | I01 = H , I11 = L | 0.09 | 0.1 | 0.11 | V | |
| Current setting comparator threshold voltage (current attenuation rate switching) | Vtatt00 | ATT1 = L, ATT2 = L | 0.29 | 0.3 | 0.31 | V | |
| | Vtatt01 | ATT1 = H, ATT2 = L | 0.185 | 0.2 | 0.215 | V | |
| | Vtatt10 | ATT1 = L, ATT2 = H | 0.135 | 0.15 | 0.165 | V | |
| | Vtatt11 | ATT1 = H, ATT2 = H | 0.09 | 0.1 | 0.11 | V | |
| Chopping frequency | Fchop | Rchop = 20KΩ | 45 | 62.5 | 75 | kHz | |
| VREF pin input current | Iref | VREF = 1.5V | -0.5 | | | μA | |

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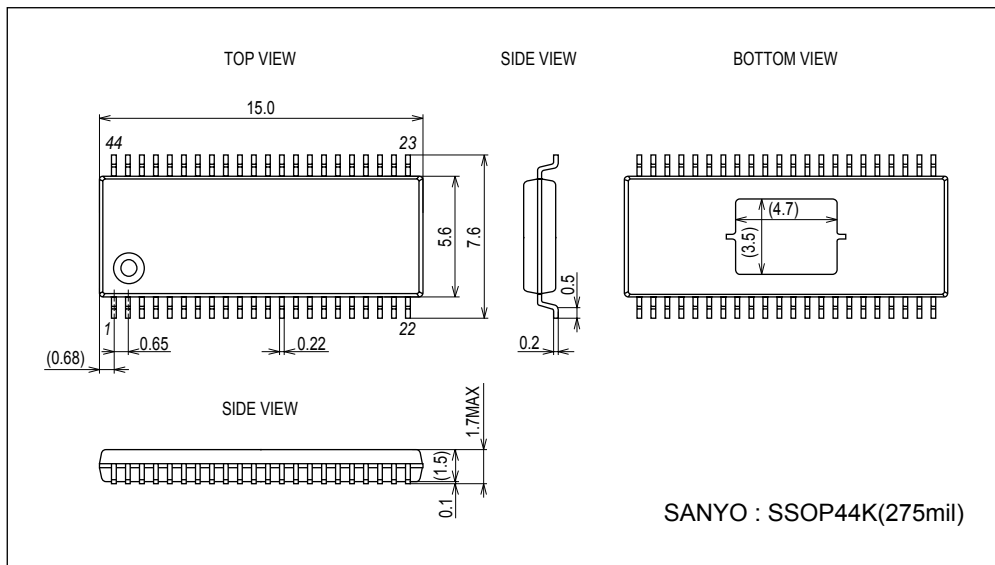
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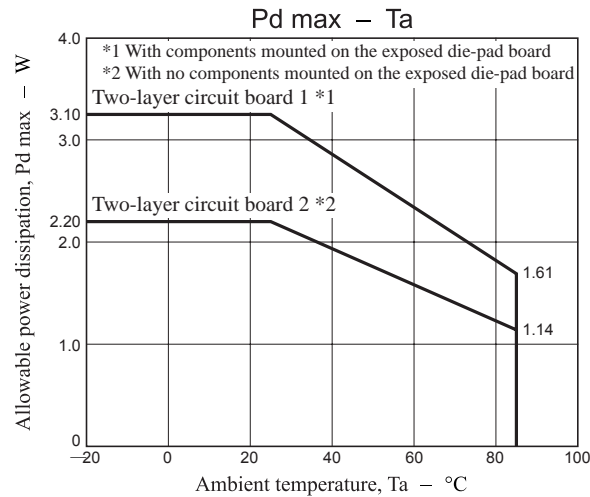
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|---------|----------------------|---------|-------|-----|---------|
| | | | min | typ | max | |
| Charge pump | | | | | | |
| VG output voltage | VG | | 28 | 28.75 | 30 | V |
| Rise time | tONG | VG = 0.1 μ F | | | 0.5 | mS |
| Oscillator frequency | Fosc | Rchop = 20K Ω | 90 | 125 | 150 | kHz |
| Output short-circuit protection | | | | | | |
| EMO pin saturation voltage | Vsatemo | lemo = 1mA | | 80 | 160 | mV |
| CEM pin charge current | Icem | Vcem = 0V | 7 | 10 | 13 | μ A |
| CEM pin threshold voltage | Vthcem | | 0.8 | 1.0 | 1.2 | V |

Package Dimensions

unit : mm (typ)

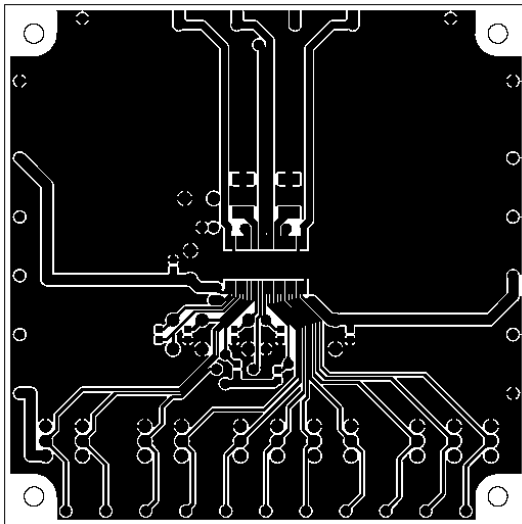
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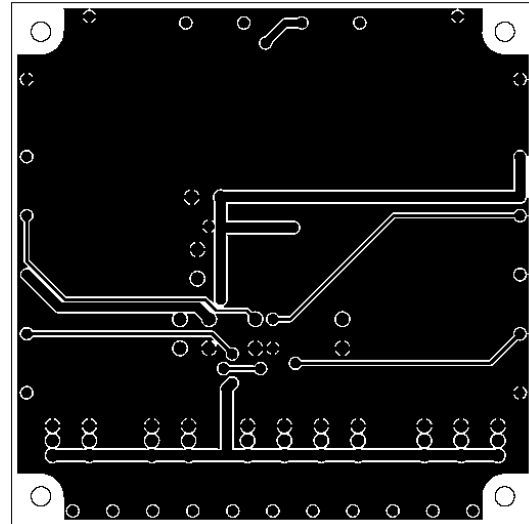


Substrate Specifications (Substrate recommended for operation of LV8746V)

Size : 90mm × 90mm × 1.6mm (two-layer substrate [2SOP])
 Material : Glass epoxy
 Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



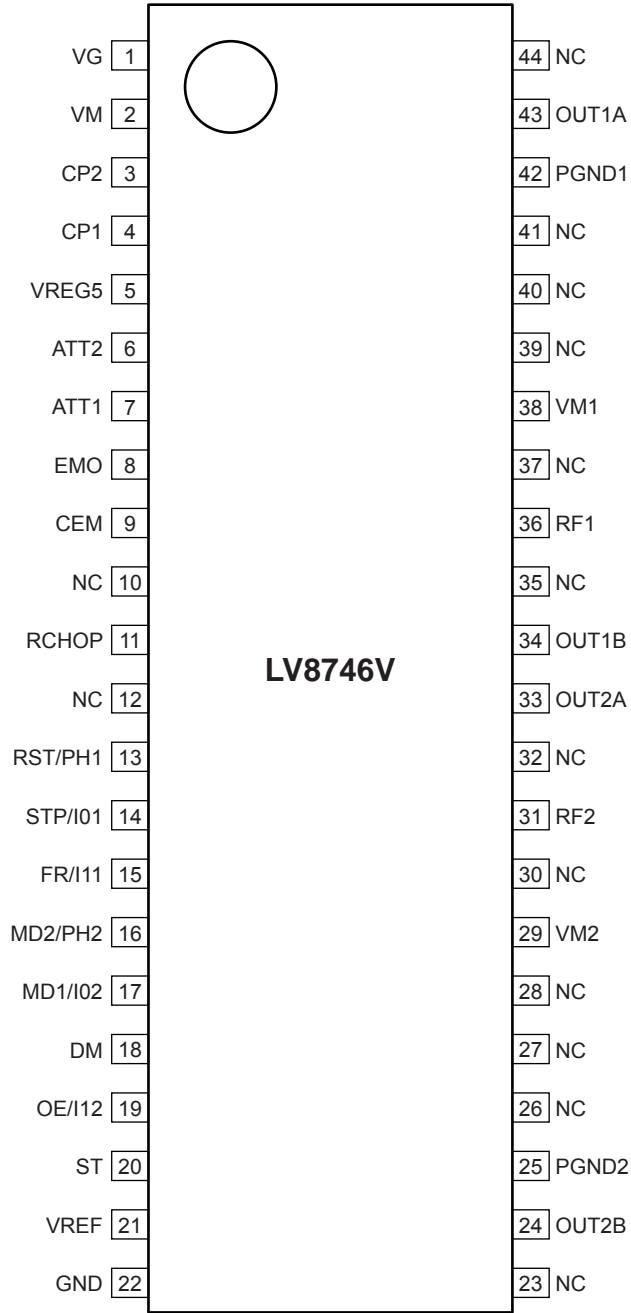
L2 : Copper wiring pattern diagram

Cautions

- 1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.
- 2) For the set design, employ the derating design with sufficient margin.
 Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
 Accordingly, the design must ensure these stresses to be as low or small as possible.
 The guideline for ordinary derating is shown below :
 - (1)Maximum value 80% or less for the voltage rating
 - (2)Maximum value 80% or less for the current rating
 - (3)Maximum value 80% or less for the temperature rating
- 3) After the set design, be sure to verify the design with the actual product.
 Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
 Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

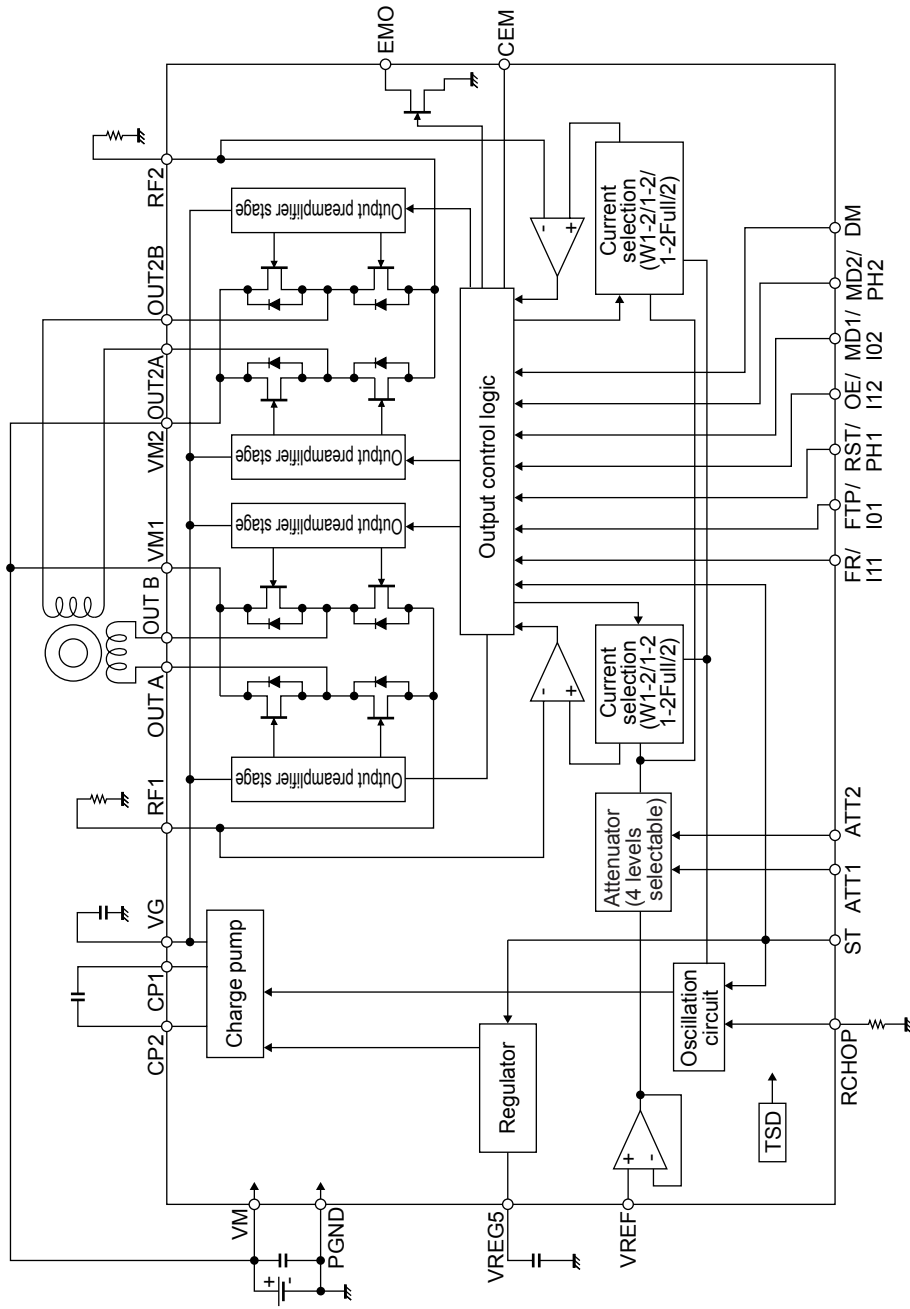
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Pin Assignment



Top view

Block Diagram



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Pin Functions

| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|--|--|---|--------------------|
| 6 7 13 14 15 16 17 18 19 | ATT2 ATT1 RST/PH1 STP/I01 FR/I11 MD2/PH2 MD1/I02 DM OE/I12 | Motor holding current switching pin. Motor holding current switching pin. CLK-IN is input , RESET input pin / Parallel is input , Channel 1 forward/reverse rotation pin. CLK-IN is input , STEP signal input pin / Parallel is input , Channel 1 output control input pin. CLK-IN is input , forward/reverse signal input pin / Parallel is input , Channel 1 output control input pin. CLK-IN is input , Excitation mode switching pin / Parallel is input , Channel 2 forward/reverse rotation pin. CLK-IN is input , Excitation mode switching pin / Parallel is input , Channel 2 output control input pin. Drive mode switching pin. CLK-IN is input , output enable signal input pin / Parallel is input , Channel 2 output control input pin. | |
| 20 | ST | Chip enable pin. | |
| 24 25 42 29 31 33 34 36 38 43 | OUT2B PGND2 PGND1 VM2 RF2 OUT2A OUT1B RF1 VM1 OUT1A | Channel 2 OUTB output pin. Power system ground pin2. Power system ground pin1. Channel 2 motor power supply connection pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 motor power supply pin. Channel 1 OUTA output pin. | |

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| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|------------------|------------------------|---|--------------------|
| 1 2 3 4 | VG VM CP2 CP1 | Charge pump capacitor connection pin. Motor power supply connection pin. Charge pump capacitor connection pin. Charge pump capacitor connection pin. | |
| 21 | VREF | Constant current control reference voltage input pin. | |
| 5 | VREG5 | Internal power supply capacitor connection pin. | |
| 8 | EMO | Output short-circuit state warning output pin. | |

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| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|---|----------|---|--------------------|
| 9 | CEM | Pin to connect the output short-circuit state detection time setting capacitor. | |
| 11 | RCHOP | Chopping frequency setting resistor connection pin. | |
| 22 | GND | Ground. | |
| 10,12 23,26 27,28 30,32 35,37 39,40 41,44 | NC | No Connection (No internal connection to the IC) | |

Description of operation

Input Pin Function

(1) Chip enable function

This IC is switched between standby and operating mode by setting the ST pin. In standby mode, the IC is set to power-save mode and all logic is reset. In addition, the internal regulator circuit and charge pump circuit do not operate in standby mode.

| ST | Mode | Internal regulator | Charge pump |
|-------------|----------------|--------------------|-------------|
| Low or Open | Standby mode | Standby | Standby |
| High | Operating mode | Operating | Operating |



(2) Input control method switching pin function

The IC input control method is switched by setting the DM pin. The CLK-IN input control and the parallel input control can be selected by setting the DM pin.

| DM | Input control method |
|-------------|------------------------|
| Low or Open | CLK-IN input control |
| High | Parallel input control |

CLK-IN input control (DM = Low or Open)

(1) STEP pin function

| Input | | Operating mode |
|-------|---|--------------------------|
| ST | STP | |
| Low | * | Standby mode |
| High |  | Excitation step proceeds |
| High |  | Excitation step is kept |

(2) Excitation mode setting function

| MD1 | MD2 | Excitation mode | Initial position | |
|------|------|------------------------------------|------------------|-----------|
| | | | Channel 1 | Channel 2 |
| Low | Low | 2 phase excitation | 100% | -100% |
| High | Low | 1-2 phase excitation (Full torque) | 100% | 0% |
| Low | High | 1-2 phase excitation | 100% | 0% |
| High | High | W1-2 phase excitation | 100% | 0% |

This is the initial position of each excitation mode in the initial state after power-on and when the counter is reset.

(3) Setting constant-current control reference voltage

| ATT1 | ATT2 | Current setting reference voltage |
|------|------|-----------------------------------|
| Low | Low | $V_{REF} / 5 \times 100\%$ |
| High | Low | $V_{REF} / 5 \times 67\%$ |
| Low | High | $V_{REF} / 5 \times 50\%$ |
| High | High | $V_{REF} / 5 \times 33\%$ |

The voltage input to the VREF pin can be switched to four-step settings depending on the statuses of the two inputs, ATT1 and ATT2. This is effective for reducing power consumption when motor holding current is supplied.

Set current value calculation method.

The reference voltage is set by the voltage applied to the VREF pin and the two inputs ATT1 and ATT2. The output current (output current at a constant-current drive current ratio of 100%) can be set from this reference voltage and the RF resistance value.

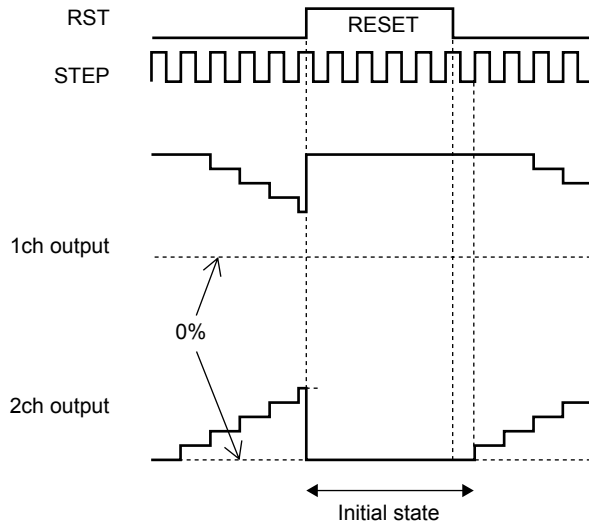
$$I_{OUT} = (V_{REF}/5) \times (\text{current attenuation ratio}) / R_F \text{ resistance}$$

Example : At VREF of 1.5V, a reference voltage setting of 100% [(ATT1, ATT2) = (L, L)] and an RF resistance of 0.5Ω, the output current is set as shown below.

$$I_{OUT} = 1.5V/5 \times 100\%/0.5\Omega = 0.6A$$

(4) Reset function

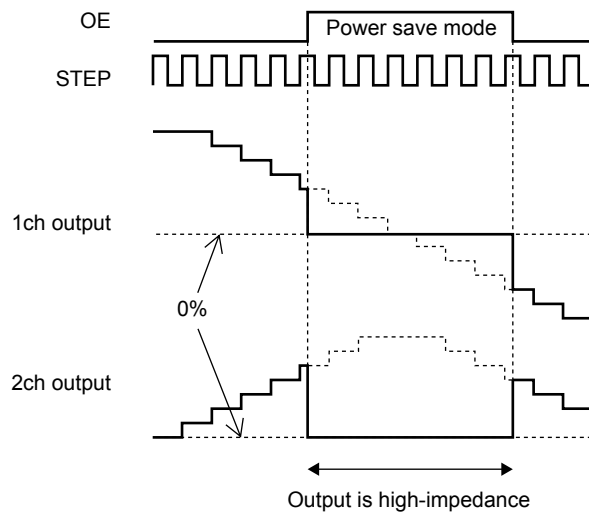
| RST | Operating mode |
|------|------------------|
| Low | Normal operation |
| High | Reset state |



When the RST pin is set to High, the excitation position of the output is forcibly set to the initial state. When RST is then set to Low, the excitation position is advanced by the next STEP input.

(5) Output enable function

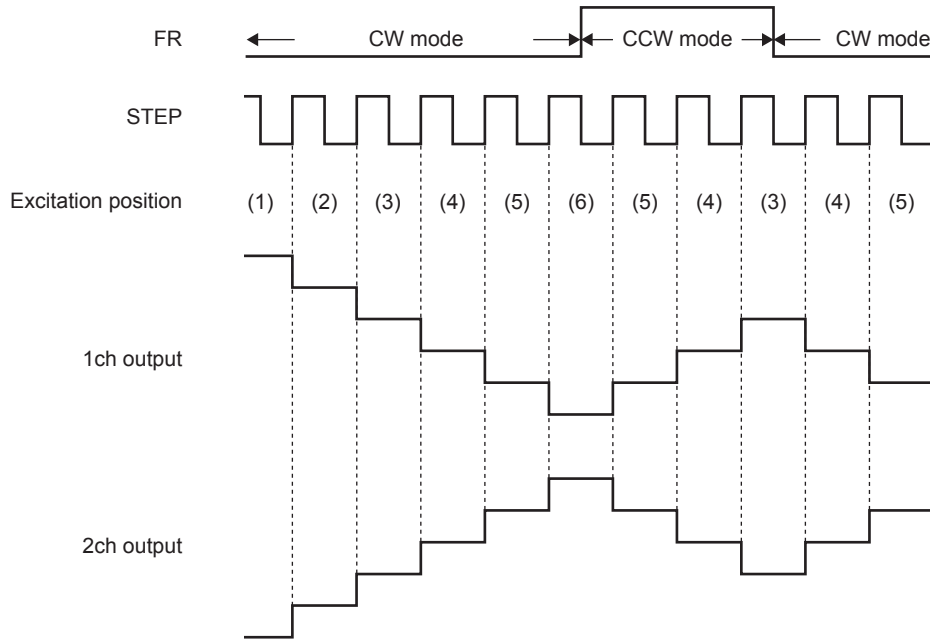
| OE | Operating mode |
|------|----------------|
| Low | Output ON |
| High | Output OFF |



When the OE pin is set High, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STEP signal is input. Therefore, when OE is returned to Low, the output level conforms to the excitation position proceeded by the STEP input.

(6) Forward/reverse switching function

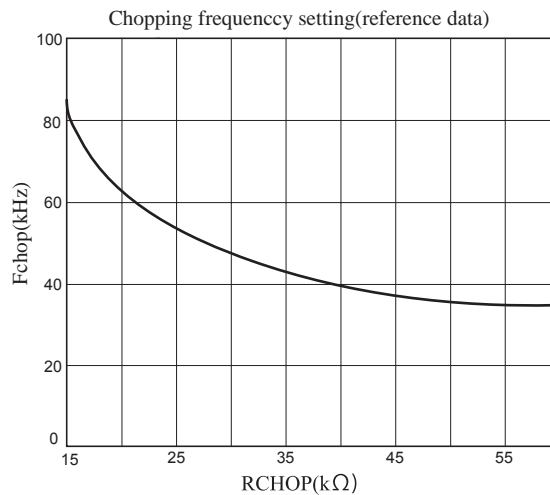
| FR | Operating mode |
|------|----------------|
| Low | CW |
| High | CCW |



The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse.
 In addition, CW and CCW mode are switched by setting the FR pin.
 In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.
 In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

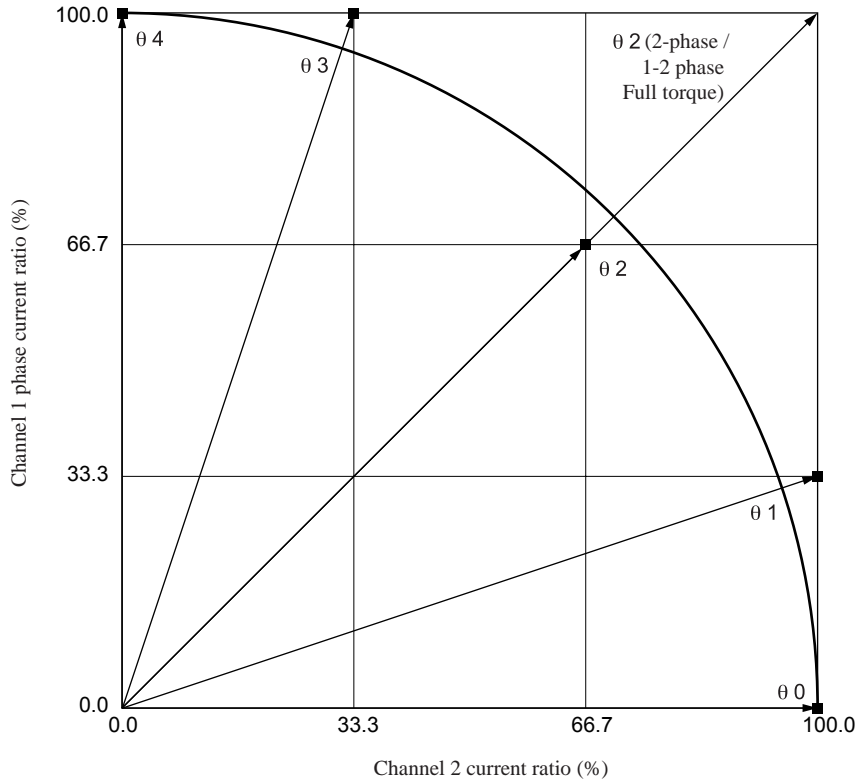
(7) Chopping frequency setting

For constant-current control, chopping operation is made with the frequency determined by the external resistor.
 The chopping frequency to be set with the resistance connected to the RCHOP pin (pin 11) is as shown below.



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(8) Output current vector locus (one step is normalized to 90 degrees)



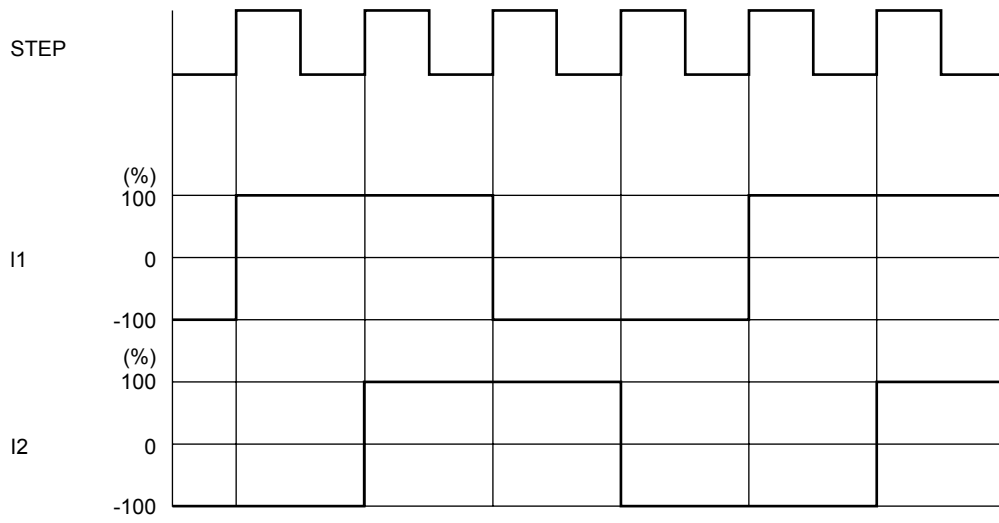
Setting current ration in each excitation mode

| STEP | W1-2 phase (%) | | 1-2 phase (%) | | 1-2 phase full torque (%) | | 2-phase (%) | |
|------|----------------|-----------|---------------|-----------|---------------------------|-----------|-------------|-----------|
| | Channel 1 | Channel 2 | Channel 1 | Channel 2 | Channel 1 | Channel 2 | Channel 1 | Channel 2 |
| 00 | 0 | 100 | 0 | 100 | 0 | 100 | | |
| 01 | 33.3 | 100 | | | | | | |
| 02 | 66.7 | 66.7 | 66.7 | 66.7 | 100 | 100 | 100 | 100 |
| 03 | 100 | 33.3 | | | | | | |
| 04 | 100 | 0 | 100 | 0 | 100 | 0 | | |

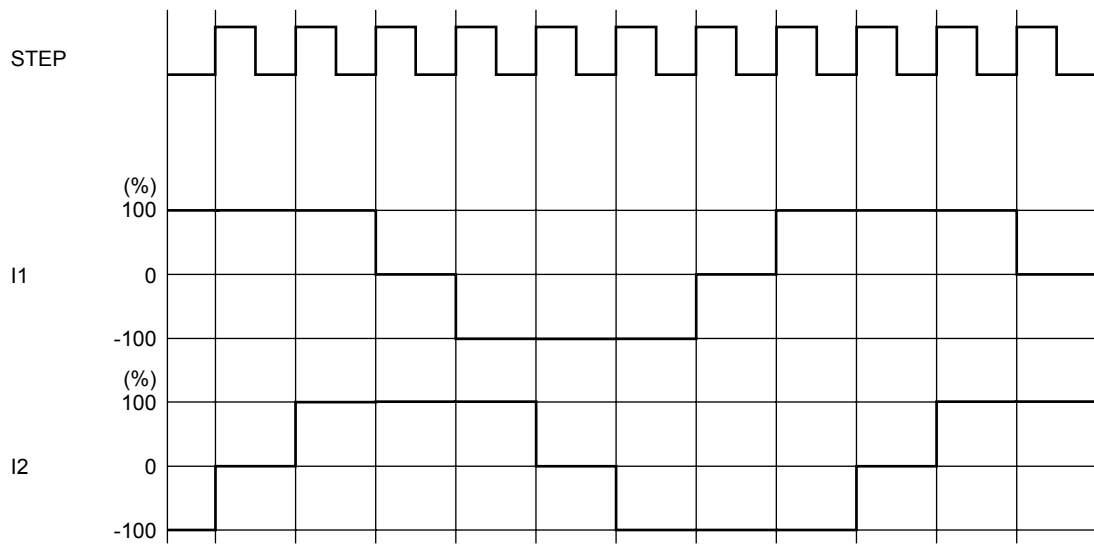
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(9) Typical current waveform in each excitation mode

2-phase excitation (CW mode)

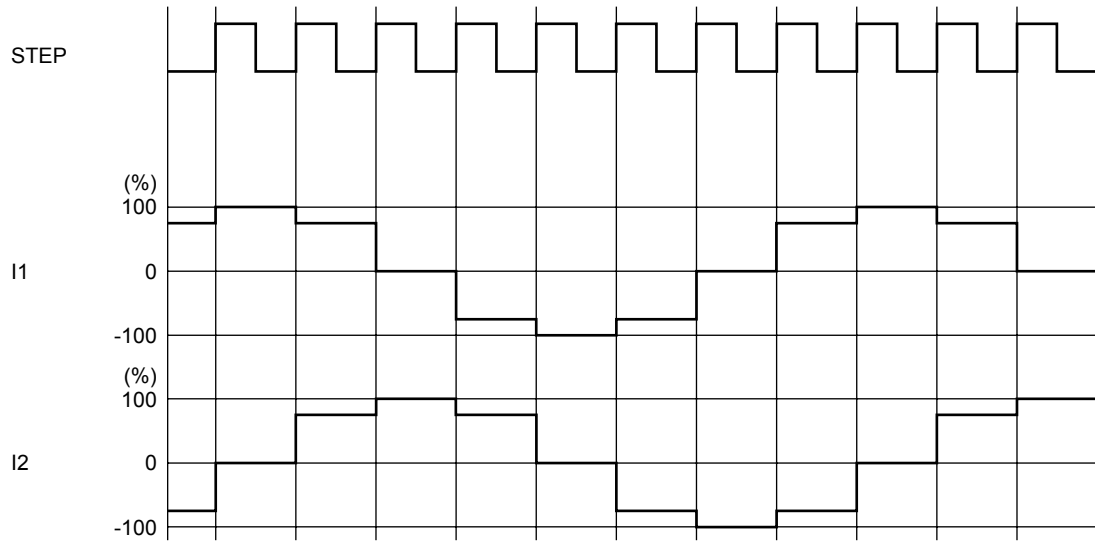


1-2 phase excitation Full torque (CW mode)

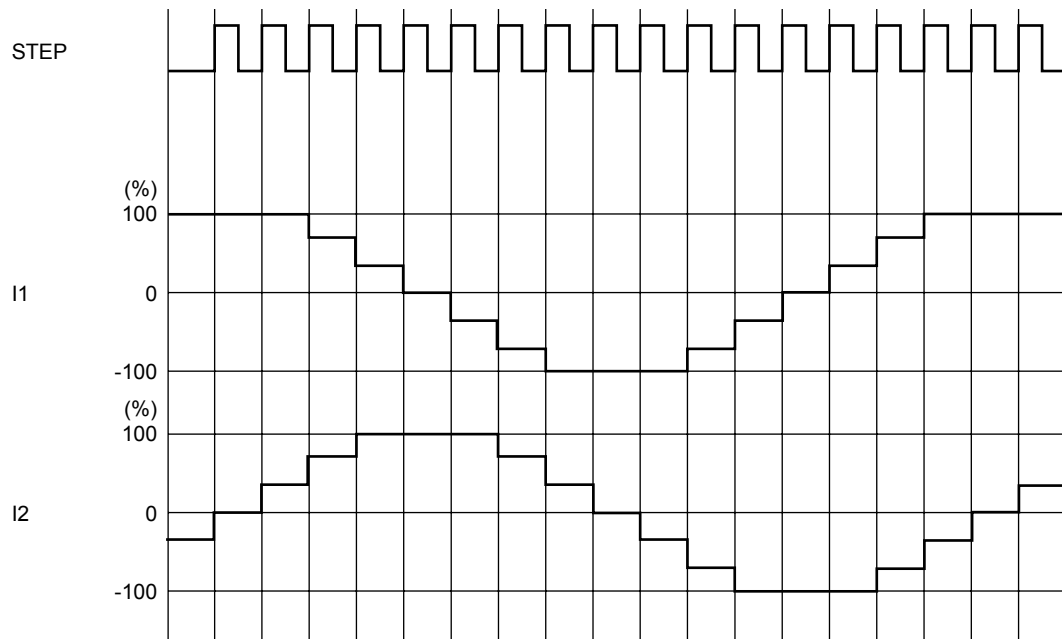


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1-2 phase excitation Full torque (CW mode)

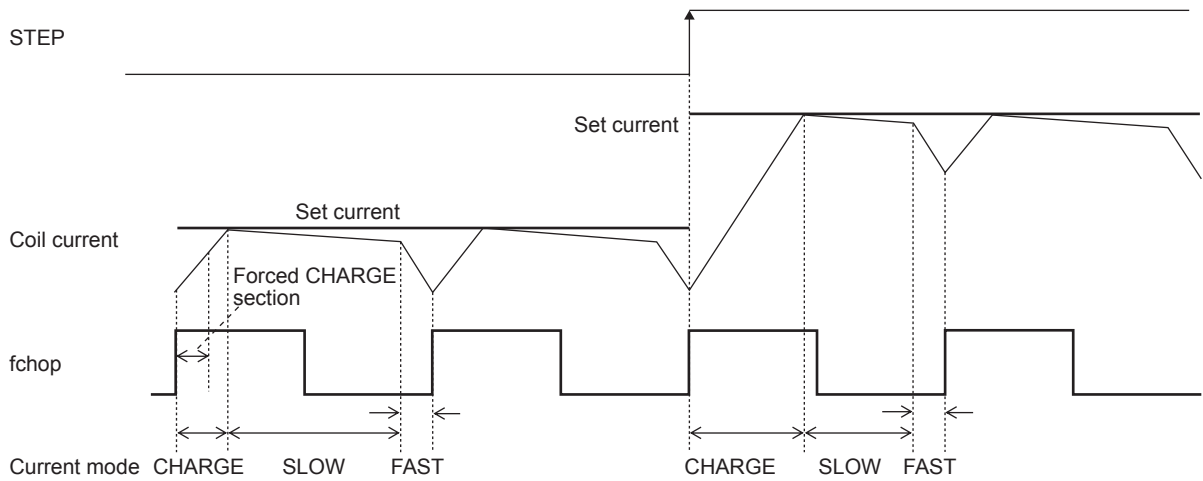


W1-2 phase excitation (CW mode)

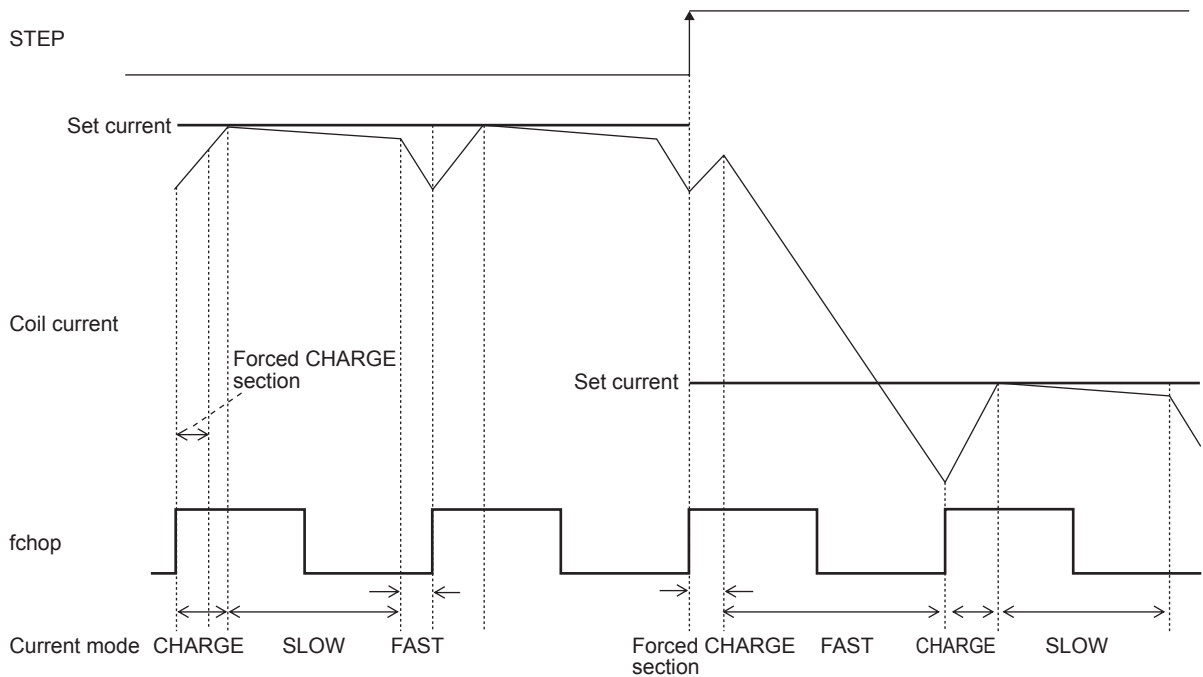


(10) Current control operation specification

(Sine wave increasing direction)



(Sine wave decreasing direction)



In each current mode, the operation sequence is as described below :

- At rise of chopping frequency, the CHARGE mode begins.(The section in which the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF) exists for 1/16 of one chopping cycle.)
- The coil current (ICOIL) and set current (IREF) are compared in this forced CHARGE section.

When $(ICOIL < IREF)$ state exists in the forced CHARGE section ;

CHARGE mode up to $ICOIL \geq IREF$, then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for the 1/16 portion of one chopping cycle.

When $(ICOIL < IREF)$ state does not exist in the forced CHARGE section;

The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

Parallel input control (DM-High)

(1) Parallel input control logic

| I01(02) | I11(12) | Output current (I _O) |
|---------|---------|----------------------------------|
| Low | Low | 0 |
| High | Low | $I_O = ((VREF/5)/RF) \times 1/3$ |
| Low | High | $I_O = ((VREF/5)/RF) \times 2/3$ |
| High | High | $I_O = (VREF/5)/RF$ |

| PH1(2) | current direction |
|--------|-------------------|
| Low | OUTB → OUTA |
| High | OUTA → OUTB |

(2) Setting constant-current control reference voltage

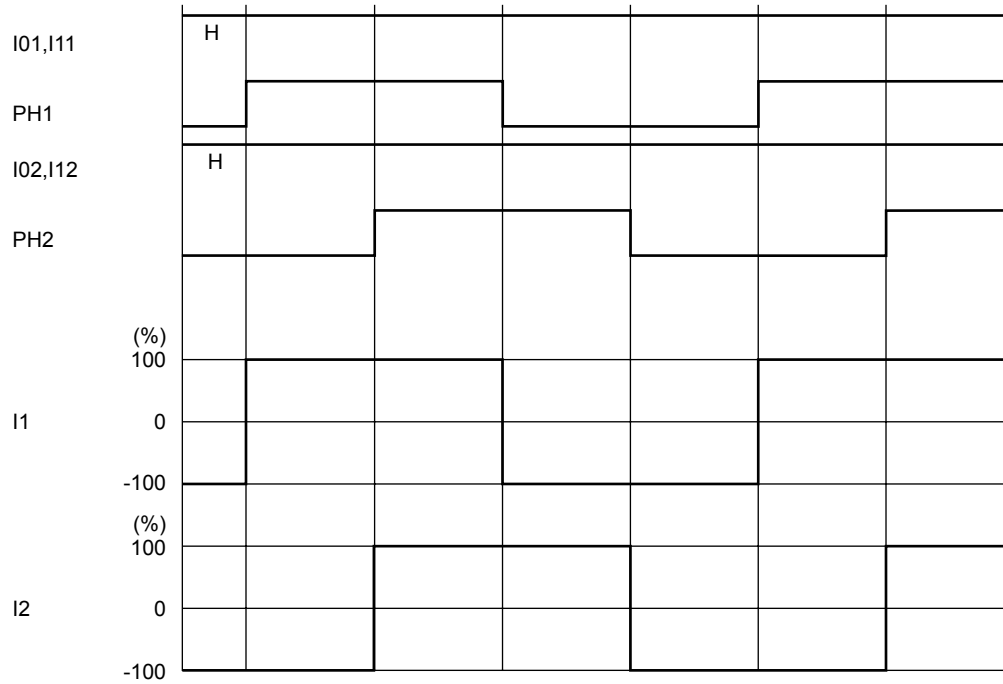
The constant current control standard voltage setting function is the same specification as the CLK-IN input control.

(3) Current control function

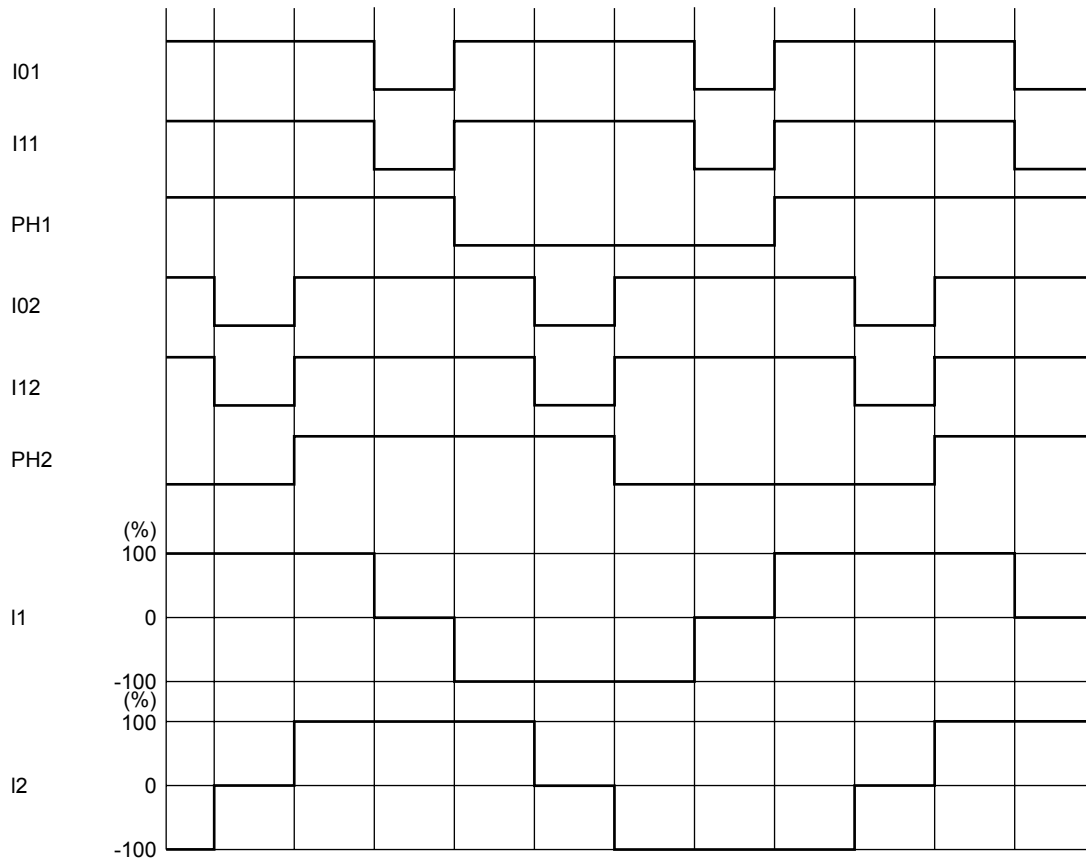
The current control function is the same use as the CLK-IN input control.

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(4) Typical current waveform in each excitation mode when stepping motor parallel input control
2-phase excitation (CW mode)

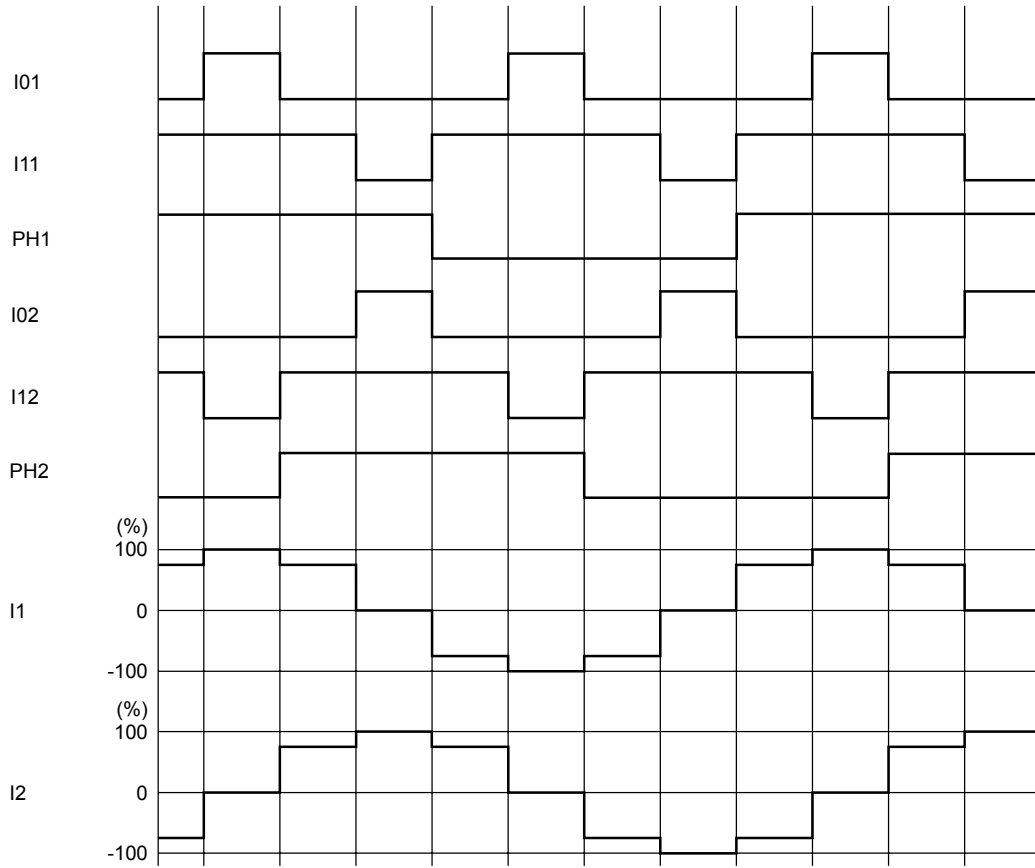


1-2 phase excitation full torque (CW mode)

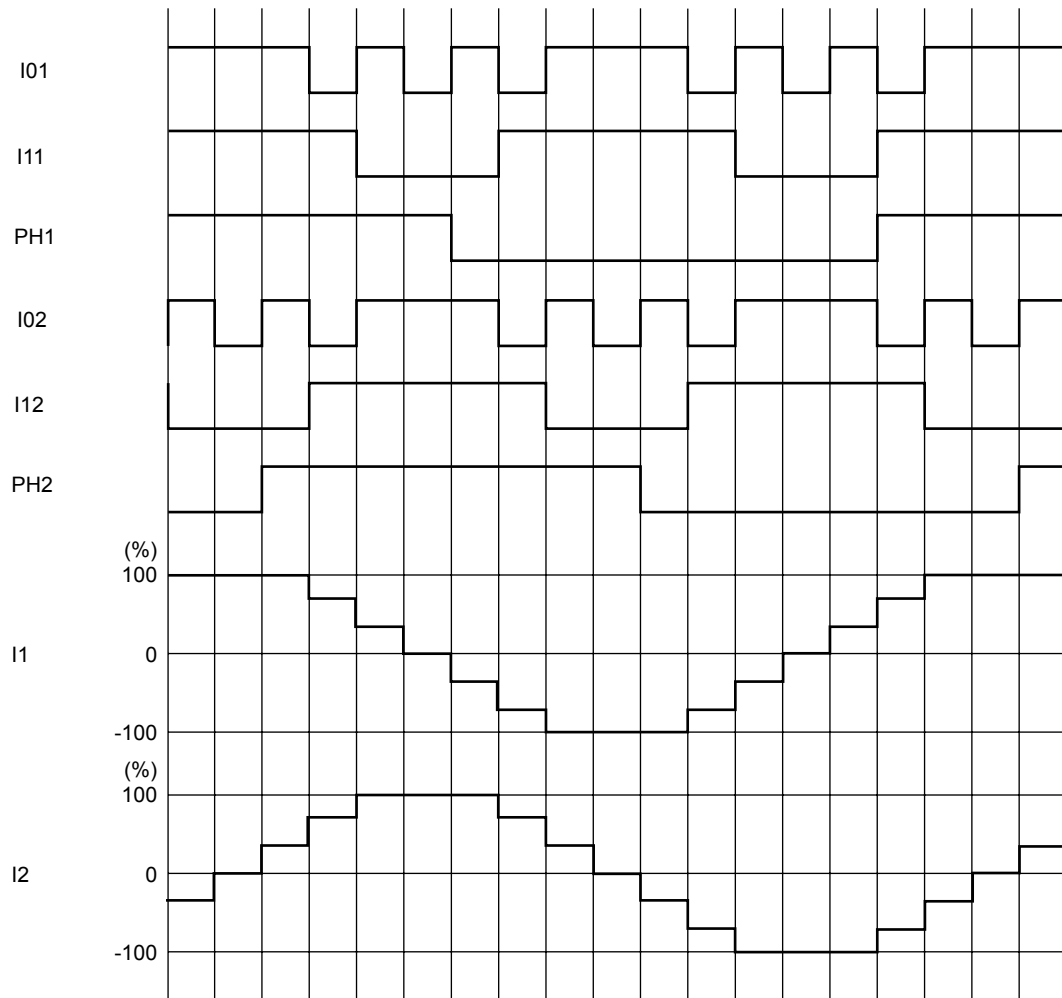


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1-2 phase excitation (CW mode)



W1-2 phase excitation (CW mode)



Output short-circuit protection function

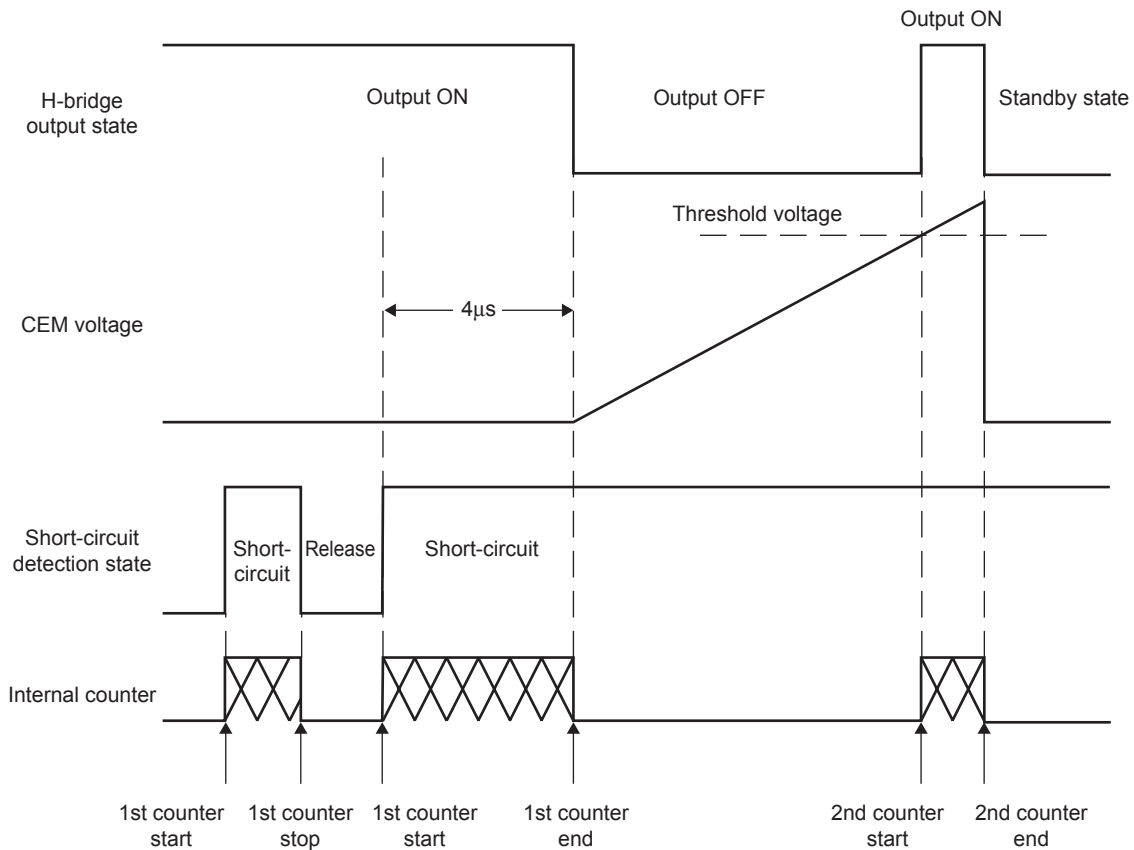
This IC incorporates an output short-circuit protection circuit that, when the output has been shorted by an event such as shorting to power or shorting to ground, to prevent the thing that IC destroys, the output short-circuit protection circuit that turns off the output is built into.

(1) Protection function operation(Latch type)

The detection of the output short-circuited state by the IC causes the output short-circuit protection circuit to be activated.

When the short-circuited state continues for the period of time set using the internal timer (approximately 4μs), the output in which the short-circuiting has been detected is first set to OFF. After this, the output is set to ON again as soon as the timer latch time (Tcem) described later has been exceeded, and if the short-circuited state is still detected, all the outputs of the channel concerned are switched to the standby mode, and this state is held.

This state is released by setting ST to low.



(2) Unusual condition warning output pins (EMO)

IC is provided with the EMO pin which notifies the CPU of an unusual condition if the protection circuit operates by detecting an unusual condition of the IC. This pin is of the open-drain output type and when an unusual condition is detected, the EMO output is placed in the ON (EMO = Low) state.

Furthermore, the EMO pin is placed in the ON state when one of the following conditions occurs.

1. Shorting-to-power, shorting-to-ground, or shorting-to-load occurs at the output pin and the output short-circuit protection circuit is activated.
2. The IC junction temperature rises and the thermal protection circuit is activated.

(3) Timer latch time (Tcem)

The time taken for the output to be set to OFF when the output has been short-circuited can be set using capacitor Ccem, connected between the CEM pin and GND. The value of capacitor Ccem is determined by the formula given below.

Timer latch : Tcem

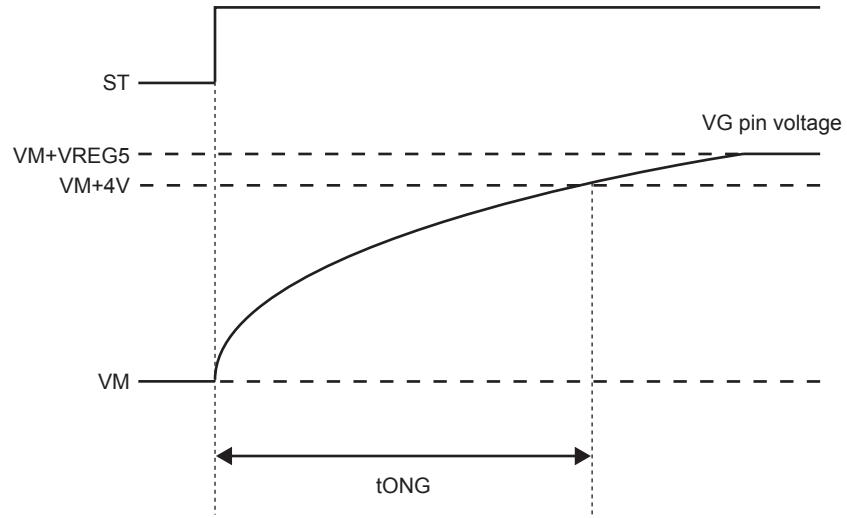
$$Tcem \approx Ccem \times Vtcm / Icem \text{ [sec]}$$

Vtcm : Comparator threshold voltage, typ 1V

Icem : CEM pin charge current, typ 10μA

Charge Pump Circuit

When the ST pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + VREG5 voltage. If the VG pin voltage is not boosted sufficiently, the output cannot be controlled, so be sure to provide a wait time of tONG or more after setting the ST pin High before starting to drive the motor.

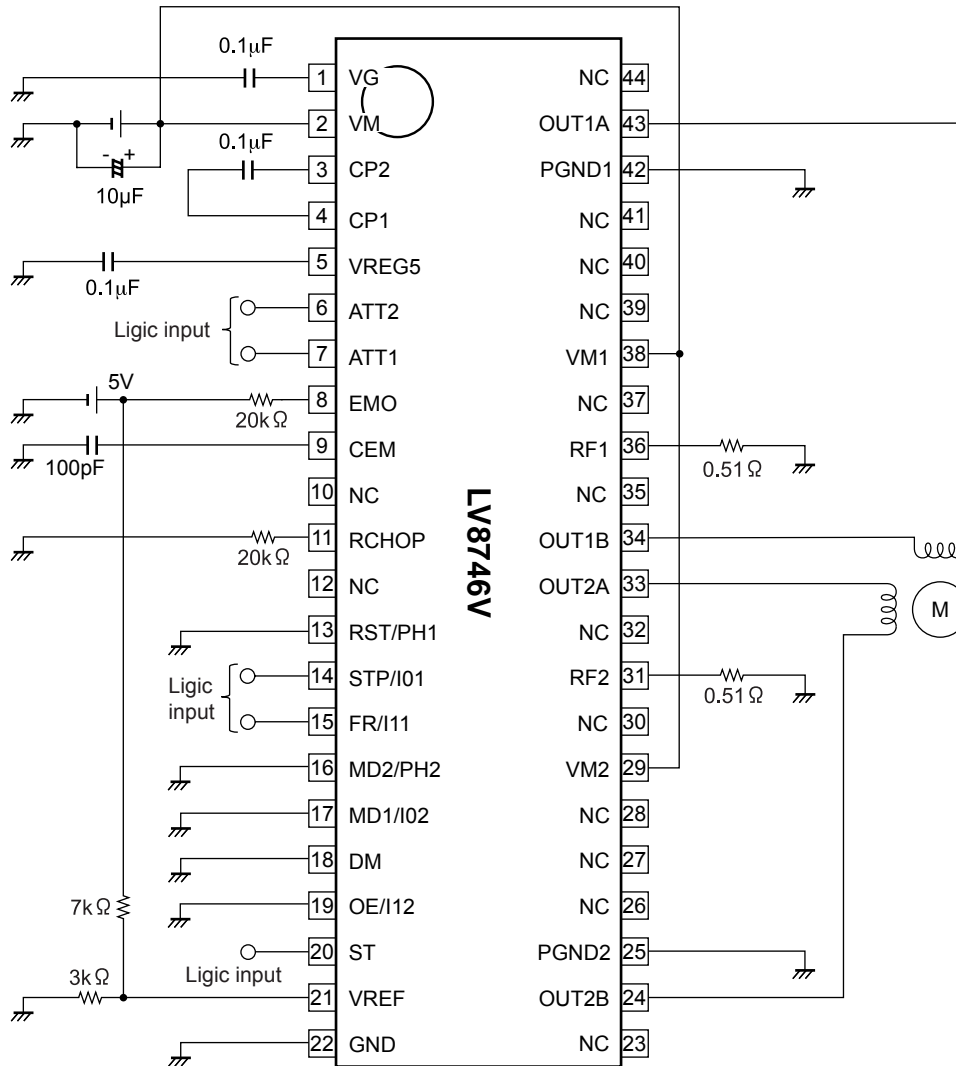


VG Pin Voltage Schematic View

LV8746V

Application Circuit Example

- Clock Inn mode application circuit



The setting conditions for the above circuit diagram example are as follows :

- 2-phase excitation (MD1/I02 = Low, MD2/PH2 = Low)
- Reset function fixed to normal operation (RST = Low)
- Chopping frequency : 62.5kHz (RCHOP = 20kΩ)

| ATT1 | ATT2 | Current setting reference voltage |
|------|------|-----------------------------------|
| Low | Low | VREF/5×100% |
| High | Low | VREF/5×67% |
| Low | High | VREF/5×50% |
| High | High | VREF/5×33% |

The set current value is as follows :

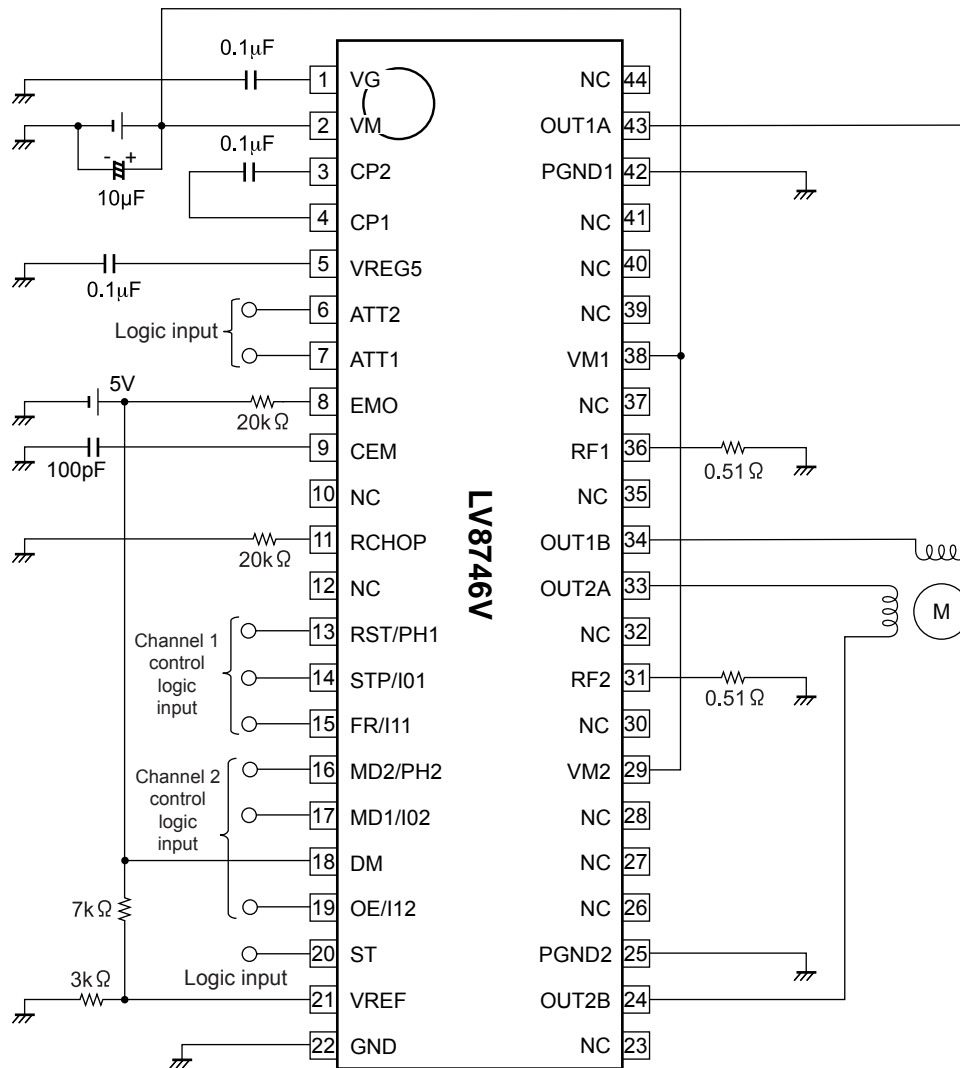
$$I_{OUT} = (VREF/5 \times \text{Voltage setting ratio}) / RF$$

Example) When ATT=Low,ATT2=Low (VREF = 1.5V,RF=0.51Ω)

$$I_{OUT} = (1.5V / 5 \times 1) / 0.51\Omega = 0.6A$$

LV8746V

- DC motor driver circuit (DM = High, and the current limit function is in use.)



The setting conditions for the above circuit diagram example are as follows :

- Chopping frequency : 62.5kHz (RCHOP = 20kΩ)

| I01(02) | I11(12) | Output current (I _O) |
|---------|---------|------------------------------------|
| Low | Low | 0 |
| High | Low | $I_O = ((VREF/5) / RF) \times 1/3$ |
| Low | High | $I_O = ((VREF/5) / RF) \times 2/3$ |
| High | High | $I_O = (VREF/5) / RF$ |

Example) When ATT=Low,ATT2=Low,I01(02)=High,I11(12)=High (VREF = 1.5V,RF=0.51Ω)

$$I_{OUT} = (1.5V / 5 \times 1) / 0.51\Omega = 0.6A$$

| PH1(2) | Electrical current direction |
|--------|------------------------------|
| Low | OUTB → OUTA |
| High | OUTA → OUTB |

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.