# HD-6409

CMOS Manchester Encoder-Decoder

The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409 easily interfaces to protocol controllers.

## Features

- Converter or Repeater Mode
- Independent Manchester encoder and decoder operation
- Static to 1Mbps data rate ensured
- Low bit error rate
- Digital PLL clock recovery
- On-chip oscillator
- Low operating power: 50mW Typical at +5V
- Pb-Free (RoHS Compliant)

## Related Literature

For a full list of related documents, visit our website:

- HD-6409 device page

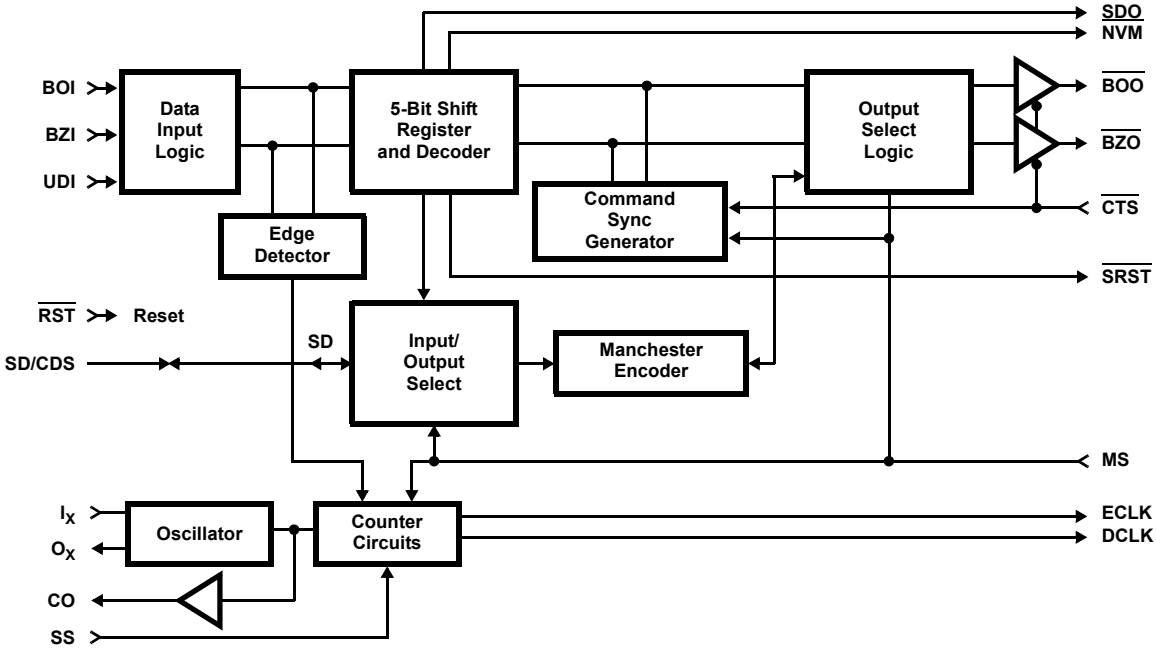
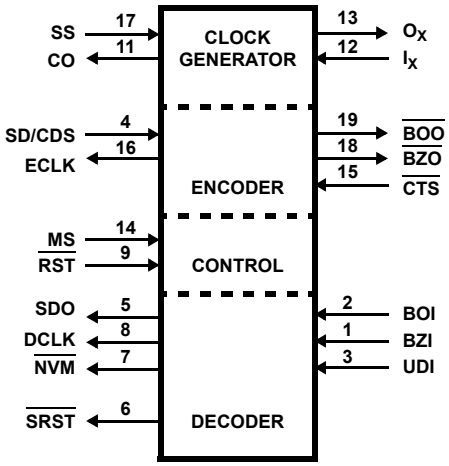



**Figure 1. Block Diagram**

# 1. Overview

## 1.1 Logic Symbol




## 1.2 Ordering Information

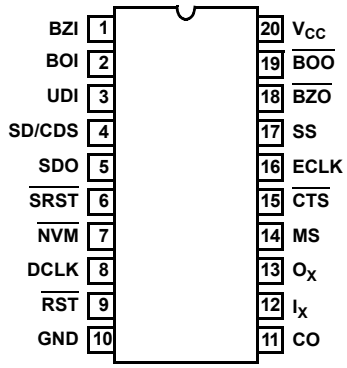
| Part Number (1Mbps) (Notes 2, 3) | Part Marking | Temp. Range (°C) | Tape and Reel (Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|---|---|---|---|---|---|
| HD3-6409-9Z **(No longer available or supported)** | HD3-6409-9Z | -40 to +85 | - | 20 Ld PDIP | E20.3 |
| HD9P6409-9Z | HD9P6409-9Z | -40 to +85 | - | 20 Ld SOIC | M20.3 |
| HD9P6409-9Z96 | HD9P6409-9Z | -40 to +85 | 1k | 20 Ld SOIC | M20.3 |

Notes:

1. See TB347 for details on reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the HD-6409 device page. For more information about MSL, see TB363.

## 1.3 Pin Configuration

20 Ld PDIP, SOIC
Top View



## 1.4 Pin Descriptions

| Pin Number | Type | Symbol | Name | Description |
|---|---|---|---|---|
| 1 | I | BZI | Bipolar Zero Input | Used in conjunction with Pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder, BZI and BOI are logical complements. When using Pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high. |
| 2 | I | BOI | Bipolar One Input | Used in conjunction with Pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder, BOI and BZI are logical complements. When using Pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low. |
| 3 | I | UDI | Unipolar Data Input | An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) inputs Manchester II encoded data to the decoder. When using Pin 1 (BZI) and Pin 2 (BOI) for data input, UDI must be held low. |
| 4 | I/O | SD/CDS | Serial Data/Command Data Sync | In the converter mode, SD/CDS is an input that receives serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern. |
| 5 | O | SDO | Serial Data Out | The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{RST}$ is low. |
| 6 | O | $\overline{SRST}$ | $\overline{Serial\ Reset}$ | In the converter mode, $\overline{SRST}$ follows $\overline{RST}$. In the repeater mode, when $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero, and a valid synchronization sequence is received. |
| 7 | O | $\overline{NVM}$ | $\overline{Nonvalid\ Manchester}$ | A low on $\overline{NVM}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{NVM}$ is set low by a low on $\overline{RST}$, and remains low after $\overline{RST}$ goes high until valid sync pulse followed by two valid Manchester bits is received. |
| 8 | O | DCLK | Decoder Clock | The decoder clock is a 1X clock recovered from BZI and BOI, or UDI to synchronously output received NRZ data (SDO). |
| 9 | I | $\overline{RST}$ | $\overline{Reset}$ | In the converter mode, a low on $\overline{RST}$ forces SDO, DCLK, $\overline{NVM}$, and $\overline{SRST}$ low. A high on $\overline{RST}$ enables SDO and DCLK, and forces $\overline{SRST}$ high. $\overline{NVM}$ remains low after $\overline{RST}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{RST}$ has the same effect on SDO, DCLK, and $\overline{NVM}$ as in the converter mode. When $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero and a valid synchronization sequence is received. |
| 10 | I | GND | Ground | Ground |
| 11 | O | $C_O$ | Clock Output | Buffered output of clock input $I_X$. Can be used as a clock signal for other peripherals. |
| 12 | I | $I_X$ | Clock Input | $I_X$ is the input for an external clock or, if the internal oscillator is used, $I_X$ and $O_X$ are used for the connection of the crystal. |
| 13 | O | $O_X$ | Clock Drive | If the internal oscillator is used, $O_X$ and $I_X$ are used for the connection of the crystal. |
| 14 | I | MS | Mode Select | MS must be held low for operation in the converter mode, and high for operation in the repeater mode. |
| 15 | I | $\overline{CTS}$ | Clear to Send | In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, $\overline{BZO}$ high and ECLK low. A high to low transition of $\overline{CTS}$ initiates transmission of a Command sync pulse. A low on $\overline{CTS}$ enables $\overline{BOO}$, $\overline{BZO}$, and ECLK. In the repeater mode, the function of $\overline{CTS}$ is identical to that of the converter mode with the exception that a transition of $\overline{CTS}$ does not initiate a synchronization sequence. |
| 16 | O | ECLK | Encoder Clock | In the converter mode, ECLK is a 1X clock output that receives serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop. |
| 17 | I | SS | Speed Select | A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency. |

| Pin Number | Type | Symbol | Name | Description |
|---|---|---|---|---|
| 18 | O | $\overline{BZO}$ | Bipolar Zero Output | $\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state. |
| 19 | O | $\overline{BOO}$ | Bipolar One Out | |
| 20 | I | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ is the +5V power supply pin. A 0.1µF decoupling capacitor from $V_{CC}$ (Pin 20) to GND (Pin 10) is recommended. |

Note: (I) Input(O) Output

# 2. Specifications

## 2.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Supply Voltage | | +7.0 | V |
| Input, Output or I/O Voltage | GND - 0.5 | VCC + 0.5 | V |
| ESD Classification | Class 1 | | |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical, Note 4) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| PDIP Package | 75 | N/A |
| SOIC Package | 100 | N/A |

Notes:
4. $\theta_{JA}$ is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Storage Temperature Range | -65 | +150 | °C |
| **Maximum Junction Temperature** | | | |
| Ceramic Package | | +175 | °C |
| Plastic Package | | +150 | °C |
| Pb-Free Reflow Profile (Note 5) | see TB493 | | |

Note:
5. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

## 2.3 Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Operating Temperature Range | -40 | +85 | °C |
| Operating Voltage Range | +4.5 | +5.5 | V |
| Input Rise and Fall Times | | 50 | ns |
| Sync. Transition Span ($t_2$) | | 1.5 Typical, (Notes 6, 7) | DBP |
| Short Data Transition Span ($t_4$) | | 0.5 Typical, (Notes 6, 7) | DBP |
| Long Data Transition Span ($t_5$) | | 1.0 Typical, (Notes 6, 7) | DBP |
| Zero Crossing Tolerance ($t_{CD5}$) | | (Note 8) | |

Notes:
6. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.
7. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ±2 $I_X$ clock cycles (16X mode) or ±6 $I_X$ clock cycles (32X mode).
8. The maximum zero crossing tolerance is ±2 $I_X$ clock cycles (16X mode) or ±6 $I_X$ clock cycles (32 mode) from the nominal.

## 2.4 Die Characteristics

| Parameter | Value |
|---|---|
| Gate Counts | 250 |

## 2.5 DC Electrical Specifications

$V_{CC}$ = 5.0V ± 10%, $T_A$ = -40°C to +85°C

| Parameter | Symbol | Test Conditions (Note 9) | Min (Note 11) | Max (Note 11) | Unit |
|---|---|---|---|---|---|
| Logical “1” Input Voltage | $V_{IH}$ | $V_{CC}$ = 4.5V | 70% $V_{CC}$ | - | V |
| Logical “0” Input Voltage | $V_{IL}$ | $V_{CC}$ = 4.5V | - | 20% $V_{CC}$ | V |
| Logic “1” Input Voltage ($\overline{Reset}$) | $V_{IHR}$ | $V_{CC}$ = 5.5V | $V_{CC}$ -0.5 | - | V |
| Logic “0” Input Voltage ($\overline{Reset}$) | $V_{ILR}$ | $V_{CC}$ = 4.5V | - | GND +0.5 | V |
| Logical “1” Input Voltage (Clock) | $V_{IHC}$ | $V_{CC}$ = 5.5V | $V_{CC}$ -0.5 | - | V |
| Logical “0” Input Voltage (Clock) | $V_{ILC}$ | $V_{CC}$ = 4.5V | - | GND +0.5 | V |
| Input Leakage Current (Except $I_X$) | $I_I$ | $V_{IN}$ = $V_{CC}$ or GND, $V_{CC}$ = 5.5V | -1.0 | +1.0 | µA |
| Input Leakage Current ($I_X$) | $I_I$ | $V_{IN}$ = $V_{CC}$ or GND, $V_{CC}$ = 5.5V | -20 | +20 | µA |
| I/O Leakage Current | $I_O$ | $V_{OUT}$ = $V_{CC}$ or GND, $V_{CC}$ = 5.5V | -10 | +10 | µA |
| Output HIGH Voltage (All Except $O_X$) | $V_{OH}$ | $I_{OH}$ = -2.0mA, $V_{CC}$ = 4.5V (Note 10) | $V_{CC}$ -0.4 | - | V |
| Output LOW Voltage (All Except $O_X$) | $V_{OL}$ | $I_{OL}$ = +2.0mA, $V_{CC}$ = 4.5V (Note 10) | - | 0.4 | V |
| Standby Power Supply Current | $I_{CCSB}$ | $V_{IN}$ = $V_{CC}$ or GND, $V_{CC}$ = 5.5V, Outputs Open | - | 100 | µA |
| Operating Power Supply Current | $I_{CCOP}$ | f = 16.0MHz, $V_{IN}$ = $V_{CC}$ or GND $V_{CC}$ = 5.5V, $C_L$ = 50pF | - | 18.0 | mA |
| Functional Test | $F_T$ | (Note 9) | - | - | - |

Notes:

9. Tested as follows: f = 16MHz, $V_{IH}$ = 70% $V_{CC}$, $V_{IL}$ = 20% $V_{CC}$, $V_{OH} \geq V_{CC}/2$, and $V_{OL} \leq V_{CC}/2$, $V_{CC}$ = 4.5V and 5.5V.
10. Interchanging of force and sense conditions is permitted.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

## 2.6 Capacitance

$T_A$ = +25°C, Frequency = 1MHz.

| Parameter | Symbol | Test Conditions | Typ | Unit |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | All measurements are referenced to device GND | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | 12 | pF |

## 2.7 AC Electrical Specifications

$V_{CC}$ = 5.0V ±10%, $T_A$ = -40°C to +85°C

| Parameter | Symbol | Test Conditions (Note 12) | Min (Note 11) | Max (Note 11) | Unit |
|---|---|---|---|---|---|
| Clock Frequency | $f_C$ | | - | 16 | MHz |
| Clock Period | $t_C$ | | $1/f_C$ | - | sec |
| Bipolar Pulse Width | $t_1$ | | $t_C$+10 | - | ns |
| One-Zero Overlap | $t_3$ | | - | $t_C$-10 | ns |
| Clock High Time | $t_{CH}$ | f = 16.0MHz | 20 | - | ns |
| Clock Low Time | $t_{CL}$ | f = 16.0MHz | 20 | - | ns |
| Serial Data Setup Time | $t_{CE1}$ | | 120 | - | ns |
| Serial Data Hold Time | $t_{CE2}$ | | 0 | - | ns |
| DCLK to SDO, $\overline{NVM}$ | $t_{CD2}$ | | - | 40 | ns |
| ECLK to $\overline{BZO}$ | $t_{R2}$ | | - | 40 | ns |

$V_{CC}$ = 5.0V ±10%, $T_A$ = -40°C to +85°C **(Continued)**

| Parameter | Symbol | Test Conditions (Note 12) | Min (Note 11) | Max (Note 11) | Unit |
|---|---|---|---|---|---|
| Output Rise Time (All except Clock) | $t_r$ | From 1.0V to 3.5V, $C_L$ = 50pF, Note 13 | - | 50 | ns |
| Output Fall Time (All except Clock) | $t_f$ | From 3.5V to 1.0V, $C_L$ = 50pF, Note 13 | - | 50 | ns |
| Clock Output Rise Time | $t_r$ | From 1.0V to 3.5V, $C_L$ = 20pF, Note 13 | - | 11 | ns |
| Clock Output Fall Time | $t_f$ | From 3.5V to 1.0V, $C_L$ = 20pF, Note 13 | - | 11 | ns |
| ECLK to $\overline{BZO}$, $\overline{BOO}$ | $t_{CE3}$ | Notes 13, 14 | 0.5 | 1.0 | DBP |
| $\overline{CTS}$ Low to $\overline{BZO}$, $\overline{BOO}$ Enabled | $t_{CE4}$ | Notes 13, 14 | 0.5 | 1.5 | DBP |
| $\overline{CTS}$ Low to ECLK Enabled | $t_{CE5}$ | Notes 13, 14 | 10.5 | 11.5 | DBP |
| $\overline{CTS}$ High to ECLK Disabled | $t_{CE6}$ | Notes 13, 14 | - | 1.0 | DBP |
| $\overline{CTS}$ High to $\overline{BZO}$, $\overline{BOO}$ Disabled | $t_{CE7}$ | Notes 13, 14 | 1.5 | 2.5 | DBP |
| UDI to SDO, $\overline{NVM}$ | $t_{CD1}$ | Notes 13, 14 | 2.5 | 3.0 | DBP |
| $\overline{RST}$ Low to CDLK, SDO, $\overline{NVM}$ Low | $t_{CD3}$ | Notes 13, 14 | 0.5 | 1.5 | DBP |
| $\overline{RST}$ High to DCLK, Enabled | $t_{CD4}$ | Notes 13, 14 | 0.5 | 1.5 | DBP |
| UDI to $\overline{BZO}$, $\overline{BOO}$ | $t_{R1}$ | Notes 13, 14 | 0.5 | 1.0 | DBP |
| UDI to SDO, $\overline{NVM}$ | $t_{R3}$ | Notes 13, 14 | 2.5 | 3.0 | DBP |

Notes:

12. AC testing as follows: f = 4.0MHz, $V_{IH}$ = 70% $V_{CC}$, $V_{IL}$ = 20% $V_{CC}$, Speed Select = 16X, $V_{OH} \geq V_{CC}/2$, $V_{OL} \leq V_{CC}/2$, $V_{CC}$ = 4.5V and 5.5V. Input rise and fall times driven at 1ns/V, Output load = 50pF.
13. Limits established by characterization and are not production tested.
14. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

## 2.8 Timing Waveforms

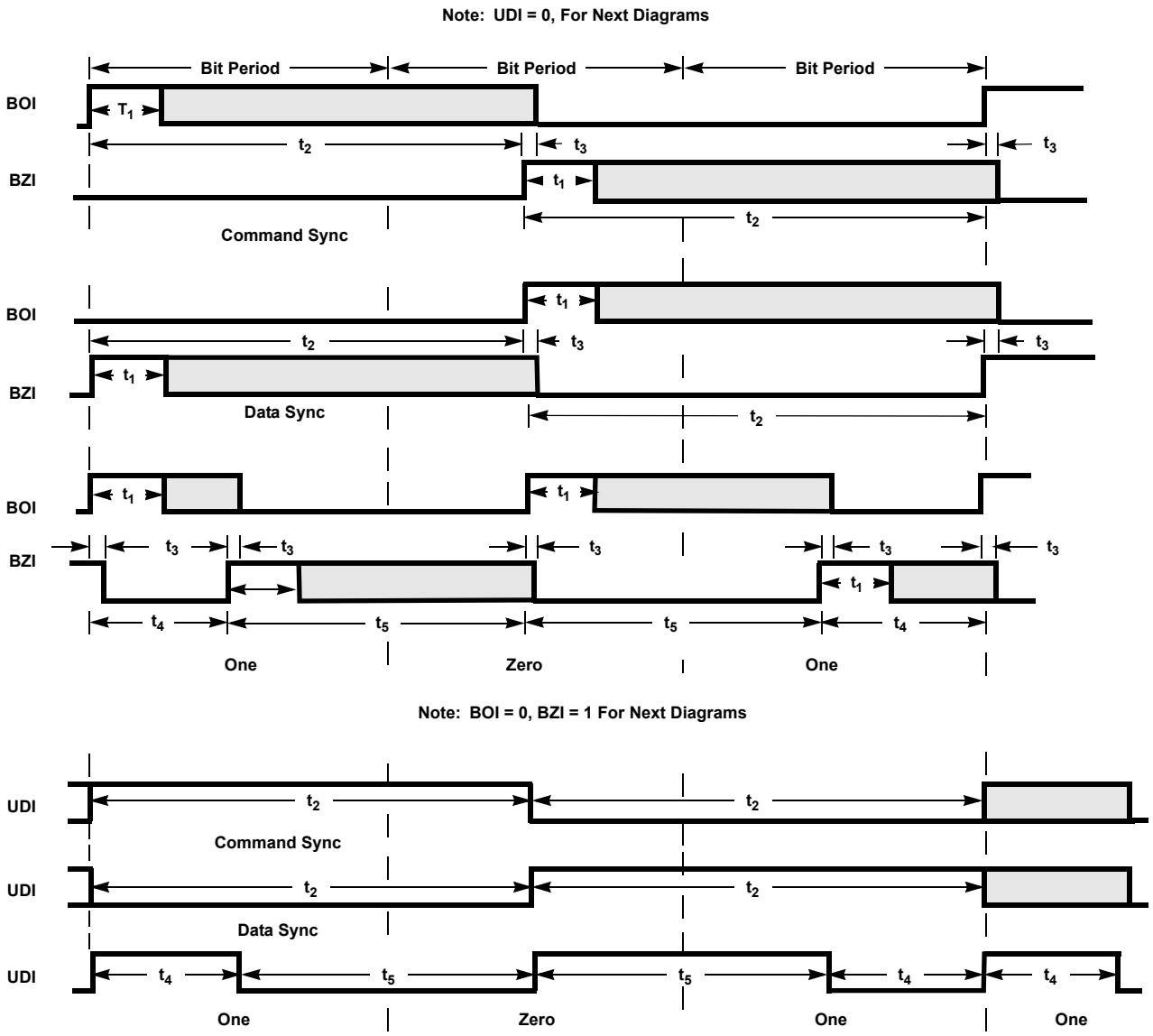



**Figure 2.**

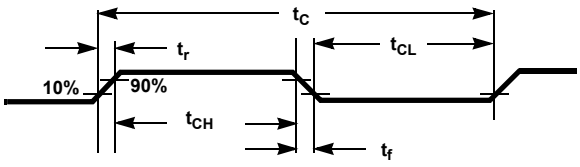



**Figure 3. Clock Timing**

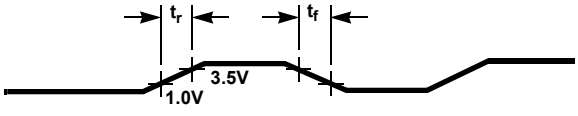



**Figure 4. Output Waveform**

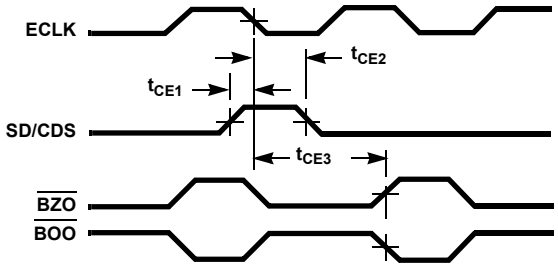



**Figure 5. Encoder Timing**

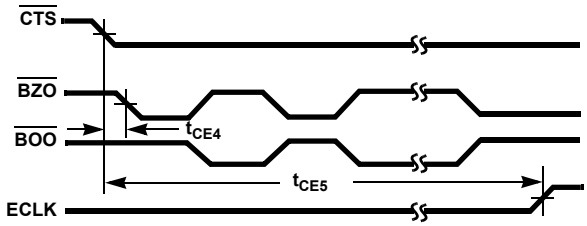



**Figure 6. Encoder Timing**

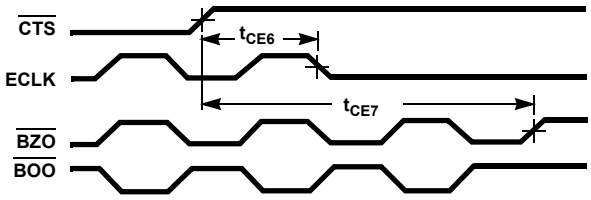
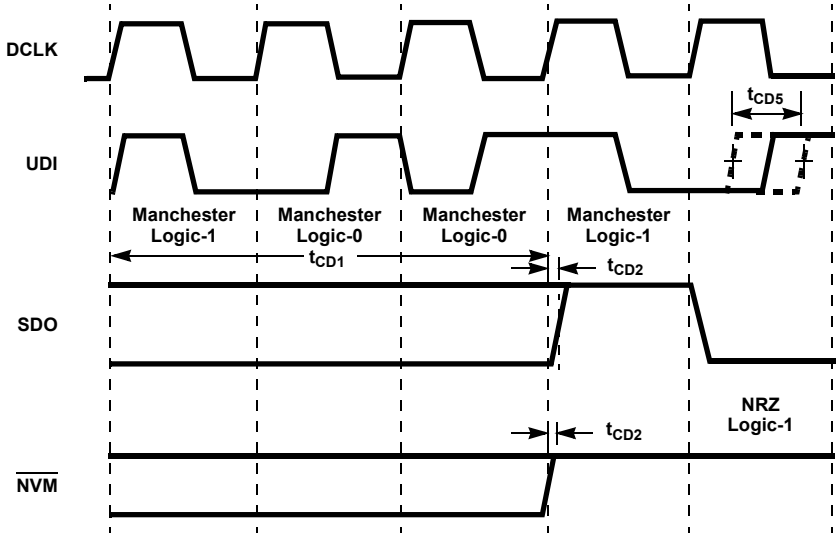



**Figure 7. Encoder Timing**




Note: Manchester Data-In is not synchronous with Decoder Clock.
Decoder Clock is synchronous with decoded NRZ out of SDO.

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**Figure 8. Decoder Timing**

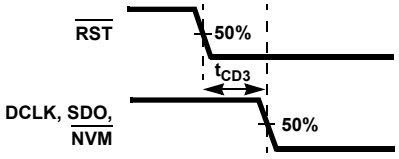



**Figure 9. Decoder Timing**

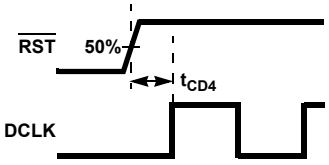



**Figure 10. Decoder Timing**

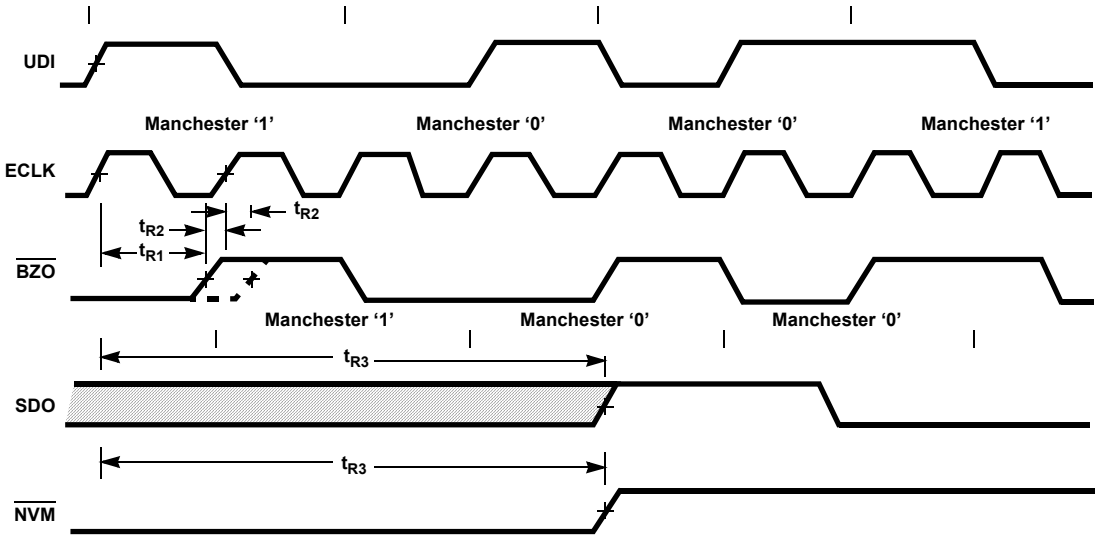
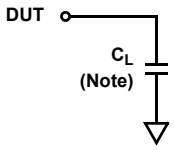



**Figure 11. Repeater Timing**

## 2.9 Test Load Circuit




**Note: Includes Stray and Jig Capacitance**

**Figure 12. Test Load Circuit**

# 3. Functional Descriptions

## 3.1 Encoder Operation

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock $I_X$ for internal timing. $\overline{CTS}$ controls the encoder outputs, ECLK, $\overline{BOO}$, and $\overline{BZO}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{CTS}$ enables encoder outputs ECLK, $\overline{BOO}$, and $\overline{BZO}$, while a high on $\overline{CTS}$ forces $\overline{BZO}$, $\overline{BOO}$ high and holds ECLK low. When $\overline{CTS}$ goes from high to low ①, a synchronization sequence is transmitted out on $\overline{BOO}$ and $\overline{BZO}$. A synchronization sequence consists of eight Manchester “0” bits followed by a command sync pulse. ② A command sync pulse is a 3-bit wide pulse with the first 1 1/2 bits high followed by 1 1/2 bits low. ③ Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{BOO}$ and $\overline{BZO}$ following the command sync pulse. ④ Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by $\overline{CTS}$. Manchester data out is inverted.

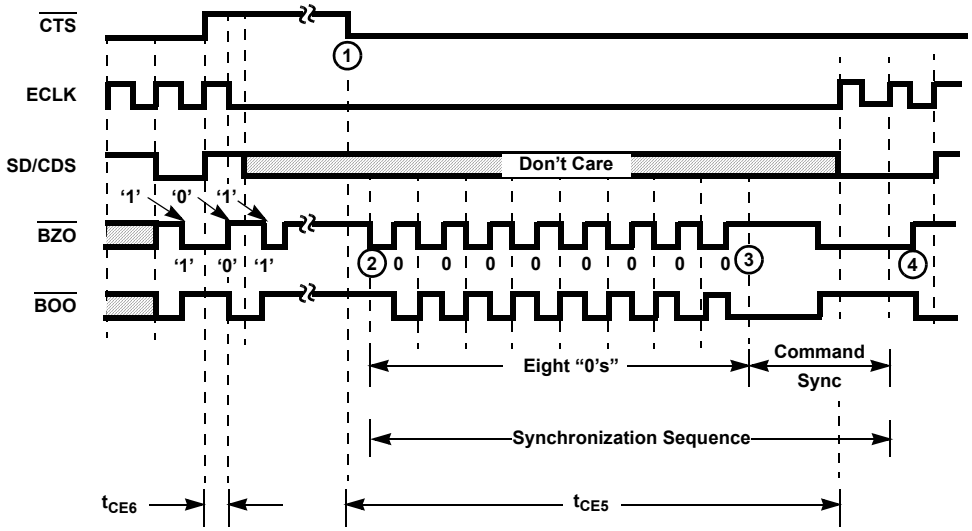



**Figure 13. Encoder Operation**

## 3.2 Decoder Operation

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data, such as $\overline{Bipolar\ One}$ $\overline{Out}$ through an inverter to Unipolar Data Input. The decoder continuously monitors this data input for valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a 3-bit delay between UDI, BOI, or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{RST}$ pin. When $\overline{RST}$ is low, SDO, DCLK, and $\overline{NVM}$ are forced low. When $\overline{RST}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{NVM}$ output remains low after a low-to-high transition on $\overline{RST}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every high-to-low transition of this clock. Three bit periods after an invalid Manchester bit is

received on UDI, or BOI, $\overline{NVM}$ goes low synchronously with the questionable data output on SDO. **Note: The decoder does not re-establish proper data decoding until another sync pattern is recognized**.

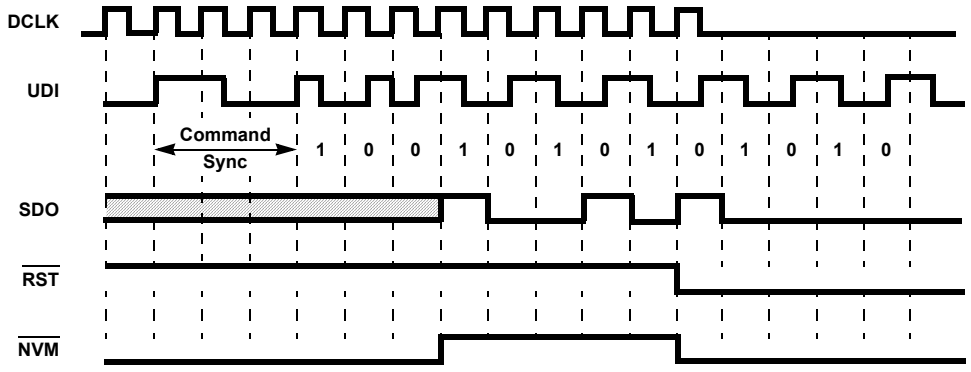



**Figure 14. Decoder Operation**

## 3.3 Repeater Operation

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only noninverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{BOO}$ and $\overline{BZO}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{BOO}$ and $\overline{BZO}$.

A low on $\overline{CTS}$ enables ECLK, $\overline{BOO}$, and $\overline{BZO}$. In contrast to the converter mode, a transition on CTS does not initiate a synchronization sequence of eight 0's and a command sync. The repeater mode does recognize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When $\overline{RST}$ is low, the outputs SDO, DCLK, and $\overline{NVM}$ are low, and $\overline{SRST}$ is set low. $\overline{SRST}$ remains low after $\overline{RST}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. The reset bit is the first data bit after the sync pulse. With RST high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

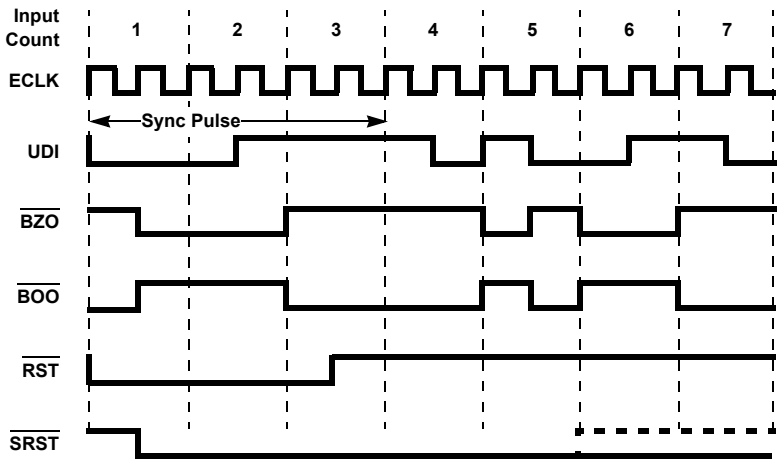



**Figure 15. Repeater Operation**

## 3.4 Manchester Code

Nonreturn-to-Zero (NRZ) code represents the binary values logic-0 and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

The Manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a low-to-high transition in the middle of the data cell, and a logic-1 as a high-to-low mid bit transition, Manchester II is also known as Biphase-L code.

The bandwidth of NRZ is from DC to the clock frequency fc/2, while that of Manchester is from fc/2 to fc. Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octave, while the ratio for NRZ is the range of 5 to 10 octaves. It is much easier to design a narrow band than a wideband amp.

Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that there is no transition, an error indiction is given, and synchronization must be re-established. This places relatively stringent requirements on the incoming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. There is no phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily have transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over successive data cells. A final synchronization advantage concerns the HD-6409's sync pulse that initiates synchronization. This 3-bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

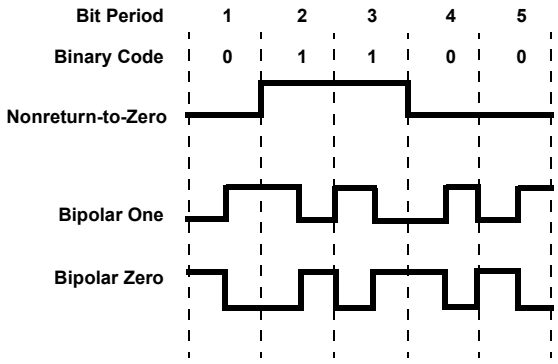



**Figure 16. Manchester Code**

## 3.5 Crystal Oscillator and LC Oscillator Modes

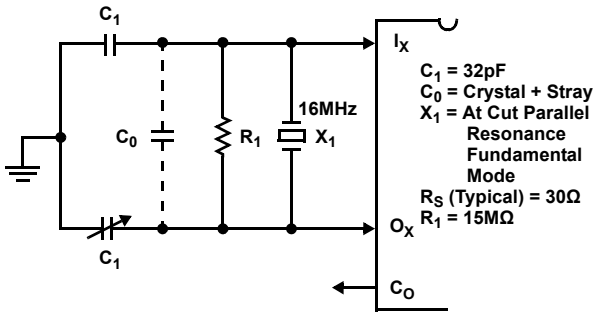



Figure 17. Crystal Oscillator Mode

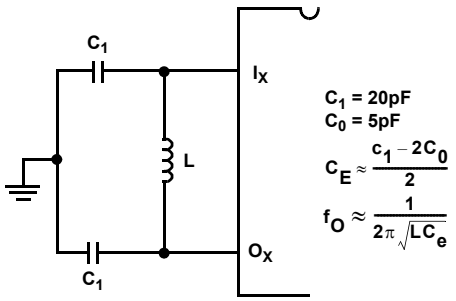



Figure 18. LC Oscillator Mode

## 3.6 Using the 6409 as a Manchester Encoded UART

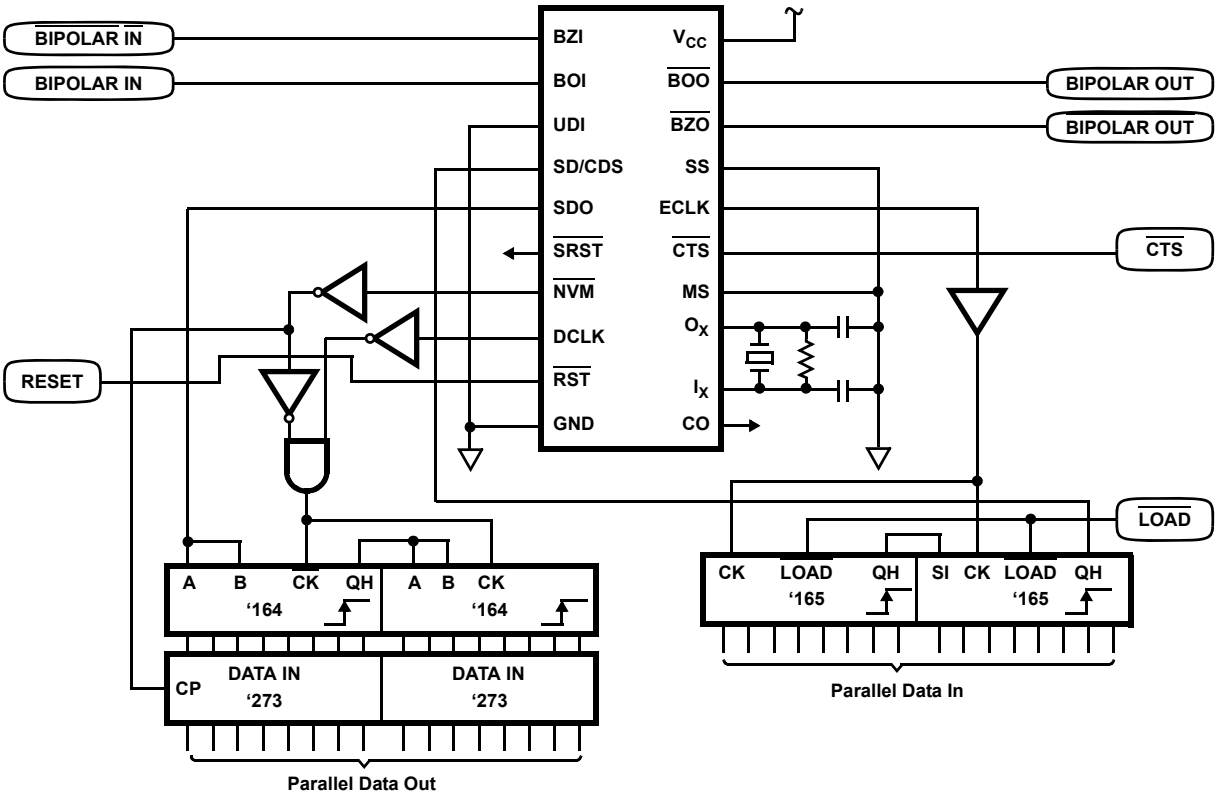



Figure 19. Manchester Encoder UART

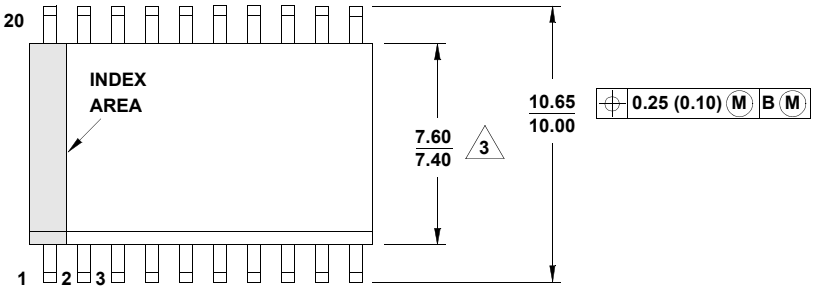
# 4. Revision History

| Rev. | Date | Description |
|---|---|---|
| 5.00 | Jul.8.19 | Applied new formatting throughout.<br>Updated links throughout.<br>Added Related Literature.<br>Updated Ordering Information table by adding tape and reel information, removing HD3-6409-9, and updating Notes 1 and 3.<br>Removed About Intersil section.<br>Updated Disclaimer |
| 4.00 | Oct.1.15 | Added Rev History beginning with Rev 4.<br>Added About Intersil Verbiage.<br>Updated Ordering Information on page 1<br>Updated POD M20.3 to most current version. Revision changes are as follows:<br>**Top View**:<br>Corrected "7.50 BSC" to "7.60/7.40" (no change from rev 2; error was introduced in conversion)<br>Changed "10.30 BSC" to "10.65/10.00" (no change from rev 2; error was introduced in conversion)<br>**Side View**:<br>Changed "12.80 BSC" to "13.00/12.60" (no change from rev 2; error was introduced in conversion)<br>Changed "2.65 max" to "2.65/2.35" (no change from rev 2; error was introduced in conversion)<br>Changed Note 1 from "ANSI Y14.5M-1982." to "ASME Y14.5M-1994"<br>Updated to new POD format by moving dimensions from table onto drawing and adding land pattern |

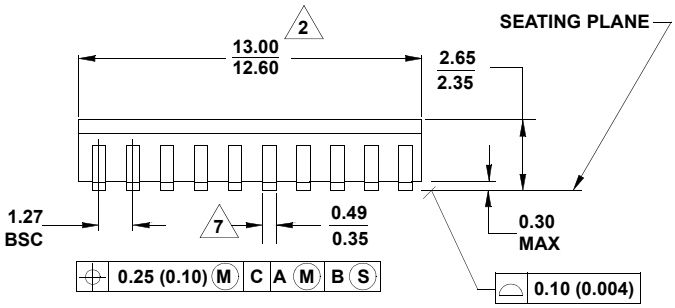
# 5. Package Outline Drawings

For the most recent package outline drawing, see M20.3.

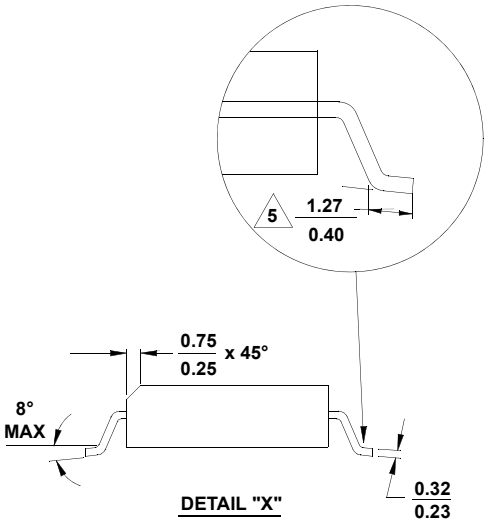
M20.3
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)
Rev 3, 2/11



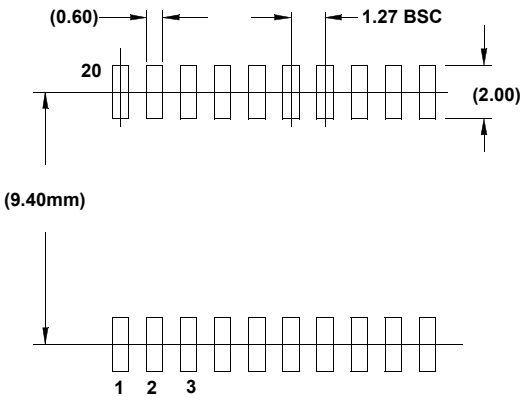

TOP VIEW




SIDE VIEW




DETAIL "X"

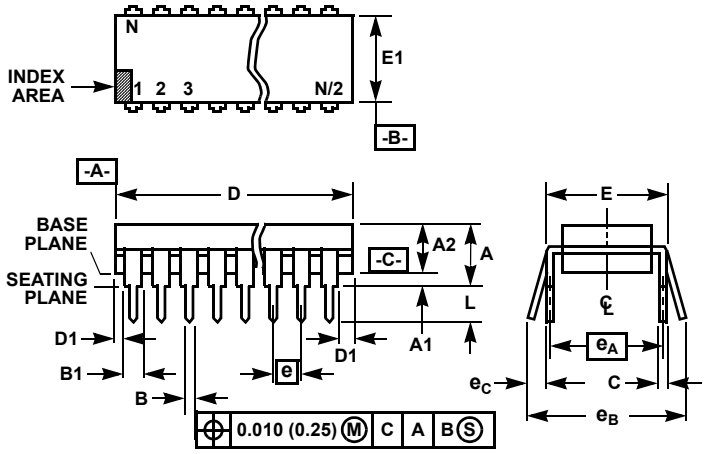



TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Dimension does not include interlead lash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Dimension is the length of terminal for soldering to a substrate.
6. Terminal numbers are shown for reference only.
7. The lead width as measured 0.36mm (0.14 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
8. Controlling dimension: MILLIMETER.
9. Dimensions in ( ) for reference only.
10. JEDEC reference drawing number: MS-013-AC.

For the most recent package outline drawing, see E20.3.




Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 Lead Dual-In-Line Plastic Package (PDIP)

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.55 | 1.77 | 8 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.980 | 1.060 | 24.89 | 26.9 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 20 | | 20 | | 9 |

Rev. 0 12/93

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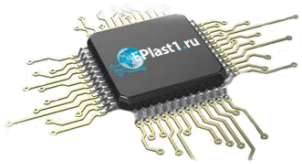


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