

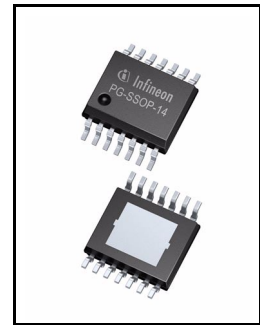
OPTIREG™ Linear TLS820B2ELVSE

Low Dropout Linear Voltage Regulator



Features

- Wide input voltage range from 3.0 V to 40 V
- Selectable output voltage 5 V or 3.3 V
- Output voltage precision $\leq \pm 2\%$
- Output current capability up to 200 mA
- Ultra low current consumption, typical 20 μ A
- Very low dropout voltage, typical 100 mV, at output currents below 100 mA
- Stable with ceramic output capacitor of 1 μ F
- Enable
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)



Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

The OPTIREG™ Linear TLS820B2ELVSE is a linear voltage regulator with high performance, very low dropout linear voltage and very low quiescent current.

With an input voltage range of 3 V to 40 V and very low quiescent current of only 20 μ A, this regulator is perfectly suitable for automotive or other supply systems permanently connected to the battery.

The new loop concept combines fast regulation and very high stability while requiring only one small ceramic capacitor of 1 μ F at the output. At output currents below 100 mA the device has a very low dropout voltage of only 100 mV (for an output voltage of 5 V) and 120 mV (for an output voltage of 3.3 V). The operating range starts at an input voltage of only 3 V (extended operating range). This makes the TLS820B2ELVSE suitable for automotive systems that need to operate during cranking condition.

The device can be switched on and off by the enable feature.

The output voltage of the TLS820B2ELVSE can be selected between 5 V and 3.3 V by connecting the SEL pin to either V_Q or GND. When the SEL pin is connected to V_Q , the regulator's output is set to 5 V; when the SEL pin is connected to GND, the regulator's output is set to 3.3 V.

Internal protection features such as output current limitation and overtemperature shutdown, protect the device from immediate damage caused by failures such as output shorted to GND, overcurrent or overtemperature conditions.

External components

An input capacitor C_1 is recommended to compensate for line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. The TLS820B2ELVSE is designed to be stable with low ESR ceramic capacitors.

| Type | Package | Marking |
|---------------|----------------|----------------|
| TLS820B2ELVSE | PG-SSOP-14 | 820B2VSE |

Table of contents

| | | |
|----------|---|-----------|
| | Features | 1 |
| | Potential applications | 1 |
| | Product validation | 1 |
| | Description | 1 |
| | Table of contents | 3 |
| 1 | Block diagram | 4 |
| 2 | Pin configuration | 5 |
| 2.1 | Pin assignment TLS820B2ELVSE | 5 |
| 2.2 | Pin definitions and functions TLS820B2ELVSE | 5 |
| 3 | General product characteristics | 7 |
| 3.1 | Absolute maximum ratings | 7 |
| 3.2 | Functional range | 8 |
| 3.3 | Thermal resistance | 9 |
| 4 | Block description and electrical characteristics | 10 |
| 4.1 | Voltage regulation | 10 |
| 4.2 | Typical performance characteristics voltage regulator | 14 |
| 4.3 | Current consumption | 18 |
| 4.4 | Typical performance characteristics current consumption | 19 |
| 4.5 | Enable | 20 |
| 4.6 | Typical performance characteristics enable | 21 |
| 4.7 | Output voltage selection | 22 |
| 5 | Application information | 23 |
| 5.1 | Application diagram | 23 |
| 5.2 | Selection of external components | 23 |
| 5.2.1 | Input pin | 23 |
| 5.2.2 | Output pin | 23 |
| 5.3 | Thermal considerations | 24 |
| 5.4 | Reverse polarity protection | 24 |
| 5.5 | Further application information | 24 |
| 6 | Package information | 25 |
| 7 | Revision history | 26 |

Block diagram

1 Block diagram

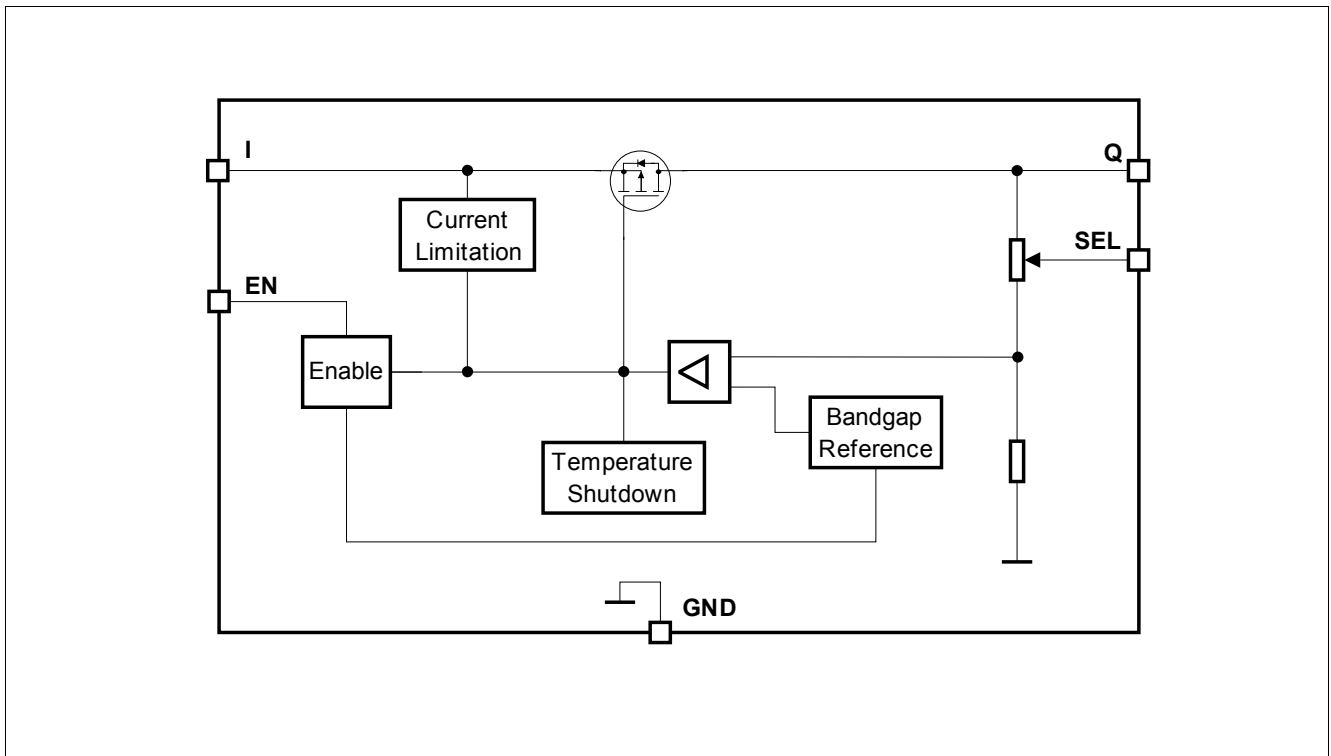


Figure 1 Block diagram TLS820B2ELVSE

Pin configuration

2 Pin configuration

2.1 Pin assignment TLS820B2ELVSE

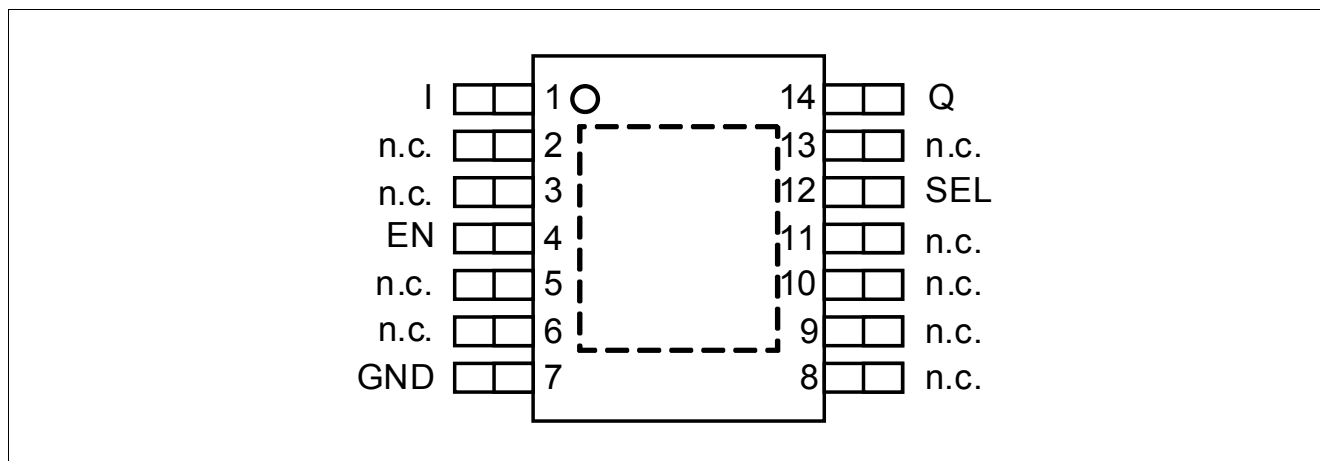


Figure 2 Pin configuration TLS820B2ELVSE

2.2 Pin definitions and functions TLS820B2ELVSE

| Pin | Symbol | Function |
|-----|--------|---|
| 1 | I | Input It is recommended to place a small ceramic capacitor to GND, close to the pins, to compensate for line influences |
| 2 | n. c. | Not connected Leave open or connect to GND |
| 3 | n. c. | Not connected Leave open or connect to GND |
| 4 | EN | Enable (integrated pull-down resistor) Enable the IC with high level input signal Disable the IC with low level input signal |
| 5 | n. c. | Not connected Leave open or connect to GND |
| 6 | n. c. | Not connected Leave open or connect to GND |
| 7 | GND | Ground |
| 8 | n. c. | Not connected Leave open or connect to GND |
| 9 | n. c. | Not connected Leave open or connect to GND |
| 10 | n. c. | Not connected Leave open or connect to GND |
| 11 | n. c. | Not connected Leave open or connect to GND |

Pin configuration

| Pin | Symbol | Function |
|------------|---------------|---|
| 12 | SEL | Output voltage selection Connect to Q to select 5 V output voltage Connect to GND to select 3.3 V output voltage |
| 13 | n. c. | Not connected Leave open or connect to GND |
| 14 | Q | Output voltage Connect output capacitor C_Q to GND close to the pin, respecting the values specified for its capacitance and ESR in “Functional range” on Page 8 |
| Pad | – | Exposed pad Connect to heatsink area; Connect to GND |

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings¹⁾

$T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------------|---------------|--------|------|------|------|-------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Input I, enable EN | | | | | | | |
| Voltage | V_I, V_{EN} | -0.3 | - | 45 | V | - | P_4.1.1 |
| Output Q | | | | | | | |
| Voltage | V_Q | -0.3 | - | 7 | V | - | P_4.1.2 |
| Select SEL | | | | | | | |
| voltage | V_{SEL} | -0.3 | - | 7 | V | - | P_4.1.3 |
| Temperatures | | | | | | | |
| Junction temperature | T_j | -40 | - | 150 | °C | - | P_4.1.5 |
| Storage temperature | T_{stg} | -55 | - | 150 | °C | - | P_4.1.6 |
| ESD absorption | | | | | | | |
| ESD susceptibility to GND | V_{ESD} | -2 | - | 2 | kV | ²⁾ HBM | P_4.1.7 |
| ESD susceptibility to GND | V_{ESD} | -750 | - | 750 | V | ³⁾ CDM at all pins | P_4.1.8 |

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. Exceeding the absolute max ratings may cause permanent damage to the device and affects the device's reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as operation outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

General product characteristics

3.2 Functional range

Table 2 Functional range

$T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------|----------------------|------|------|------------------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Input voltage range | V_I | $V_{Q,nom} + V_{dr}$ | – | 40 | V | ¹⁾ – | P_4.2.1 |
| Extended input voltage range | $V_{I,ext}$ | 3.0 | – | 40 | V | ²⁾ – | P_4.2.2 |
| Enable voltage range | V_{EN} | 0 | – | 40 | V | – | P_4.2.3 |
| Capacitance of output capacitor for stability | C_Q | 1 | – | – | μF | ³⁾⁴⁾ – | P_4.2.4 |
| Equivalent series resistance of output capacitor | $ESR(C_Q)$ | – | – | 50 | Ω | ³⁾ – | P_4.2.5 |
| Junction temperature | T_j | -40 | – | 150 | $^\circ\text{C}$ | – | P_4.2.6 |

1) Output current is limited internally and depends on the input voltage, see electrical characteristics for more details.

2) If $V_{I,ext,min} \leq V_I \leq V_{Q,nom} + V_{dr}$, then $V_Q = V_I - V_{dr}$. If $V_I < V_{I,ext,min}$, then V_Q can drop to 0 V.

3) Not subject to production test, specified by design.

4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

General product characteristics

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 3 Thermal resistance of TLS820B2ELVSE in PG-SSOP-14 package

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------|------------|--------|------|------|------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Junction to case | R_{thJC} | – | 10 | – | K/W | ¹⁾ – | P_4.3.1 |
| Junction to ambient | R_{thJA} | – | 41 | – | K/W | ¹⁾²⁾ 2s2p board | P_4.3.2 |
| Junction to ambient | R_{thJA} | – | 125 | – | K/W | ¹⁾³⁾ 1s0p board, footprint only | P_4.3.3 |
| Junction to ambient | R_{thJA} | – | 59 | – | K/W | ¹⁾³⁾ 1s0p board, 300 mm ² heatsink area on PCB | P_4.3.4 |
| Junction to ambient | R_{thJA} | – | 51 | – | K/W | ¹⁾³⁾ 1s0p board, 600 mm ² heatsink area on PCB | P_4.3.5 |

- 1) Not subject to production test, specified by design
- 2) Specified R_{thJA} value is according to Jecdec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
- 3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 μm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the following factors:

- output capacitor C_Q
- load current
- chip temperature
- internal circuit design

Output capacitor

To ensure stable operation, the capacitance of the output capacitor and its equivalent series resistor (ESR) requirements as specified in **“Functional range” on Page 8** must be maintained. The output capacitor must be sized according to the requirements of the application to be able to buffer load steps.

Input capacitors, reverse polarity protection diode

An input capacitor C_I is recommended to compensate for line influences.

In order to block influences such as pulses and high frequency distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

Smooth ramp-up

In order to prevent overshoots during startup, a smooth ramp-up function is implemented. This ensures almost no output voltage overshoots during startup, mostly independent from load and output capacitance.

Output current limitation

If the load current exceeds the specified limit, due to a short-circuit for example, then the output current is limited and the output voltage decreases.

Overtemperature shutdown

The overtemperature shutdown circuit prevents the IC from immediate destruction in case of a fault condition (for example a permanent short-circuit at the output) by switching off the power stage. After the IC has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the IC.

Block description and electrical characteristics

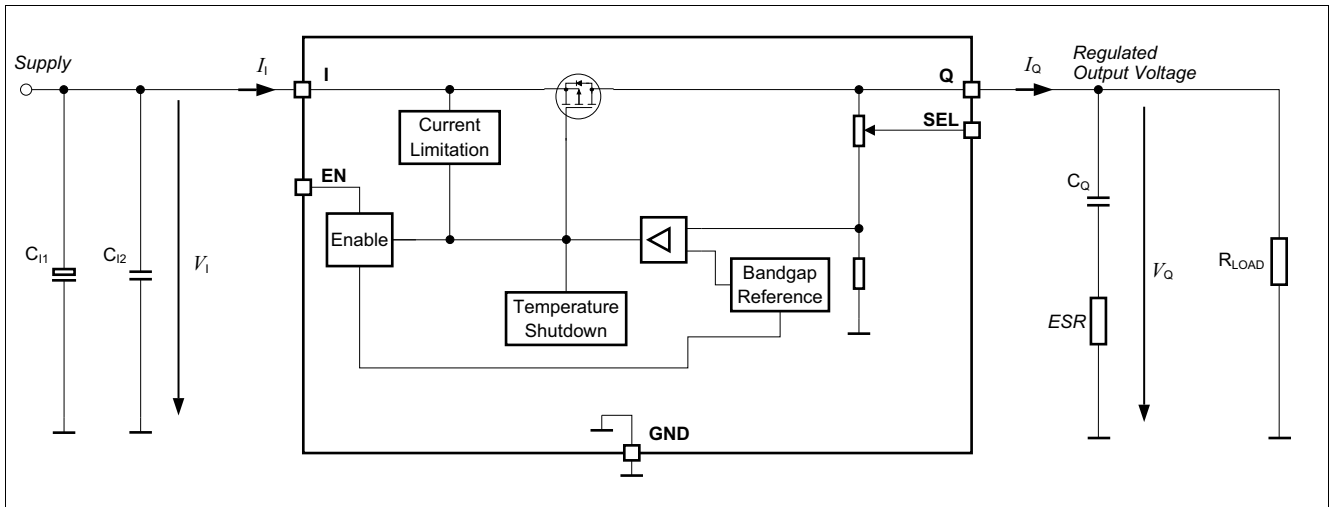


Figure 3 Voltage regulation

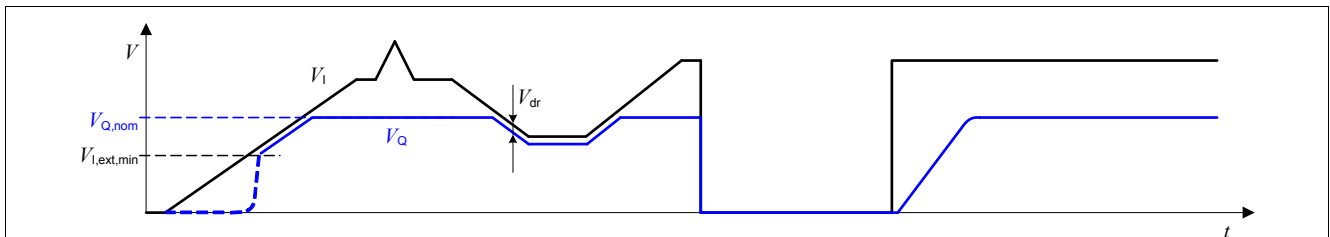


Figure 4 Output voltage vs. input voltage

Block description and electrical characteristics

Table 4 Electrical characteristics voltage regulator

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified)
 Typical values are given at $T_j = 25^\circ\text{C}$

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---------------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| 5 V output voltage | | | | | | | |
| Output voltage accuracy | V_Q | 4.9 | 5.0 | 5.1 | V | $0.05\text{ mA} \leq I_Q \leq 200\text{ mA}$ $5.5\text{ V} \leq V_I \leq 28\text{ V}$ SEL connected to Q | P_5.1.1 |
| Output voltage accuracy | V_Q | 4.9 | 5.0 | 5.1 | V | $0.05\text{ mA} \leq I_Q \leq 100\text{ mA}$ $5.3\text{ V} \leq V_I \leq 40\text{ V}$ SEL connected to Q | P_5.1.2 |
| Dropout voltage $V_{dr} = V_I - V_Q$ | V_{dr} | – | 200 | 400 | mV | ¹⁾ $I_Q = 200\text{ mA}$, SEL connected to Q | P_5.1.8 |
| Dropout voltage $V_{dr} = V_I - V_Q$ | V_{dr} | – | 100 | 200 | mV | ¹⁾ $I_Q = 100\text{ mA}$, SEL connected to Q | P_5.1.9 |
| Power supply ripple rejection | $PSRR$ | – | 60 | – | dB | ²⁾ $f_{\text{ripple}} = 100\text{ Hz}$ $V_{\text{ripple}} = 0.5 V_{pp}$ $I_Q = 10\text{ mA}$ SEL connected to Q | P_5.1.10 |
| 3.3 V output voltage | | | | | | | |
| Output voltage accuracy | V_Q | 3.23 | 3.3 | 3.37 | V | $0.05\text{ mA} \leq I_Q \leq 200\text{ mA}$ $3.85\text{ V} \leq V_I \leq 28\text{ V}$ SEL connected to GND | P_5.1.12 |
| Output voltage accuracy | V_Q | 3.23 | 3.3 | 3.37 | V | $0.05\text{ mA} \leq I_Q \leq 100\text{ mA}$ $3.61\text{ V} \leq V_I \leq 40\text{ V}$ SEL connected to GND | P_5.1.13 |
| Dropout voltage $V_{dr} = V_I - V_Q$ | V_{dr} | – | 240 | 480 | mV | ¹⁾ $I_Q = 200\text{ mA}$, SEL connected to GND | P_5.1.19 |
| Dropout voltage $V_{dr} = V_I - V_Q$ | V_{dr} | – | 120 | 240 | mV | ¹⁾ $I_Q = 100\text{ mA}$, SEL connected to GND | P_5.1.20 |
| Power supply ripple rejection | $PSRR$ | – | 63 | – | dB | ²⁾ $f_{\text{ripple}} = 100\text{ Hz}$ $V_{\text{ripple}} = 0.5 V_{pp}$ $I_Q = 10\text{ mA}$ SEL connected to GND | P_5.1.21 |
| Other electrical characteristics | | | | | | | |
| Output current limitation | $I_{Q,max}$ | 201 | 350 | 550 | mA | $0\text{ V} < V_Q < V_{Q,nom} - 0.1\text{ V}$ | P_5.1.23 |
| Load regulation steady-state | $\Delta V_{Q,load}$ | -15 | -5 | – | mV | $I_Q = 0.05\text{ mA}$ to 200 mA $V_I = 6.5\text{ V}$ | P_5.1.29 |
| Line regulation steady-state | $\Delta V_{Q,line}$ | – | 1 | 10 | mV | $V_I = 8\text{ V}$ to 32 V $I_Q = 5\text{ mA}$ | P_5.1.30 |

Block description and electrical characteristics

Table 4 Electrical characteristics voltage regulator (cont'd)

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified)
 Typical values are given at $T_j = 25^\circ\text{C}$

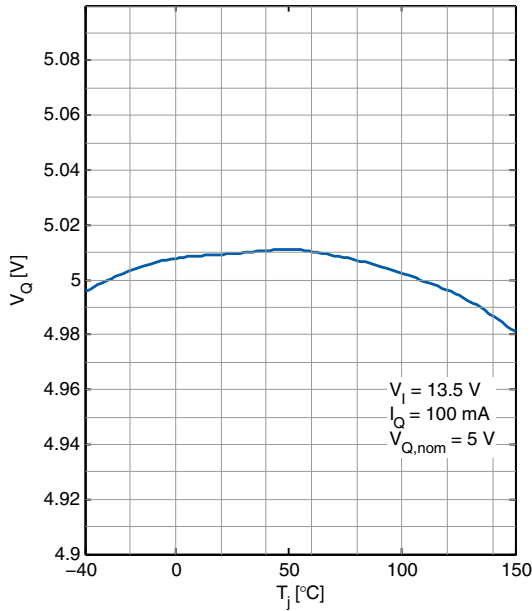
| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-------------|--------|------|------|------------------|--------------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Overtemperature shutdown threshold | $T_{j,sd}$ | 151 | 175 | 200 | $^\circ\text{C}$ | ²⁾ T_j increasing | P_5.1.31 |
| Overtemperature shutdown threshold hysteresis | $T_{j,sdh}$ | – | 15 | – | K | ²⁾ T_j decreasing | P_5.1.32 |

1) Measured when the output voltage V_O has dropped by 100 mV while input voltage was gradually decreased.

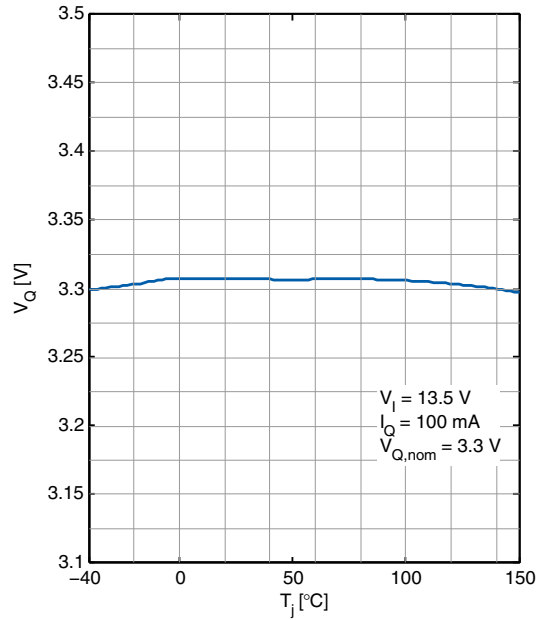
2) Not subject to production test, specified by design

4.2 Typical performance characteristics voltage regulator

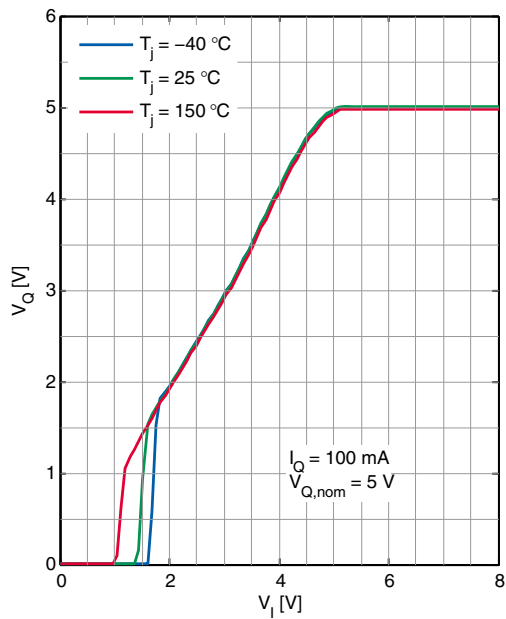
Output voltage V_Q versus junction temperature T_j



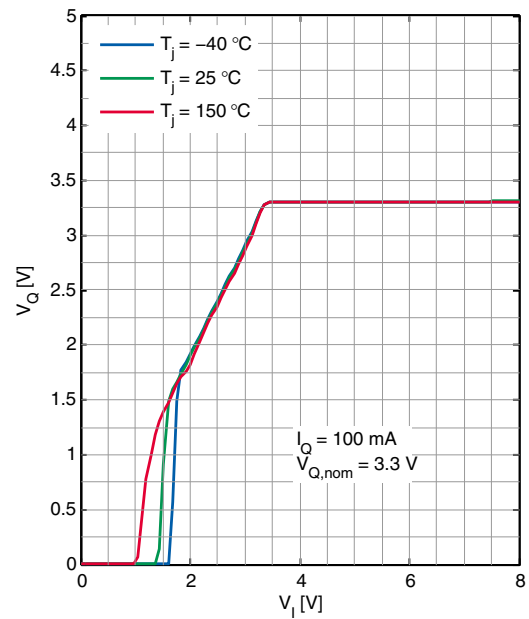
Output voltage V_Q versus junction temperature T_j



Output voltage V_Q versus input voltage V_i

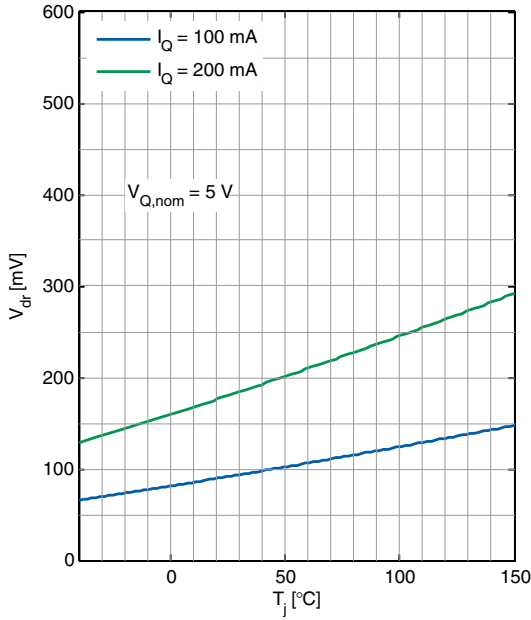


Output voltage V_Q versus input voltage V_i

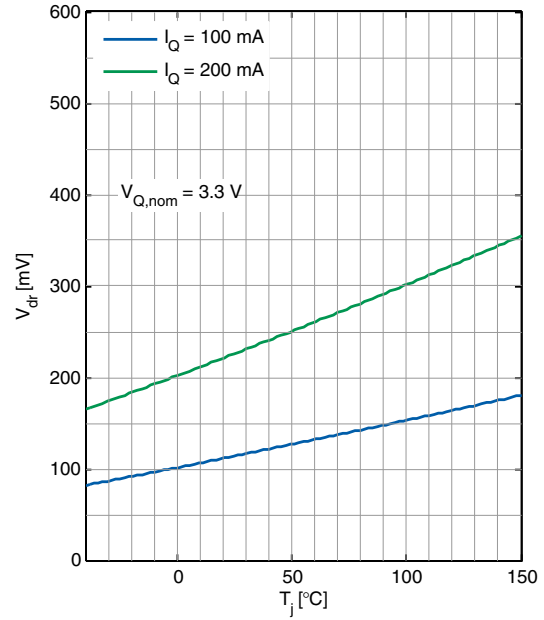


Block description and electrical characteristics

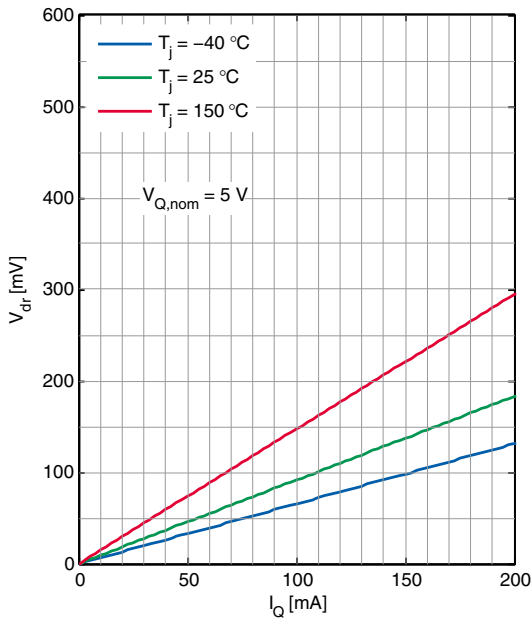
Dropout voltage V_{dr} versus junction temperature T_j



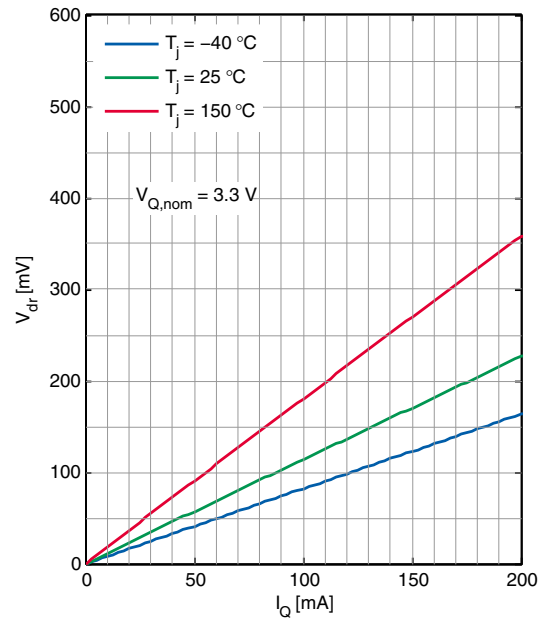
Dropout voltage V_{dr} versus junction temperature T_j



Dropout voltage V_{dr} versus output current I_Q

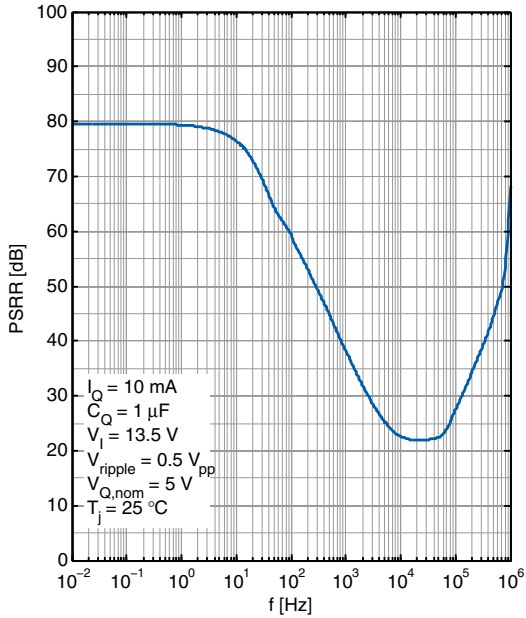


Dropout voltage V_{dr} versus output current I_Q

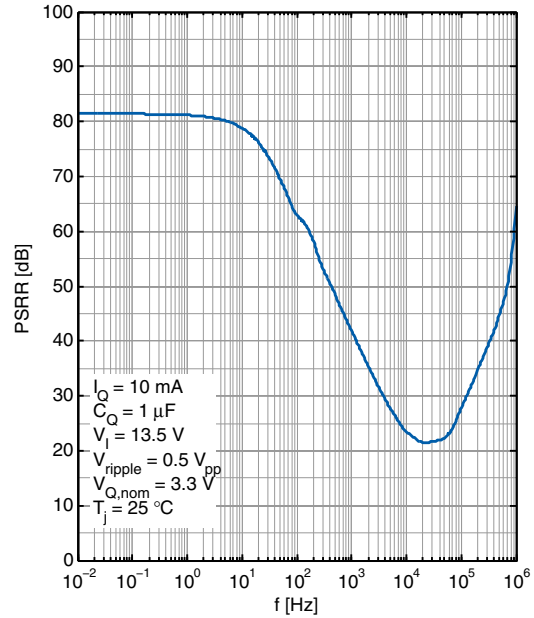


Block description and electrical characteristics

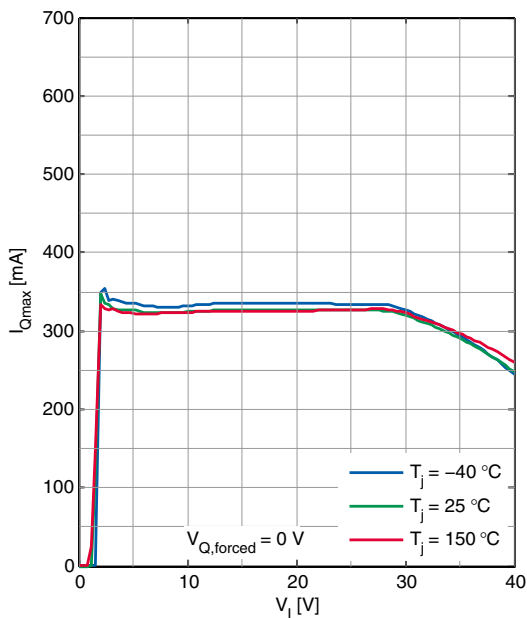
Power supply ripple rejection $PSRR$ versus ripple frequency f



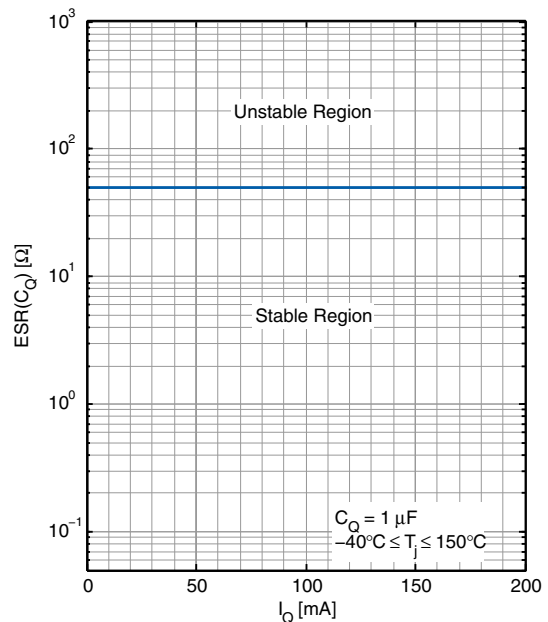
Power supply ripple rejection $PSRR$ versus ripple frequency f



Maximum output current $I_{Q,max}$ versus input voltage V_I

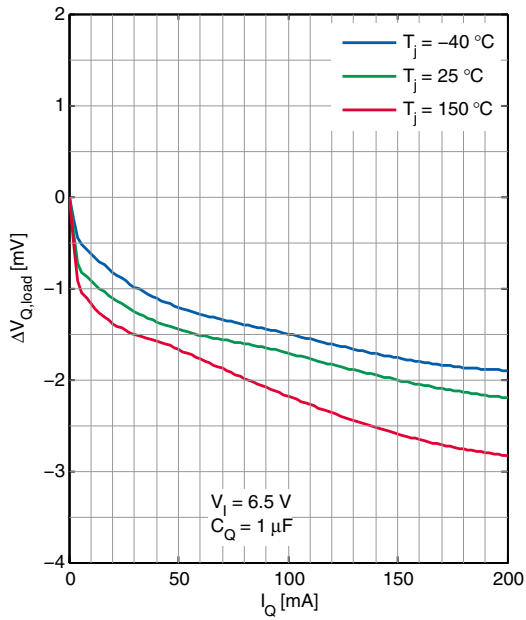


Equivalent series resistance of output capacitor $ESR(C_Q)$ versus output current I_Q

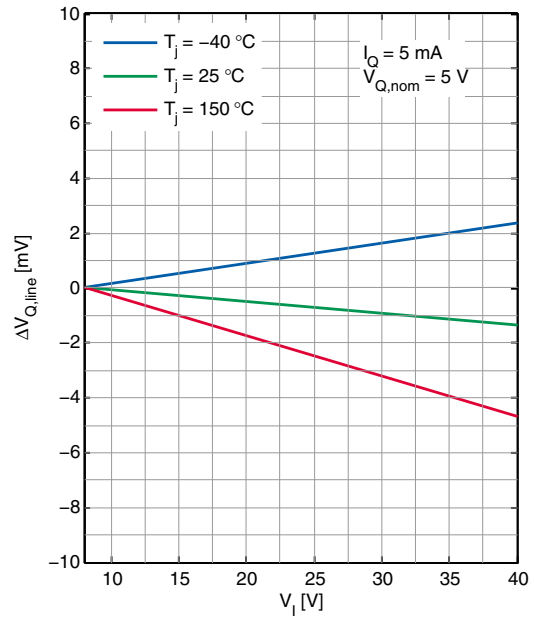


Block description and electrical characteristics

Load regulation $\Delta V_{Q,load}$ versus output current change I_Q



Line regulation $\Delta V_{Q,line}$ versus input voltage V_I



Block description and electrical characteristics

4.3 Current consumption

Table 5 Electrical characteristics current consumption

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$ (unless otherwise specified)

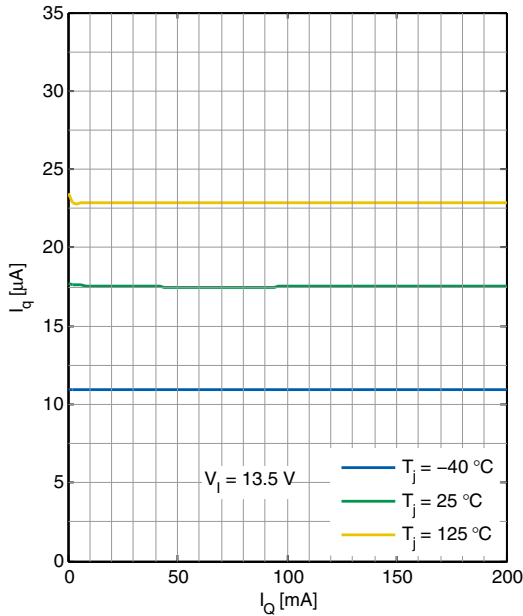
Typical values are given at $T_j = 25^\circ\text{C}$

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------|--------|------|------|---------------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Current consumption $I_q = I_I$ | $I_{q,off}$ | – | – | 1 | μA | $V_{EN} = 0\text{ V}; T_j < 105^\circ\text{C}$ | P_5.3.1 |
| Current consumption $I_q = I_I$ | $I_{q,off}$ | – | – | 2 | μA | $V_{EN} = 0.4\text{ V}; T_j < 125^\circ\text{C}$ | P_5.3.3 |
| Current consumption $I_q = I_I - I_Q$ | I_q | – | 17 | 25 | μA | $I_Q = 0.05\text{ mA}; T_j = 25^\circ\text{C}$ | P_5.3.4 |
| Current consumption $I_q = I_I - I_Q$ | I_q | – | 20 | 30 | μA | $I_Q = 0.05\text{ mA}; T_j < 125^\circ\text{C}$ | P_5.3.5 |
| Current consumption $I_q = I_I - I_Q$ | I_q | – | 22 | 33 | μA | ¹⁾ $I_Q = 200\text{ mA}; T_j < 125^\circ\text{C}$ | P_5.3.6 |

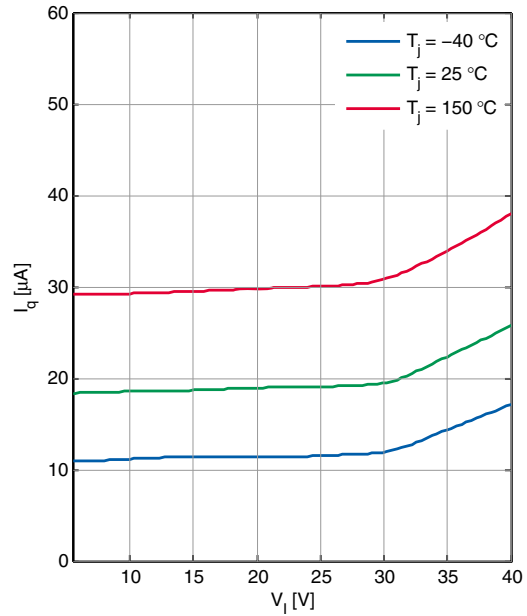
1) Not subject to production test, specified by design

4.4 Typical performance characteristics current consumption

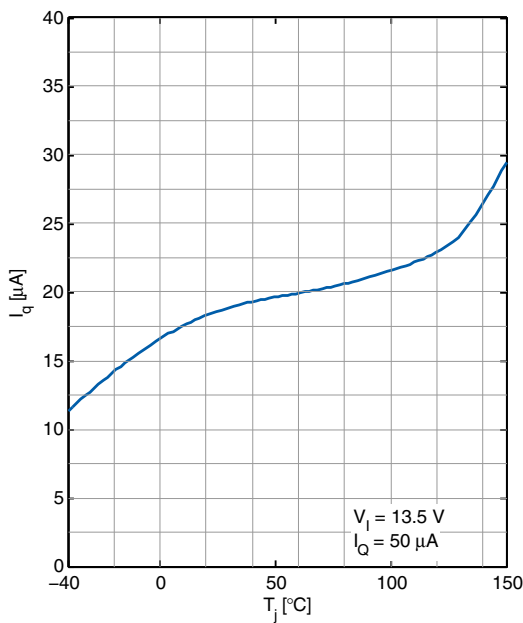
Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_i



Current consumption I_q versus junction temperature T_j



Block description and electrical characteristics

4.5 Enable

The TLS820B2ELVSE can be switched on and off by the enable feature. Applying a “high” level as specified below with $V_{EN} \geq 2\text{ V}$ to the EN pin enables the device. Applying a “low” level as specified below with $V_{EN} \leq 0.8\text{ V}$ shuts down the device. The enable feature has a built-in hysteresis to avoid toggling between the ON/OFF state, when a signal with slow slope is applied to the EN pin.

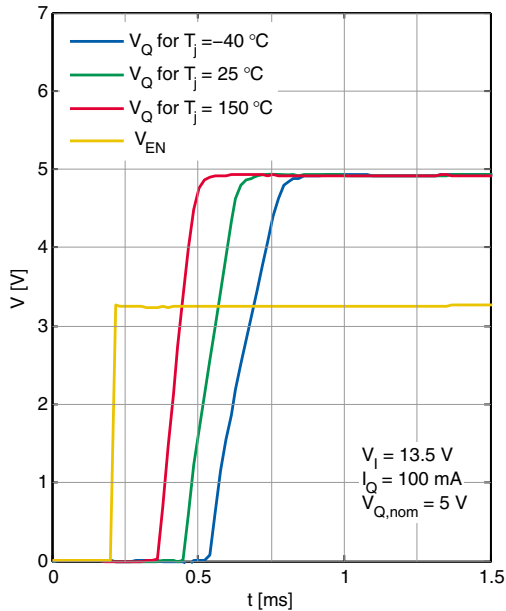
Table 6 Electrical characteristics enable

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified)
 Typical values are given at $T_j = 25^\circ\text{C}$

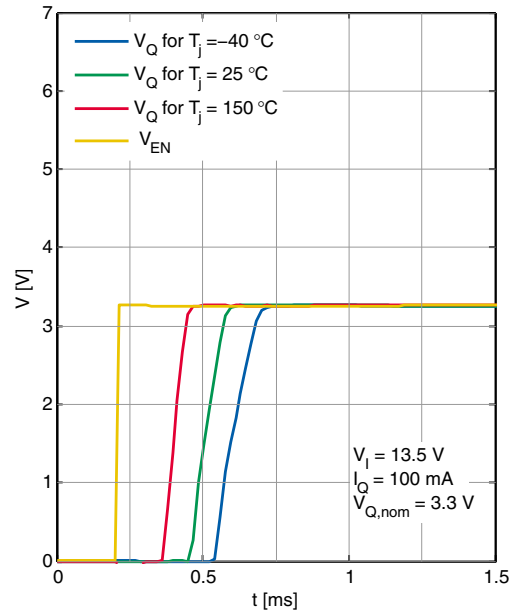
| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------------------|-------------|--------|------|------|------------------|---------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Enable “high” input voltage | $V_{EN,H}$ | 2 | – | – | V | – | P_5.5.1 |
| Enable “low” input voltage | $V_{EN,L}$ | – | – | 0.8 | V | – | P_5.5.2 |
| Enable threshold hysteresis | $V_{EN,Hy}$ | 90 | – | – | mV | – | P_5.5.3 |
| Enable “high” input current | $I_{EN,H}$ | – | – | 1 | μA | $V_{EN} = 5\text{ V}$ | P_5.5.4 |
| Enable “high” input current | $I_{EN,H}$ | – | – | 6 | μA | $V_{EN} \leq 18\text{ V}$ | P_5.5.5 |
| Enable internal pull-down resistor | R_{EN} | 2.8 | 10 | 20 | $\text{M}\Omega$ | – | P_5.5.6 |

4.6 Typical performance characteristics enable

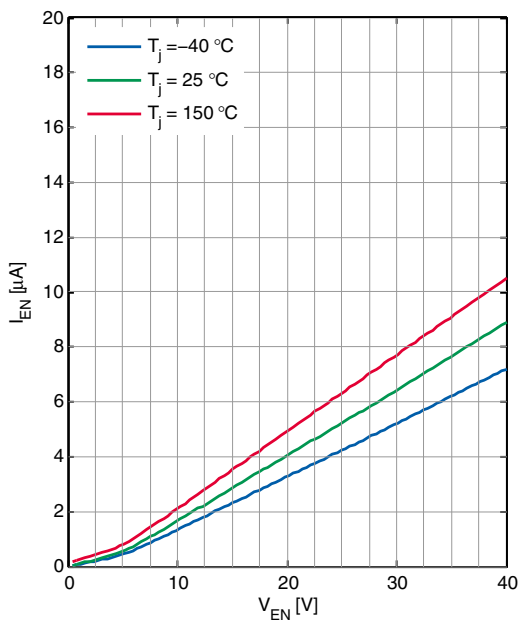
Output voltage V_Q versus time t (EN switched on)



Output voltage V_Q versus time t (EN switched on)



Enable input current I_{EN} versus enable input voltage V_{EN}



4.7 Output voltage selection

The output voltage V_Q of TLS820B2ELVSE can be selected by the SEL pin as follows:

SEL pin connected to Q: $V_Q = 5\text{ V}$;

SEL pin connected to GND: $V_Q = 3.3\text{ V}$.

Application information

5 Application information

5.1 Application diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

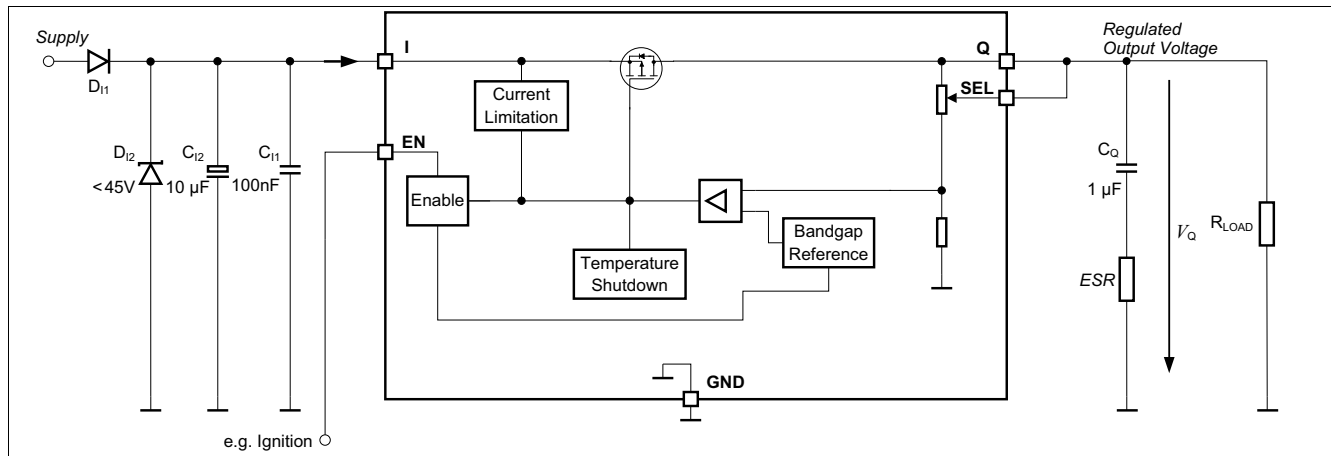


Figure 5 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

5.2 Selection of external components

5.2.1 Input pin

Figure 5 shows an example of the input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulses 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended to deal with possible external disturbances.

5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators. Furthermore it serves as an energy buffer during load jumps, to compensate and maintain a constant output voltage potential. It must be dimensioned according to the specific requirements of the application. The requirements for the output capacitor are given in **“Functional range” on Page 8**.

Application information

TLS820B2ELVSE is designed to also be stable with low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin and on the same side of the PCB as the regulator itself.

In case of input voltage or load current transients, the capacitance should be dimensioned accordingly. The configuration has to be verified in the real application to ensure that the output stability requirements are fulfilled.

5.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated as follows:

$$P_D = (V_I - V_Q)I_Q + V_I I_q \quad (5.1)$$

with

- P_D : continuous power dissipation
- V_I : input voltage
- V_Q : output voltage
- I_Q : output current
- I_q : quiescent current

The maximum acceptable thermal resistance R_{thJA} is given by:

$$R_{thJA} = \frac{T_{j,max} - T_a}{P_D} \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined by referencing the specification for **“Thermal resistance” on Page 9**.

5.4 Reverse polarity protection

TLS820B2ELVSE is not protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is necessary. The absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 7** must be maintained.

5.5 Further application information

For further information you may contact <https://www.infineon.com/>

Package information

6 Package information

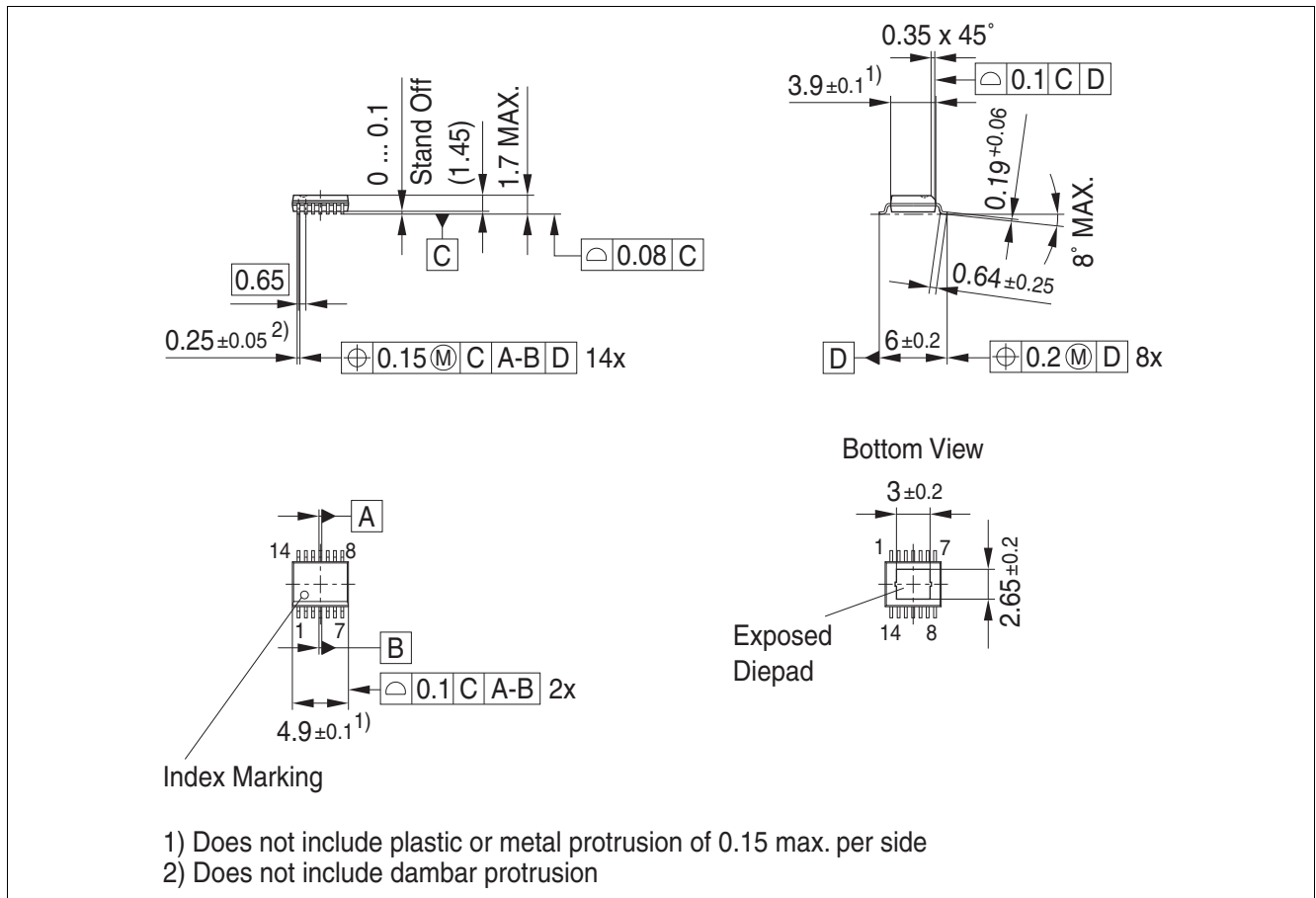


Figure 6 PG-SSOP-14¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

Revision history

7 Revision history

| Revision | Date | Changes |
|----------|------------|---|
| 1.1 | 2018-09-17 | Editorial changes Updated T to T_j in graph of “Equivalent series resistance of output capacitor $ESR(C_Q)$ versus output current I_Q ” Updated the output current range of typical performance graphs to reflect the maximum of $I_Q = 200$ mA |
| 1.0 | 2018-03-20 | Initial Version |

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.