

Enpirion EP53A8xQI DC/DC Converter Module Evaluation Board

Introduction

Thank you for choosing Altera Enpirion power products!

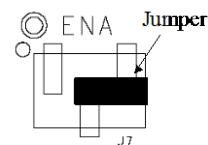
This application note describes how to test the EP53A8LQI and the EP53A8HQI converters using the Altera Enpirion EP53A8QI Eval Board shown in Fig. 1. In addition to this document you will also need the device datasheet for a thorough evaluation of the power converter module.

The EP53A8xQI converters are a complete power system on chip or PowerSoC.

- These devices are complete modules including magnetics, and require only ceramic input and output capacitors.
- The evaluation board is designed to offer a wide range of engineering evaluation capabilities. This includes the base configuration of a 0603 input capacitor and a 0805 output capacitor.
- Pads are available to add up to one additional input capacitor and one additional output capacitor for evaluation of performance over a wide range of input/output capacitor combinations.
- Pads are available to populate an external voltage divider (for feedback) if desired. The pads are labeled R1 and R2. Pads are also available for placing an optional feed-forward capacitor (labeled C9) across resistor R1 to modify the compensation.
- Jumpers are provided for easy programming of the following signals:
 - Enable
 - VS0-VS2 output voltage selection pins
- Test points are provided as well as clip leads for input and output connections
- The board comes with input decoupling, and input reverse polarity protection to safeguard the device from common setup mishaps.

Quick Start Guide

STEP 1: Set the “ENABLE” jumper to the Disable Position. Set VS0, VS1 and VS2 pins for the desired output setting.



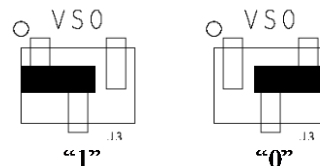
CAUTION: The signal pins ENA, VS0, VS1 and VS2 must be connected to a logic “high”, jumper to the left, or a logic “low”, jumper to the right. If left floating the state is indeterminate.

STEP 2: Connect a power supply to the input test points, TP8 (+) and TP5 (-) as indicated in Figure 1. The same test points can also be used to measure the input voltage.

CAUTION: Be mindful of the polarity and the voltage magnitude. If V_{IN} is greater than 6V, the board may get damaged. If the input voltage polarity is wrong, diode D1 will conduct, and draw excessive input current.

STEP 3: Set the output voltage select pins for the desired output voltage. Refer to Tables 1 and 2 to determine the setting.

CAUTION: The external resistor divider is not populated in the standard board configuration. Choosing the “EXT” option for the EP53A8LQI without the external resistors R1 and R2 will result in unpredictable behavior.



STEP 4: Connect the load to the output connectors TP7 (+) and TP6 (-), as indicated in Figure 1. The same test points are also used to measure the DC output voltage.

CAUTION: Please note the polarity of the output terminals is opposite from the input terminals.

STEP 5: Move the ENABLE jumper to the enabled position, and power up the board. The EP53A8xQI should now be operational.

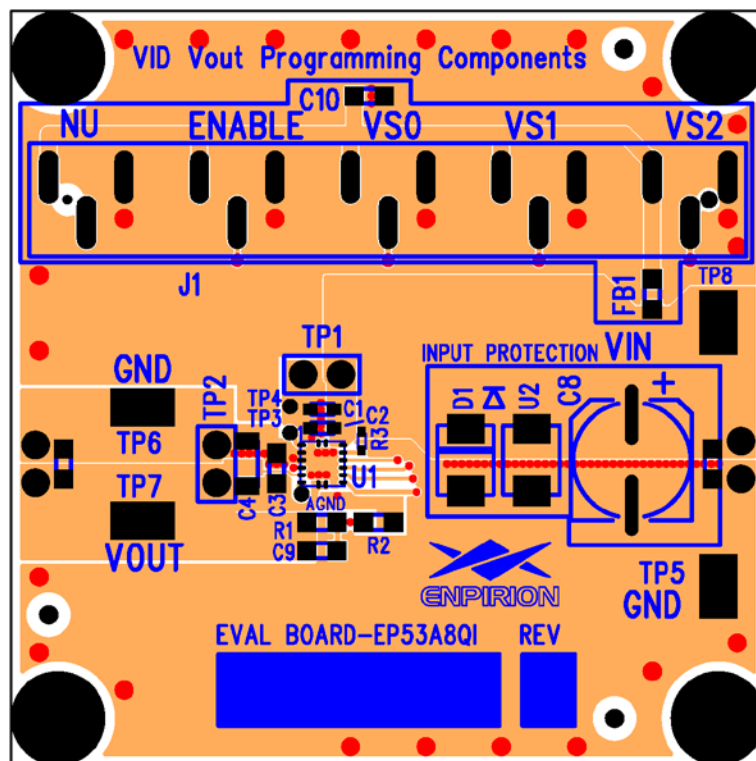


Figure 1. Evaluation Board Layout

Output Voltage Select

The EP53A8xQI utilizes a 3 pin output voltage select scheme. The output voltage is programmed by setting the VSx jumpers to either logic “1” or logic “0” as described in the Quick Start section. Tables 1 and 2 show the truth table for V_{OUT} selection. There are seven preset output voltage levels for the EP53A8LQI, and eight preset levels for the EP53A8HQI.

Table 1. EP53A8LQI Output Voltage Select Table

VS2	VS1	VS0	VOUT
0	0	0	1.50
0	0	1	1.45
0	1	0	1.20
0	1	1	1.15
1	0	0	1.10
1	0	1	1.05
1	1	0	0.8
1	1	1	EXT

Table 2. EP53A8HQI Output Voltage Select Table

VS2	VS1	VS0	VOUT
0	0	0	3.3
0	0	1	3.0
0	1	0	2.9
0	1	1	2.6
1	0	0	2.5
1	0	1	2.2
1	1	0	2.1
1	1	1	1.8

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a low-loop-inductance probe tip as shown in Figure 2, and through-hole test point pair TP2 to measure the output voltage ripple to avoid noise coupling into the probe ground lead. For more accurate ripple measurement, please refer to Enpirion Output Ripple Measurement Methods Application Note (www.altera.com/enpirion).

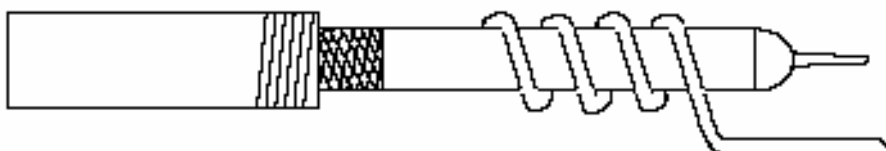


Figure 2: Balanced-impedance oscilloscope probe. Wrap bare wire around the ground shaft and bring the wire close to the probe tip. This minimizes probe loop inductance and stray noise pickup by the probe.

Please contact Power Applications support (www.altera.com/mysupport) for any questions regarding this evaluation board.

Using the External Voltage Divider

The EP53A8xQI evaluation board is designed to provide a great deal of flexibility in evaluating the performance of the Altera Enpirion DC/DC module.

Pre-tinned pads are provided to place 0805 sized resistors on the board to implement an external resistor divider for the EP53A8LQI to choose an output voltage other than one of the pre-set voltages available on the VID. See Figure 3 for the basic circuit.

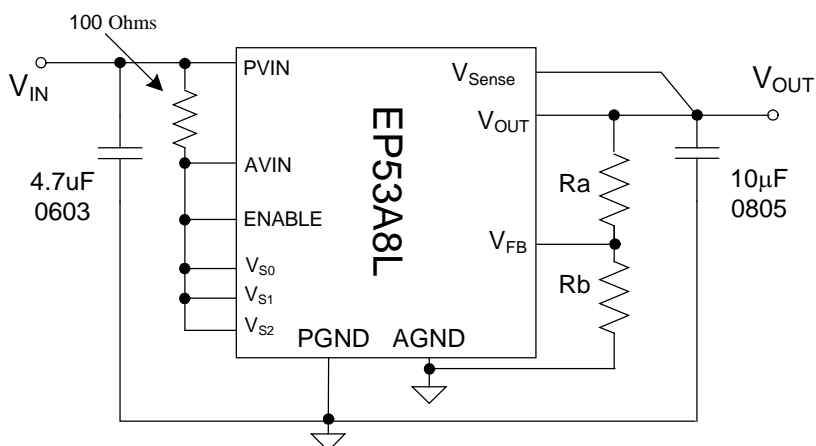


Figure 3. External divider schematic for the EP53A8LQI

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V \left(1 + \frac{R_a}{R_b} \right)$$

R_a must be chosen as 237k Ω to maintain control loop stability. Then R_b is given as:

$$R_2 = \frac{142.2 \times 10^3}{V_{OUT} - 0.6} \Omega$$

The external voltage divider option is chosen by setting the jumpers VS0 – VS3 to logic “high”.

Dynamically Adjustable Output

The EP53A8xQI is designed to allow for dynamic switching between the predefined voltage levels by toggling the VID pins. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is defined in the datasheet.

This feature can be tested by connecting the VSx jumper center pins to logic driver to toggle between the various V_{OUT} states.

Evaluation Board Schematic

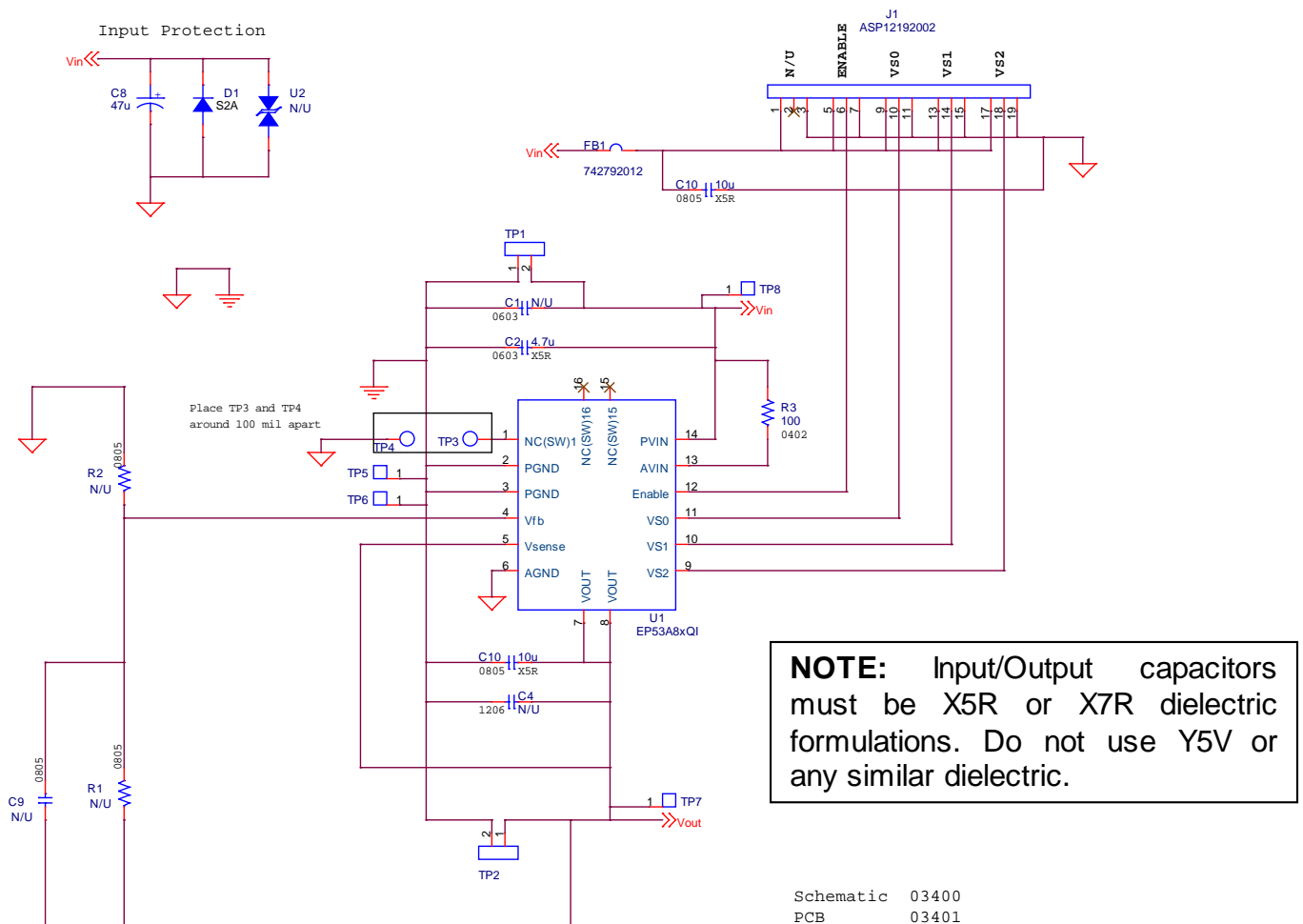


Figure 4: EP53A8xQI Evaluation Board Schematic



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