

2.7V to 5.5V Input, Integrated 3A MOSFET 1ch Synchronous Buck DC/DC Converter





BD9A300MUV

Description

BD9A300MUV is a synchronous buck switching regulator with built-in low On-resistance power MOSFETs. It is capable of providing current up to 3A. The SLLMTM control provides excellent efficiency characteristics in light-load conditions which make the product ideal for equipment and devices that demand minimal standby power consumption. The oscillating frequency is high at 1MHz using a small value of inductance. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Features

- Synchronous 1 ch DC/DC converter
- I SLLM[™] (Simple Light Load Mode) control
- Over Current Protection
- Short Circuit Protection
- Thermal Shutdown protection
- Under Voltage lockout protection
- Adjustable soft start function
- Power Good output
- VQFN016V3030 package (backside heat dissipation)

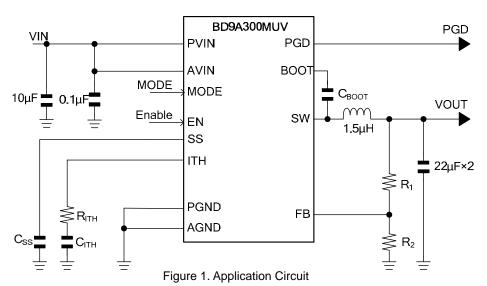
Applications

- Step-down power supply for DSPs, FPGAs, microprocessors, etc.
- Laptop PCs/ tablet PCs/ servers
- LCD TVs
- Storage devices (HDDs/SSDs)
- Printers, OA equipment
- Entertainment devices
- Distributed power supply, secondary power supply

Typical Application Circuit

- Key Specifications
 Input voltage range: 2.7V to 5.5V
 Output voltage range: 0.8V to V_{PVIN} x 0.7V
 Output current: 3A (Max.)
 Switching frequency: 1MHz (Typ.)
 High-Side MOSFET On-Resistance: 60mΩ (Typ.)
 Low-Side MOSFET On-Resistance: 60mΩ (Typ.)
 Standby current: 0µA (Typ.)
- Package
 VQFN016V3030
 W (Typ.) x D (Typ.) x H (Max.)
 3.00mm x 3.00mm x 1.00mm





Pin Configuration

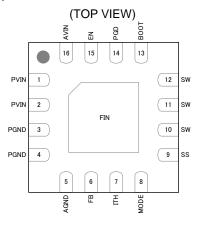


Figure 2. Pin Assignment

Pin Descriptions

Pin No.	Symbol	Description					
1, 2	PVIN	Power supply terminals for the switching regulator. These terminals supply power to the output stage of the switching regulator. Connecting a 10µF ceramic capacitor is recommended.					
3, 4	PGND	Ground terminals for the output stage of the switching regulator.					
5	AGND	Ground terminal for the control circuit.					
6	FB	An inverting input node for the gm error amplifier. See page 23 for how to calculate the resistance of the output voltage setting.					
7	ITH	An input terminal for the gm error amplifier output and the output switch current comparator. Connect a frequency phase compensation component to this terminal. See page 24 for how to calculate the resistance and capacitance for phase compensation.					
8	MODE	urning this terminal signal Low (0.2V or lower) forces the device to operate in the fixed equency PWM mode. Turning this terminal signal High (0.8V or higher) enables the SLLM ontrol and the mode is automatically switched between the SLLM control and fixed equency PWM mode.					
9	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified b connecting a capacitor to this terminal. See page 23 for how to calculate the capacitance.					
10, 11, 12	SW	Switch nodes. These terminals are connected to the source of the High-Side MOSFET and drain of the Low-Side MOSFET. Connect a bootstrap capacitor of $0.1\mu F$ between these terminals and BOOT terminals. In addition, connect an inductor of $1.5\mu H$ considering the direct current superimposition characteristic.					
13	воот	Connect a bootstrap capacitor of 0.1µF between this terminal and SW terminals. The voltage of this capacitor is the gate drive voltage of the High-Side MOSFET.					
14	PGD	A "Power Good" terminal, an open drain output. Use of pull up resistor is needed. See page 18 for how to specify the resistance. When the FB terminal voltage reaches within ±7% of 0.8V (typ.), the internal Nch MOSFET turns off and the output turns High.					
15	EN	Turning this terminal signal Low (0.8V or lower) forces the device to enter the shutdown mode. Turning this terminal signal High (2.0V or higher) enables the device. This terminal must be terminated.					
16	AVIN	Supplies power to the control circuit of the switching regulator. Connecting a 0.1µF ceramic capacitor is recommended.					
-	FIN	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using multiple vias provides excellent heat dissipation characteristics.					

Block Diagram

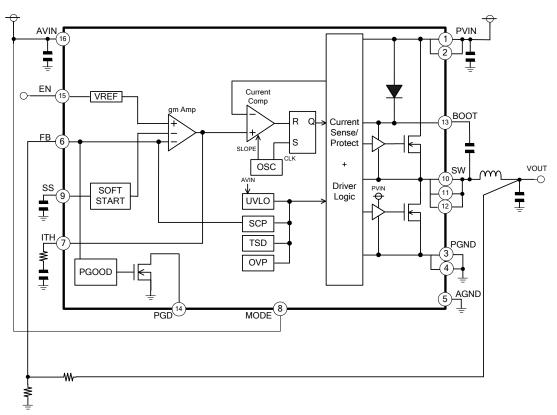


Figure 3. Block Diagram

Description of Blocks

VREF

The VREF block generates the internal reference voltage.

UVLO

The UVLO block is for Under Voltage lockout protection. It will shut down the IC when the VIN falls to 2.45V (typ.) or lower. The threshold voltage has a hysteresis of 100mV (typ.).

SCP

After the soft start is completed and when the feedback voltage of the output voltage has fallen below 0.4V (typ.) for 1msec (typ.), the SCP stops the operation for 16msec (typ.) and subsequently initiates restart.

OVP

Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 0.88V (typ.) it turns MOSFET of output part MOSFET OFF. After output voltage drop it returns with hysteresis.

TSD

The TSD block is for thermal protection. The thermal protection circuit shuts down the device when the internal temperature of IC rises to 175°C (typ.) or higher. Thermal protection circuit resets when the temperature falls. The circuit has a hysteresis of 25°C (typ.).

SOFT START

The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. A built-in soft start function is provided and a soft start is initiated in 1msec (typ.) when the SS terminal is open.

• gmAmp

The gmAmp block compares the reference voltage with the feedback voltage of the output voltage. The error and the ITH terminal voltage determine the switching duty. A soft start is applied at startup. The ITH terminal voltage is limited by the internal slope voltage.

Current Comp

The Current Comp block compares the output ITH terminal voltage of the error amplifier and the slope block signal to determine the switching duty. In the event of over current, the current that flows through the High-Side MOSFET is limited at each cycle of the switching frequency.

• OSC

This block generates the oscillating frequency.

• DRIVER LOGIC

This block is a DC/DC driver. A signal from Current Comp is applied to drive the MOSFETs.

• PGOOD

When the FB terminal voltage reaches within ±7% of 0.8V (typ.), the Nch MOSFET of the built-in open drain output turns off and the output turns High.

■ Absolute Maximum Ratings (Ta = 25°C)

2001010 111001111111111190 (110	/		
Parameter	Symbol	Rating	Unit
Supply Voltage	V _{PVIN} , V _{AVIN}	-0.3 to +7	V
EN Voltage	V _{EN}	-0.3 to +7	V
MODE Voltage	V _{MODE}	-0.3 to +7	V
PGD Voltage	V_{PGD}	-0.3 to +7	V
Voltage from GND to BOOT	V _{воот}	-0.3 to +7	V
Voltage from SW to BOOT	∠V _{BOOT}	-0.3 to +7	V
FB Voltage	V _{FB}	-0.3 to +7	V
ITH Voltage	V _{ITH}	-0.3 to +7	V
SW Voltage	Vsw	-0.3 to V _{PVIN} + 0.3	V
Output Current	I _{OUT}	3.5	Α
Allowable Power Dissipation	Pd	2.66 ^{*1}	W
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

^{*1} When mounted on a 70mm x 70mm x 1.6mm 4-layer glass epoxy board (copper foil area: 70 mm x 70 mm) Derate by 21.3mW when operating above 25°C.

Recommended Operating Range

Parameter	Symbol		Unit		
Faiametei	Symbol	Min	Тур	Max	Offic
Supply Voltage	V _{PVIN} , V _{AVIN}	2.7	-	5.5	V
Output Current	Іоит	-	-	3	Α
Output Voltage Range	V _{RANGE}	0.8	-	V _{PVIN} × 0.7	V

• Electrical Characteristics

(Ta = 25°C, $V_{AVIN} = V_{PVIN} = 5 V$, $V_{EN} = 5 V$ unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions	
Farameter	Symbol	Min	Тур	Max	Offic	Conditions	
<avin pin=""></avin>							
Standby Supply Current	I _{STB}	-	0	10	μΑ	EN = GND	
Operating Supply Current	Icc	1	350	500	μΑ	IOUT = 0 mA Non-switching	
UVLO Detection Voltage	V _{UVLO1}	2.35	2.45	2.55	V	V _{IN} falling	
UVLO Release Voltage	V_{UVLO2}	2.425	2.55	2.7	V	V _{IN} rising	

			Limits			Conditions
Parameter	Symbol	Min	Тур	Max	Unit	
<enable></enable>						
EN Input High Level Voltage	V_{ENH}	0.8	1.5	2.0	V	
EN Input Low Hysteresis Voltage	V _{ENL}	100	200	300	mV	
EN Input Current	I _{EN}	-	5	10	μΑ	EN = 5 V
<mode></mode>						
MODE Input High Level Voltage	V_{MODEH}	0.2	0.4	0.8	V	
MODE Input Current	I _{MODE}	-	10	20	μΑ	MODE=5V
<reference amplifier="" error="" voltage,=""></reference>						
FB Terminal Voltage	V_{FB}	0.792	0.8	0.808	V	
FB Input Current	I _{FB}	-	0	1	μΑ	FB = 0.8V
ITH Sink Current	I _{THSI}	10	20	40	μΑ	FB = 0.9 V
ITH Source Current	I _{THSO}	10	20	40	μΑ	FB = 0.7 V
Soft Start Time	T _{SS}	0.5	1.0	2.0	ms	With internal constant
Soft Start Current	I _{SS}	0.9	1.8	3.6	μΑ	
<frequency generation=""></frequency>						
Switching Frequency	Fosc	800	1000	1200	kHz	
<power good=""></power>						
Falling (Fault) Voltage	V_{PGDFF}	87	90	93	%	FB falling V _{PGDFF} = FB/VFB x 100
Rising (Good) Voltage	V_{PGDRG}	90	93	96	%	FB rising V _{PGDRG} = FB/VFB x 100
Rising (Fault) Voltage	V_{PGDRF}	107	110	113	%	FB rising V _{PGDRF} = FB/VFB x 100
Falling (Good) Voltage	V_{PGDFG}	104	107	110	%	FB falling V _{PGDFG} = FB/VFB x 100
PGD Output Leakage Current	I_{LKPGD}	-	0	5	μΑ	PGD = 5 V
Power Good ON Resistance	R_{PGD}	-	100	200	Ω	
Power Good Low Level Voltage	P _{GDVL}	-	0.1	0.2	V	I _{PGD} = 1mA
<sw></sw>					<u> </u>	
High Side FET ON Resistance	R _{ONH}	-	60	120	mΩ	BOOT - SW = 5 V
Low Side FET ON Resistance	R _{ONL}	-	60	120	mΩ	
High Side Output Leakage Current	R _{ILH}	-	0	10	μA	Non-switching
Low Side Output Leakage Current	R _{ILL}	-	0	10	μA	Non-switching
<scp></scp>						
Short Circuit Protection Detection Voltage	V _{SCP}	0.28	0.4	0.52	V	

Typical Performance Curves

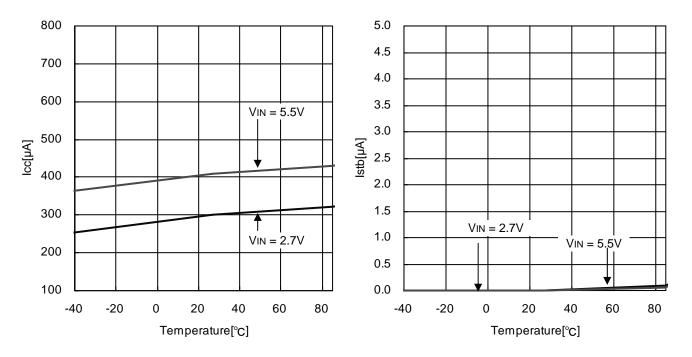


Figure 4. Operating Current - Temperature

Figure 5. Stand-by Current - Temperature

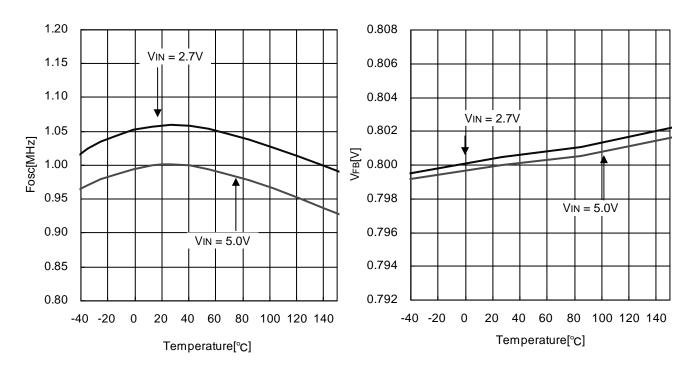


Figure 6. Switching Frequency - Temperature

Figure 7. FB Voltage Reference - Temperature

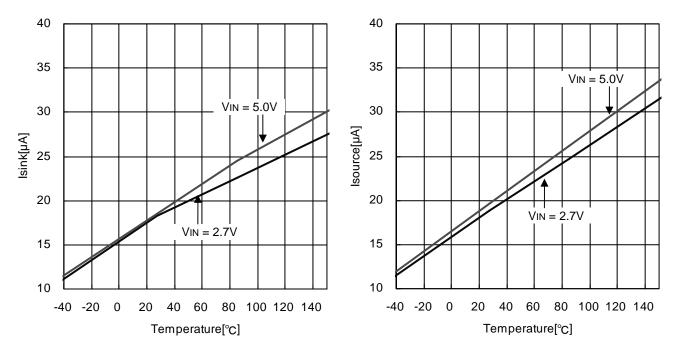


Figure 8. ITH Sink Current - Temperature

Figure 9. ITH Source Current - Temperature

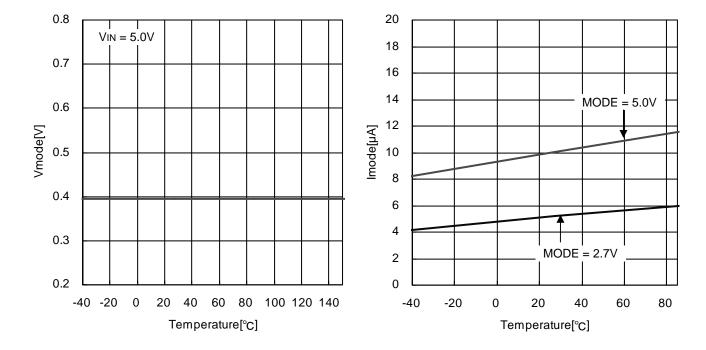
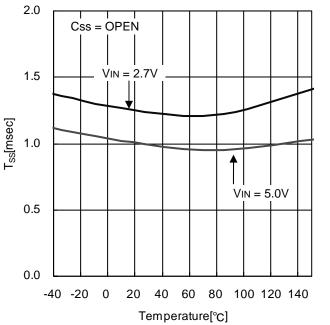


Figure 10. Mode Threshold - Temperature

Figure 11. Mode Input Current - Temperature



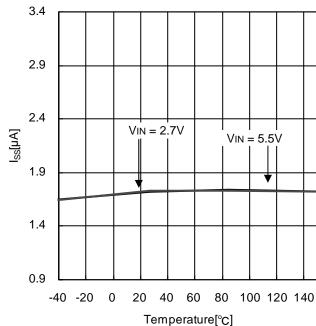


Figure 12. Soft Start Time - Temperature

Figure 13. Soft Start Terminal Current - Temperature

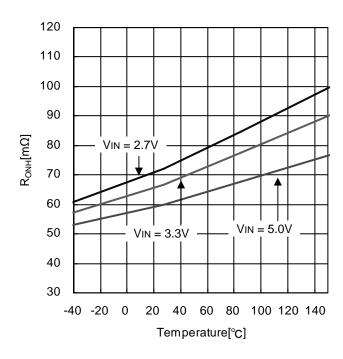


Figure 14. High side FET ON-Resistance - Temperature

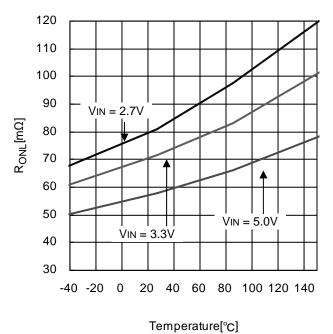
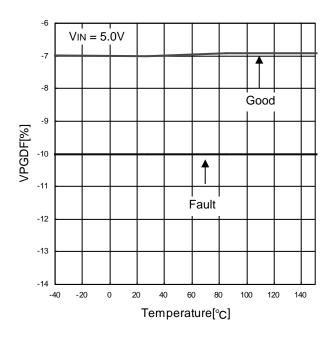


Figure 15. Low side FET ON-Resistance - Temperature



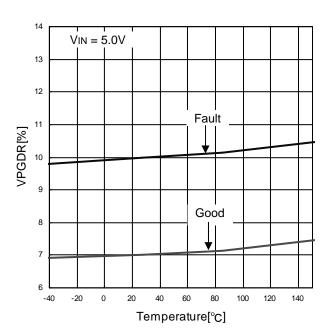
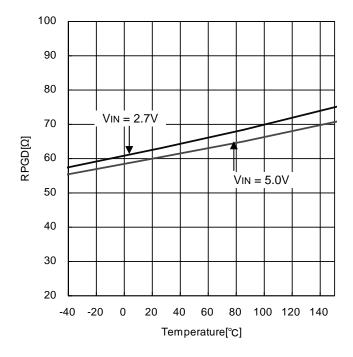


Figure 16. PGD Falling Voltage - Temperature

Figure 17. PGD Rising Voltage - Temperature





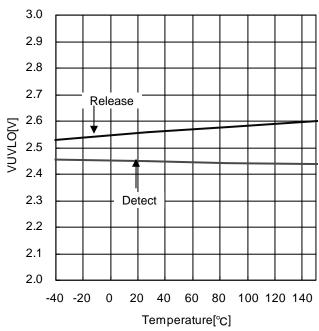
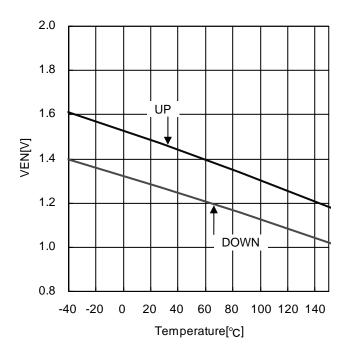


Figure 19. UVLO Threshold - Temperature



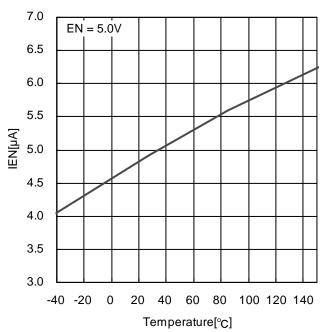


Figure 20. EN Threshold - Temperature

Figure 21. EN Input Current - Temperature

● Typical Performance Curves (Application)

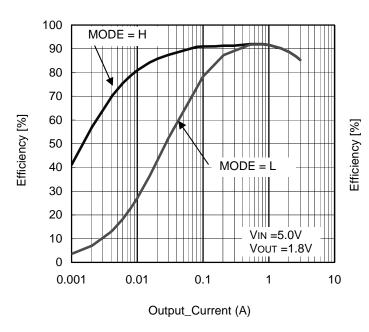


Figure 22. Efficiency – Output Current (VIN=5V, VOUT=1.8V, L=1.5µH)

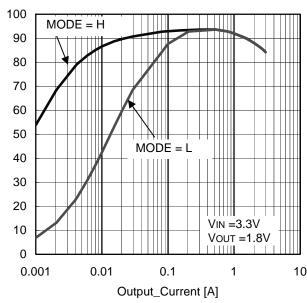


Figure 23. Efficiency – Output Current (VIN=3.3V, VOUT=1.8V, L=1.5µH)

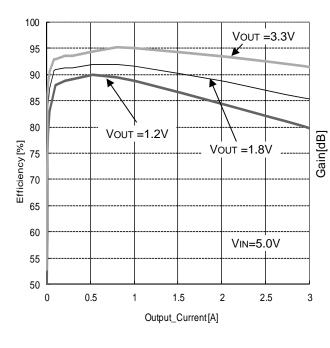


Figure 24. Efficiency – Output Current (VIN = 5.0V, MODE = 5.0V, L=1.5µH)

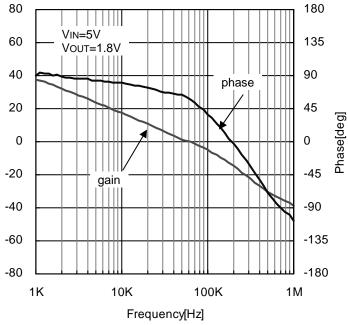


Figure 25. Loop Response (VIN=5V, VOUT=1.8V, IOUT=1A, L=1.5 μ H, C_{OUT}=Ceramic44 μ F)

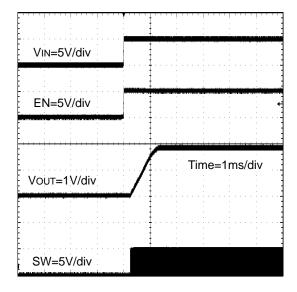


Figure 26. Power Up (VIN = EN)

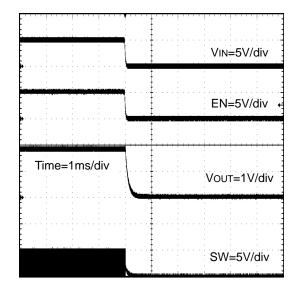


Figure 27. Power Down (VIN = EN)

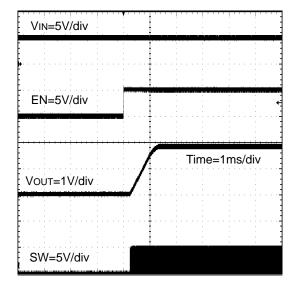


Figure 28. Power Up (EN = $0V\rightarrow5V$)

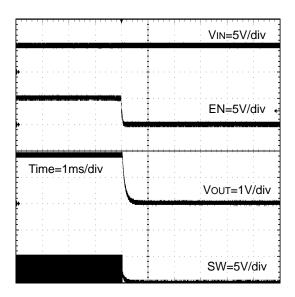


Figure 29. Power Down (EN = $5V \rightarrow 0V$)

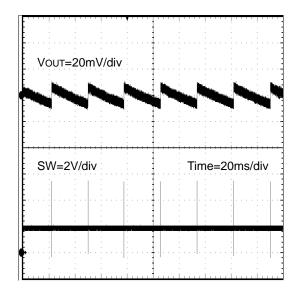


Figure 30. Vout Ripple ($V_{IN} = 5V$, $V_{OUT} = 1.8V$, $I_{OUT} = 0A$)

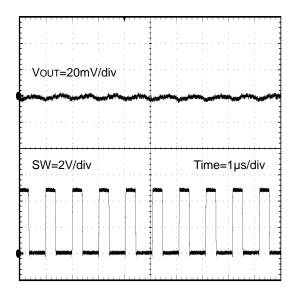


Figure 31. Vout Ripple $(V_{IN} = 5V, Vout = 1.8V, Iout = 3A)$

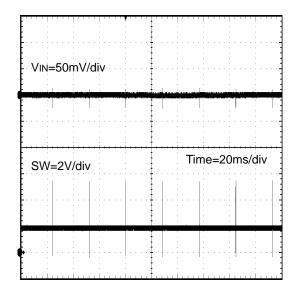


Figure 32. VIN Ripple $(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A)$

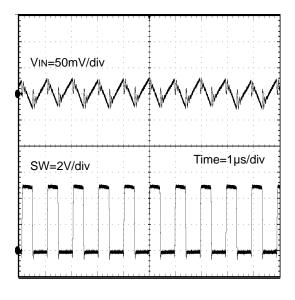


Figure 33. VIN Ripple $(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)$

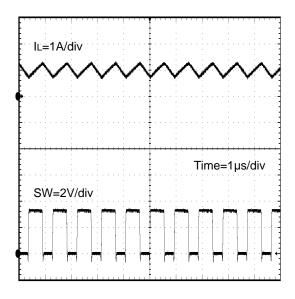


Figure 34. Switching Waveform (VIN = 3.3V, VOUT = 1.8V, IOUT = 1A, L=1.5uH)

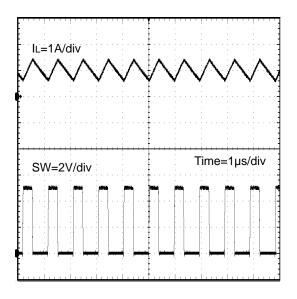


Figure 35. Switching Waveform (VIN = 5.0V, VOUT = 1.8V, IOUT = 1A, L=1.5uH)

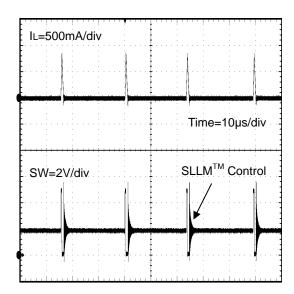


Figure 36. Switching Waveform (VIN = 3.3V, VOUT = 1.8V, IOUT = 30mA, L=1.5uH)

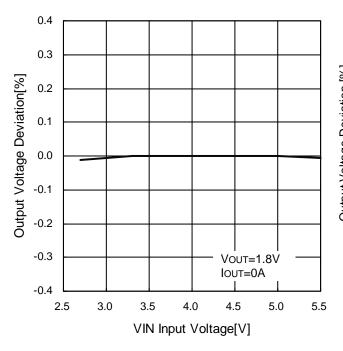


Figure 37. Vout Line Regulation (Vout = 1.8V)

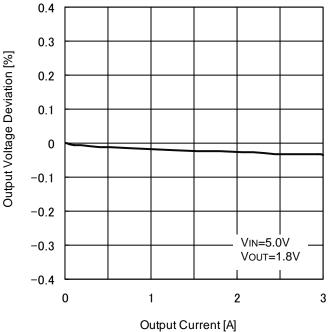


Figure 38. Vout Load Regulation (Vout = 1.8V)

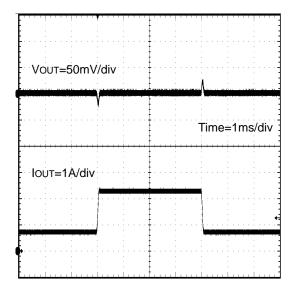


Figure 39. Load Transient Response Iout=0.75A – 2.25A (VIN=5V, VOUT=1.8V, COUT=Ceramic44μF)

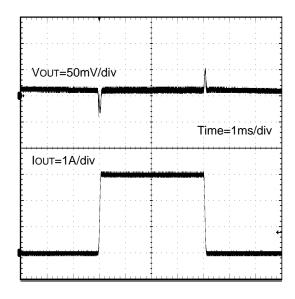


Figure 40. Load Transient Response Iout=0A - 3A (VIN=5V, VOUT=1.8V, COUT=Ceramic44µF)

1 Function Explanations

1-1 DC/DC converter operation

BD9A300MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) control for lighter load to improve efficiency.

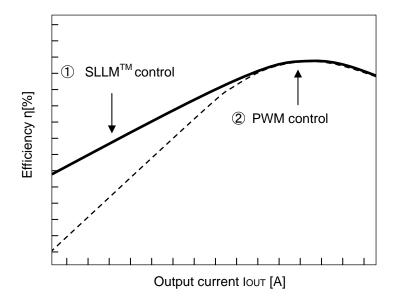


Figure 41. Efficiency (SLLMTM control and PWM control)

①SLLM[™] control

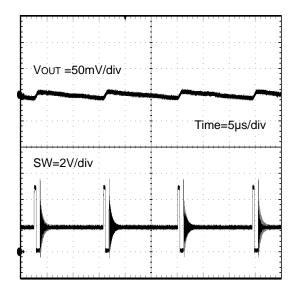


Figure 42. SW Waveform (①SLLMTM control) $(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=50mA)$

2PWM control

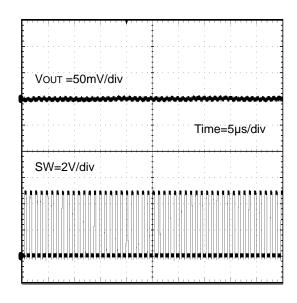


Figure 43. SW Waveform (?PWM control) (V_{IN} =5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A)

1-2 Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When VEN reaches 2.0V (typ.), the internal circuit is activated and the IC starts up. To enable shutdown control with the EN terminal, the shutdown interval (Low level interval of EN) must be set to 100µs or longer.

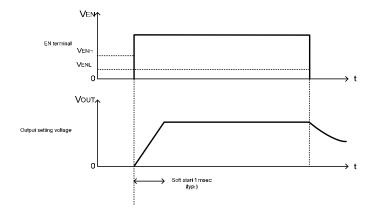


Figure 44. Start Up and Down with Enable

1-3 Power Good Function

When the output voltage reaches outside $\pm 10\%$ of the voltage setting, the open drain NMOSFET internally connected to the PGD terminal turns on and the PGD terminal is pulled down with an impedance of 100Ω (typ.). A hysteresis of 3% applies to resetting. Connecting a pull up resistor $(10k\Omega$ to $100k\Omega$) is recommended.

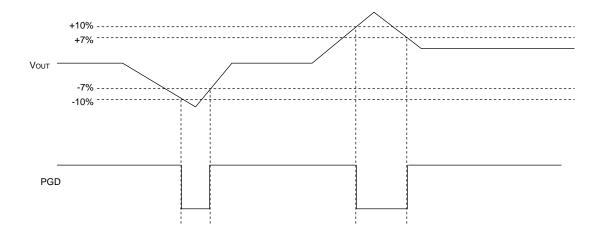


Figure 45. PGD Timing Chart

2 Protective Functions

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

2-1 Short Circuit Protection Function (SCP)

The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.4V (typ.) and remained there for 1msec (typ.), SCP stops the operation for 16msec (typ.) and subsequently initiates a restart.

EN Terminal	FB Terminal	Short Circuit Protection Function	Short Circuit Protection Operation
2.0\/ or higher	< 0.4V (Typ.)	Enabled	ON
2.0V or higher	> 0.4V (Typ.)	Enabled	OFF
0.8V or lower -		Disabled	OFF

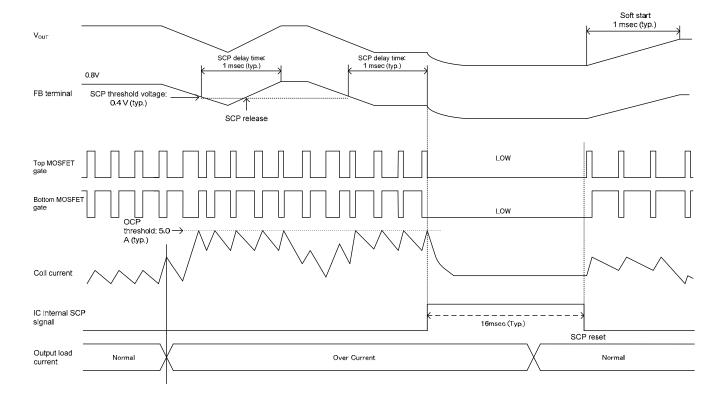


Figure 46. Short Circuit Protection function (SCP) timing chart

2-2 Under Voltage Lockout Protection (UVLO)

The Under Voltage Lockout Protection circuit monitors the AVIN terminal voltage. The operation enters standby when the AVIN terminal voltage is 2.45V (typ.) or lower. The operation starts when the AVIN terminal voltage is 2.55V (typ.) or higher.

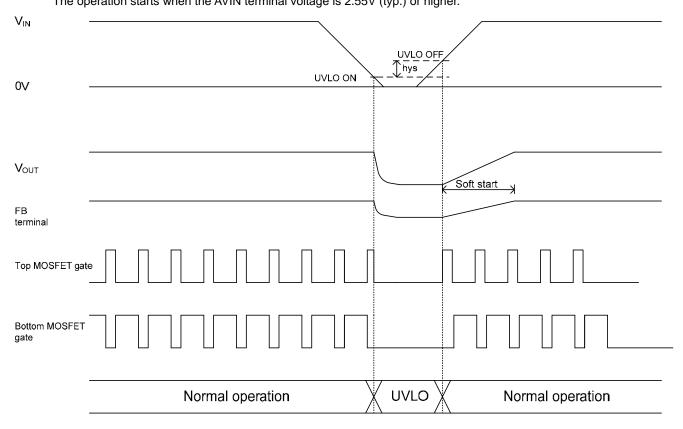


Figure 47. UVLO Timing Chart

2-3 Thermal Shutdown Function

When the chip temperature exceeds $Tj = 175^{\circ}C$, the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding $Tjmax = 150^{\circ}C$. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

2-4 Over Current Protection Function

The Over Current Protection function operates by using the current mode control to limit the current that flows through the High-Side MOSFET at each cycle of the switching frequency. The designed over current limit value is 6.0A (typ.).

2-5 Over Voltage Protection Function (OVP)

Over voltage protection function (OVP) compares FB terminal voltage with internal standard voltage VREF and when FB terminal voltage exceeds0.88V (typ.) it turns MOSFET of output part MOSFET OFF. After output voltage drop it returns with hysteresis.

Application Example

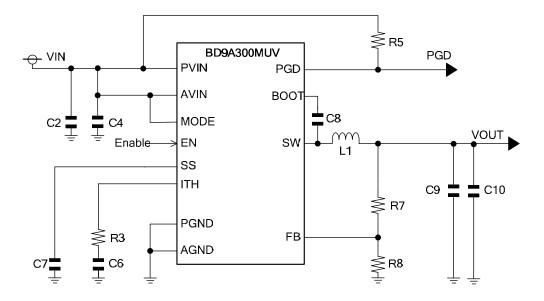


Figure 48. Application Circuit

Table 1. Recommendation Circuit constants

Part Number			Vout			Description
Part Number	1.1V	1.2V	1.5V	1.8V	3.3V	Description
R3	8.2 kΩ	8.2 kΩ	9.1 kΩ	9.1 kΩ	18 kΩ	-
R5	100 kΩ	-				
R7	10 kΩ	10 kΩ	16 kΩ	30 kΩ	75 kΩ	-
R8	27 kΩ	20 kΩ	18 kΩ	24 kΩ	24 kΩ	-
C2	10µF	10µF	10µF	10µF	10µF	10V, X5R, 1206
C4	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	25V, X5R, 0603
C6	2700pF	2700pF	2700pF	2700pF	2700pF	-
C7	0.01µF	0.01µF	0.01µF	0.01µF	0.01µF	-
C8	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	-
C9	22µF	22µF	22µF	22µF	22µF	10V, X5R, 1210
C10	22µF	22µF	22µF	22µF	22µF	10V, X5R, 1210
L1	1.5µH	1.5µH	1.5µH	1.5µH	1.5µH	TOKO, FDSD0630

Selection of Components Externally Connected

(1) Output LC Filter Constant

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. BD9A300MUV is returned to the IC and IL ripple current flowing through the inductor for SLLM TM control. This feedback current, Inductance value is the behavior of the best when the 1.5 μ H. Therefore, the inductor to use is recommended 1.5 μ H.

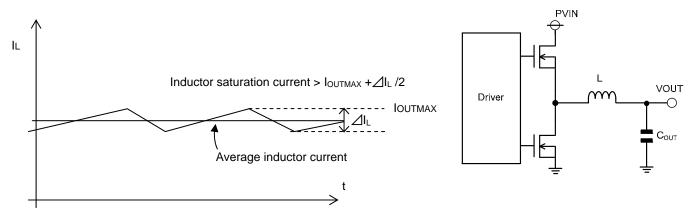


Figure 49. Waveform of current through inductor

Figure 50. Output LC filter circuit

Computation with VIN = 5V, VOUT = 1.8V, $L=1.5\mu H$, and the switching frequency $F_{OSC} = 1MHz$, the method is as below.

Inductor ripple current ⊿IL

$$\triangle$$
IL = $V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} = 768 \text{ [mA]}$

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L .

The output capacitor C_{OUT} affects the output ripple voltage characteristics. The output capacitor C_{OUT} must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta VRPL = \Delta IL \times (RESR + \frac{1}{8 \times Cout \times Fosc}) [V]$$

 R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor. With $Cout = 44\mu$ F, $Resr = 10m\Omega$ the output ripple voltage is calculated as

$$\triangle VRPL = 0.768 \times (10m + 1 / (8 \times 44 \mu \times 1MHz)) = 9.8[mV]$$

*Be careful of total capacitance value, when additional capacitor CLOAD is connected in addition to output capacitor COUT. Use maximum additional capacitor CLOAD(max.) condition which satisfies the following method.

Maximum starting inductor ripple current lLSTART < Over Current limit 3.8A (min.)

Maximum starting inductor ripple current llstart can be expressed in the following method.

ILSTART = Maximum starting output current (IOMAX) + Charge current to output capacitor(ICAP) + $\frac{\angle IIL}{2}$ Charge current to output capacitor ICAP can be expressed in the following method.

$$ICAP = \frac{(COUT + CLOAD) \times VOUT}{TSS} [A]$$

Computation with VIN = 5V, VOUT = 3.3V, $L = 1.5\mu H$, switching frequency Fosc= 800kHz (min.), Output capacitor $COUT = 44\mu F$, Soft Start time Tss = 0.5ms (min.), Load Current during Soft Start loss = 2A the method is as below.

CLOAD (max.)
$$< \frac{(3.8 - loss - \Delta lL/2) \times Tss}{Vout} - Cout = 157.9 [\mu F]$$

If the value of CLOAD is large, and can not meet the above equation,

CLOAD (max.)
$$< \frac{(3.8 - loss - $\triangle lL/2) \times VFB}{Vout \times lss} \times Css$ — Cout$$

Please adjust the value of the capacitor Css to meet the above formula.

(Please refer to the following items (3) Soft Start Setting equation of time Tss and soft-start value of the capacitor to be connected to the Css.)

Computation with VIN = 5V, VOUT = 3.3V, L = 1.5 μ H, Load Current during Soft Start Ioss = 2A, switching frequency Fosc= 800kHz (min.), Output capacitor COUT = 44 μ F, VFB = 0.792V(max.), Iss = 3.6 μ A(max.), A capacitor connected to the Css if you want to connect the CLOAD = 220 μ F is the following equation.

Css >
$$\frac{\text{Vout} \times \text{Iss}}{(3.8 - \text{loss} - \triangle \text{IL}/2) \times \text{VFB}} \times (\text{CLOAD} + \text{Cout}) = 2.97 [nF]$$

(2) Output Voltage Setting

The output voltage value can be set by the feedback resistance ratio.

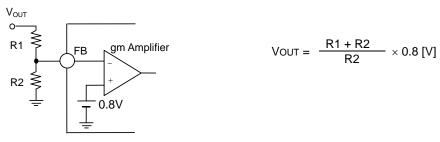


Figure 51. Feedback Resistor Circuit

(3) Soft Start Setting

Turning the EN terminal signal High activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

Tss = (Css x V_{FB}) / Iss

Tss: Soft Start Time

Css: Capacitor connected to Soft Start Time Terminal

VFB: FB Terminal Voltage (0.8V (Typ.))

Iss: Soft Start Terminal Source Current (1.8µA (Typ.))

With CSS = 0.01
$$\mu$$
F,
Tss = (0.010[μ F] x 0.8[V]) / 1.8[μ A]
= 4.44[msec]

Turning the EN terminal signal High with the SS terminal open (no capacitor connected) or with the terminal signal High causes the output voltage to rise in 1 msec (typ.).

(4) Phase Compensation Component

A current mode control buck DC/DC converter is a two-pole, one-zero system. Two poles are formed by an error amplifier and load and the one zero point is added by phase compensation. The phase compensation resistor R_{ITH} determines the crossover frequency F_{CRS} where the total loop gain of the DC/DC converter is 0dB. A high value crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, a low value crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired. Here, select the constant so that the crossover frequency F_{CRS} will be 1/20 of the switching frequency.

(i) Selection of Phase Compensation Resistor RITH

The Phase Compensation Resistance R_{ITH} can be determined by using the following equation.

RITH =
$$\frac{2\pi \text{ x Vout x Fcrs x Cout}}{\text{V}_{\text{FB}} \text{ x GMP x GMA}} [\Omega]$$

V_{OUT}: Output Voltage F_{CRS}: Crossover Frequency C_{OUT}: Output Capacitance

 V_{FB} : Feedback Reference Voltage (0.8 V (Typ.))

G_{MP}: Current Sense Gain (13 A/V (Typ.))

G_{MA}: Error Amplifier Trans conductance (260µA/V (Typ.))

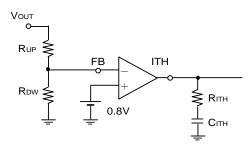
(ii) Selection of Phase Compensation Capacitance CITH

For stable operation of the DC/DC converter, inserting a zero point at 1/6 of the zero crossover frequency cancels the phase delay due to the pole formed by the load often provides favorable characteristics.

The phase compensation capacitance C_{ITH} can be determined by using the following equation.

(iii) Loop stability

To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. A phase margin of at least 45° in the worst conditions is recommended.



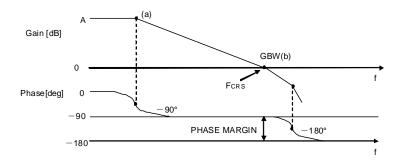


Figure 52. Phase Compensation Circuit

Figure 53. Bode Plot

PCB Layout Design

In the buck DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the High-Side FET is turned ON. The flow starts from the input capacitor C_{IN} , runs through the FET, inductor L and output capacitor C_{OUT} and back to GND of C_{IN} via GND of C_{OUT} . The second loop is the one into which the current flows when the Low-Side FET is turned on. The flow starts from the Low-Side FET, runs through the inductor L and output capacitor C_{OUT} and back to GND of the Low-Side FET via GND of C_{OUT} . Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

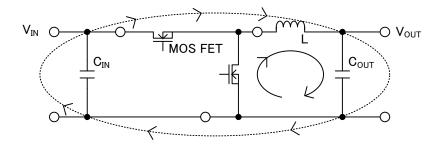
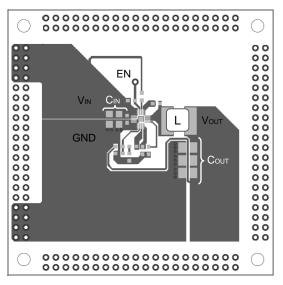


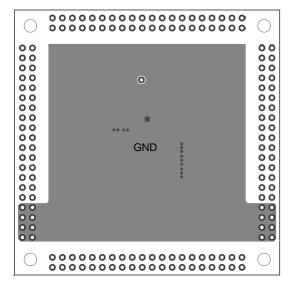
Figure 54. Current Loop of Buck DC/DC Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC PVIN terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and ITH far from the SW nodes.
- · Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



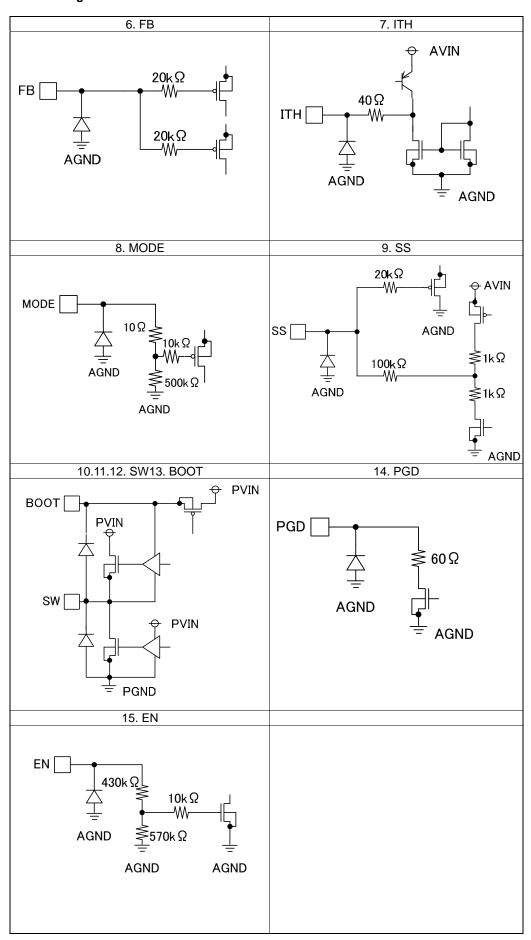




Bottom Layer

Figure 55. Example of evaluation board layout

● I/O Equivalent Circuit Diagram



Operational Notes

1) Absolute Maximum Ratings

Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

2) GND Voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

3) Thermal Consideration

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

4) Short between pins and Mounting errors

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins. Avoid short-circuiting between VIN and Vout/SW. Short-circuiting between these may result in damage to the IC and smoke generation.

5) Operation under strong Electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

6) Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7) PCB Layout

Connect PVIN and AVIN to the power supply of the board and connect PGND and AGND to the GND of the board. Ensure that the wiring for PVIN, AVIN, PGND and AGND are thick and short for sufficiently lowering impedance. Take the output voltage of the DC/DC converter from the two ends of the output capacitor.

The PCB layout and peripheral components may influence the performance of the DC/DC converter. Give sufficient consideration to the design of the peripheral circuitry.

8) Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure 19):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

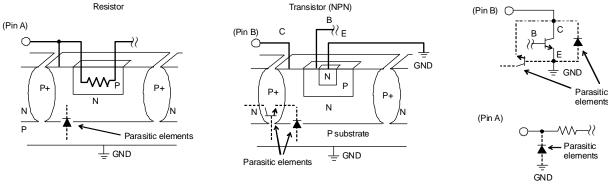


Figure 56. Example of simplified structure of monolithic IC

9) Over Current Protection Circuit (OCP)

The IC incorporates an over-current protection circuit that operates in accordance with the rated output capacity. This circuit protects the IC from damage when the load becomes shorted. It is also designed to limit the output current (without latching) in the event of a large transient current flow, such as from a large capacitor or other component connected to the output pin. This protection circuit is effective in preventing damage to the IC in cases of sudden and unexpected current surges. The IC should not be used in applications where the over current protection circuit will be activated continuously.

10) Thermal Shutdown Circuit (TSD)

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

11) Enable Function

If the rate of fall of the EN terminal signal is too slow, chattering may occur. Chattering with the output voltage remaining may generate a reverse current that boosts the voltage from the output to the input, possibly leading to damage. For on/off control with the EN signal, ensure that the signal falls within 100 µsec.

12) Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

13) Load at Startup

Ensure that the respective output has light load at startup of this IC. Also, restrain the power supply line noise at startup and voltage drop generated by operating current within the hysteresis width of UVLO. Noise exceeding the hysteresis noise width may cause the IC to malfunction.

14) External Elements

Use a ceramic capacitor with low ESR for the bypass capacitor between PVIN and PGND and connect it as close as possible to the IC. For external components such as inductors and capacitors, use the recommended values in this specification and connect these components as close to the IC as possible. For those traces in which large current flows, in particular, ensure that the wiring is thick and short.

15) IC Applications

This IC is not developed for automotive or military applications or equipment/devices that may affect human lives. Do not use the IC for such applications. If this IC is used by customers in any of such applications as described above, ROHM shall not be held responsible for failure to satisfy the requirements concerned.

16) Usage Environment

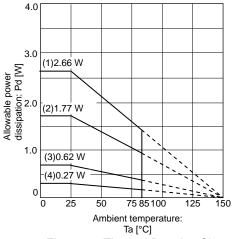
The operating temperature range is intended to guarantee functional operation and does not guarantee the life of the LSI within this range. The life of the LSI is subject to derating depending on usage environment such as the voltage applied, ambient temperature and humidity. Consider derating in the design of equipment and devices.

Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.

This package incorporates an exposed thermal pad. Solder directly to the PCB ground plane. After soldering, the PCB can be used as a heatsink.

The exposed thermal pad dimensions for this package are shown in page 30.



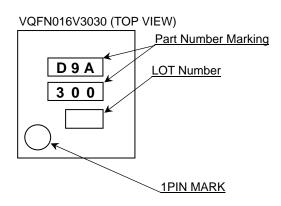
- (1) 4-layer board (surface heat dissipation copper foil 5505mm²)
 (copper foil laminated on each layer)
 θ j-a = 47.0°C/W
- (2) 4-layer board (surface heat dissipation copper foil 6.28mm²)
 (copper foil laminated on each layer)
 θ i-a = 70.62°C/W
- (3) 1-layer board (surface heat dissipation copper foil 6.28mm²)
 θ j-a = 201.6°C/W
- (4) IC only θ j-a = 462.9°C/W

Figure 57. Thermal Derating Characteristics (VQFN016V3030)

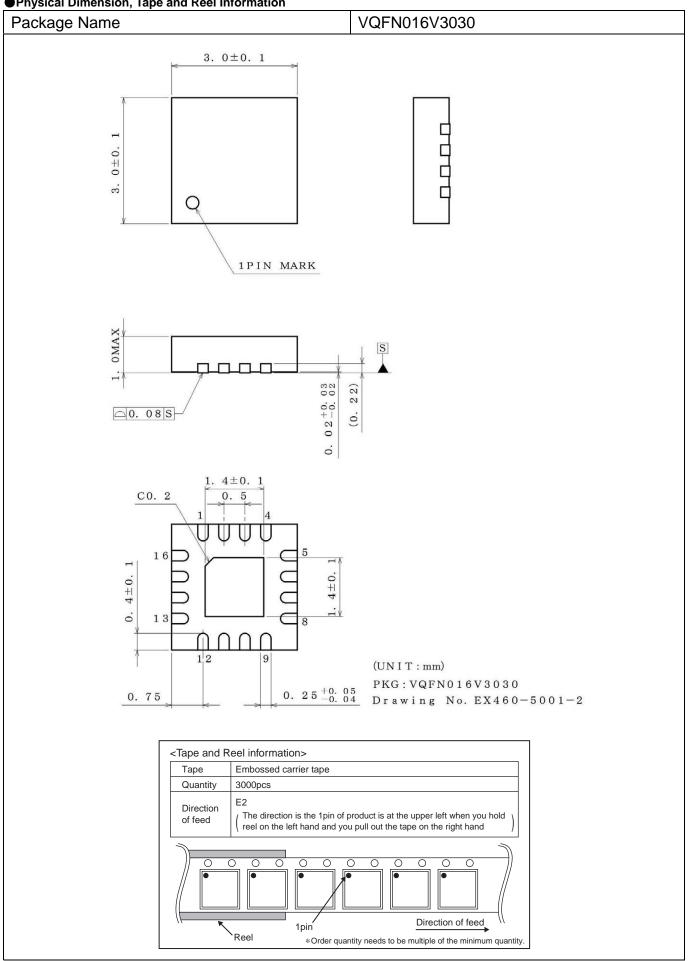
Ordering Information



Marking Diagram



●Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Description
3.Jun.2013	001	Created

Notice

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JAPAN	USA	EU	CHINA
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CLASSIV	CLASSIII	CLASSⅢ	CLASSⅢ

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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
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For details, please refer to ROHM Mounting specification

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Rev.001



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- Подбор аналогов;
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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