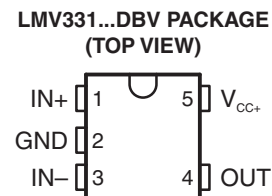
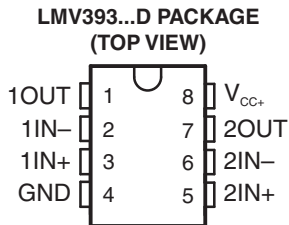


GENERAL-PURPOSE LOW-VOLTAGE COMPARATORS

Check for Samples: [LMV331-Q1 SINGLE](#), [LMV393-Q1 DUAL](#)

FEATURES

- Qualified for Automotive Applications
- 2.7-V and 5-V Performance
- Low Supply Current
 - LMV331 . . . 60 μ A Typ
 - LMV393 . . . 100 μ A Typ
- Input Common-Mode Voltage Range Includes Ground
- Low Output Saturation Voltage . . . 200 mV Typ
- Open-Collector Output for Maximum Flexibility



DESCRIPTION/ORDERING INFORMATION

The LMV393-Q1 device is a low-voltage (2.7 V to 5.5 V) version of the dual and quad comparators, LM393 and LM339, which operate from 5 V to 30 V. The LMV331-Q1 is the single-comparator version.

The LMV331-Q1 and LMV393-Q1 are the most cost-effective solutions for applications where low-voltage operation, low power, space saving, and price are the primary specifications in circuit design for portable consumer products. These devices offer specifications that meet or exceed the familiar LM339 and LM393 devices at a fraction of the supply current.

ORDERING INFORMATION⁽¹⁾

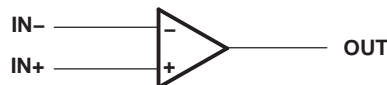
| T_A | PACKAGE ⁽²⁾ | | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|------------------------|---------------|--------------|-----------------------|---------------------------------|
| –40°C to 125°C | Single | SOT23-5 – DBV | Reel of 3000 | LMV331QDBVRQ1 | LADQ |
| | Dual | SOIC – D | Reel of 2500 | LMV393QDRQ1 | V393Q1 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

Figure 1. SYMBOL (EACH COMPARATOR)

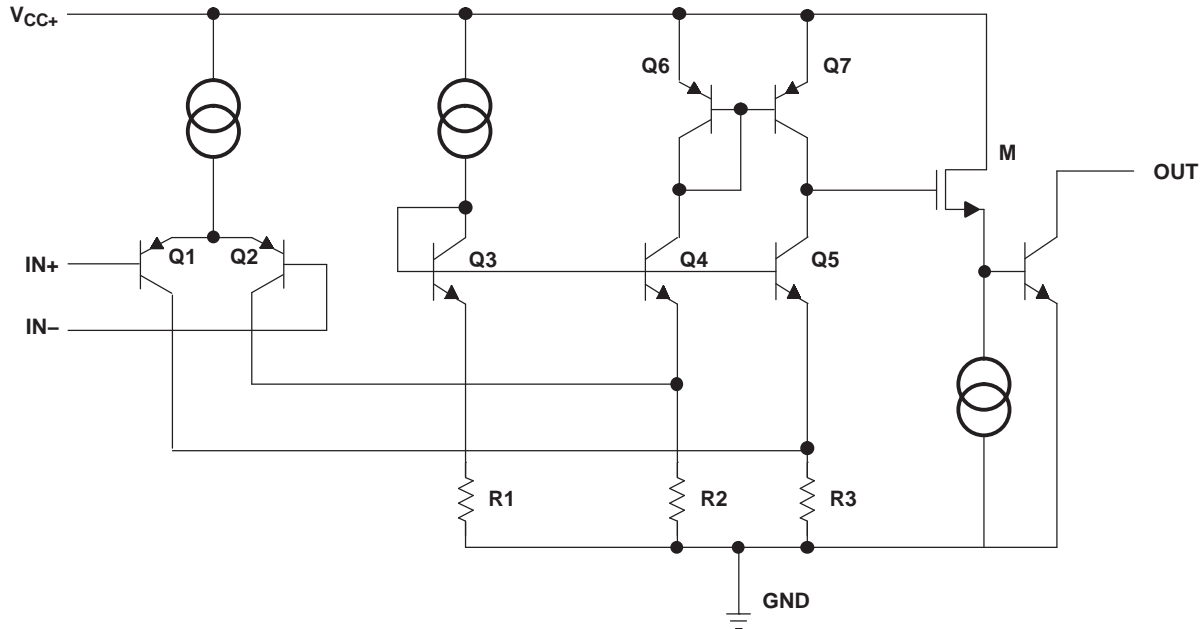


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Figure 2. SIMPLIFIED SCHEMATIC



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--|--------------------|------|------|
| V _{CC+} | Supply voltage ⁽²⁾ | | 5.5 | V |
| V _{ID} | Differential input voltage ⁽³⁾ | | ±5.5 | V |
| V _I | Input voltage range (either input) | 0 | 5.5 | V |
| θ _{JA} | Package thermal impedance ^{(4) (5)} | D (8-pin) package | | 97 |
| | | D (14-pin) package | | 86 |
| | | DBV package | | 206 |
| T _J | Operating virtual junction temperature | | 150 | °C |
| T _{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC+} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/θ_{JA}. Selecting the maximum of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|------------------|--|-----|------------------------|------|
| V _{CC+} | Supply voltage (single-supply operation) | 2.7 | 5.5 | V |
| V _{OUT} | Output voltage | | V _{CC+} + 0.3 | V |
| T _A | Operating free-air temperature | –40 | 125 | °C |

Electrical Characteristics

at specified free-air temperature, $V_{CC+} = 2.7\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|-----------------|---|-------------------------------|----------------|-----|-----------|-----|------------------------------|
| V_{IO} | Input offset voltage | | 25°C | | 1.7 | 7 | mV |
| αV_{IO} | Average temperature coefficient of input offset voltage | | –40°C to 125°C | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IB} | Input bias current | | 25°C | | 10 | 250 | nA |
| | | | –40°C to 125°C | | | 400 | |
| I_{IO} | Input offset current | | 25°C | | 5 | 50 | nA |
| | | | –40°C to 125°C | | | 150 | |
| I_O | Output current (sinking) | $V_O \leq 1.5\text{ V}$ | 25°C | 5 | 23 | | mA |
| | Output leakage current | | 25°C | | 0.003 | | μA |
| | | | –40°C to 125°C | | | 1 | |
| V_{ICR} | Common-mode input voltage range | | 25°C | | –0.1 to 2 | | V |
| V_{SAT} | Saturation voltage | $I_O \leq 1\text{ mA}$ | 25°C | | 200 | | mV |
| I_{CC} | Supply current | LMV331 | 25°C | | 40 | 100 | μA |
| | | LMV393 (both comparators) | | | 70 | 140 | |
| | | LMV339 (all four comparators) | | | 140 | 200 | |

Switching Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 2.7\text{ V}$, $R_L = 5.1\text{ k}\Omega$, $GND = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|--|--------------------------|------|------|
| t_{PHL} | Propagation delay, high- to low-level output switching | Input overdrive = 10 mV | 1000 | ns |
| | | Input overdrive = 100 mV | 350 | |
| t_{PLH} | Propagation delay, low- to high-level output switching | Input overdrive = 10 mV | 500 | ns |
| | | Input overdrive = 100 mV | 400 | |

Electrical Characteristics

at specified free-air temperature, $V_{CC+} = 5\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|-----------------|---|-------------------------------|----------------|-----|-------------|-----|------------------------------|
| V_{IO} | Input offset voltage | | 25°C | | 1.7 | 7 | mV |
| | | | –40°C to 125°C | | | 9 | |
| αV_{IO} | Average temperature coefficient of input offset voltage | | 25°C | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IB} | Input bias current | | 25°C | | 25 | 250 | nA |
| | | | –40°C to 125°C | | | 400 | |
| I_{IO} | Input offset current | | 25°C | | 2 | 50 | nA |
| | | | –40°C to 125°C | | | 150 | |
| I_O | Output current (sinking) | $V_O \leq 1.5\text{ V}$ | 25°C | 10 | 84 | | mA |
| | Output leakage current | | 25°C | | 0.003 | | μA |
| | | | –40°C to 125°C | | | 1 | |
| V_{ICR} | Common-mode input voltage range | | 25°C | | –0.1 to 4.2 | | V |
| A_{VD} | Large-signal differential voltage gain | | 25°C | 20 | 50 | | V/mV |
| V_{SAT} | Saturation voltage | $I_O \leq 4\text{ mA}$ | 25°C | | 200 | 400 | mV |
| | | | –40°C to 125°C | | | 700 | |
| I_{CC} | Supply current | LMV331 | 25°C | | 60 | 120 | μA |
| | | | –40°C to 125°C | | | 150 | |
| | | LMV393 (both comparators) | 25°C | | 100 | 200 | |
| | | | –40°C to 125°C | | | 250 | |
| | | LMV339 (all four comparators) | 25°C | | 170 | 300 | |
| | | | –40°C to 125°C | | | 350 | |

Switching Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{ V}$, $R_L = 5.1\text{ k}\Omega$, $GND = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|--|--------------------------|-----|------|
| t_{PHL} | Propagation delay, high- to low-level output switching | Input overdrive = 10 mV | 600 | ns |
| | | Input overdrive = 100 mV | 200 | |
| t_{PLH} | Propagation delay, low- to high-level output switching | Input overdrive = 10 mV | 450 | ns |
| | | Input overdrive = 100 mV | 300 | |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| LMV331QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| LMV393QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| LMV393QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF LMV331-Q1, LMV393-Q1 :

- Catalog: [LMV331](#), [LMV393](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R-PDSO-G8)

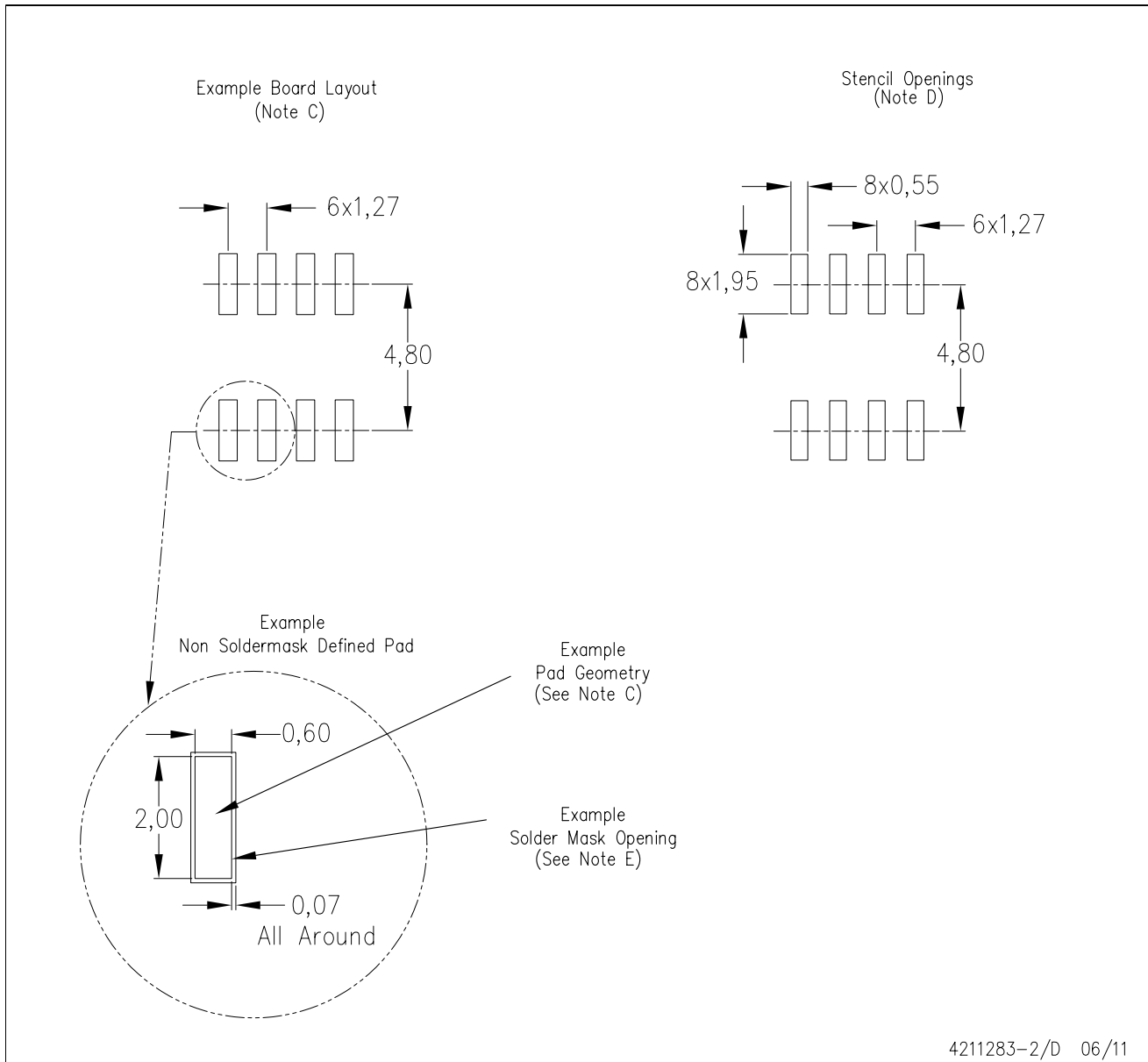
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/D 06/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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