

**OptiMOS™ Power-MOSFET**
**Features**

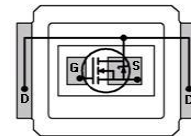
- Optimized for high performance Buck converter
- Low parasitic inductance
- Low profile (<0.7 mm)
- 100% avalanche tested
- 100%  $R_G$  Tested
- Double-sided cooling
- Compatible with DirectFET® package SQ footprint and outline <sup>1)</sup>
- Qualified according to JEDEC<sup>2)</sup> for target applications


**Product Summary**

$V_{DS}$	25	V
$R_{DS(on),max}$	3.5	mΩ
$I_D$	69	A
$Q_{OSS}$	13	nC
$Q_g(0V..10V)$	19	nC

**CanPAK™ S  
MG-WDSO-2**


Type	Package	Outline	Marking
BSF035NE2LQ	MG-WDSO-2	SQ	04E2


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	69	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	44	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}^3)$	22	
Pulsed drain current <sup>4)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	276	
Avalanche current, single pulse <sup>5)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	40	
Avalanche energy, single pulse	$E_{AS}$	$I_D=35\text{ A}, R_{GS}=25\text{ Ω}$	50	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> CanPAK™ uses DirectFET® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.

<sup>2)</sup> J-STD20 and JESD22

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

<sup>4)</sup> See figure 3 for more detailed information

<sup>5)</sup> See figure 13 for more detailed information

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	28	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=58\text{ K/W}$	2.2	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-40 ... 150	°C
IEC climatic category; DIN IEC 68-1				

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	1.0	-	K/W
		top	-	-	4.5	
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>5)</sup>	-	-	58	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{D}}=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{D}}=250\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=25\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=25\text{ °C}$	-	0.1	10	$\mu\text{A}$
		$V_{\text{DS}}=25\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}$ , $V_{\text{DS}}=0\text{ V}$		10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$ , $I_{\text{D}}=30\text{ A}$	-	3.7	4.6	m $\Omega$
		$V_{\text{GS}}=10\text{ V}$ , $I_{\text{D}}=30\text{ A}$	-	2.9	3.5	
Gate resistance	$R_{\text{G}}$		0.3	0.6	1.2	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=30\text{ A}$	55	110	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=12\text{ V},$ $f=1\text{ MHz}$	-	1400	1862	pF
Output capacitance	$C_{oss}$		-	630	838	
Reverse transfer capacitance	$C_{rss}$		-	59	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=12\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_{G,ext}=1.6\ \Omega$	-	1.8	-	ns
Rise time	$t_r$		-	3.2	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	$t_f$		-	2.2	-	

**Gate Charge Characteristics<sup>6)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=12\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	3.1	4.1	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.2	-	
Gate to drain charge	$Q_{gd}$		-	2.0	3.0	
Switching charge	$Q_{sw}$		-	3.0	-	
Gate charge total	$Q_g$		-	9.1	12	
Gate plateau voltage	$V_{plateau}$		-	2.3	-	
Gate charge total	$Q_g$	$V_{DD}=12\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	19	25	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	7.9	-	
Output charge	$Q_{oss}$	$V_{DD}=12\text{ V}, V_{GS}=0\text{ V}$	-	13	17	

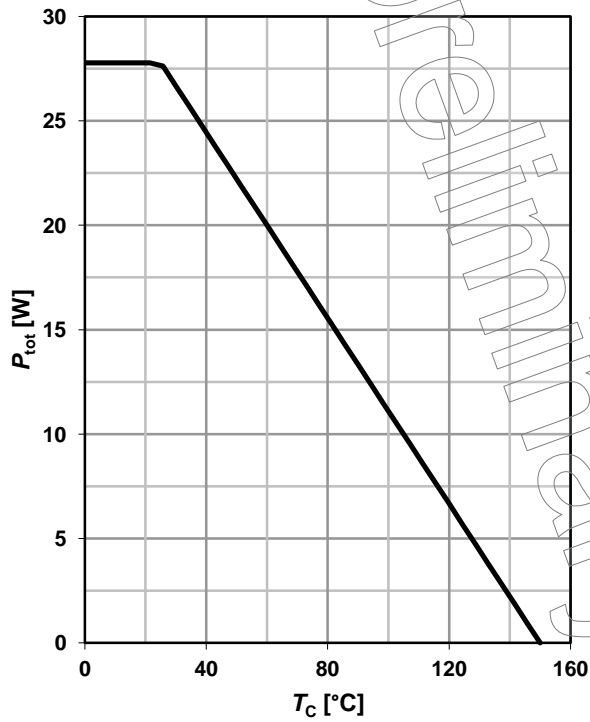
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ °C}$	-	-	28	A
Diode pulse current	$I_{S,pulse}$		-	-	112	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ °C}$	-	0.84	-	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	10	-	nC

<sup>6)</sup> See figure 16 for gate charge parameter definition

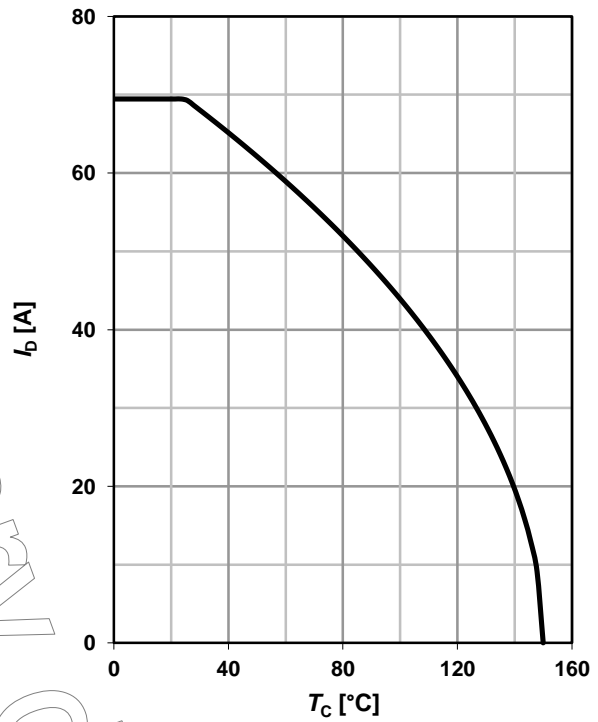
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

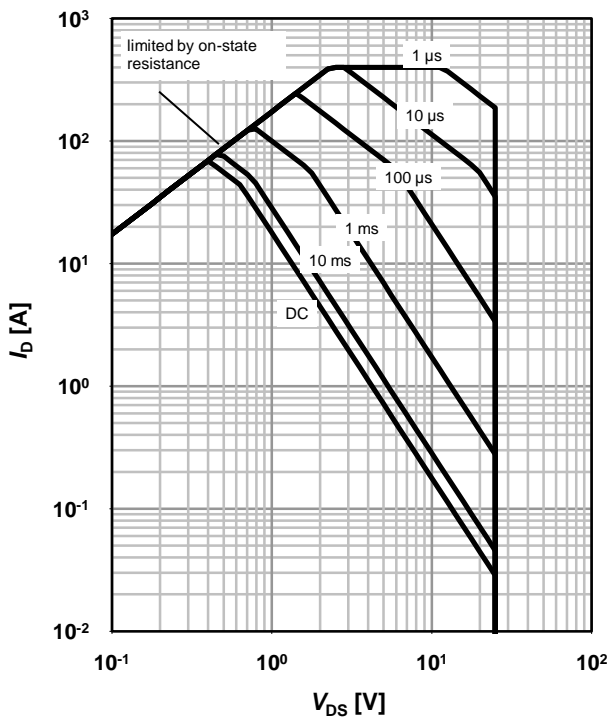
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

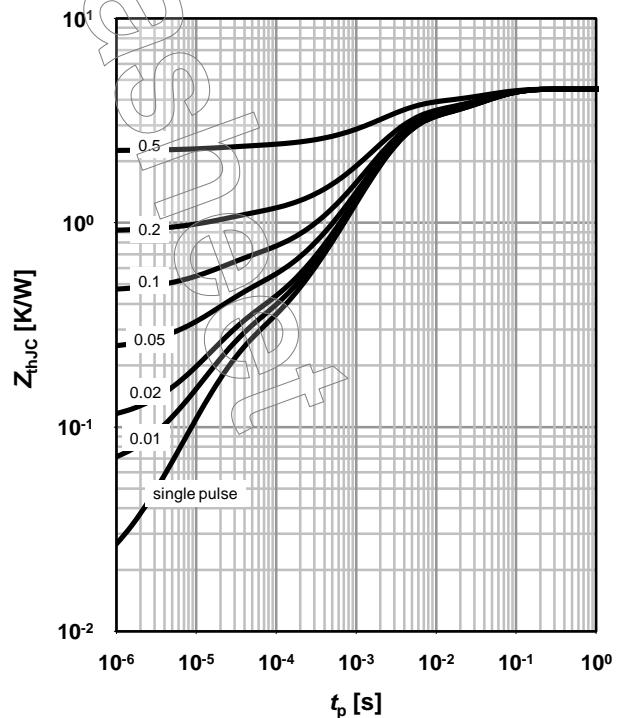
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

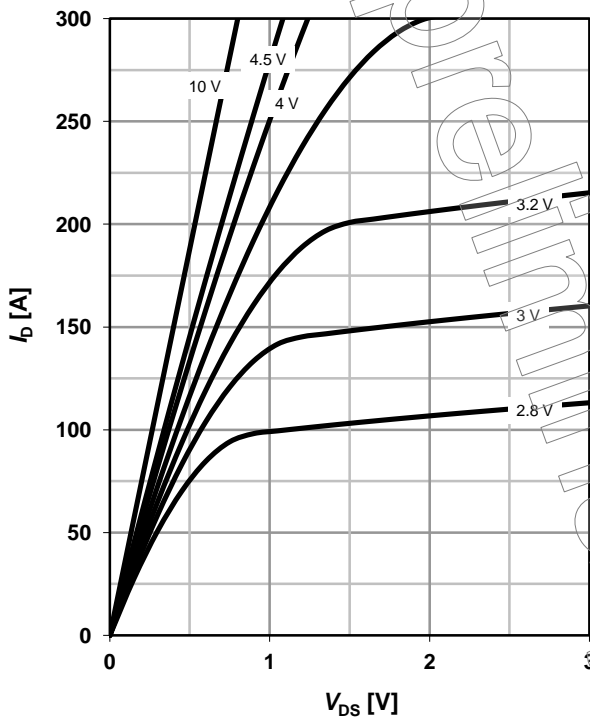
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

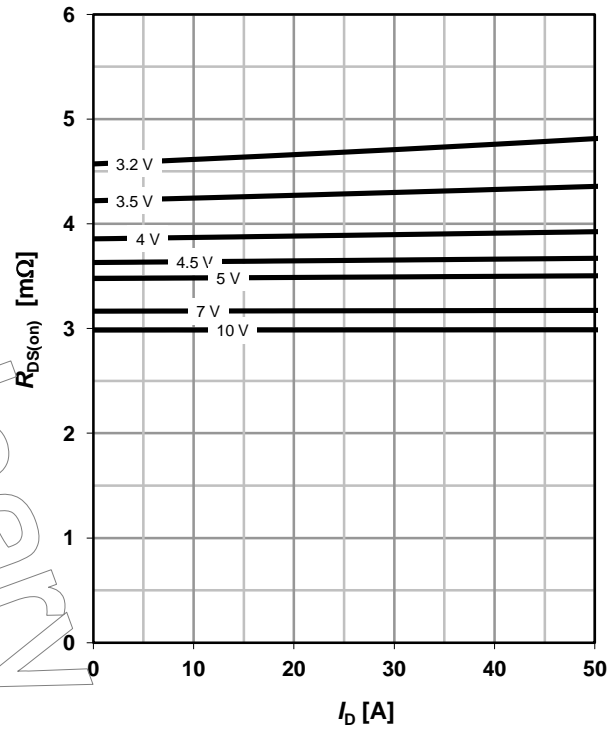
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

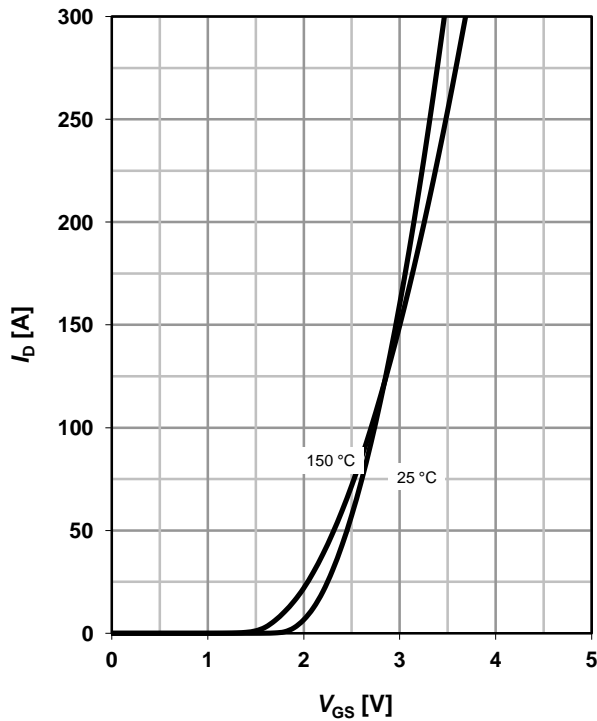
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

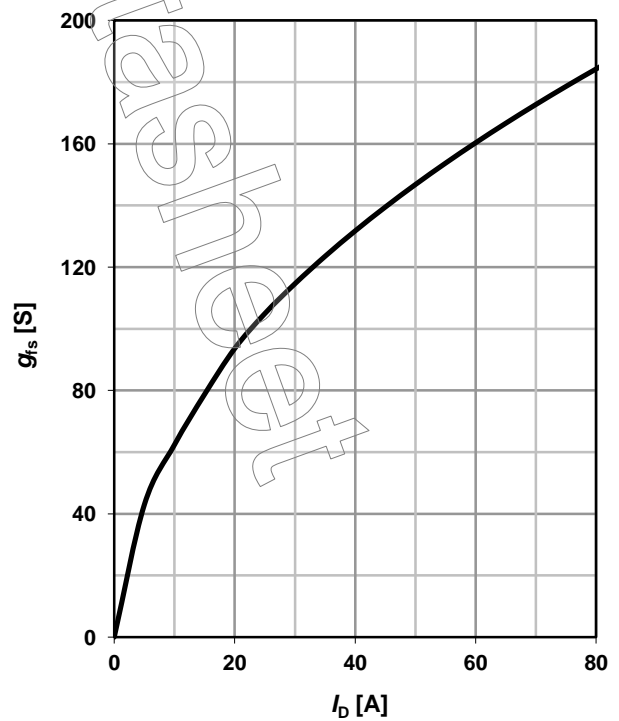
$I_D = f(V_{GS}); |V_{DS}| > 2I_D R_{DS(on)max}$

parameter:  $T_j$



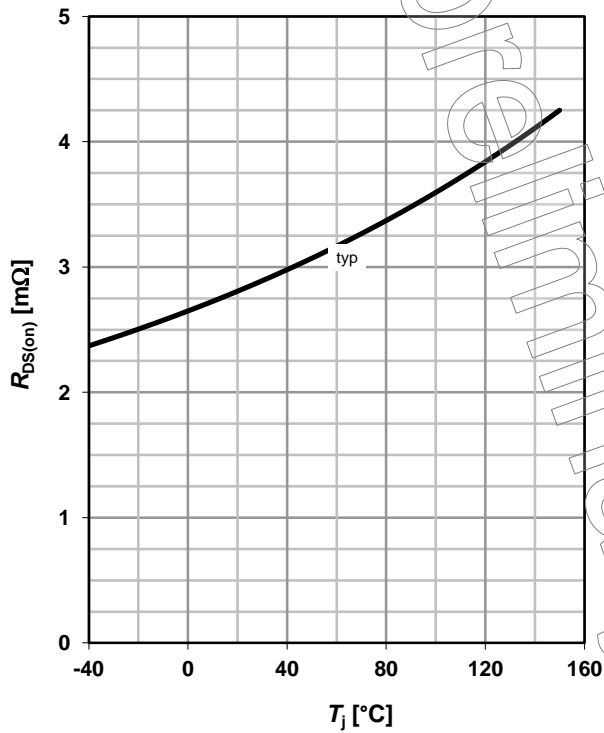
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



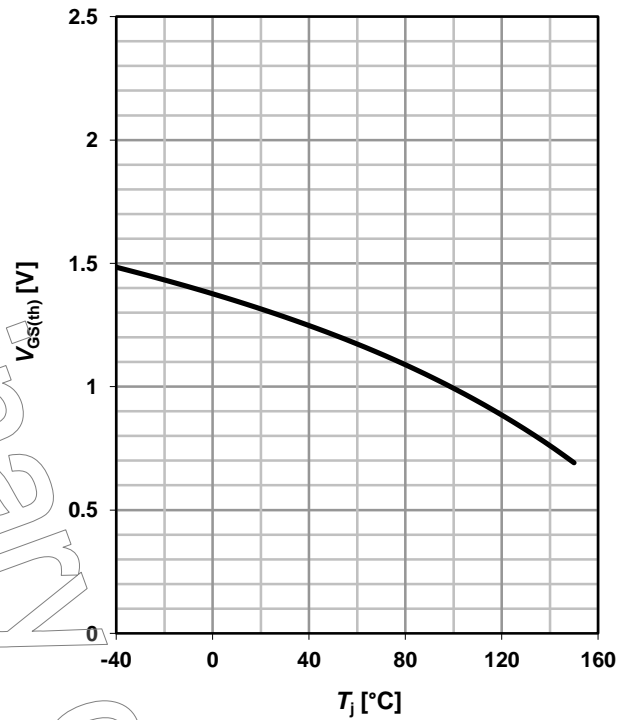
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}$



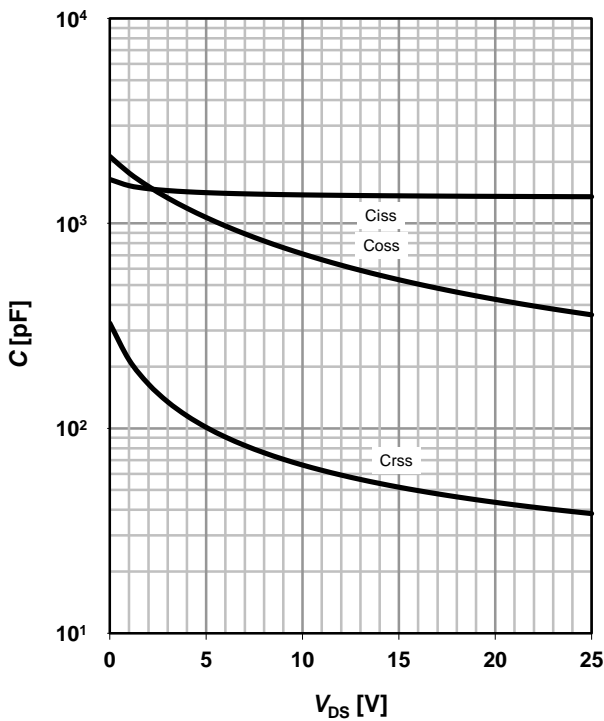
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=250\text{ }\mu\text{A}$



**11 Typ. capacitances**

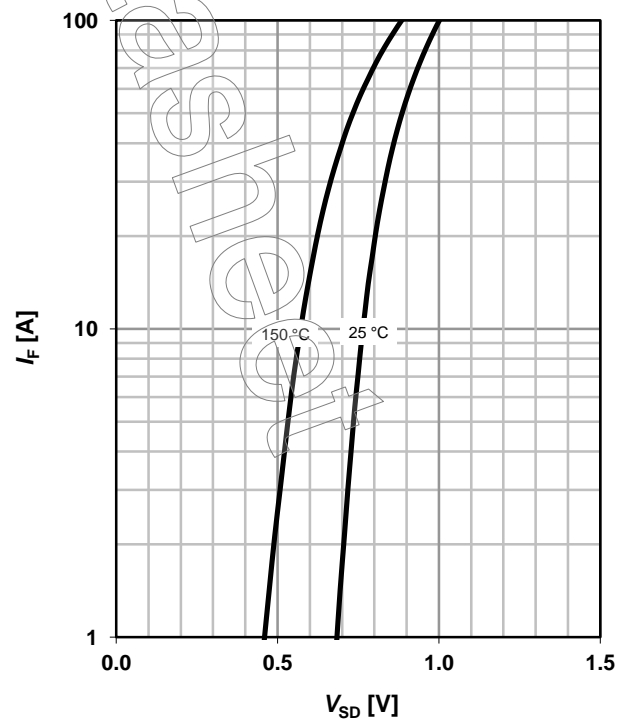
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

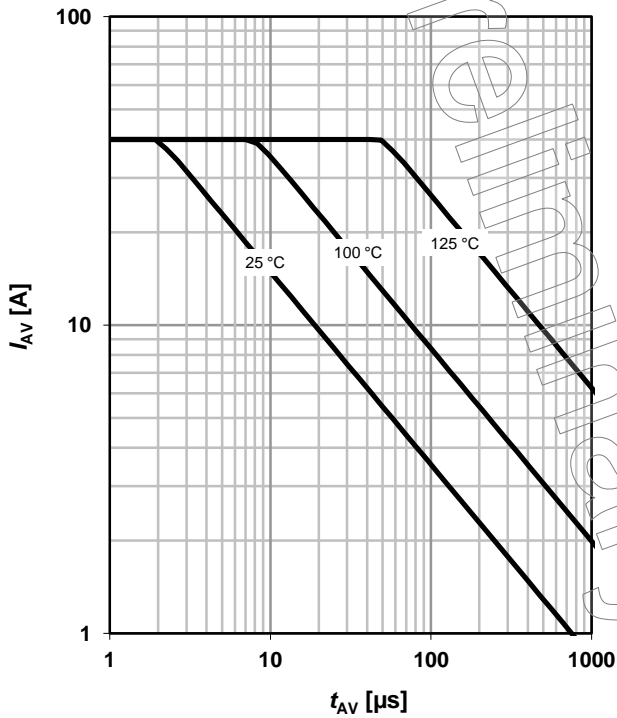
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

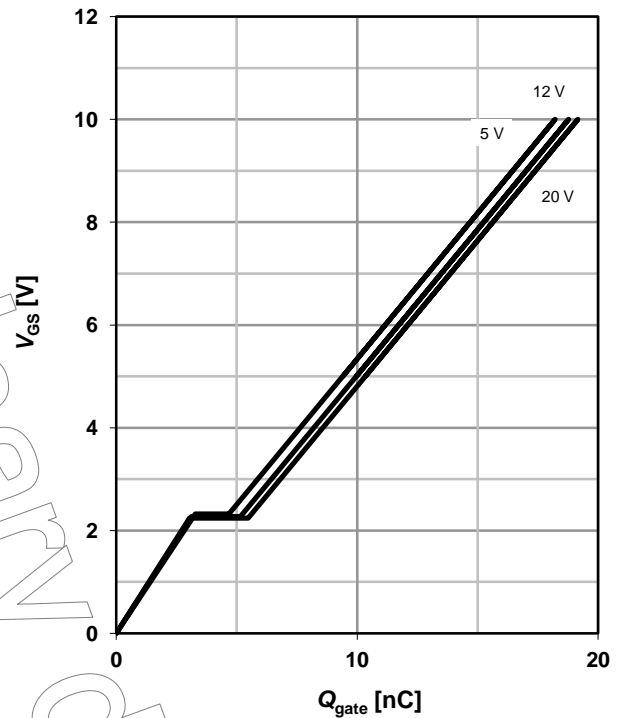
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

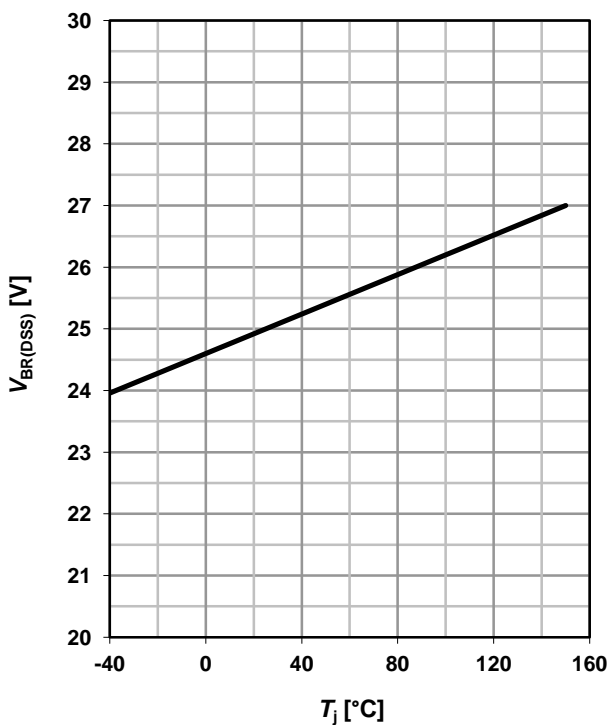
$V_{GS}=f(Q_{\text{gate}}); I_D=30 \text{ A pulsed}$

parameter:  $V_{DD}$

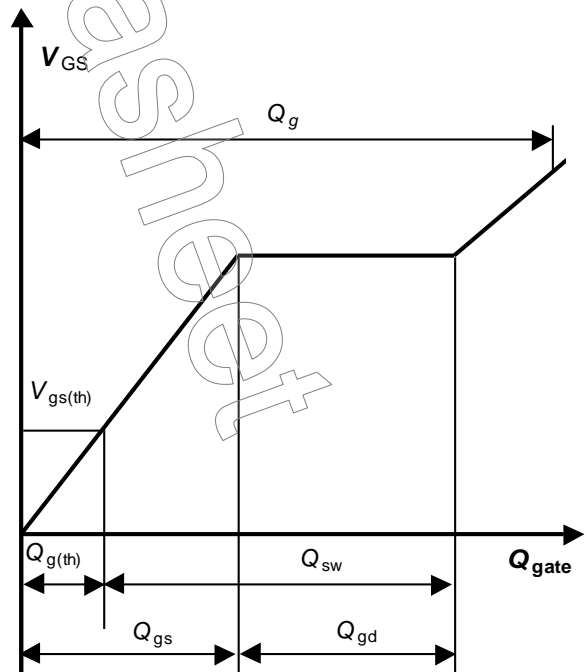


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

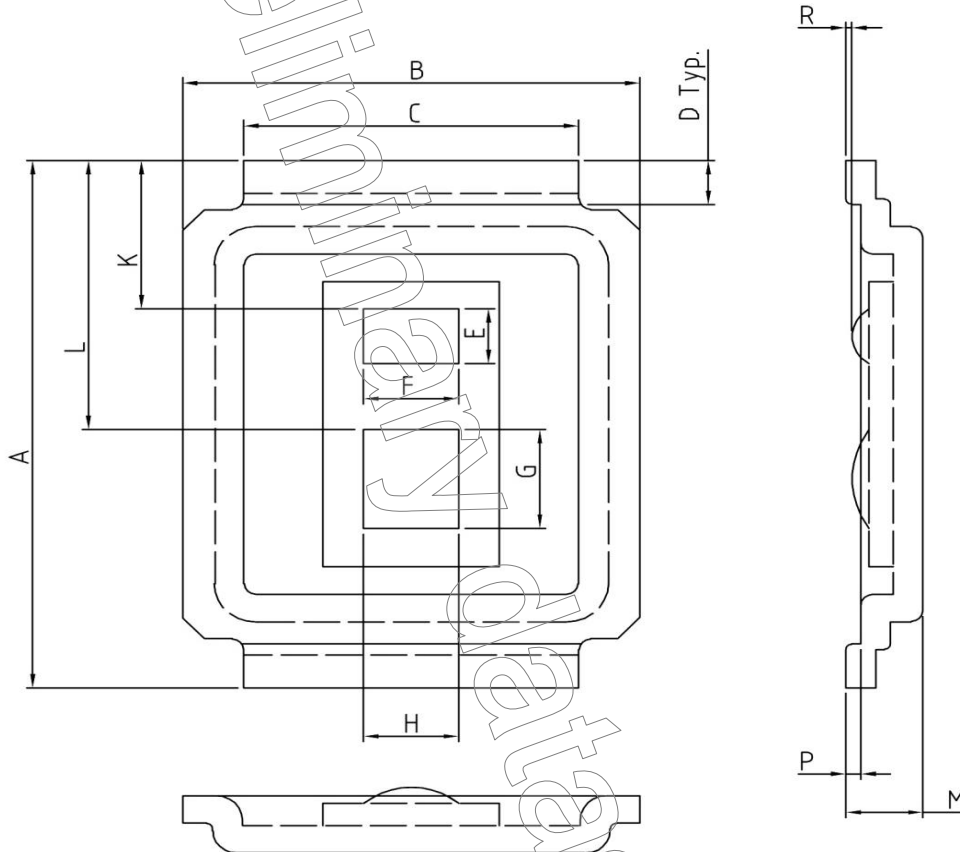


**16 Gate charge waveforms**



Package Outline

MG-WDSO N-233/-53



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.75	4.88	0.187	0.192
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.48	0.52	0.019	0.020
F	0.78	0.82	0.031	0.032
G	0.88	0.92	0.035	0.036
H	0.78	0.82	0.031	0.032
K	1.25	1.45	0.049	0.057
L	2.35	2.55	0.093	0.100
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

DOCUMENT NO.  
Z8B00134584

SCALE

EUROPEAN PROJECTION

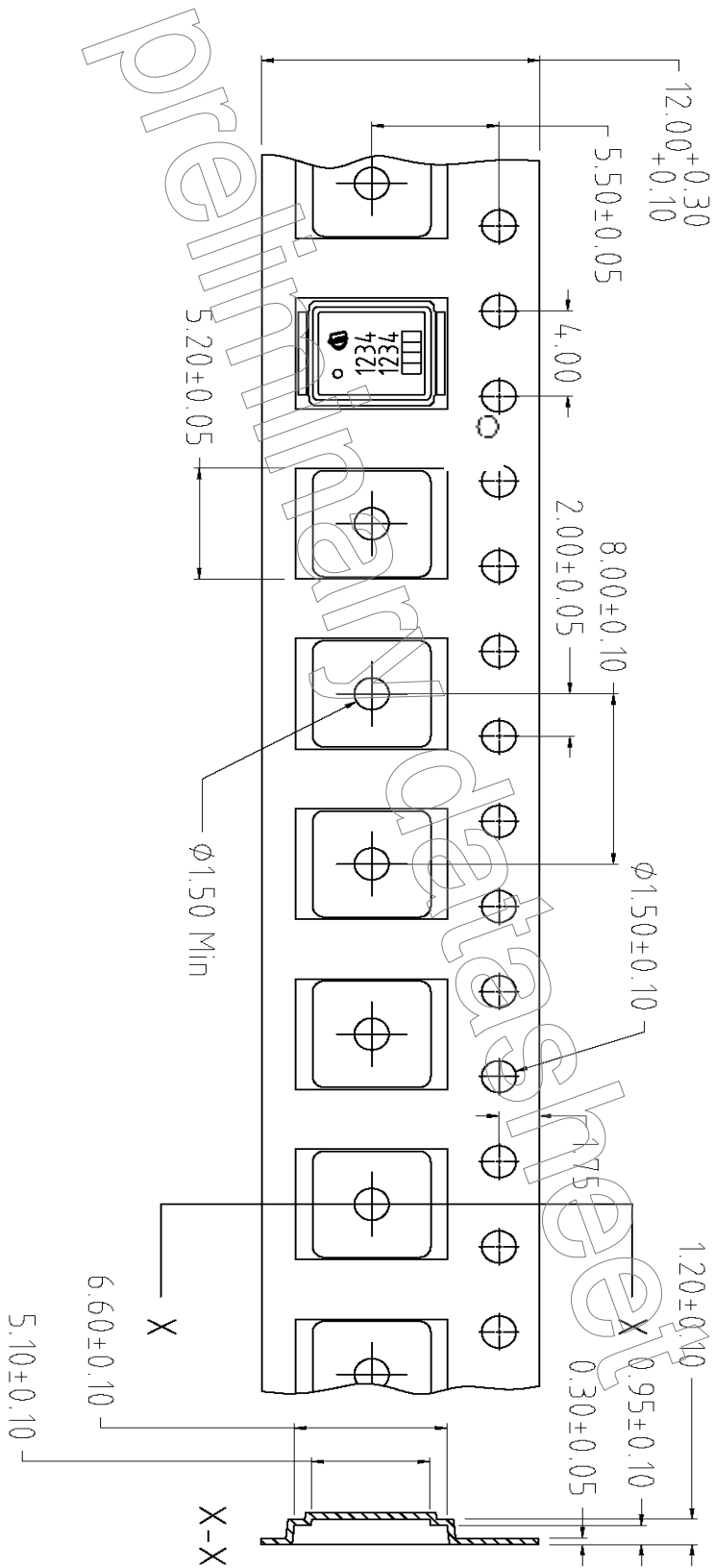
ISSUE DATE  
05-05-2009

REVISION  
02



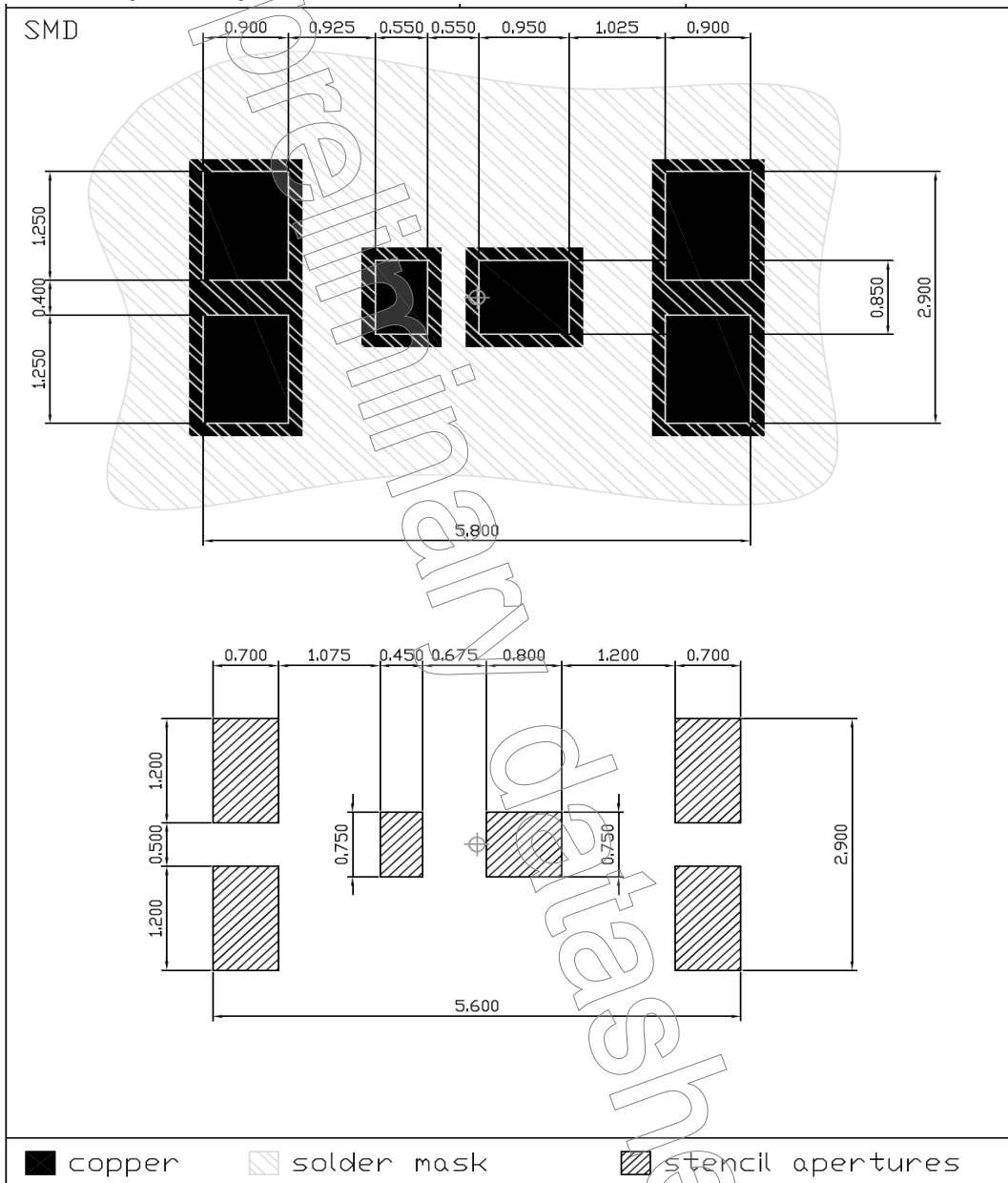
Package Outline

MG-WDSO-N-2



Dimensions in mm

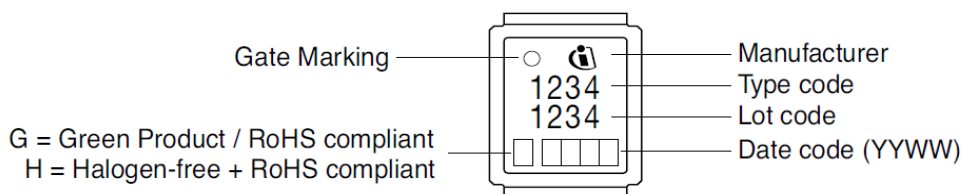
CanPAK SQ: Boardpads & Apertures



Dimensions in mm

Recommended stencil thickness 150 µm

Marking Layout



**Published by**

**Infineon Technologies AG**  
81726 Munich, Germany  
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- Техническая поддержка проекта;
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