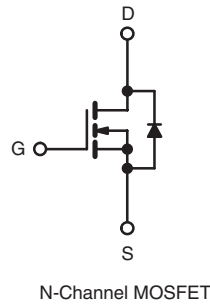
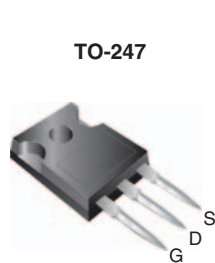


## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.40
$Q_g$ (Max.) (nC)	150	
$Q_{gs}$ (nC)	20	
$Q_{gd}$ (nC)	80	
Configuration	Single	



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



Available

**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

### ORDERING INFORMATION

Package	TO-247
Lead (Pb)-free	IRFP450PbF
	SiHFP450-E3
SnPb	IRFP450
	SiHFP450

### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

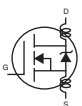

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	500	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	56		
Linear Derating Factor		1.5	$W/^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	760	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	8.7	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	19	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	190	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	3.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 7.0\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 14\text{ A}$  (see fig. 12).
- $I_{SD} \leq 14\text{ A}$ ,  $dI/dt \leq 130\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.63	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$   $I_D = 8.4\text{ A}^b$	-	-	0.40	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 8.4\text{ A}^b$	9.3	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5	-	2600	-	pF
Output Capacitance	$C_{oss}$		-	720	-	
Reverse Transfer Capacitance	$C_{rss}$		-	340	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$   $I_D = 14\text{ A}$ , $V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	150	nC
Gate-Source Charge	$Q_{gs}$		-	-	20	
Gate-Drain Charge	$Q_{gd}$		-	-	80	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$ , $I_D = 14\text{ A}$ , $R_G = 6.2\text{ }\Omega$ , $R_D = 17\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	17	-	ns
Rise Time	$t_r$		-	47	-	
Turn-Off Delay Time	$t_{d(off)}$		-	92	-	
Fall Time	$t_f$		-	44	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	5.0	-	nH
Internal Source Inductance	$L_S$		-	13	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	56	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 14\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	1.4	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 14\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	540	810	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	4.8	7.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

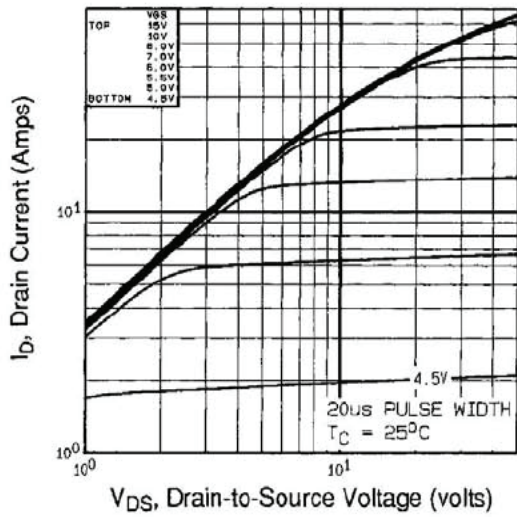


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

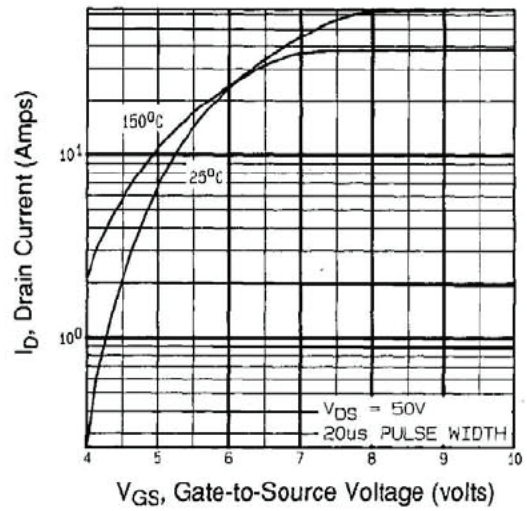


Fig. 3 - Typical Transfer Characteristics

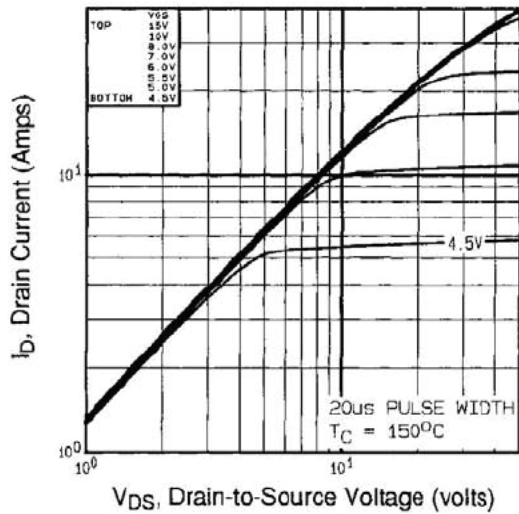


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

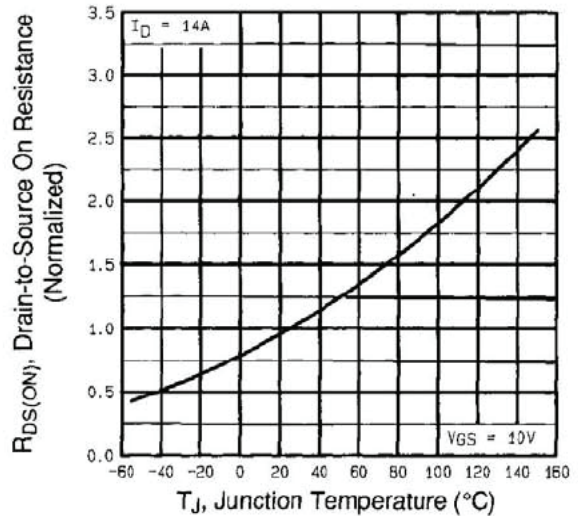


Fig. 4 - Normalized On-Resistance vs. Temperature

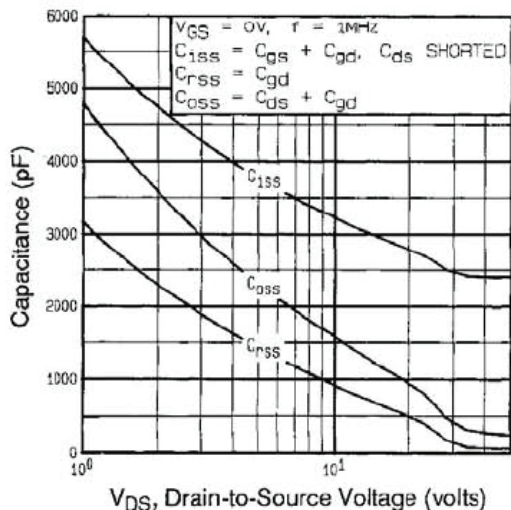


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

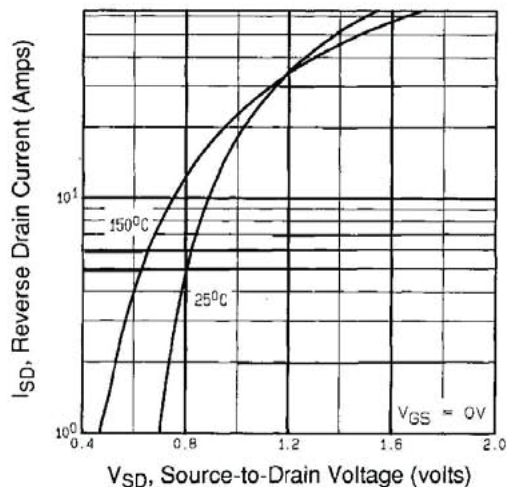


Fig. 7 - Typical Source-Drain Diode Forward Voltage

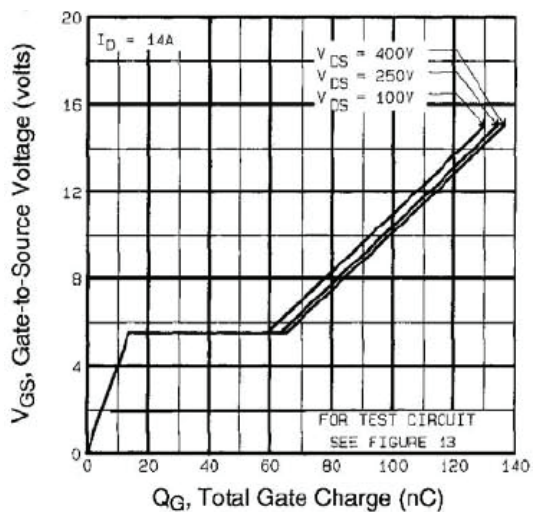


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

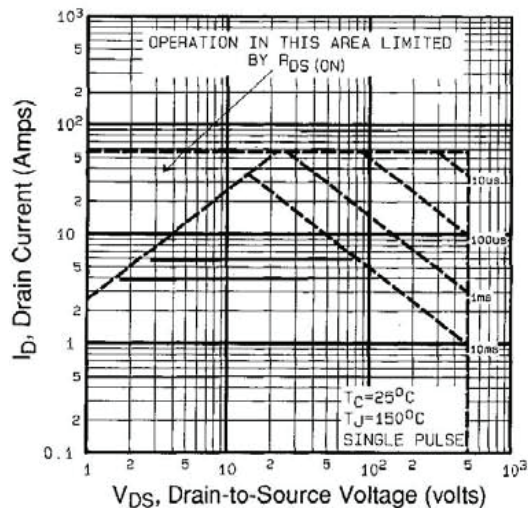


Fig. 8 - Maximum Safe Operating Area

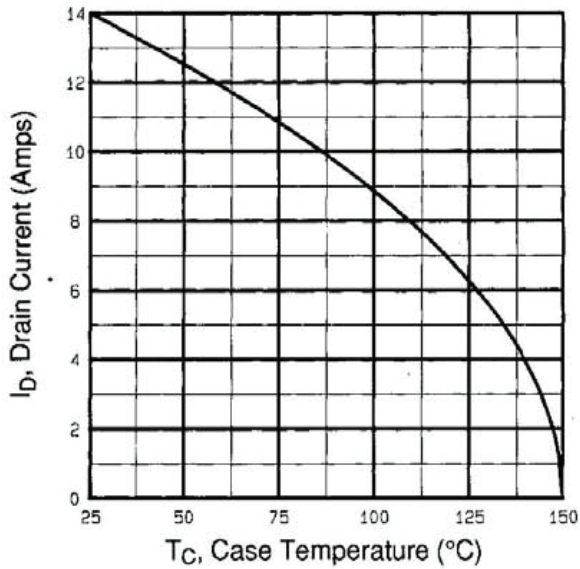


Fig. 9 - Maximum Drain Current vs. Case Temperature

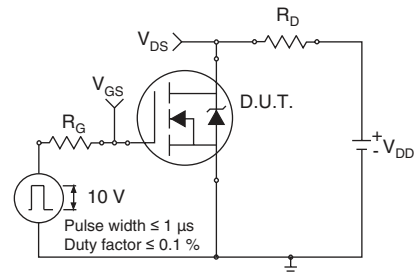


Fig. 10a - Switching Time Test Circuit

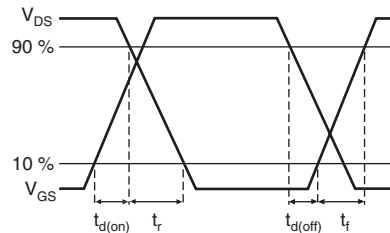


Fig. 10b - Switching Time Waveforms

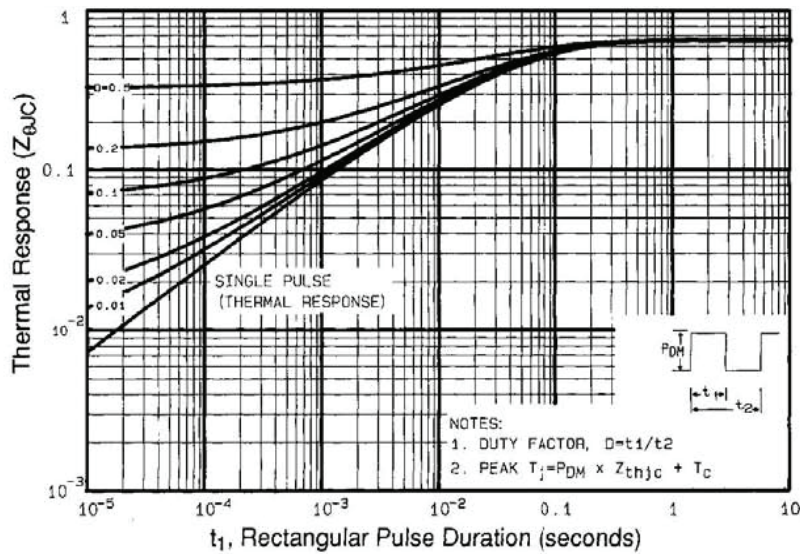


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

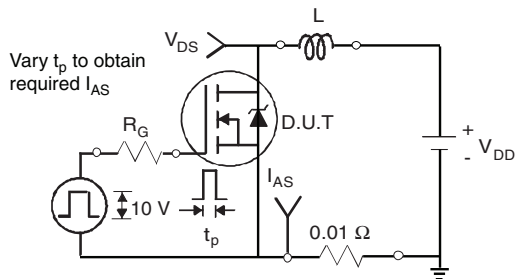


Fig. 12a - Unclamped Inductive Test Circuit

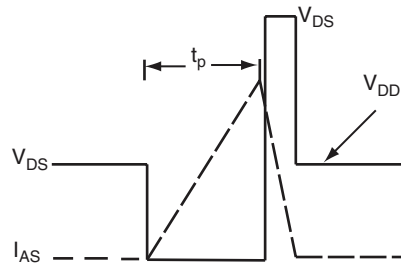


Fig. 12b - Unclamped Inductive Waveforms

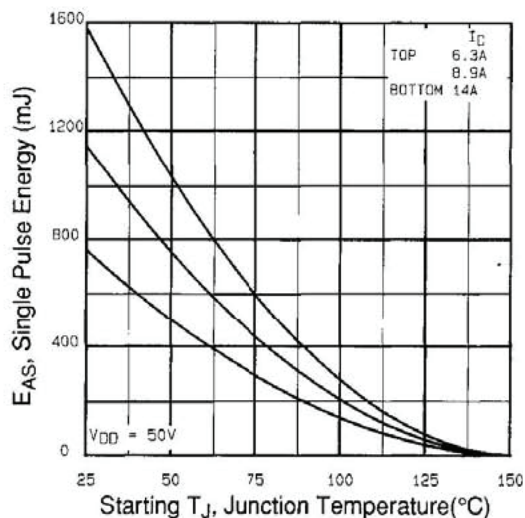


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

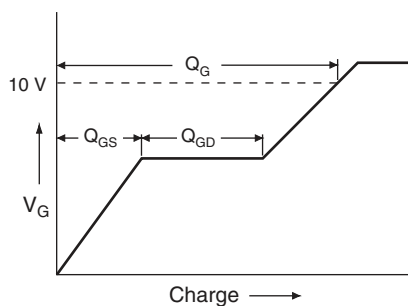


Fig. 13a - Basic Gate Charge Waveform

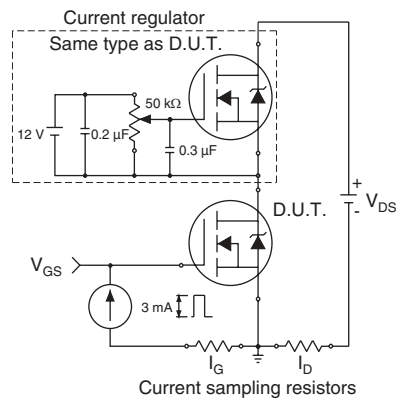
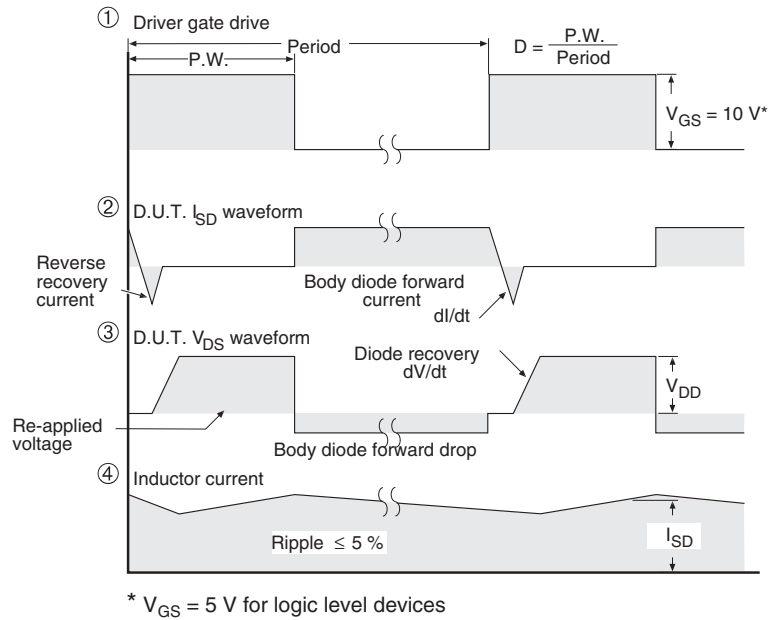
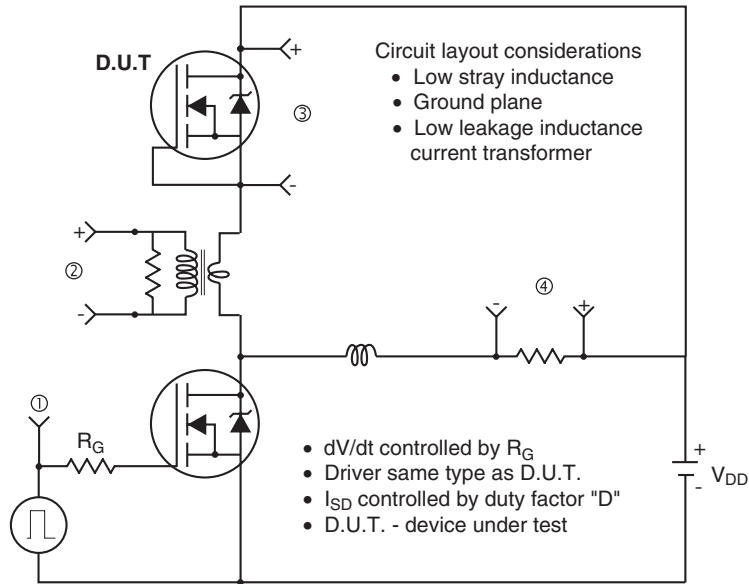


Fig. 13b - Gate Charge Test Circuit

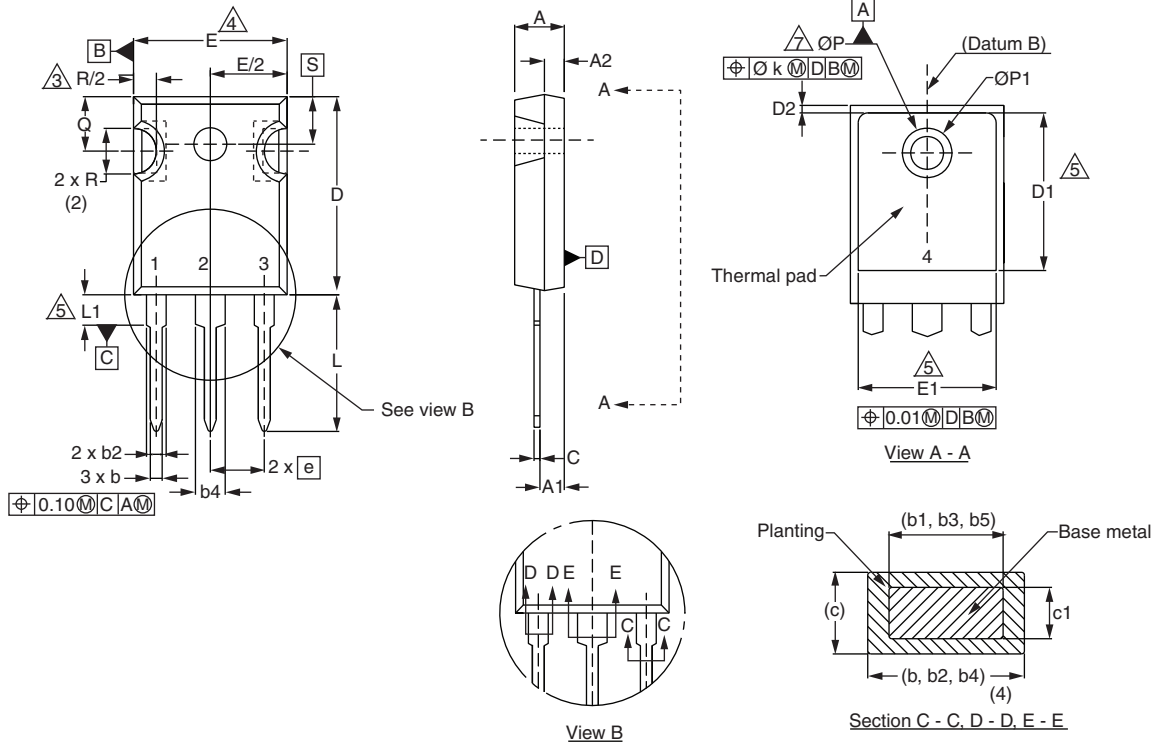
## Peak Diode Recovery $dV/dt$ Test Circuit



**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?91233>.

### TO-247AC (High Voltage)



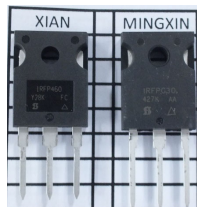
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0045-Rev. C, 18-Mar-13  
DWG: 5971

#### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Contour of slot optional.
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- Thermal pad contour optional with dimensions D1 and E1.
- Lead finish uncontrolled in L1.
- Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- Xian and Mingxin actually photo.







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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.