EVAL-ADG5208FEBZ User Guide
UG-874

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Evaluation Board for the ADG5208F, Overvoltage Protected 8:1 Multiplexer

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- Parallel interface compatible with 3 V logic
- On-board low dropout (LDO) regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

- EVAL-ADG5208FEBZ evaluation board

ONLINE RESOURCES

- Documents Needed
  - ADG5208F data sheet
  - EVAL-ADG5208FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital logic supply: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG5208FEBZ is the evaluation board for the ADG5208F, and features an overvoltage protected 8:1 multiplexer. The ADG5208F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5208FEBZ in a typical evaluation setup. The ADG5208F is soldered to the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals are used to power the device, with a fourth terminal used to provide a user defined digital logic supply voltage, if required. Alternatively, a low dropout (LDO) regulator is provided for 5 V digital logic supply.

Full specifications on the ADG5208F are available in the ADG5208F data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

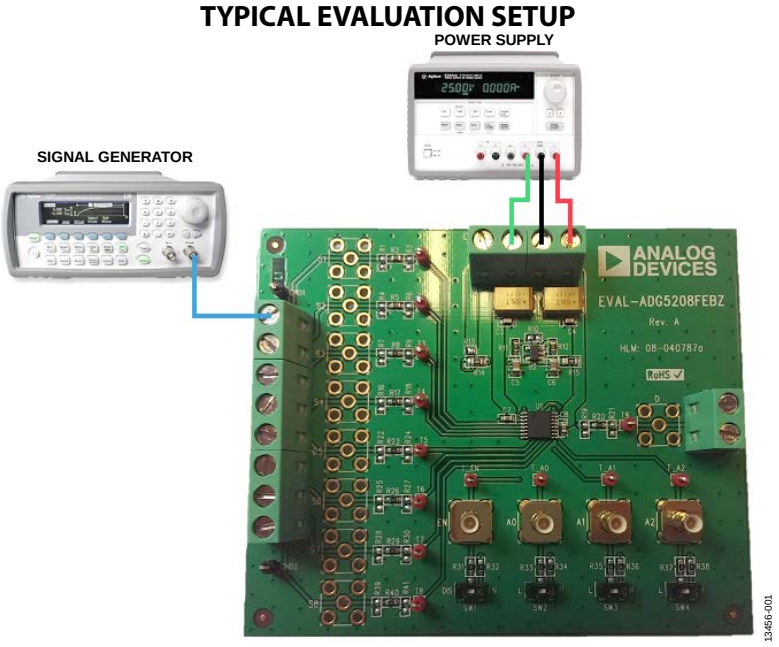


Figure 1. EVAL-ADG5208FEBZ, Power Supply, and Signal Generator

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REVISION HISTORY

5/2016—Rev. A to Rev. B

Changes to Figure 1 1
Changes to Evaluation Board Setup Procedure Section 3
Changes to Input Signals Section 4
Changes to Table 1 5

3/2016—Rev. 0 to Rev. A

Changes to Table 1 5

8/2015—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5208FEBZ evaluation board operates independently and does not require any additional evaluation boards or software to operate. An on-board LDO regulator is provided as the digital power supply to manually control the ADG5208F.

Supply the evaluation board with a dual power source of up to ±22 V or a single supply of up to 44 V by connecting VSS and GND together.

A functionality test can be set up as follows:

1. Connect a power supply to J3. Connect VSS and GND together if a single supply is required.
2. Ensure that a 0 Ω resistor is inserted in R15 to use the on-board LDO regulator, and that a 0 Ω resistor is inserted in R14.
3. SW1 through SW4 control the digital signals for the ADG5208F. See Table 1 for the logic control truth table.

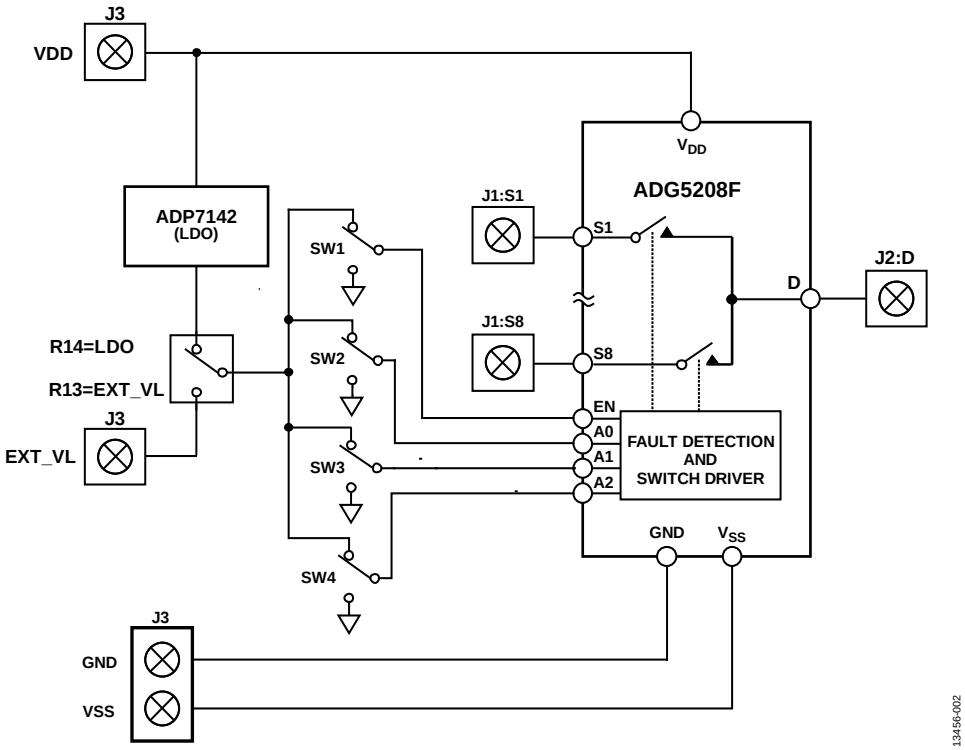


Figure 2. EVAL-ADG5208FEBZ Block Diagram

EVALUATION BOARD HARDWARE

The operation of the ADG5208F is evaluated using the EVAL-ADG5208FEBZ. Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the block diagram of the main components of the evaluation board.

Using this evaluation board, the ADG5208F passes signals from either the source or drain connectors. The source pins have fault detection circuitry that react to an overvoltage event. During an overvoltage event, the channel on which the fault occurs is turned off. See the ADG5208F data sheet for more details.

POWER SUPPLY

Connector J3 provides access to the supply pins of the ADG5208F. VDD, GND, and VSS on J5 link to the appropriate pins on the ADG5208F. For dual supply voltages, the evaluation board can be powered from ±5 V to ±22 V. For single supply voltages the GND and VSS terminals must be connected together, and power the evaluation board with 8 V to 44 V. Additionally, an on-board LDO regulator is provided for a digital control voltage. If necessary, a secondary voltage source can be connected to EXT_VL and used to control the digital voltages. To use EXT_VL, move the 0 Ω resistor from R14 to R13. Do not expose the on-board LDO regulator to voltages greater than 28 V; remove R15 and supply an alternative digital voltage via EXT_VL, if required.

INPUT SIGNALS

Two screw connectors are provided to connect to both the source and drain pins of the ADG5208F. Additional subminiature Version B (SMB) connector pads are available if extra connections are required. The ADG5208F is overvoltage protected on the source side, and each source terminal (S1 to S8) can be presented with a voltage of up to +55 V or −55 V. See the ADG5208F data sheet for more details.

Each trace on the source and drain side includes two sets of 0603 pads, which can be used to place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can be used to create a simple resistor-capacitor (RC) filter.

The ADG5208F uses a parallel interface to control the operation of the switches. The switch operation can be manually controlled using the SW1 to SW4 switches, or an external controller can be interfaced directly to the control pins by using the SMB connectors (EN, A0, A1, and A2) and removing the 0 Ω R31, R33, R35 and R37 resistors. See Table 1 for the logic control truth table.

JUMPER SETTINGS

SWITCHES AND 0 Ω RESISTORS

Switches are used to control the ADG5208F manually and 0 Ω resistors are used to configure the digital control voltage. Table 2 shows a summary of the switches and 0 Ω resistors and how they are used on the evaluation board.

Use Switch SW2 to Switch SW4 to control the switches of the ADG5208F. Position L is tied to GND and sets the logic low, and Position H is tied to VL and sets the logic high.

Use SW1 to enable or disable the device. Position DIS is tied to GND and disables the device, and Position EN is tied to VL and enables the device.

Resistor R15 connects the on-board LDO regulator to the VDD supply. Remove this resistor to protect the LDO regulator from voltages higher than 28 V. Change the 0 Ω resistor to Position R13 to use an alternative digital voltage connected to DC_V1.

Table 1. ADG5208F Truth Table

SW4 (A2)	SW3 (A1)	SW2 (A0)	SW1 (EN)	Connected Sx
X[1]	X[1]	X[1]	DIS	All switches off
L	L	L	EN	S1
L	L	H	EN	S2
L	H	L	EN	S3
L	H	H	EN	S4
H	L	L	EN	S5
H	L	H	EN	S6
H	H	L	EN	S7
H	H	H	EN	S8

[1] X means don't care.

SMB CONNECTORS

The parallel interface of the ADG5208F is controlled manually using the link headers of Switch SW1 to Switch SW4, or it can be accessed using the SMB connectors, EN, A0, A1, and A2. To use the SMB connectors, remove the 0 Ω R31, R33, R35, and R37 resistors.

Table 2. Switch and 0 Ω Resistor Descriptions

Label	Position	Description
SW1	EN	Logic 0 on the EN pin
	DIS	Logic 1 on the EN pin
SW2	L	Logic 0 on the A0 pin
	H	Logic 1 on the A0 pin
SW3	L	Logic 0 on the A1 pin
	H	Logic 1 on the A1 pin
SW4	L	Logic 0 on the A2 pin
	H	Logic 1 on the A2 pin
R13, R14	R14	On-board LDO regulator digital voltage
	R13	EXT_VL digital voltage
R15	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
R31, R33, R35, R37	Inserted	SW1 to SW4 control digital logic
	Removed	SMB connectors control digital logic

EVALUATION BOARD SCHEMATICS AND ARTWORK

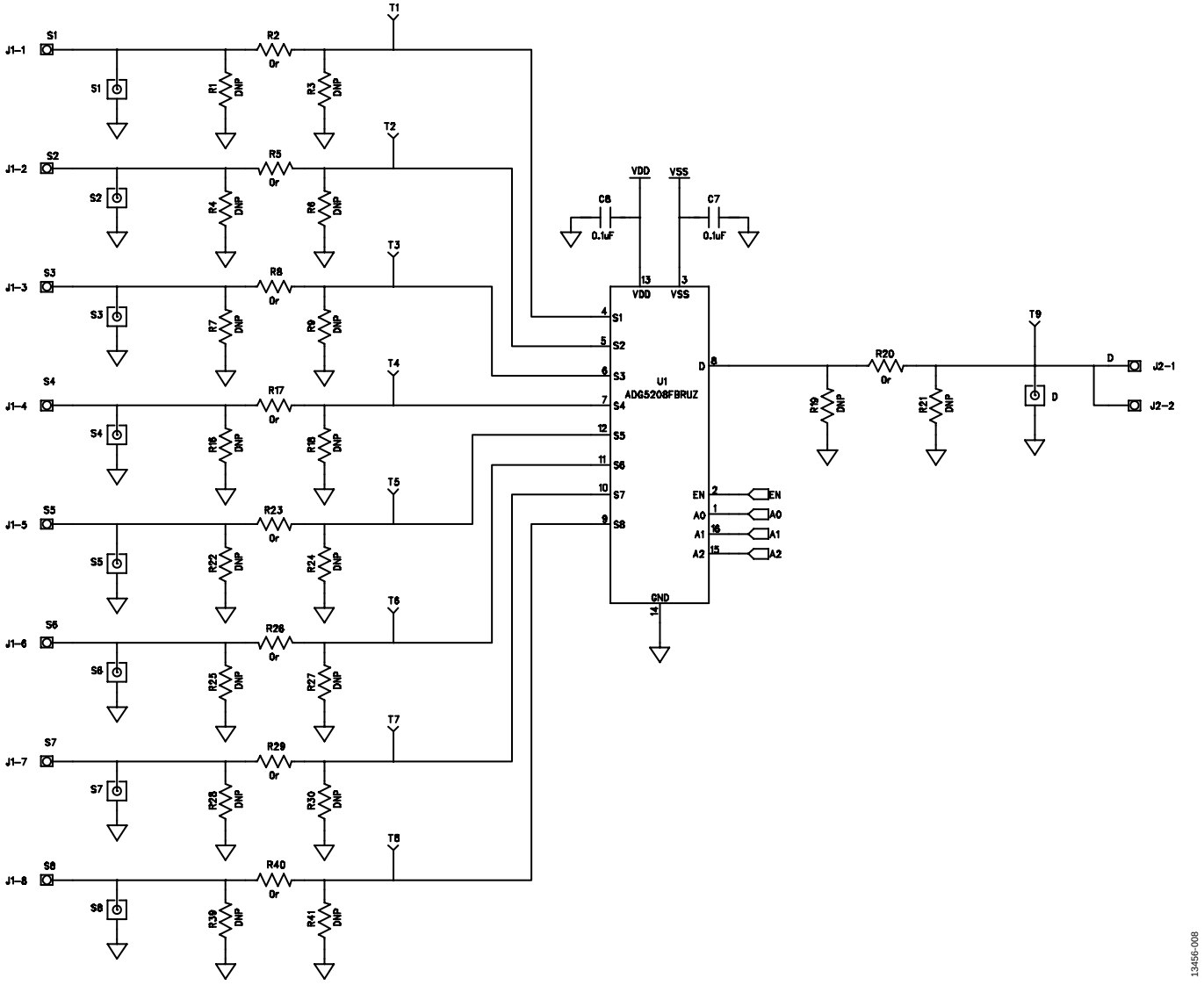


Figure 3. ADG5208F Evaluation Board Schematic (Part 1)

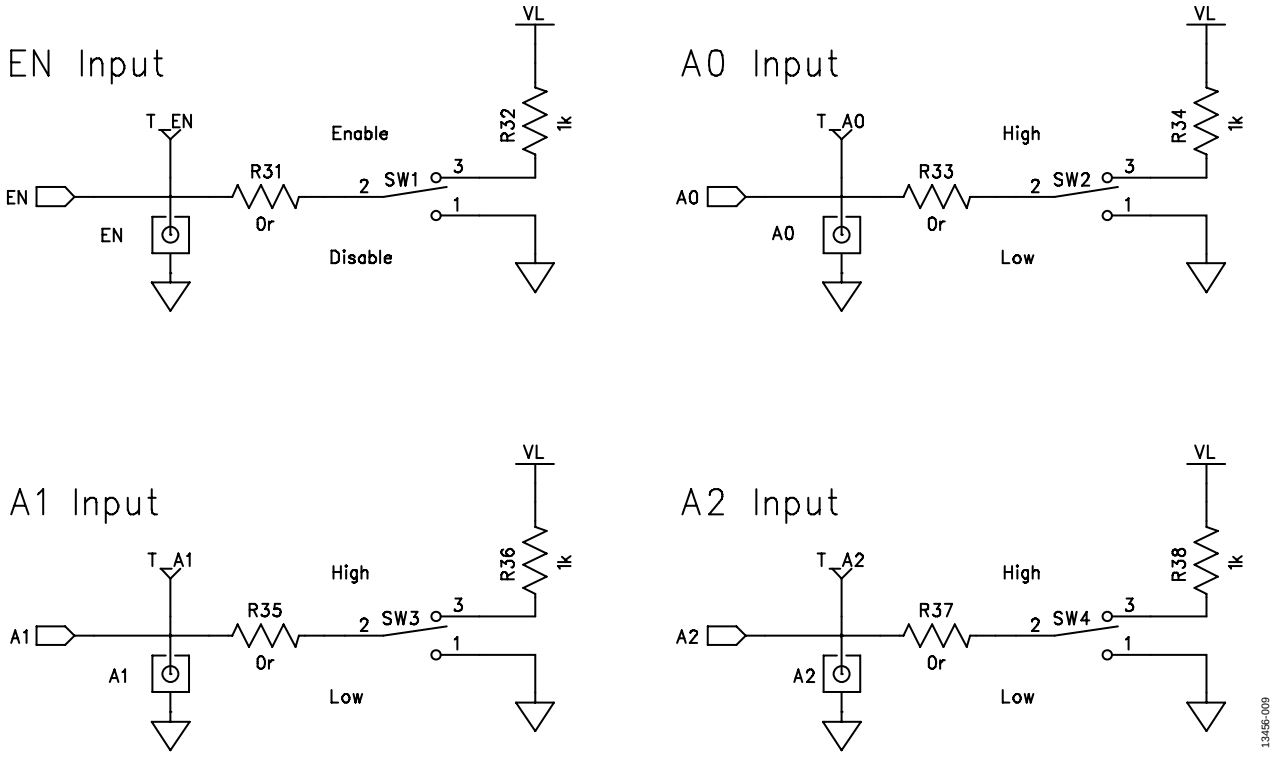


Figure 4. ADG5208F Evaluation Board Schematic (Part 2)

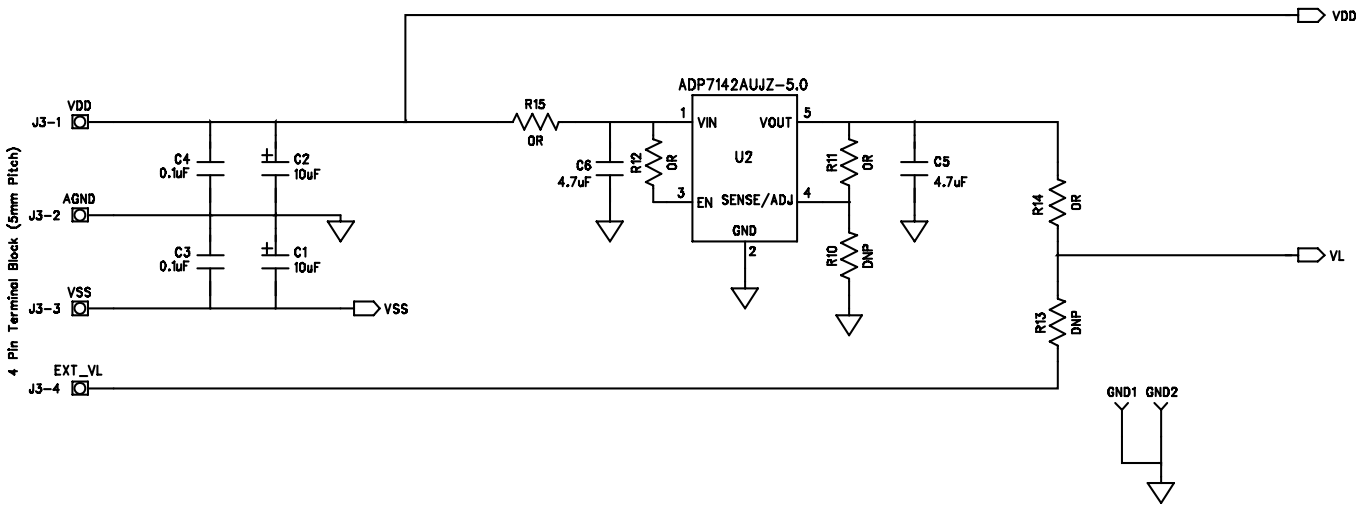


Figure 5. ADG5208F Evaluation Board Schematic (Part 3)

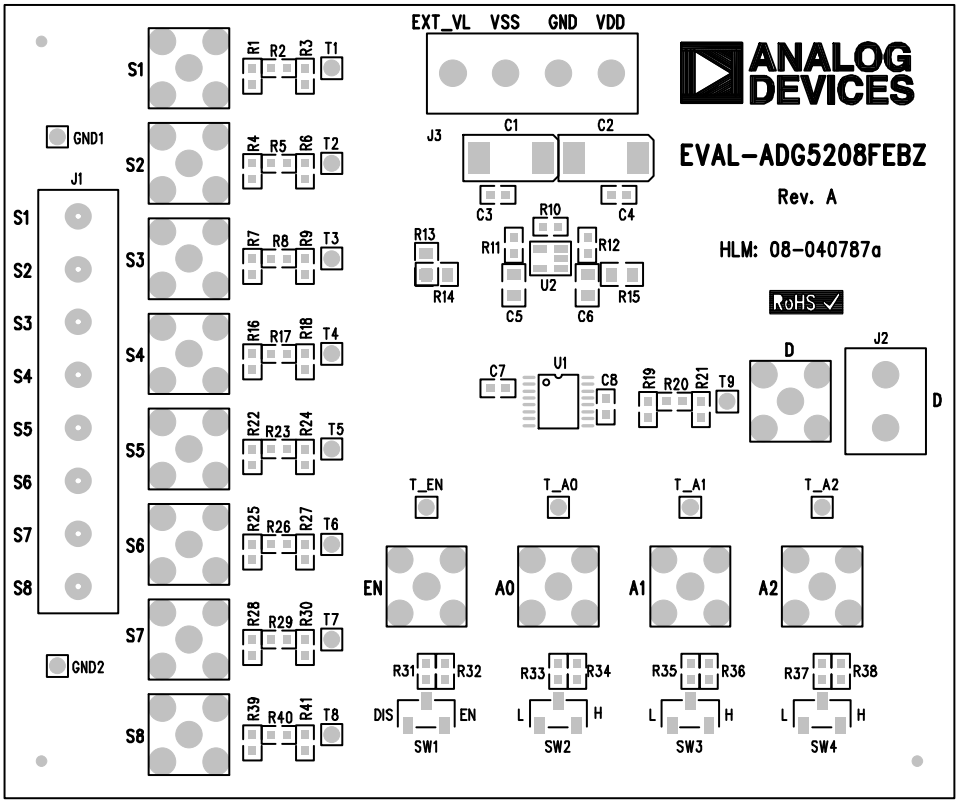


Figure 6. EVAL-ADG5208FEBZ Silkscreen

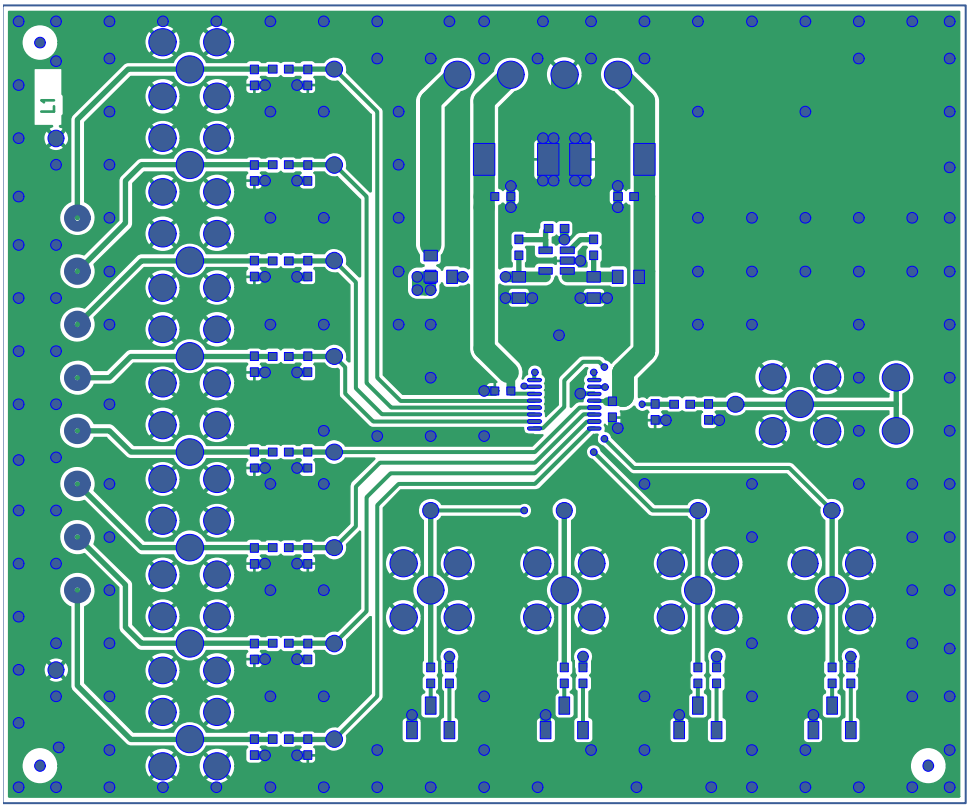


Figure 7. EVAL-ADG5208FEBZ Top Layer

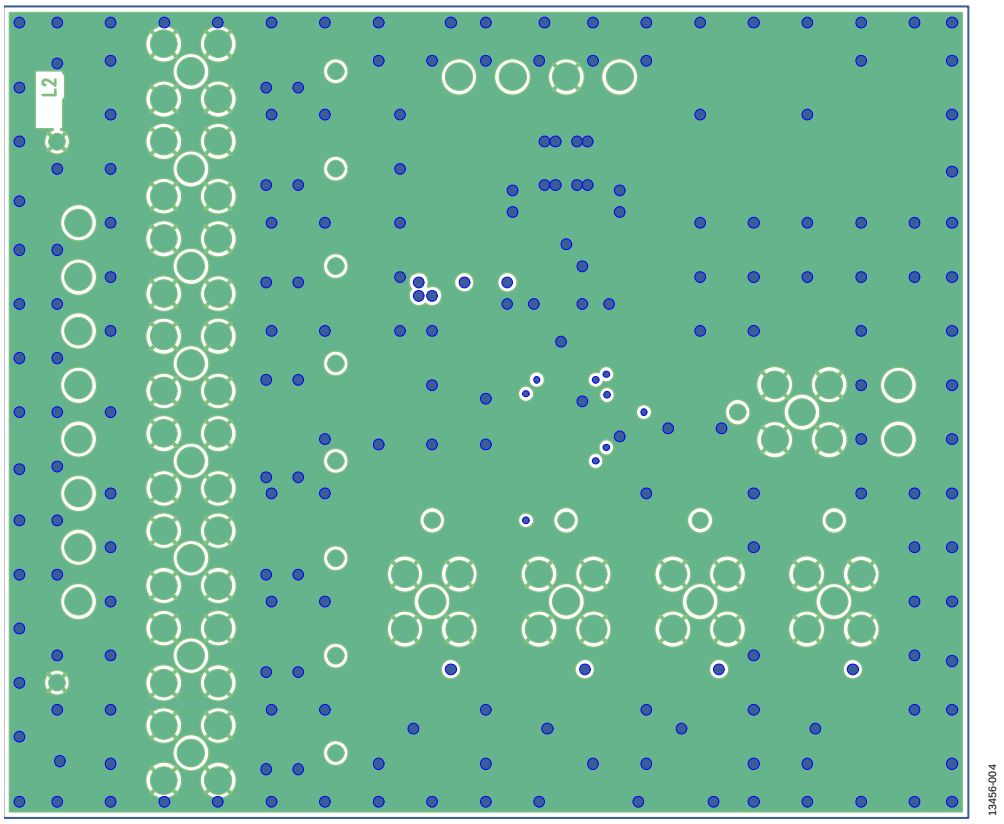


Figure 8. EVAL-ADG5208FEBZ Layer 2

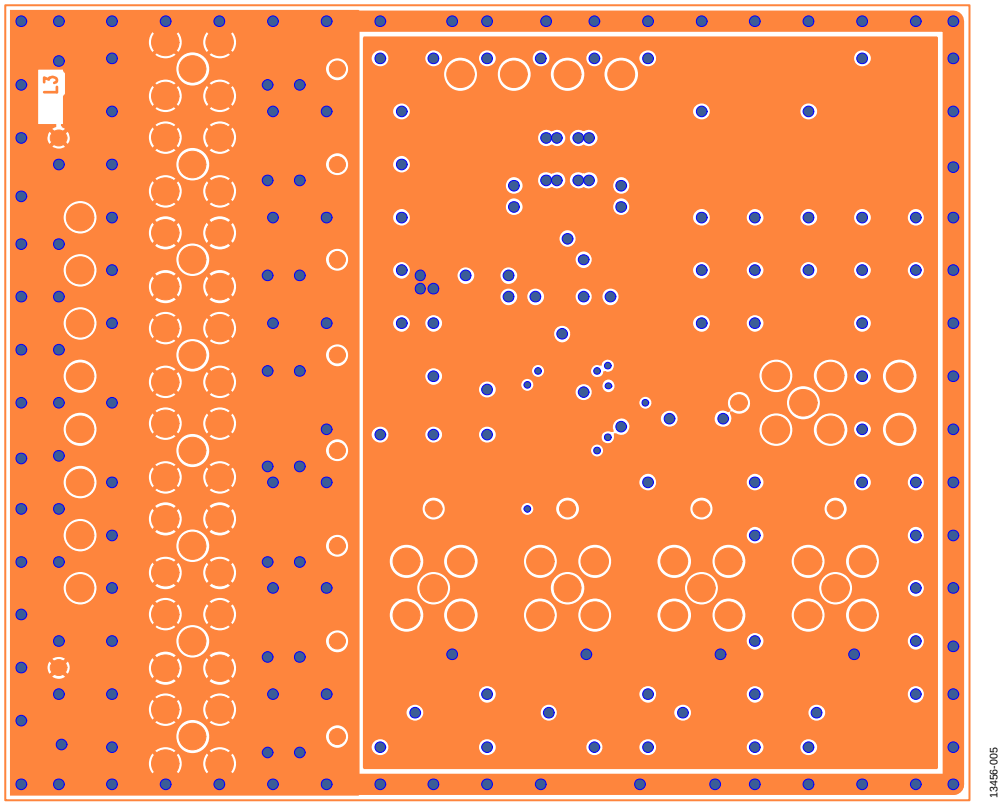


Figure 9. EVAL-ADG5208FEBZ Layer 3

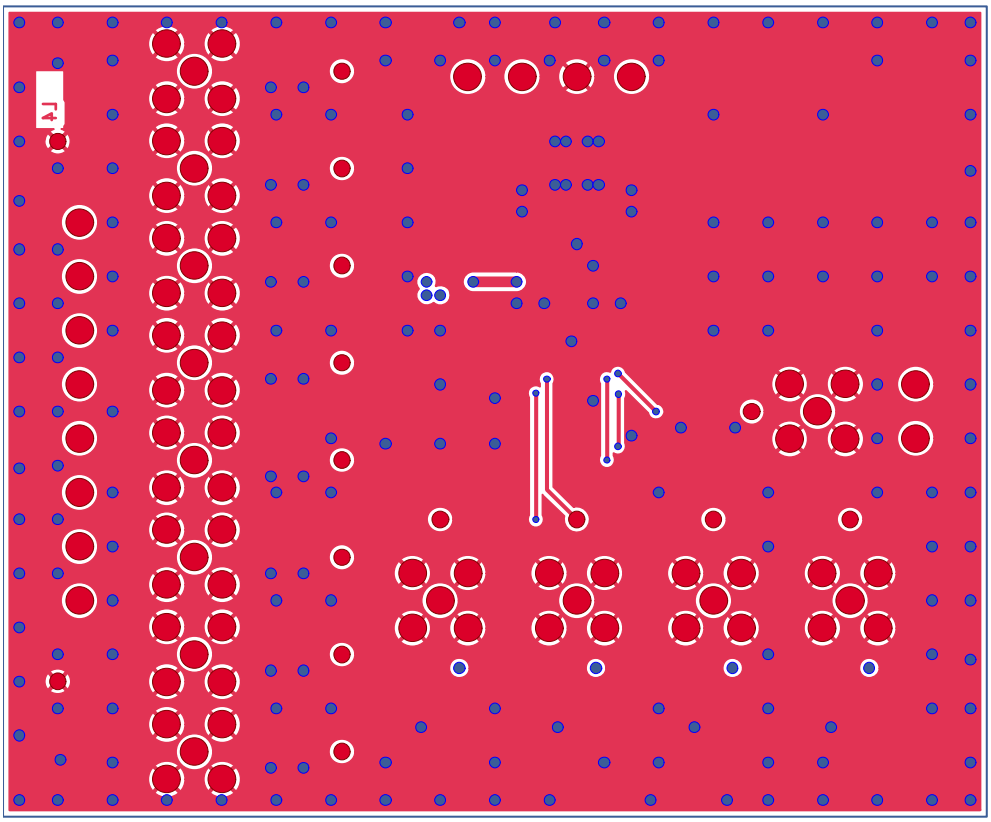


Figure 10. EVAL-ADG5208FEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Manufacturer Part Number	Stock Code
A0 to A2, EN	50 Ω, straight, SMB jacks	SMB1251B1-3GT30G-50	FEC 1111349
C3, C4, C7, C8	50 V, X7R, multilayer ceramic, 0603 size, 0.1 µF capacitors	GRM188R71H104KA93D	FEC 882-0023
C1, C2	50 V, tantalum, D size, 10 µF capacitors	TAJD106K050RNJ	FEC 143-2387
C5, C6	Ceramic, multilayer, 4.7 µF capacitors	C2012X5R1H475K125AB	FEC 2346932
D	50 Ω, SMB socket	SMB1251B1-3GT30G-50	Do not insert
GND1, GND2	Black test points	20-2137	FEC 873-1128
J1	8-pin terminal block (5 mm pitch)	CTB5000/8	FEC 9633014
J2	2-pin terminal block (5 mm pitch)	CTB5000/2	FEC 151789
J3	4-pin terminal block (5 mm pitch)	CTB5000/4	FEC 151791
R2, R5, R8, R11, R12, R17, R20, R23, R26, R29, R31, R33, R35, R37, R40	0603, 1%, 0 Ω resistors	MC0063W06030R	FEC 9331662
R1, R3, R4, R6, R7, R9, R10, R16, R18, R19, R21, R22, R24, R25, R27, R28, R30, R39, R41	SMD, 0603 resistors	Not applicable	Do not insert
R32, R34, R36, R38	1 kΩ, 0.063 W, 1%, 0603 resistors	MC0063W060311K	FEC 9330380
R14, R15	0805, 1%, 0 Ω resistors	MC01W08050R	FEC 9333681
R13	SMD, 0805 resistor	Not applicable	Do not insert
S1 to S8	50 Ω, SMB sockets	SMB1251B1-3GT30G-50	Do not insert
SW1 to SW4	Single-pole, double throw (SPDT), SMT slide switches	CAS-120TA	Digi-Key CAS120JCT-ND
T1 to T9, T_A0 to T_A2, T_EN	Red test points	20-313137	FEC 873-1144
U1	Fault protection, −0.4 pC Q_{INJ}, 8:1 multiplexer	ADG5208FBRUZ	ADG5208FBRUZ
U2	Linear regulator, 5.0 V, LDO	ADP7142AUJZ-5.0	ADP7142AUJZ-5.0-R7

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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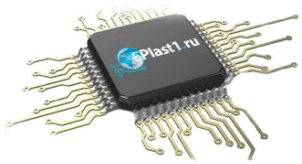
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