ATA8520D

Single-Chip SIGFOX RF Transceiver

DATASHEET

Features

- Fully integrated, single-chip RF transceiver (SIGFOX™ compliant)
- System-on-chip solution including SIGFOX related protocol handling for modem operation
- AVR® microcontroller core with embedded firmware, SIGFOX, protocol stack and ID/PAC
- Supports up- and downlink operation, i.e. transmit and receive of data telegrams with SIGFOX base stations
- Operating frequencies: for uplink 868.0 to 868.6MHz, for downlink 869.4 to 869.65MHz
- Low current consumption: 32.7mA during transmit and 10.4mA during receive operation
- Typical OFF mode current: 5nA (maximum 600nA at V_S = +3.6V and T = +85°C)
- Data rate: 100bit/s with DBPSK modulation for uplink and 600bit/s with GFSK modulation for downlink
- SPI interface for data access and transceiver configuration and control
- Event signal indicates the status of the IC to an external microcontroller
- Power-up (typical 10ms OFF mode -> IDLE mode)
- Supply voltage ranges 1.9V to 3.6V and 2.4V to 5.5V (SIGFOX compliant supply range 3V±5% and 3.3V to 5.5V)
- Temperature range –40°C to +85°C
- ESD protection at all pins (±4kV HBM, ±200V MM, ±750V FCDM)
- Small 5×5mm QFN32 package/pitch 0.5mm

Applications

SIGFOX compatible modem for long-range, low-power and low-cost applications using the SIGFOX network

- Home and building automation
- Alarm and security systems
- Smart environment and industrial
- Smart parking
- Tracking
- Metering

1. General Description

1.1 Introduction

The Atmel® ATA8520D is a highly integrated, low-power RF transceiver with an integrated AVR® microcontroller for applications using the wide area SIGFOX™ network

The Atmel ATA8520D is partitioned into three sections: an RF front end, a digital baseband and the low-power 8-bit AVR microcontroller. The product is designed for the ISM frequency band in the range of 868.0MHz to 868.6MHz and 869.4 to 869.65MHz. The external part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The transmit path uses a closed loop fractional-N modulator.

The SPI interface enables external control and device configuration.

1.2 System Overview

Figure 1-1. Circuit Overview

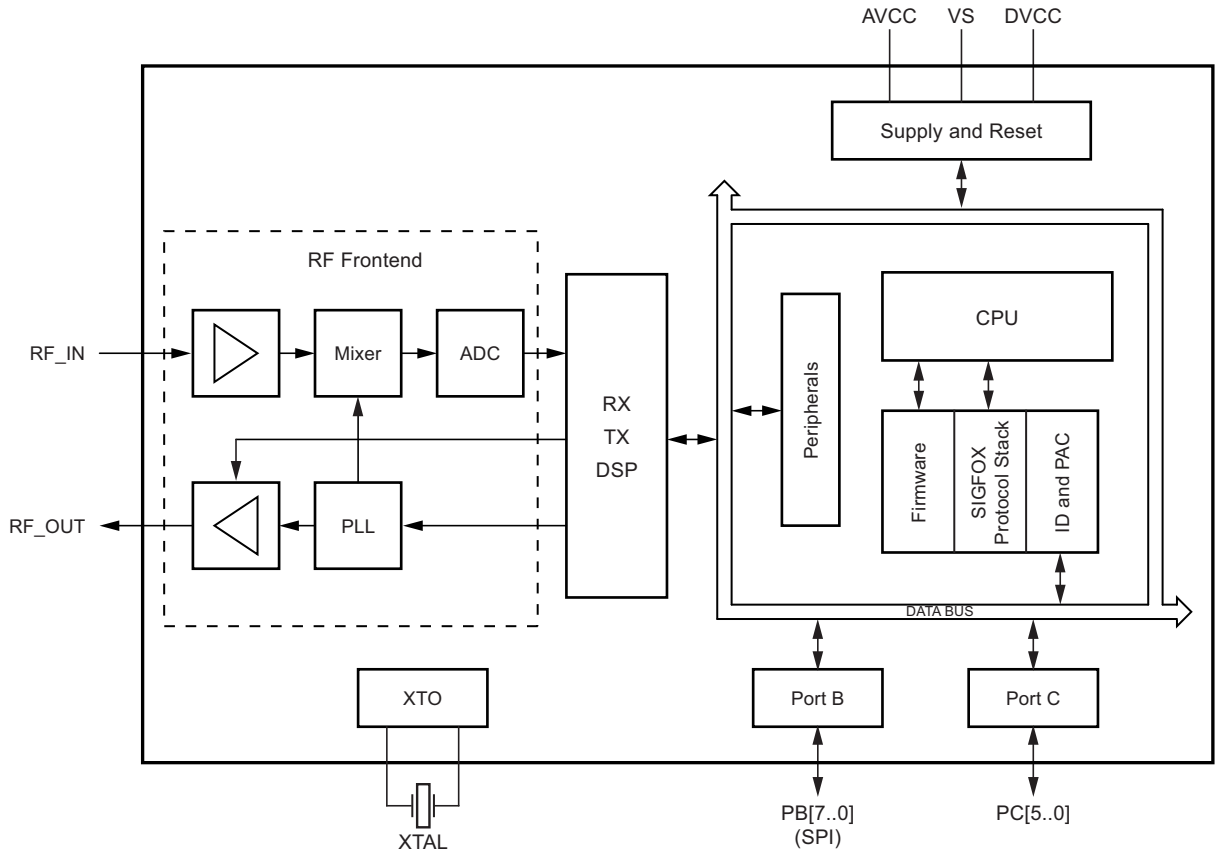


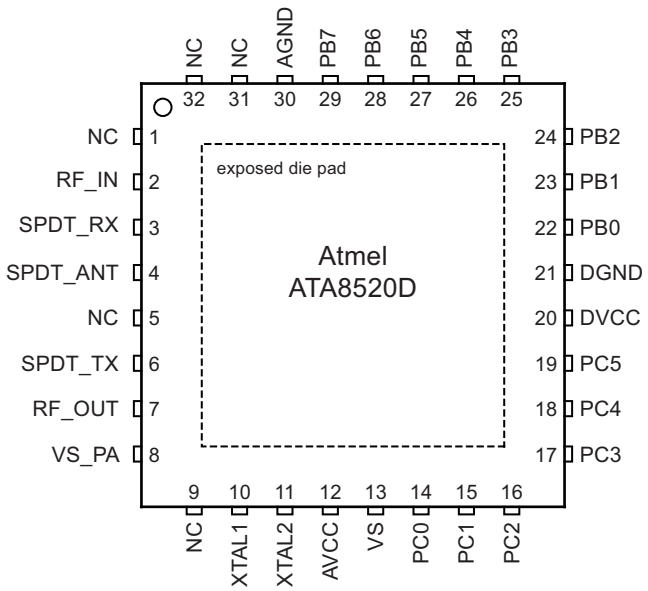
Figure 1-1 shows an overview of the main functional blocks of the Atmel ATA8520D. External control of the Atmel ATA8520D is performed through the SPI pins SCK, MOSI, MISO, and NSS. The functionality of the device is defined by the internal firmware and processed by the AVR. SPI commands are used to control the device and to start the data telegram transmission. The end of the telegram transmission is signaled to an external microcontroller on pin 28 (PB6/EVENT).

It is important to note that all PWRON and NPWRON pins (PC1..5, PB4, PB7) are active in OFF mode. This means that even if the Atmel ATA8520D is in OFF mode and the DVCC voltage is switched off, the power management circuitry within the Atmel ATA8520D biases these pins with VS.

The AVR microcontroller ports can be used as button inputs, LED drivers, EVENT pin, general purpose digital inputs, or wake-up inputs, etc. Functionality of these ports is already implemented in the firmware.

1.3 Pinning

Figure 1-2. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 1-1. Pin Description

Pin No.	Pin Name	Type	Description	
1	NC		Connected to GND	
2	RF_IN	Analog	Receiver input	
3	SPDT_RX	Analog	Rx switch output (damped signal output)	
4	SPDT_ANT	Analog	Antenna input (downlink) and output (uplink) of the SPDT switch	
5	NC		Leave open	
6	SPDT_TX	Analog	TX mode input of the SPDT switch	
7	RF_OUT	Analog	Power amplifier output	
8	VS_PA	Analog	Power amplifier supply. 3V supply: connect to VS. 5V supply: leave open. Use SPI command “Write System Configuration” (0x11) to enable 5V supply mode.	
9	NC	–	Connected to GND	
10	XTAL1	Analog	Crystal oscillator pin 1 (input)	
11	XTAL2	Analog	Crystal oscillator pin 2 (output)	
12	AVCC	Analog	RF front-end supply regulator output	
13	VS	Analog	Main supply voltage input	
14	PC0	Digital	Main	: NRESET
15	PC1	Digital	Main Alternate	: AVR Port C1 : NPWRON1
16	PC2	Digital	Main Alternate	: AVR Port C2 : NPWRON2
17	PC3	Digital	Main Alternate	: AVR Port C3 : NPWRON3

Table 1-1. Pin Description (Continued)

Pin No.	Pin Name	Type	Description	
18	PC4	Digital	Main Alternate	: AVR Port C4 : NPWRON4
19	PC5	Digital	Main Alternate	: AVR Port C5 : NPWRON5
20	DVCC	–	Digital supply voltage regulator output	
21	DGND	–	Digital ground	
22	PB0	Digital	Main	: control Front-End-Module; ='1' enable, ='0' disable
23	PB1	Digital	Main	: SCK
24	PB2	Digital	Main	: MOSI (SPI master out Slave in)
25	PB3	Digital	Main	: MISO (SPI master in Slave out)
26	PB4	Digital	Main	: PWRON
27	PB5	Digital	Main	: NSS
28	PB6	Digital	Main	: EVENT
29	PB7	Digital	Main Alternate	: ='1' TX active, ='0' RX active : NPWRON6
30	AGND	–	Analog ground	
31	NC	–	Connected to GND	
32	NC	–	Connected to GND	
	GND	–	Ground/backplane on exposed die pad	

1.4 Applications

This section provides application examples for the two supply modes for the Atmel® ATA8520D device. In addition the recommended PCB design and layout is described to achieve the SIGFOX™ certification.

1.4.1 3V Application Example

Figure 1-3. 3V Application with External Microcontroller

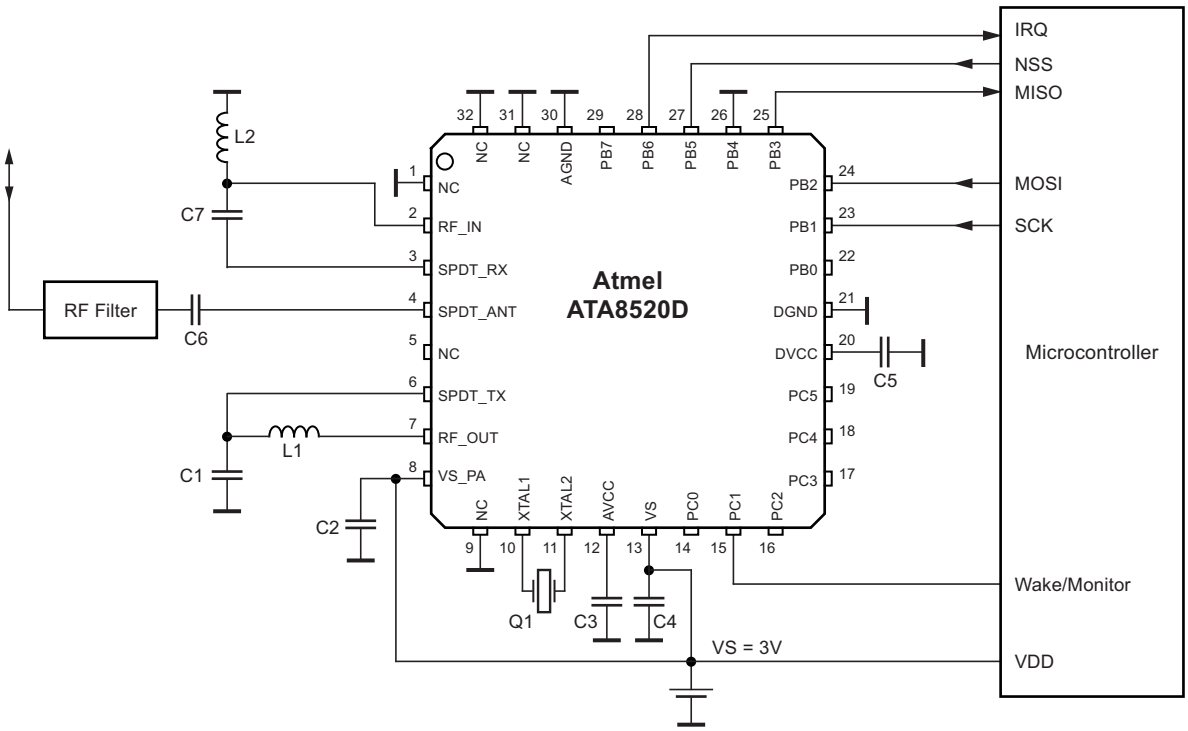


Figure 1-3 shows a typical application circuit with an external host microcontroller operating from a 3V lithium cell. The Atmel ATA8520D stays in OFFMode until NPWRON1 (PC1) is used to wake it up. In OFFMode the Atmel ATA8520D draws typically less than 5nA at 25°C.

In OFFMode all Atmel ATA8520D AVR® ports PB0..PB7 and PC0..PC5 are switched to input. PC0..PC5 and PB7 have internal pull-up resistors ensuring that the voltage at these ports is VS. PB0..PB6 are tri-state inputs and require additional consideration. PB1, PB2, and PB5 have defined voltages since they are connected to the output of the external microcontroller. PB4 is connected to ground to avoid unwanted power-ups. PB0, PB3 and PB6 do not require external circuitry since the internal circuit avoids transverse currents in OFFMode. The external microcontroller has to tolerate the floating inputs. Otherwise additional pull-down resistors are required on these floating lines.

Typically, the Atmel ATA8520D wake-up is done by pulling NPWRON1 (pin 15) to ground.

RF_OUT is matched with C1/L1 for 50Ω antenna connection and RF_IN with the components C7/L2. The internal SPDT switch uses SPDT_RX for receive and SPDT_TX for transmit connection with SPDT_ANT to be connected to the external 50Ω antenna. The RF filter is required to suppress unwanted side and spurious emissions. The design of this filter depends on the final PCB and system layout and is subject to SIGFOX and ETSI certification procedures.

Together with the fractional-N PLL within the Atmel ATA8520D, an external crystal is used to set the Tx and Rx frequency. Accurate load capacitors for this crystal are integrated to reduce the system part count and cost. Only four supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC, VS, and VS_PA of the Atmel ATA8520D. The exposed die pad is the RF and analog ground of the Atmel ATA8520D. It is connected directly to AGND via a fused lead. The Atmel ATA8520D is controlled using specific SPI commands via the SPI interface.

Figure 1-4. 3V Application with External Microcontroller and Front-End-Module

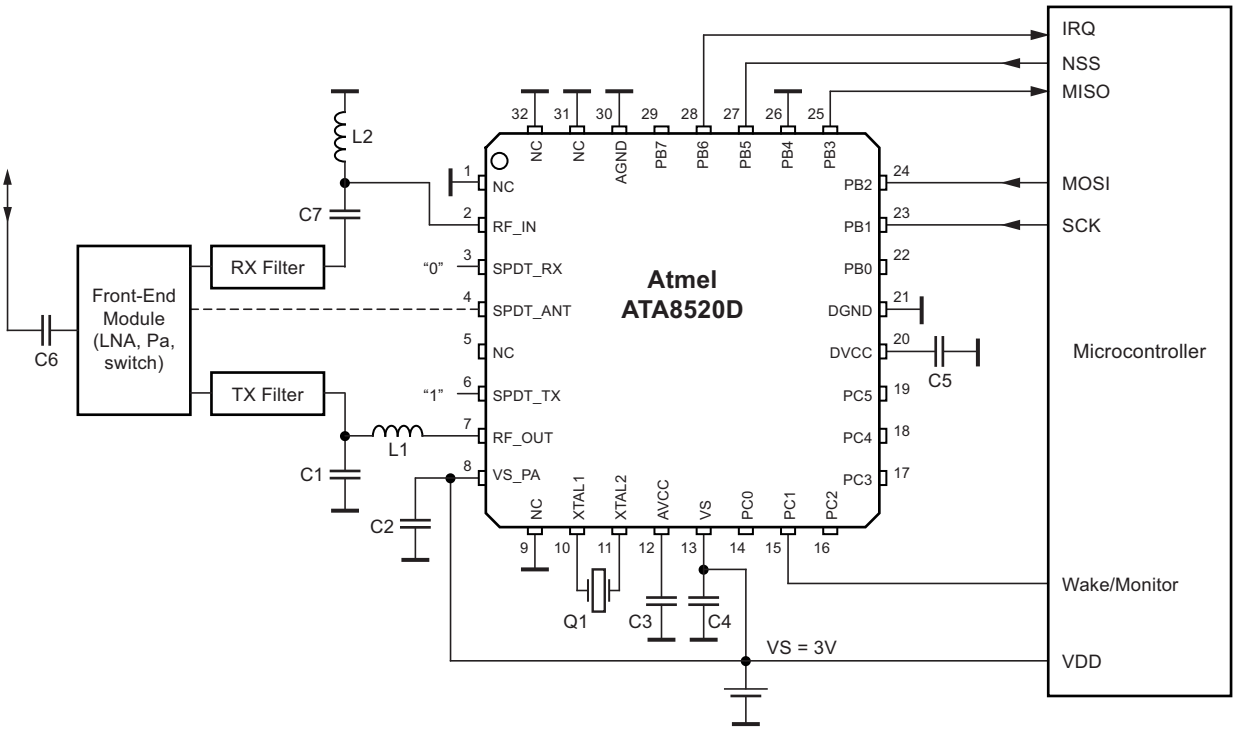


Figure 1-4 shows an alternative for the usage of external filter and amplifier components using a front-end-module. This FEM typically includes an antenna switch, a LNA for the receive direction and a PA for the transmit connection in one device. The RX and TX filters are additional to increase out-of-band jamming immunity in receive direction and to reduce spurious emissions in transmit direction. For these filters SAW components are typically used. The pins PB0 and PB7 can be used to control the FEM or the unused internal SPDT switch which is controlled by the Atmel® ATA8520D for transmit and receive operation.

Applications which are not using the receive function can connect the antenna to RF_OUT without using the internal SPDT switch. The receive and SPDT pins are then connected to GND.

1.4.2 5V Application Example

Figure 1-5. 5V Application with External Microcontroller

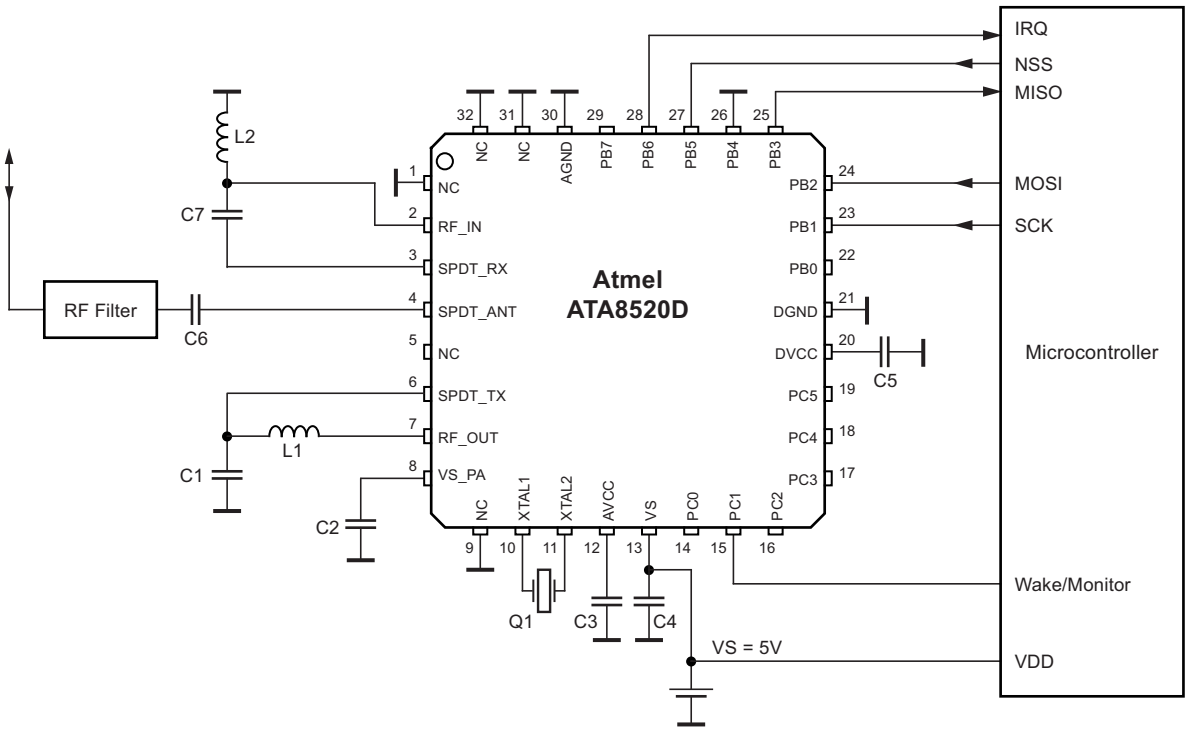


Figure 1-5 shows a typical application circuit with an external host microcontroller operating from a 5V supply. This application differs from the 3V supply mode that VS is not connected to VS_PA. Instead an internal LDO must be activated using the SPI command “Write System Configuration” (0x11) after powering the device and before transmitting a data telegram.

2. System Functional Description

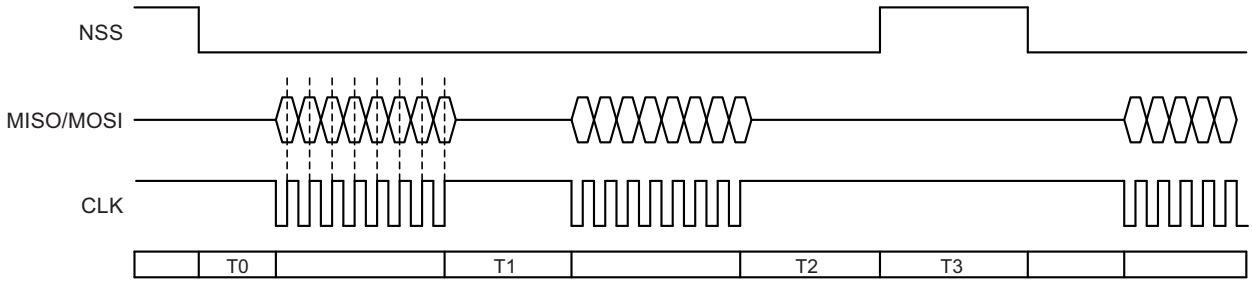
2.1 SPI Command Interface

The SPI command interface requires a timing setup as described in the following section and provides a set of commands to control the operation of the Atmel® ATA8520D device. The SPI transmission occurs with MSB first.

2.1.1 SPI Timing

The SPI communication requires a special timing to prevent data corruption. The SPI peripheral uses a SCK frequency of 125kHz for the bit transmission and requires timing delays between the CS signals and the start and stop of the SPI communication as shown in Figure 2-1.

Figure 2-1. SPI Timing Parameters



T0 ≥ 65µs, T1 ≥ 40µs, T2 ≥ 100µs, T3 ≥ 50µs, SPI CLK ≤ 125kHz (SPI Mode 0: CPOL = CPHA = 0)

2.1.2 SPI Command Set

The following SPI commands are available to control the Atmel ATA8520D operation from a host microcontroller.

2.1.2.1 System Reset

This command uses the system internal WDT to do a complete hardware reset of the Atmel ATA8520D. Resetting the device takes ~10ms.Afterwards the system restarts and generates an event on the EVENT signal after ~10ms. This event will be cleared with the “Get Status” SPI command (0x0A).

Master	System Reset (0x01)
ATA8520D	Dummy

2.1.2.2 I/O Init

The I/O lines of port C can be used as additional I/O lines for an application. The port C I/O Init command defines the internal data direction register of output port PORTC (DDRC). Pin PC0 is used as NRESET signal and will always be an input pin, i.e. bit 0 will be written as 0 to be an input pin.

Master	I/O Init (0x02)	DDRC content
ATA8520D	Dummy	Dummy

2.1.2.3 I/O Write

The I/O write command writes directly to the output port register PORTC to set the I/O pins. Pin PC0 is used as NRESET signal and will always be an input pin with enabled pull-up, i.e. bit 0 will be written as 1 to enable the internal pull-up resistor.

Master	I/O Init (0x03)	PORTC content
ATA8520D	Dummy	Dummy

2.1.2.4 I/O Read

The I/O read command reads the status of the I/O pins directly from the input port register PINC. Pin PC0 is used as NRESET signal and will always be read as 1.

Master	I/O Read (0x04)	Dummy	Dummy
ATA8520D	Dummy	Dummy	PINC content

2.1.2.5 OFF Mode

The OFF mode command puts the Atmel® ATA8520D into off mode. To wake up the Atmel ATA8520D device, one of the power on lines has to be activated, i.e. set PWRON line to high or NPWRONx line to low. To switch the device into OFF mode the power on lines have to be de-activated before otherwise the device will remain in the on state.

Master	OFF Mode (0x05)
ATA8520D	Dummy

2.1.2.6 Atmel Version

The Atmel version command reads the version information including a major and a minor version number.

Master	Atmel Version (0x06)	Dummy	Dummy	Dummy
ATA8520D	Dummy	Dummy	MajorVers	MinorVers

2.1.2.7 Write TX Buffer

The write TX buffer command fills the TX buffer to be sent with the next SIGFOX™ data frame with payload data of up to 12 bytes. The buffer can hold any number of bytes ranging from 0 to 12 bytes and are not buffered, i.e. a new SPI command will override the previous data.

Master	Write TX Buffer (0x07)	RF TX **Num** bytes	RF TX Bytes 0	.....	RF TX **Num** bytes-1
ATA8520D	Dummy	Dummy	Dummy		Dummy

2.1.2.8 SIGFOX Version

The SIGFOX version reads the SIGFOX library version information as a text string with N = 11 characters.

Master	SIGFOX Version (0x09)	Dummy	Dummy	.....	Dummy
ATA8520D	Dummy	Dummy	SFX Verinfo[0]		SFX Verinfo[N]

2.1.2.9 Get Status

The get status command reads the internal status of the device. Issuing this command clears the systems event line (PB6) and the status bytes. The event line is set to low when:

a. System is ready after power-up or reset
b. Finishes the transmit/receive operation
c. finishes a temperature and supply measurement
d. finishes the EEPROM write operation.

The following status information is read after the event line is activated, i.e. polling using the Get Status command is not necessary:

Hardware SSM status

Atmel® status:

- Bit6: System ready to operate (system ready event)
- Bit5: Frame sent (frame ready event)
- Bit4 to Bit1: Error code
  - 0000: no error
  - 0001: command error / not supported
  - 0010: generic error
  - 0011: frequency error
  - 0100: usage error
  - 0101: opening error
  - 0110: closing error
  - 0111: send error
- Bit0: PA on/off indication

SIGFOX™ status:

- 0x00: No error
- 0x01: Manufacturer error
- 0x02: ID or key error
- 0x03: State machine error
- 0x04: Frame size error
- 0x05: Manufacturer send error
- 0x06: Get voltage/temperature error
- 0x07: Close issues encountered
- 0x08: API error indication
- 0x09: Error getting PN9
- 0x0A: Error getting frequency
- 0x0B: Error building frame
- 0x0C: Error in delay routine
- 0x0D: callback causes error
- 0x0E: timing error
- 0x0F: frequency error
- 0x10: receiving frame error

Master	Get Status (0x0A)	Dummy	Dummy	Dummy	Dummy
ATA8520D	Dummy	Dummy	SSM status	Atmel status	SIGFOX status

2.1.2.10 Send Single Bit

This command sends a data bit (0/1) within a SIGFOX RF frame as specified by SIGFOX. An event on the EVENT signal is generated when finished.

Master	Send Bit (0x0B)	Bit Status (0/1)
ATA8520D	Dummy	Dummy

2.1.2.11 Send Frame

The send frame command triggers the start of a frame transmit process. The payload data has to be written into the TX buffer before using the write TX buffer command. The transmit operation will take ~7 seconds and will generate an event on the EVENT signal when finished. With pins PB0 and PB7 a front-end-module can be controlled (see Section 2.1.4 “System and Pin Configuration” on page 15).

Master	Send Frame (0x0D)
ATA8520D	Dummy

2.1.2.12 Send/Receive Frame

The send/receive frame command triggers the start of a frame transmit process followed by a receive process. The payload data has to be written into the TX buffer before using the write TX buffer command. The transmit and receive operation will take up to 50 seconds and will generate an event on the EVENT signal when finished. The received data bytes can be read with the SPI command (0x10). With pins PB0 and PB7 a front-end-module can be controlled (see Section 2.1.4 “System and Pin Configuration” on page 15).

Master	Send/Receive Frame (0x0E)
ATA8520D	Dummy

2.1.2.13 Get PAC

The get PAC command will read the 16 byte PAC information which is used for the device registration process at the SIGFOX backend. Only the 8 lower bytes (0) .. (7) are used, the remaining 8 upper bytes (8) .. (15) are read as 0.

Master	Get PAC (0x0F)	Dummy	Dummy	.....	Dummy
ATA8520D	Dummy	Dummy	PAC ID[0]		PAC ID[15]

2.1.2.14 Read RX Buffer

This command triggers the read out of the received data packet. The packet length is always 8 bytes.

Master	Read RX Buffer (0x10)	Dummy	Dummy	.....	Dummy
ATA8520D	Dummy	Dummy	RX Byte 0		RX Byte 7

2.1.2.15 Write System Configuration

The Write System Configuration command writes the configuration data for the port C and the system configuration into the internal EEPROM. This changes will be applied by performing a system reset. An event on the EVENT signal is generated when finished. DDRC register defines the data direction for the port C pins (0: input, 1: output). PORTC register defines the output level for an output pin and enables a pull-up resistor for input pins when set. SysConf is used to configure the supply voltage and the up-/downlink operation (see Section 2.1.4 “System and Pin Configuration” on page 15).

Master	Write Sys Conf (0x11)	DDRC	PORTC	0x02	SysConf
ATA8520D	Dummy	Dummy	Dummy	Dummy	Dummy

2.1.2.16 Get ID

The get ID command will read the 4 byte ID information which is used for the device registration process at the SIGFOX™ backend.

Master	Get ID (0x12)	Dummy	Dummy	.....	Dummy
ATA8520D	Dummy	Dummy	UID[3]		UID[0]

2.1.2.17 Read Supply Temperature

This command triggers the read out of the measured supply voltage in idle and active mode and the device temperature. To trigger a measurement the SPI command (0x14) has to be used. The return voltage level is in mV and the temperature value has to be calculated as T = (TM – 500)/10 in °C. All values are of type 16 bit unsigned integer (with high and low byte).

Master	Read Supply Temperature (0x13)	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy
ATA8520D	Dummy	Dummy	VH idle	VL idle	VH active	VL active	TMH	TML

2.1.2.18 Start Measurement

This command triggers the measurement of the supply voltages and the temperature value. An event on the EVENT signal is triggered when finished which is cleared by reading the supply and temperature values.

Master	Trigger Measurement (0x14)
ATA8520D	Dummy

2.1.2.19 Trigger TX Test

This command triggers the uplink test procedure defined by SIGFOX. An event on the EVENT signal is generated when finished.

The command parameter are:

- FRL, FRH: number of frames to be send. Each frame is send 3 times [0...32768, –1 for infinite].
- CHL, CHH: Channel number used for transmission [0...480, –1 is for hopping deactivation].

Master	Trigger TX Test (0x15)	FRL	FRH	CHL	CHH
ATA8520D	Dummy	Dummy	Dummy	Dummy	Dummy

2.1.2.20 Trigger RX Test

This command triggers the downlink test procedure defined by SIGFOX. An event on the EVENT signal is generated when finished.

The command parameter are:

- CHL, CHH: Channel number used for reception [0...480].
- SQL, SQH: sequence number for permanent reception.

Master	Trigger RX Test (0x16)	SQL	SQH	CHL	CHH
ATA8520D	Dummy	Dummy	Dummy	Dummy	Dummy

2.1.2.21 Send CW

This command triggers the transmission of a continuous carrier on the programmed RF frequency as defined by SIGFOX.

Master	Send CW (0x17)	On=0x11/Off=0x00
ATA8520D	Dummy	Dummy

2.1.2.22 Set TX Frequency

Set TX center frequency temporarily for testing purposes. This settings are lost after reset or when switching the device off. The frequency value is an unsigned 32-bit integer within the range [868.000.000Hz to 868.600.000Hz]. Default is 868.130.000Hz.

Master	TX Frequency (0x1B)	TX[31:24]	TX[23:16]	TX[15:8]	TX[7:0]
ATA8520D	Dummy	Dummy	Dummy	Dummy	Dummy

2.1.2.23 Set RX Frequency

Set RX center frequency temporarily for testing purposes. This settings are lost after reset or when switching the device off. The frequency value is an unsigned 32-bit integer within the range [869.400.000Hz to 869.650.000Hz]. Default is 869.525.000Hz.

Master	RX Frequency (0x1C)	RX[31:24]	RX[23:16]	RX[15:8]	RX[7:0]
ATA8520D	Dummy	Dummy	Dummy	Dummy	Dummy

2.1.3 Command Table Overview

Table 2-1. Command Table Overview

CMD	Index	Write Data	Read Data
System reset	0x01	None	None
I/O Init	0x02	DDRC register setting	None
I/O Write	0x03	PORTC register setting	None
I/O Read	0x04	None	PINC register setting
OFF mode	0x05	None	None
Atmel version	0x06	None	Major / minor
Write TX buffer	0x07	Data written to TX buffer	None
Reserved	0x08	-	-
SIGFOX™ version	0x09	None	Version L-H
Get status	0x0A	None	SSM / Atmel® FW / SIGFOX library
Send bit	0x0B	Bit status	None
Reserved	0x0C	-	-
Send frame	0x0D	None	None
Send/receive frame	0x0E	None	None
Get PAC	0x0F	None	PAC[0], PAC[1] …. PAC[15]
Read RX buffer	0x10	None	RX buffer data
Write Sys Conf	0x11	DDRC, PORTC, SysConf	None
Get ID	0x12	None	ID[3] … ID[0]
Read supply temperature	0x13	None	V_{idle}, V_{active}, temperature
Trigger measurement	0x14	None	None
Trigger TX test	0x15	Frame, channel	None
Trigger RX test	0x16	Channel, sequence	None
Send CW	0x17	On/off	None
Reserved	0x18	-	-
Reserved	0x19	-	-
Reserved	0x1A	-	-
Set TX frequency	0x1B	TX frequency	None
Set RX frequency	0x1C	RX frequency	None

2.1.4 System and Pin Configuration

This section specifies the system configuration settings used in the SPI RF transmit command (0x11). This system configuration has to be set after the system issues a system ready event and before using any other SPI command. The settings are stored in the internal EEPROM and will be applied after a system reset. This settings are typically applied at the EOL testing in the factory. Table 2-2 summarizes the configuration settings.

Table 2-2. System Configuration

Function	Bit No.	Settings
None	7 to 4	:1111 (default)
Supply voltage	3	:0, 5V supply :1, 3V supply (default)
Rx/TX select	2	:0, up-/downlink enabled :1, uplink only enabled (default)
None	1 to 0	:11 (default)

For an additional front-end-module, which includes an antenna switch, a low-noise amplifier for downlink operation and a power amplifier for uplink operation, two control signals are available at the port pins PB0 and PB7. These pins are controlled by the Atmel® ATA8520D device during transmission and reception of a RF data telegram. Table 2-3 summarizes the function of these pins.

Table 2-3. FEM Control Pins

Function/Pin	PB0	PB7
FEM disabled	0	X
Uplink active	1	1
Downlink active	1	0

In case the internal SPDT switch is not used for RF control this switch can be used in addition to control an external FEM. During uplink operation the path between pins SPDT_ANT and SPDT_TX is closed and for downlink operation the path between pins SPDT_ANT and SPDT_RX is closed.

Caution: The device is delivered with default configuration, i.e. with 3V supply mode enabled. When using the device with 5V supply it has to be ensured that before using the RF transmit operation the 5V supply mode is configured!

2.2 Operating Modes Overview

This section gives an overview of the operating modes supported by the Atmel ATA8520D.

After connecting the supply voltage to the VS pin, the Atmel ATA8520D always starts in OFF mode. All internal circuits are disconnected from the power supply. Therefore, no SPI communication is supported. The Atmel ATA8520D can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence which will set the event line PB6 to low. After the system initialization the Atmel ATA8520D reaches the IDLE Mode.

The IDLE Mode is the basic system mode supporting SPI communication and transitions to the other operating modes.

The transmit mode (TX Mode) starts the data transmission using the payload data which has to be previously written into the TX buffer with the SPI command “Write TX Buffer”. The data transmission is started with the SPI command “Send Frame”. After transmitting the data frame, the end of the transmission is indicated when the event pin PB6 switches to low and the device enters the IDLE Mode again.

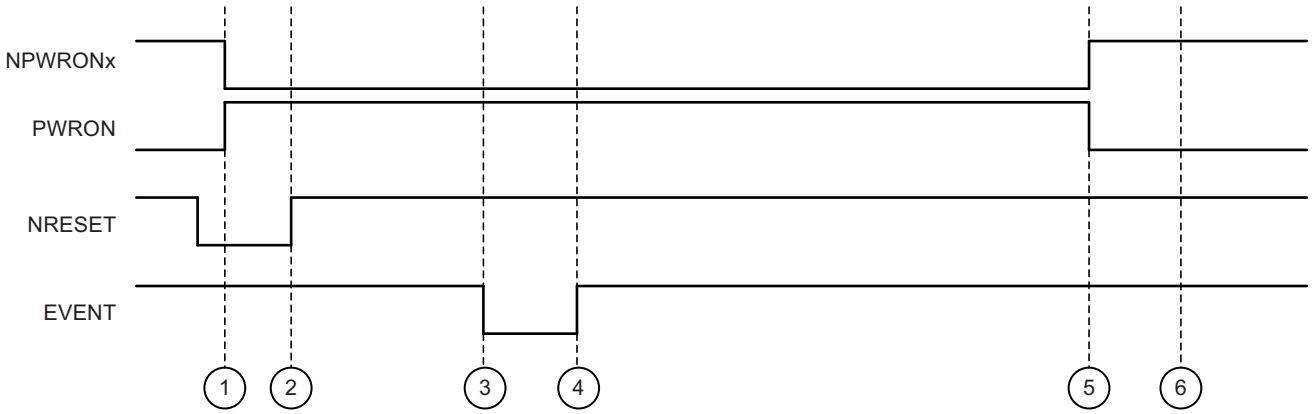
Reading the device status with the “Get Status” SPI command clears the PB6 event line, setting it to high level again.

The transmit/receive mode (TX/RX Mode) will send at first a data telegram in uplink direction and then enter receive mode for downlink direction. The downlink request is captured by the SIGFOX™ backend and processed. After transmission of the uplink frame the device will wait for 20 seconds before entering the receive mode. This receive mode will take up to 30 seconds and will end with an event on pin PB6. This event is cleared when reading the device status with the SPI command “Get Status”. If no error occurs during the downlink operation (Atmel status error code = 0000), the received data telegram of 8 bytes can be read with the SPI command “Read RX Buffer”.

2.2.1 Power-up Sequence

This section describes the power-up sequence for the device as described in Figure 2-2. The device is usually in OFF mode were the signals NPWRONx, PWRON and NRESET are inactive but VS is supplied with power. Switching the NRESET signal active or sending the SPI command System Reset (0x01) will have no effect in OFF mode. Switching one of the power-on pins active will wake-up the device and an internal power-on reset is performed. In addition the external NRESET line can be used to keep the device in reset state when waking-up the device. The minimum activation time for the NPWRONx, PWRON and NRESET signals is 10µs.

Figure 2-2. Power-up Sequence



After applying the reset signal NRESET one of the power-up signals NPWRON1...6 or PWRON is applied at timing point T1. At timing point T2 (~10µs after T1) the external reset signal is removed and the device starts its internal power-up sequence. This internal sequence is finished at timing point T3 (~10ms after T2) and is signaled with the event line. Reading the device status with the SPI command (0x0A) “Get status” will clear the event line at timing point T4. The device is now in idle mode and operational even if the NPWRONx and PWRON signals are deactivated.

To shutdown the device into OFF mode the power-up signals NPWRON1...6 or PWRON have to be deactivated at first (shown in timing point T5). The shutdown into OFF mode is then performed by sending the SPI command (0x05) “OFF mode” to the device.

2.2.2 Application Example

The software to control the device and to transmit only a data frame (without reception) has to perform the following steps:

1. Initialize device as shown in Figure 2-2 for the power-up sequence
2. Check for the startup event and read the device status with SPI command (0x0A) “Get status” to clear this event
3. Load the transmit buffer with up to 12 bytes using the SPI command (0x07) “Write TX Buffer”
4. Start the data transmit with SPI command (0x0D) “Send Frame”
5. Wait until the event signal appears (this takes about 7-8 seconds)
6. Read the device status with SPI command (0x0A) “Get status” to clear this event
7. Switch off the power-on signals as shown in Figure 2-2
8. Send the SPI command (0x05) “OFF mode” to the shutdown the device

The software to control the device and to transmit and receive a data frame has to perform the following steps:

1. Initialize device as shown in Figure 2-2 for the power-up sequence
2. Check for the startup event and read the device status with SPI command (0x0A) “Get status” to clear this event
3. Load the transmit buffer with up to 12 bytes using the SPI command (0x07) “Write TX Buffer”
4. Start the data transmit with SPI command (0x0E) “Send/Receive Frame”
5. Wait until the event signal appears (this takes about 20-50 seconds)
6. Read the device status with SPI command (0x0A) “Get status” to clear this event
7. Read the receive buffer with SPI command (0x10) “Read RX Buffer” for the 8 data bytes
8. Process received data, etc.
9. Switch off the power-on signals as shown in Figure 2-2
10. Send the SPI command (0x05) “OFF mode” to the shutdown the device

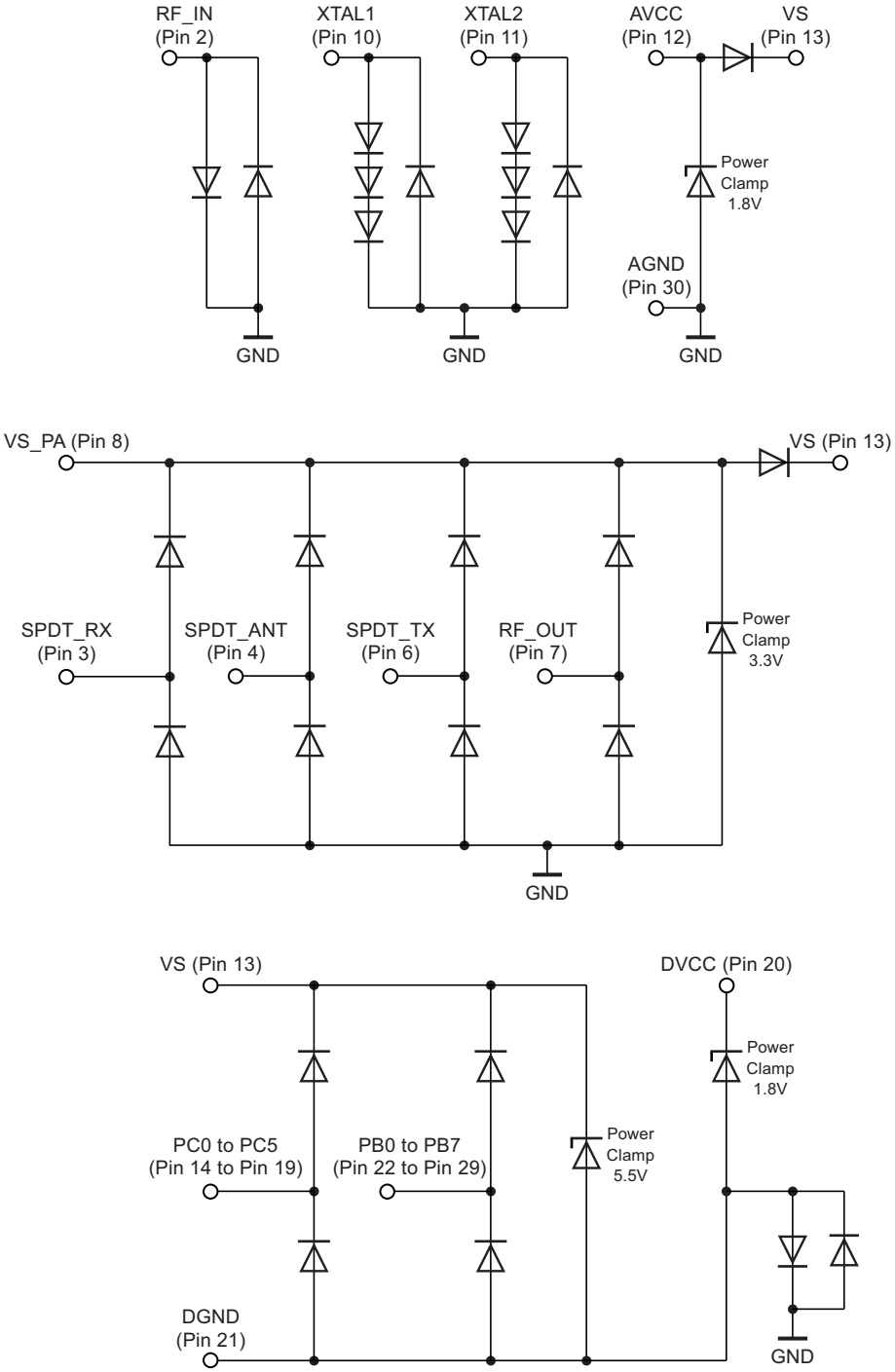
For the SPI communication it is important to keep the timing as shown in Figure 2-1 on page 8. With the SPI commands (0x0F) „Get PAC” and (0x12) „Get ID” the SIGFOX™ registration information can be read to register the device in the SIGFOX cloud.

3. Electrical Characteristics

3.1 ESD Protection Circuits

GND is the exposed die pad of the Atmel® which is internally connected to AGND (pin 30). All Zener diodes shown in Figure 3-1 (marked as power clamps) are realized with dynamic clamping circuits and not physical Zener diodes. Therefore, DC currents are not clamped to the shown voltages.

Figure 3-1. Atmel ESD Protection Circuit



3.2 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	Tj		+150	°C
Storage temperature	Tstg	–55	+125	°C
Ambient temperature	Tamb	–40	+85	°C
Supply voltage	V_{VS}	–0.3	+6.0	V
Supply voltage PA (1.9 to 3.6V application)	V_{VS_PA}	–0.3	+4.0	V
ESD (human body model) all pins	HBM	–4	+4	kV
ESD (machine model) all pins	MM	–200	+200	V
ESD (field induced charged device model) all pins	FCDM	–750	+750	V
Maximum peak voltage at pin 4 (SPDT_ANT)(1)	SPDTANT	–0.3	VS_PA(2) + 0.3	V
Maximum peak voltage at pin 6 (SPDT_TX)(1)	SPDTTX	–0.3	VS_PA(2) + 0.3	V

Notes: 1. The customer application needs to be properly designed.
2. VS_PA is the voltage applied to pin 8.

3.3 Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance, junction ambient, soldered in compliance with JEDEC	R_{th_JA}	35	K/W

3.4 Supply Voltages and Current Consumption

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V across all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.00	Supply voltage range VS	3V application	13	V_{VS}	1.9	3.0	3.6	V	A
		5V application	13	V_{VS}	2.4	5.0	5.5	V	A
1.01	Supply voltage for SIGFOX™ compliance	3V application	13	V_{VS}	2.9	3.0	3.1	V	
		5V application	13	V_{VS}	3.3	5.0	5.5	V	
1.05	Supply voltage rise time		13	V_{VS_rise}			1	V/µs	D
1.10	Supply voltage range VS_PA	3V application	8	V_{VS_PA}	1.9	3	3.6	V	A
		5V application	8	V_{VS_PA}		3		V	A
		SIGFOX compliant	8	V_{VS_PA}		3		V	
1.20	OFF mode Current consumption	T_{amb} = 25°C T_{amb} = 85°C	8, 13	$I_{OFFMode\_3V}$		5	150 600	nA nA	B B

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

3.4 Supply Voltages and Current Consumption (Continued)

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V across all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.30	Idle Mode current consumption	Temperature range –40°C to +65°C	13	$I_{IdleMode}$		50	90	µA	B
1.80	RX Mode current consumption	f_{RF} = 869.5MHz	13	I_{RXMode}		10.4	14.6	mA	A
2.00	TX mode current consumption	Pout = +14dBm f_{RF} = 868.3MHz	(7), 8, 13	I_{TXMode}		32.7	45	mA	B
2.05	SIGFOX™ TX mode current consumption	T_{amb} = 25°C, 3V application	(7), 8, 13	$I_{SIGFOXMode}$		31.8	40.1	mA	B
2.06	SIGFOX TX mode current consumption	T_{amb} = 85°C, 3V application	(7), 8, 13	$I_{SIGFOXMode}$		32.7	41.1	mA	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

3.5 RF Receive Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V across all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.50	Frequency range	Defined by SIGFOX protocol	(2)	f_{RX}	869.40		869.65	MHz	
4.90	Sensitivity level	FSK at 25kHz IF bandwidth T_{amb} = 25°C 0.75Kbit/s ±0.75kHz	17, 19	SFSK	–1.5dB	–121.5	+1.5dB	dBm	B
7.30	Blocking	FSK at 25kHz IF bandwidth, T_{amb} = 25°C 2.4Kbit/s ±2.4kHz	(2)	fdist. ≥ 50kHz fdist. ≥ 100kHz fdist. ≥ 225kHz fdist. ≥ 450kHz fdist. ≥ 1MHz fdist. ≥ 4MHz fdist.>10MHz		34 40 52 58 67 75 75		dBc	C C C C C C C
7.70	Image rejection	Large disturber applied before useful signal	(2)	IM_{RED}	38	47		dB	A
7.80	Blocking $3f_{LO}$, $5f_{LO}$	$3 \times f_{LO} - f_{IF}$ $5 \times f_{LO} + f_{IF}$	(2)	BL_{NfLO}		39 45		dB	C C
8.50	Input impedance	Measured on application board, RC parallel equivalent circuit	2	Z_{in}	–20%	340 1.4	+20%	Ω pF	C
8.70	SPDT switch RX insertion loss	Sensitivity matching RF_IN with SPDT to 50Ω compared to matching RF_IN directly to 50Ω	(3, 4)	IL_{Switch_RX}		1.0	1.4	dB	C
9.00	RSSI accuracy	P_{RFIN} = –70dBm	(2), 4	$RSSI_{ABS\_ACCU}$	–5.5		+5.5	dB	B
9.20	RSSI resolution	DSP property	(2), 4	$RSSI_{RES}$		0.5		dB/ value	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

3.6 RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V across all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.00	Output power range	T_{amb} = 25°C	(7)	P_{Range}			+14.5	dBm	B
10.01	Output power for SIGFOX™ compliance	T_{amb} = 25°C, V_{VS} = 2.9V to 3.1V, 3V application (for 5V applications see no. 11.50)	(7)	P_{SIGFOX}	13.5	13.8	14.0	dBm	B
10.02	Output power for SIGFOX compliance	T_{amb} = –45°C to +85°C, V_{VS} = 3.0V, 3V application (for 5V applications see no. 11.50)	(7)	P_{SIGFOX}	13.1	13.8	14.7	dBm	B
10.05	Frequency range	Defined by SIGFOX protocol	(7)	f_{TX}	868.0		868.6	MHz	
11.00	Output power at 14dBm	T_{amb} = 25°C using 14dBm matching	(7)	P_{out_14dBm}	–1.5dB	14	+1.5dB	dBm	B
11.10	Output 2nd harmonic at 14dBm	T_{amb} = 25°C using 14dBm matching	(7)	$HM2_{14dBm}$		–24		dBc	C
11.20	Output 3rd harmonic at 14dBm	T_{amb} = 25°C using 14dBm matching	(7)	$HM3_{14dBm}$		–50		dBc	C
11.50	Output power change full temperature and supply voltage range	For 13.8dBm V_{VS_PA} = 3.0V +-0.3V $P = P_{out} + \Delta P$	(7)	$\Delta P_{TambVs2}$	–3.5		+2	dB	C C
11.60	Spurious emission	at $\pm f_{XTO}$ at $\pm f_{AVR}$ (f_{XTO} / 4) at $\pm f_{CLK\_OUT}$ (f_{XTO} / 6)	(7)	SP_{TX}		–72 –85 –78	–60 –60 –60	dBc	B C C
12.40	SPDT insertion loss TX	Transmitted power using matching RF_OUT with SPDT to 50Ω compared to matching RF_OUT directly to 50Ω	(4, 6)	IL_{Switch_TX}		0.7	1.2	dB	C
12.45	Maximum peak voltage on SPDT_ANT (pin 4)		4	$V_{PEAK\_SPDT\_ANT}$	–0.3		VS_PA + 0.3	V	D
12.50	Maximum peak voltage on SPDT_TX (pin 6)		6	$V_{PEAK\_SPDT\_TX}$	–0.3		VS_PA + 0.3	V	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

3.7 RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances, quartz parameters C_m = 4fF and C_0 = 1pF unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13.30	XTO frequency range		10, 11	f_{xto}		24.305		MHz	C
13.35	XTO frequency for SIGFOX™ compliance	KDS: 1C324305AB0B NDK: NX3225SA EXS00A-CS08559 NX2016SA EXS00A-CS08560	10, 11	f_{SIGFOX_XTO}		24.305		MHz	
13.40	XTO pulling due to internal capacitance and XTO tolerance	C_m = 4fF, T_{amb} = 25°C	10, 11	ΔF_{XTO1}	–10		+10	ppm	B
13.50	XTO pulling due to temperature and supply voltage	C_m = 4fF T_{amb} = –40°C to +85°C	10, 11	ΔF_{XTO2}	–4		+4	ppm	B
13.60	Maximum C_0 of XTAL	XTAL parameter	10, 11	C_{0_max}		1	2	pF	D
13.70	XTAL, C_m motional capacitance	XTAL parameter	10, 11	C_m		4	10	fF	D
13.80	XTAL, real part of XTO impedance at start-up	C_m = 4fF, C_0 = 1pF	10, 11	R_{m_start1}	950			Ω	B
13.90	XTAL, real part of XTO impedance at start-up	C_m = 4fF, C_0 = 1pF, T_{amb} < 85°C	10, 11	R_{e_start2}	1100			Ω	B
14.00	XTAL, maximum R_m after start-up	XTAL parameter	10, 11	R_{m_max}	110			Ω	D
14.10	Internal load capacitors	Including ESD and package capacitance. XTAL has to be specified for 7.5pF load capacitance (incl. 1pF PCB capacitance per pin)	10, 11	C_{L1}, C_{L2}	13.3	14	14.7	pF	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

3.8 I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
15.00	Input low voltage	PC0 to PC5 PB0 to PB7	14-19 22-29	V_{IL}	–0.3		$0.2 \times V_{VS}$	V	A
15.05	Input low leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19 22-29	I_{IL}			–1	µA	A
15.10	Input high voltage	PC0 to PC5 PB0 to PB7	14-19 22-29	V_{IH}	$0.8 \times V_{VS}$		V_{VS} + 0.3	V	A
15.15	Input high leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19 22-29	I_{IH}			1	µA	A
15.20	Output low voltage	I_{OL} = 0.2mA	14-19 22-29	V_{OL_3V}			$0.1 \times V_{VS}$	V	A
15.30	Output high voltage	I_{OH} = –0.2mA	14-19 22-29	V_{OH_3V}	$0.9 \times V_{VS}$			V	A
15.40	I/O pin pull-up resistor	OFF mode: see port B and port C	14-19 22-29	R_{PU}	30	50	70	kΩ	A
16.10	I/O pin output delay time (rising edge)	C_{Load} = 10pF	14-19 22-29	$T_{del\_rise\_3V}$	13.6	17.5	22.4	ns	D
16.20	I/O pin rise time ($0.1 \times V_{VS}$ to $0.9 \times V_{VS}$)	C_{Load} = 10pF	14-19 22-29	T_{rise_3V}	20.7	23.9	28.4	ns	D
16.30	I/O pin slew rate (rising edge)	C_{Load} = 10pF	14-19 22-29	$T_{sr\_rise\_3V}$	0.115	0.100	0.084	V/ns	D
16.40	I/O pin output delay time (falling edge)	C_{Load} = 10pF	14-19 22-29	$T_{del\_fall\_3V}$	13.7	17.4	22.7	ns	D
16.50	I/O pin fall time ($0.9 \times V_{VS}$ to $0.1 \times V_{VS}$)	C_{Load} = 10pF	14-19 22-29	T_{fall_3V}	16.2	19.2	22.5	ns	D
16.60	I/O pin slew rate (falling edge)	C_{Load} = 10pF	14-19 22-29	$T_{sr\_fall\_3V}$	0.148	0.125	0.106	V/ns	D

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = characterized on samples, D = design parameter

3.9 Hardware Timings

All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to + 85°C, V_{VS} =1.9V to 3.6V over all process tolerances. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
17.50	Startup time	PWRON = ‘1’ or NPWRON = ‘0’ to EVENT generation	13, 20	$T_{STARTUP}$		10		ms	C

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = characterized on samples, D = design parameter

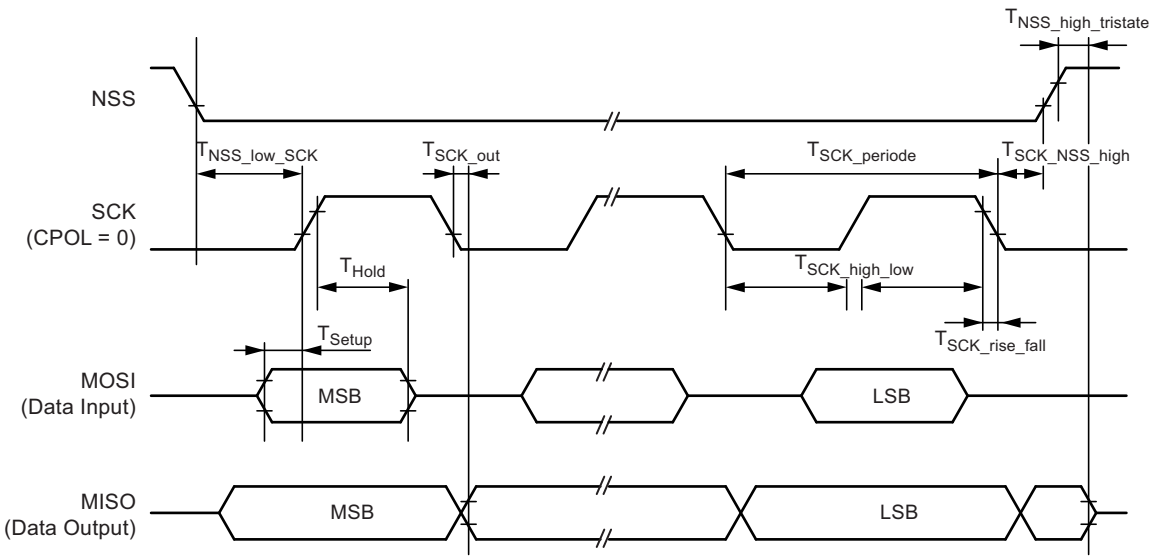
3.10 Hardware SPI Timing Characteristics

Timing shown for CPHA=0 and CPOL=0 in Figure 3-2, timing is valid for all CPHA and CPOL configurations. See also Section 2.1 “SPI Command Interface” on page 8 for functional SPI description and for firmware limitations on SPI data transfer.
All parameters refer to GND (backplane) and are valid for T_{amb} = –40°C to +85°C, V_{VS} = 1.9V to 3.6V (3V Application) and 4.5V to 5.5V (5V Application) over all process tolerances. Typical values are given at V_{VS} = 5V, T_{amb} = 25°C, and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305MHz.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
49.10	SCK cycle time		23	$T_{SCK\_periode}$	8			µs	D
49.20	SCK high or low time		23	$T_{SCK\_high\_low}$	330			ns	D
49.30	SCK rise or fall time		23	$T_{SCK\_rise\_fall}$			100	ns	D
49.40	MOSI setup time to active edge of SCK		23, 24	T_{Setup}	80			ns	D
49.50	MOSI hold time to active edge of SCK		23, 24	T_{Hold}	245			ns	D
49.60	Time periode active edge of SCK to data out at MISO	C_{LOAD_MISO} = 10pF	23, 25	T_{SCK_out}			250	ns	D
49.70	Time periode SCK inactive to NSS high		23, 27	$T_{SCK\_NSS\_high}$	100			µs	D
49.80	Time periode NSS high to MISO tristate	C_{LOAD_MISO} = 10pF	25, 27	$T_{NSS\_high\_tristate}$			250	ns	D
49.90	Time periode NSS low to active edge SCK		23, 27	$T_{NSS\_low\_SCK}$	65			µs	D

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = characterized on samples, D = design parameter

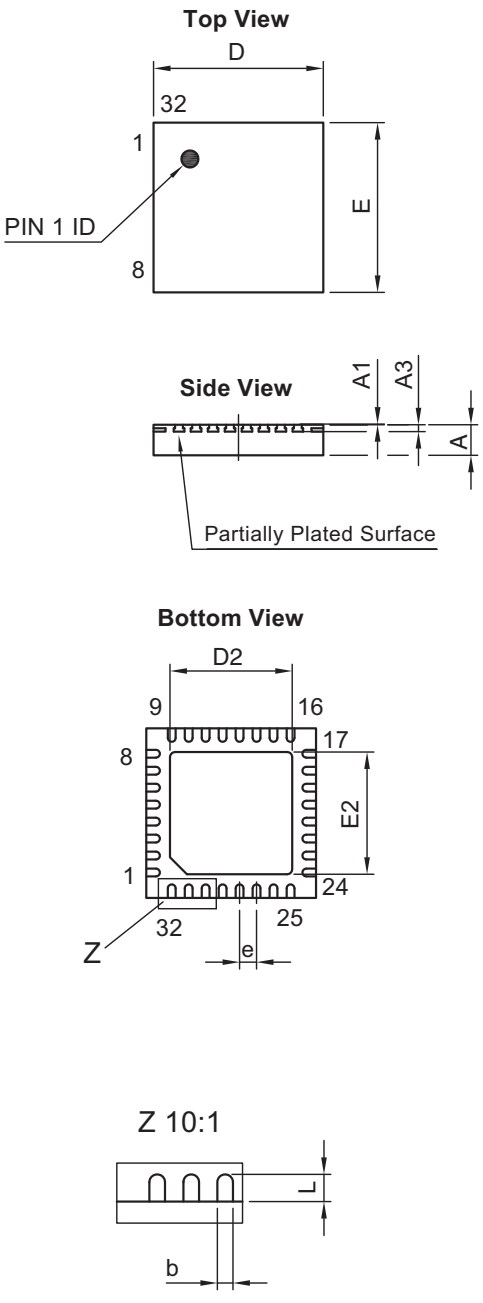
Figure 3-2. SPI Interface Timing Requirements



4. Ordering Information

Extended Type Number	Package	Remarks
ATA8520D-GHQW	QFN32	5mm × 5mm, Pb-free, 6k, taped and reeled

5. Package Information



technical drawings according to DIN specifications

Dimensions in mm

Two Step Singulation process

COMMON DIMENSIONS (Unit of Measure = mm)				
SYMBOL	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	4.9	5	5.1	
D2	3.5	3.6	3.7	
E	4.9	5	5.1	
E2	3.5	3.6	3.7	
L	0.35	0.4	0.45	
b	0.2	0.25	0.3	
e		0.5		

10/18/13

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VQFN_5x5_32L** Exposed pad 3.6x3.6		6.543-5124.03-4	1

6. Disclaimer

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7. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9390E-INDCO-11/15	• Section 2.1.4 “System and Pin Configuration” on page 15 updated
9390D-INDCO-11/15	• Table 1-1 “Pin Description” on page 3 updated • Section 1.4 “Applications” on pages 5 to 7 updated
9390C-INDCO-09/15	• Section 1.4.3 “Recommended PCB Design and Layout” removed • Section 3.4 “Supply Voltages and Current Consumption” on page 20 updated • Section 3.6 “RF Transmit Characteristics” on page 21 updated
9390B-INDCO-08/15	• Section 1.4.3 “Recommended PCB Design and Layout” on page 8 updated • Section 2.1 “SPI Command Interface” on pages 9 to 13 updated • Section 2.2 “Operating Modes Overview” on pages 16 to 17 updated • Section 3.10 “Hardware SPI Timing Characteristics” on page 25 added

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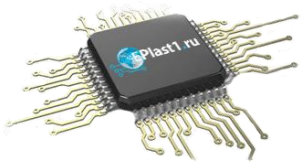
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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