	Digital Tri-axis Gyroscope/ Tri-axis Accelerometer PRELIMINARY Specifications	PART NUMBER: KXG03 Rev. 0.16 25-Nov-15

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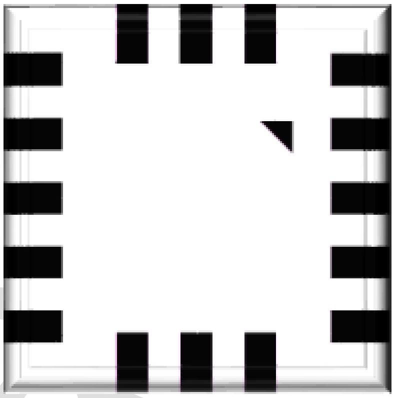
Product Description



16pin 3x3x0.9mm LGA bottom view

KXG03 is a 6 Degrees-of-Freedom inertial sensor system that features digital outputs accessed through I^{2}C or SPI communication available in two product offerings:

- KXG03-1034 Digital I^{2}C communication
- KXG03-1047 Digital SPI communication

The KXG03 sensor consists of a tri-axial micro machined gyroscope plus a tri-axial accelerometer and an ASIC packaged in a 3x3x0.9mm 16pin Land Grid Array (LGA) package. The ASIC is realized in standard CMOS technology and features flexible user programmable gyroscope full scale ranges of ±256, ±512, ±1024, and ±2048°/sec and user-programmable ±2g/±4g/±8g/±16g full scale range for the accelerometer. An auxiliary I^{2}C master serial interface exists for communication to up to 2 other sensors to access data that can be accumulated in an internal 1024 byte FIFO buffer and transmitted to the application processor. In addition, the KXG03 has an embedded temperature sensor.

During operation, the gyroscope sensor elements are forced into vibration. When angular velocities are applied about the sensing axes, vibration is transferred to sensing elements, causing capacitance changes at the sensor electrodes. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias and sensitivity adjustment, as well as temperature compensation. The DSP also feeds back the driving signal to ensure the proper sensor excitation.

The KXG03 series is designed to strike a balance between current consumption and noise performance with excellent bias stability over temperature. These sensors can accept supply and digital communication voltages between 1.8V and 3.3V.

Features

- 3 x 3 x 0.9 mm LGA
- User-selectable low power or high resolution mode
- User selectable gyroscope full scale ranges of:
  ±256 deg/s
  ±512 deg/s
  ±1024 deg/s
  ±2048 deg/s
- User selectable accelerometer full scale rages of:
  ±2g
  ±4g
  ±8g
  ±16g
- Temperature sensor with min measurement range of -40 C to +85 C with 16 bit output
- User-selectable Output Data Rate (ODR) up to 51200Hz
- 1024 byte FIFO buffer
- Wake-up and Back-to-sleep functions
- Auxiliary I2C master interface to control up to 2 auxiliary sensors
- Independent Output Data Rate (ODR) : Over Sampling Rate (OSR) control for accelerometer
- User-configurable wake-up function
- Digital I^2C up to 3.4MHz
- Digital SPI up to 10MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

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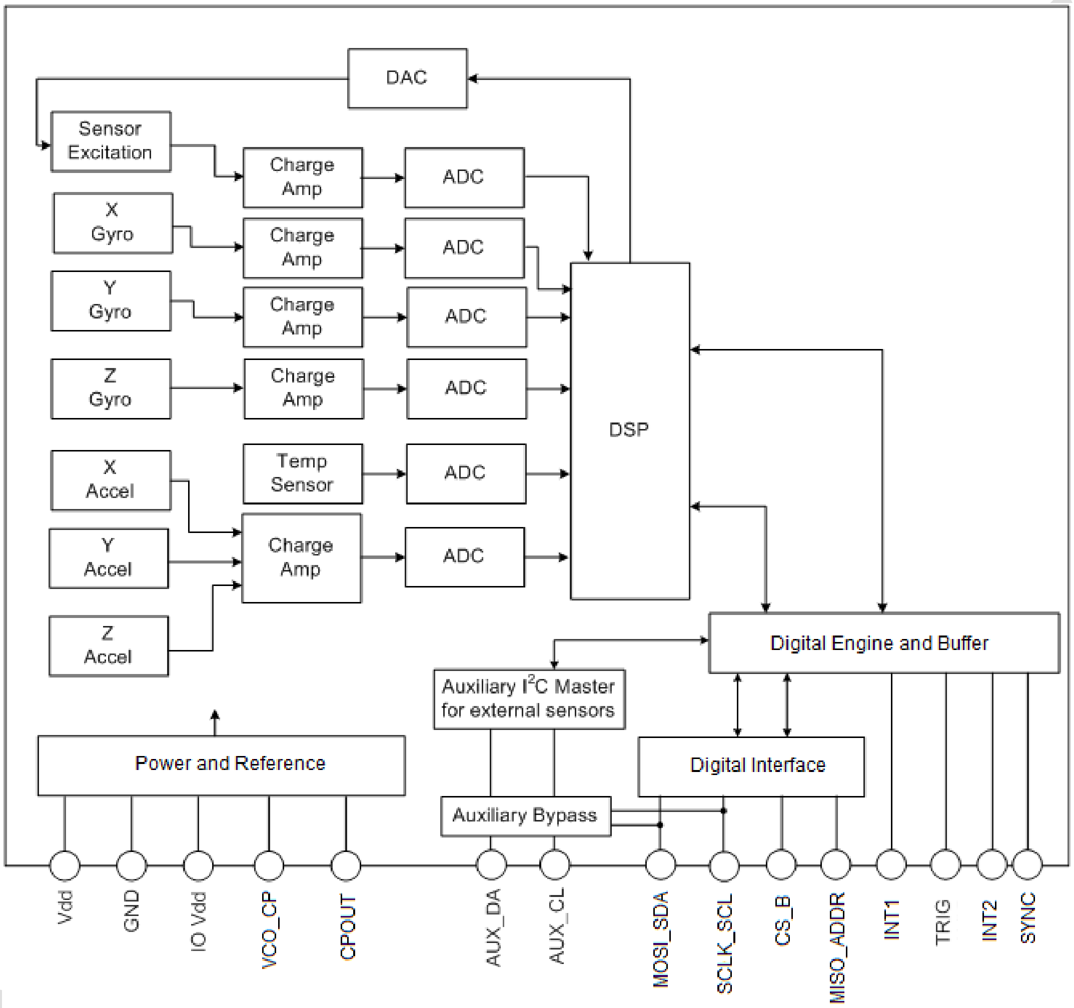
Functional Diagram



Product Specifications

Gyroscope Mechanical

(Specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	85
Zero Rate Output, Digital		counts		0	
Zero Rate Output Stability		± % of FS		1	
Zero Rate Output Variation over Temperature		± dps / °C		0.04	
Sensitivity (16-bit) [1]	RSEL1 = 0, RSEL0 = 0, ±256 deg/sec	counts/deg/sec		128	
	RSEL1 = 0, RSEL0 = 1, ±512 deg/sec			64	
	RSEL1 = 1, RSEL0 = 0, ±1024 deg/sec			32	
	RSEL1 = 1, RSEL0 = 1, ±2048 deg/sec			16	
Sensitivity Variation over Temperature		± % / °C		0.04	
Noise Density		deg/sec/√Hz		0.03	
Output Noise (10 Hz BW)		dps-rms		0.23	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		± %		1	
Bandwidth [2]		Hz	10		160

Table 1: Gyroscope Mechanical Specifications

Notes:

1. Resolution and rotation rate ranges are user selectable.
2. User selectable via control register.

Accelerometer Mechanical

(Specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	85
Zero-g Offset		mg	-	±25	
Zero-g Offset Variation from RT over Temp.		± mg/ °C		0.25	
Sensitivity (16-bit)[1]	GSEL1=1, GSEL0=1 (± 2g)	counts/g		16384	
	GSEL1=0, GSEL0=0 (± 4g)			8192	
	GSEL1=0, GSEL0=1 (± 8g)			4096	
	GSEL1=1, GSEL0=0 (± 16g)			2048	
Sensitivity Variation from RT over Temp.		± % / °C		0.01 (xy) 0.03 (z)	
Self-Test Output		g		0.5	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		%		2	
Noise Density		$\mu g / \sqrt{Hz}$		150	
Bandwidth (-3dB)[3]		Hz		ODR/2	

Table 2: Accelerometer Mechanical Specifications

Notes:

1. Resolution and acceleration ranges are user selectable.
2. Resonance as defined by the dampened mechanical sensor.
3. User selectable via control register.

Temperature Sensor

(Specifications are for operation at VDD = 2.5V and T = 25 °C unless stated otherwise)

Parameters	Units	Min	Typical	Max
Operating Temperature Range	°C	-40	-	85
Output Accuracy	± °C		1	
Sensitivity (16-bit digital)	counts/ °C		256	

Table 3: Temperature Sensor Specifications

Electrical

(Specifications are for operation at VDD = 2.5V and T = 25 °C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.8	3.0	3.3
I/O Pads Supply Voltage (IO_VDD)		V	1.7		VDD
Current Consumption	Operating (gyroscope + accelerometer)	mA		2.1	
	Gyroscope only	mA		1.85	
	Accelerometer only High Res Mode	µA		300	
	Accelerometer only Low Power Mode [6]	µA		5	
	Standby	µA		1.5	
Output Low Voltage[1] (V_{OL})		V	-	-	0.3 * IO_VDD
Output High Voltage (V_{OH})		V	0.9 * IO_VDD	-	-
Input Low Voltage (V_{IL})		V	-	-	0.2 * IO_VDD
Input High Voltage(V_{IH})		V	0.8 * IO_VDD	-	-
Turn on Time (Power on Reset Time)[2]		msec			50
Sensor Start-Up Time[3]	Gyroscope	msec		30	
	Accelerometer (100Hz)	msec		20	
I^{2}C Communication Rate[4,5]		MHz			3.4
I^{2}C Address				4Eh / 4Fh	
SPI communication Rate		MHz			10

Table 4: Electrical Specifications

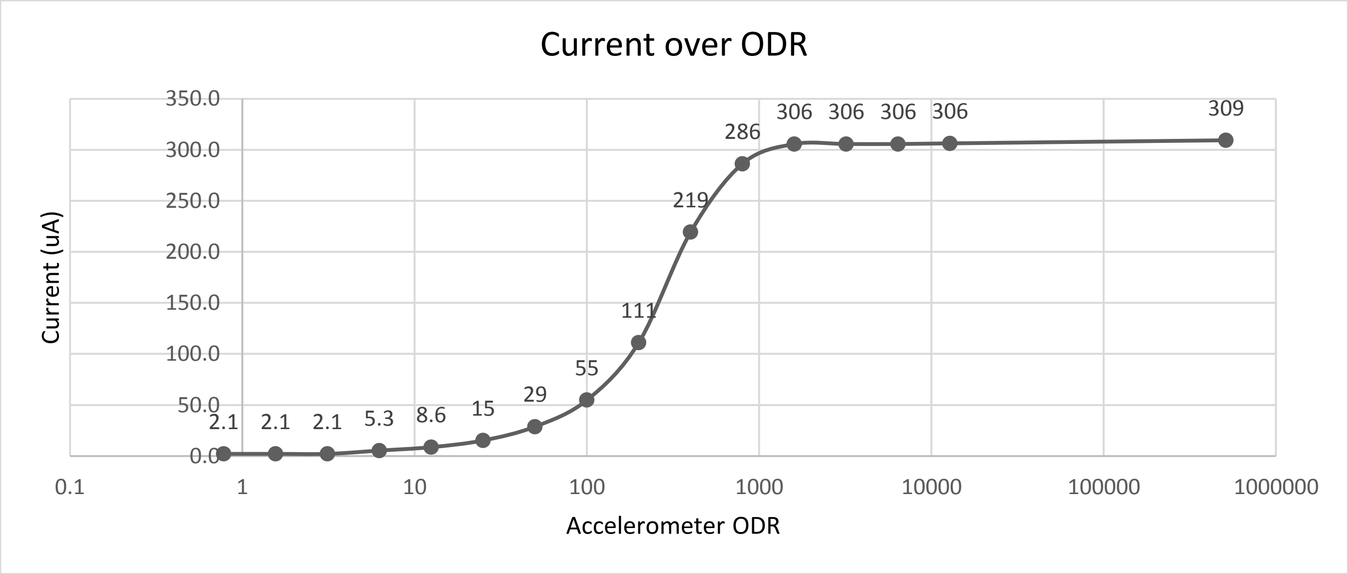
Notes:

1. Assuming I^{2}C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA.
2. From OFF to Standby mode after VDD and IO_VDD are valid
3. Time to valid sensor output (within 10% of Full Scale Range selected output after sensor standby mode to operating mode). Accelerometer time varies with accelerometer Output Data Rate (ODR) per table below.
4. Assuming max bus capacitance load of 20pF.
5. The I^{2}C bus supports Standard-Mode, Fast-Mode and High Speed Mode.
6. Accelerometer only in Low Power Mode current varies with accelerometer Output Data Rate (ODR) and Output Wake-up Function (OWUF) per table below.

Accelerometer Start-up time versus ODR profile:

TBD

Accelerometer Low Power Mode Current versus ODR profile:



Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD$_{Low}$**, **T$_{VDD}$** (rise time), and **T$_{VDD\_Off}$** profile of individual applications. It is recommended to minimize **VDD$_{Low}$**, and **T$_{VDD}$**, and maximize **T$_{VDD\_Off}$**. It is also advised that the VDD ramp up time **T$_{VDD}$** be monotonic. To assure proper POR in all environmental conditions the application should be evaluated over the customer specified range of **VDD, VDD$_{Low}$**, **T$_{VDD}$**, **T$_{VDD\_Off}$** and temperature as POR performance can vary depending on these parameters

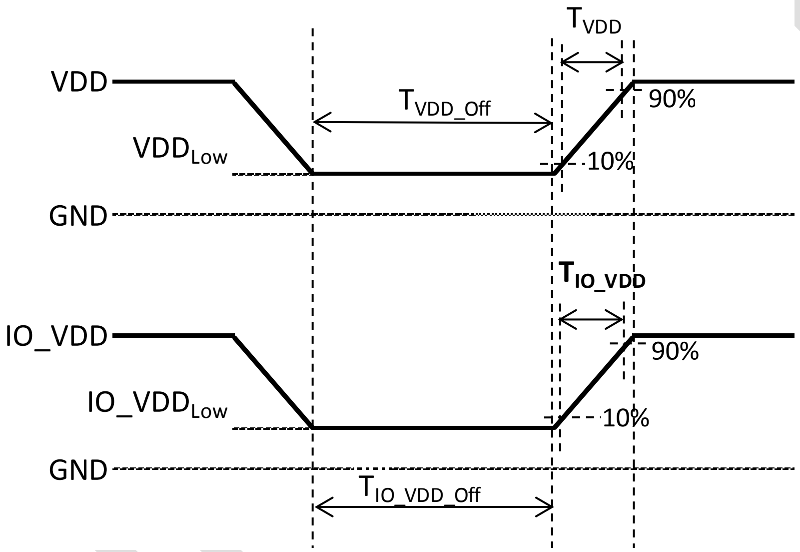


Figure 1: POR Procedure Timing Diagram

Bench Testing has demonstrated POR performance regions for a proper POR trigger. To assure POR trigger properly executes, setting operational thresholds consistent with the Table 5 below is suggested.

POR Performance

Parameters	Units	Min	Typical	Max
VDD rise time : T_{VDD}	msec			5
IO_VDD rise time : T_{IO_VDD}	msec			5
VDD off time : T_{VDD_Off}	msec	20		
IO_VDD off time : $T_{IO\_VDD\_Off}$	msec	20		
VDD low voltage : VDD_{Low}	mV			200
IO_VDD low voltage : $IO\_VDD_{Low::}$	mV			200

Table 5: POR Performance Specifications

Notes:

1. VDD and IO_VDD must always be monotonic ramps without ambiguous state
2. T_{VDD} and T_{IO_VDD} rise from 10% to 90% of final value needs to be ≤ 5ms.
3. IO_VDD amplitude must remain ≤ VDD amplitude.
4. In order to prevent the accelerometer from entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND (≤ 200mV) for a duration of time ≥ 20ms.
5. It is important the user determines the timing (**T_{VDD_Off}**) and threshold (**VDD_{Low}**) levels by evaluating the performance in the specific system for which the device will be incorporated.

The data provided by Kionix is intended for initial customer design guidance only. Kionix POR testing looks at a finite number of test configurations. Each customer application will have varying input sensor parameters (electrical, mechanical, and environmental) that will be different than the configurations tested by Kionix. Each customer utilizing the sensor will need to properly validate the sensor (including POR function) within their application under their specific use cases to ensure it responds as required.

Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		°C	-40	-	85
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5 msec 10000 for 0.2 msec
ESD	HBM	V	-	-	2000

Table 6: Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: *7C-I - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*

These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-161) as identified by the European Chemicals Agency as of 17 December 2014.

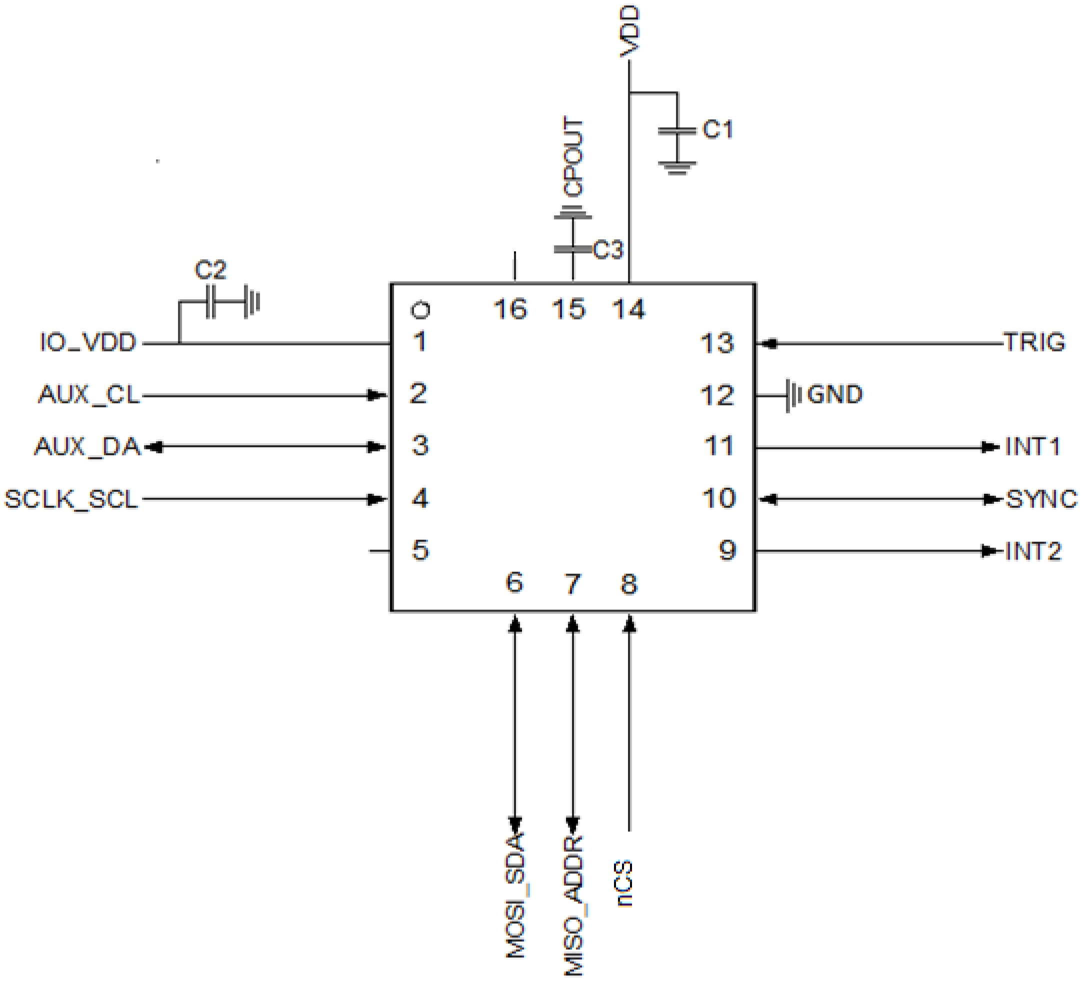
HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic



ID	Stress	Value	Rating	Type
C1	3 V	0.1 µF	16 V	Y5V
C2	3 V	0.1 µF	16 V	Y5V
C3	20 V	2.2 nF	50 V	Y5V

Pin Descriptions

Pin	Name	Description
1	IO_VDD	External supply for IO ring. Connect bypass capacitor C2
2	AUX_CL	Auxiliary I^2C master serial clock
3	AUX_DA	Auxiliary I^2C master serial data
4	SCLK_SCL	SPI/I2C serial clock[1]
5	RESERVED	Connect to GND or leave floating. Do not connect to IO_VDD.
6	MOSI_SDA	SPI MOSI / I^2C serial data[2]
7	MISO_ADDR	SPI MISO / I^2C slave_addr[0]
8	nCS	SPI enable / I^2C mode select (0=SPI enabled, I^2C communication disabled / 1=SPI disabled, I^2C communication enabled)
9	INT2	Programmable interrupt output
10	SYNC	Sync input or output. If configured as input, connect to IO_VDD or GND. If configured as output, leave floating[3].
11	INT1	Programmable interrupt output
12	GND	Ground
13	TRIG	External trigger input for buffer actions. Connect to IO_VDD or GND if unused.
14	VDD	External supply with bypass capacitor C1
15	CPOUT	External charge pump reservoir cap C3
16	RESERVED	Connect to GND or leave floating

Table 7: Pin Descriptions

Notes:

1, 2 For I^2C communication, connect an external IO_VDD pull-up resistors on SCL (pin 4) and SDA (pin 6). The value of the pull up resistors should be 1.5kΩ or above to ensure a V_{OL} that is less than the maximum specified value.

3 Care must be taken with external connection of the SYNC pin. The reset state of the SYNC pin is tri-stated. If pin is not used in application, connect to IO_VDD or GND and ensure the state of the pin is never changed to output through register write to FSYNC_CNT register. If pin is configured as Output in the application, the pin must be left floating to avoid internal short circuit to IO_VDD or GND.

Package Dimensions and Orientation:

Dimensions

3 x 3 x 0.9 mm LGA Dimensions

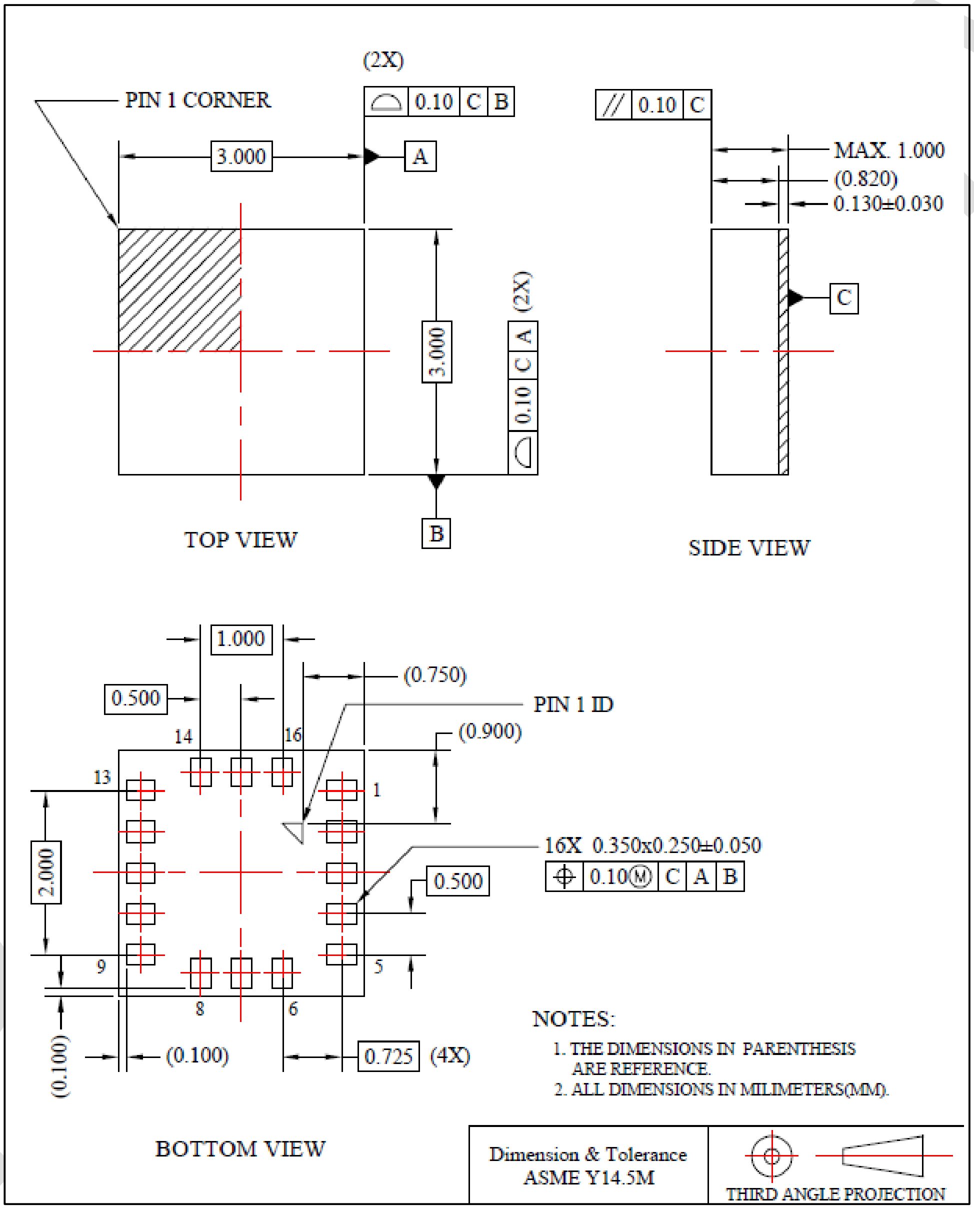


Figure 2: Package Dimensions

Orientation

When the device is accelerated or rotated in +X, +Y, or +Z direction, the corresponding output will increase.

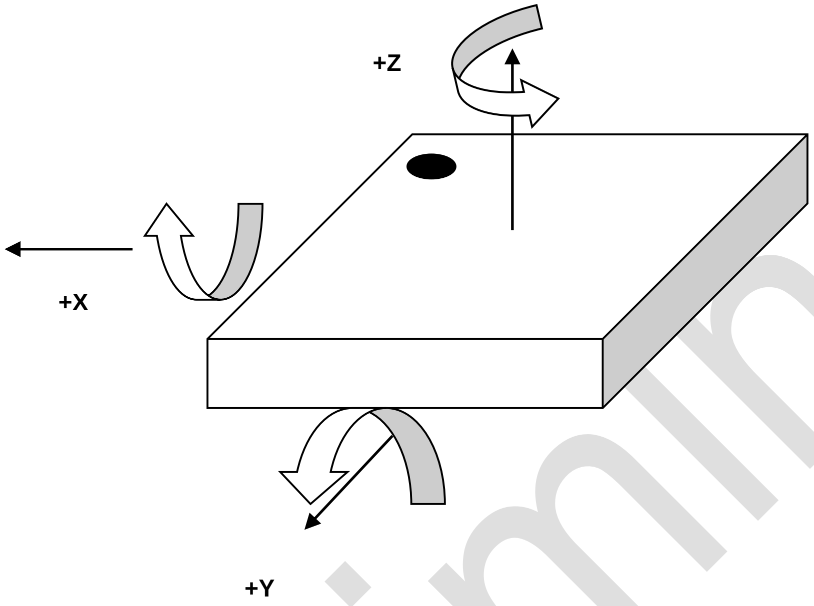


Figure 3: Device Orientation

Digital Interface

The Kionix KXG03 digital sensor has the ability to communicate via the I^{2}C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in the table below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 8: Serial Interface Terminologies

I^{2}C Serial Interface

As previously mentioned, the KXG03 has the ability to communicate on an I^{2}C bus. I^{2}C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXG03 always operates as a Slave device during standard Master-Slave I^{2}C operation.

I^{2}C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^{2}C bus is considered free when both lines are high.

The I^{2}C interface is compliant with high-speed mode, fast mode and standard mode I^{2}C protocols.

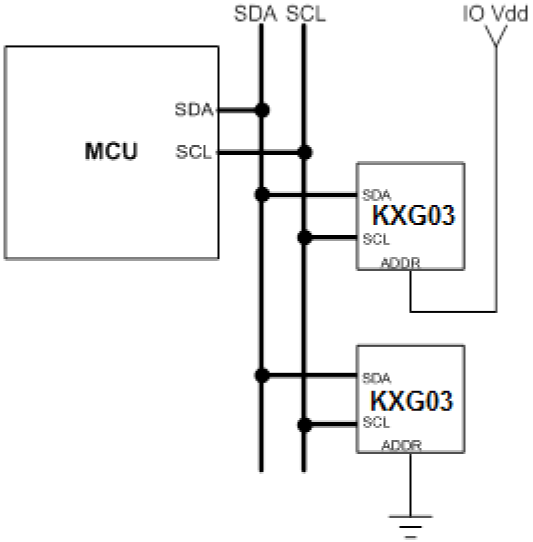


Figure 4: Multiple KXG03 I2C Connection

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	IO_VDD	4Fh	9Eh	1	0	0	1	1	1	1	0
I2C Rd	IO_VDD	4Fh	9Fh	1	0	0	1	1	1	1	1
I2C Wr	GND	4Eh	9Ch	1	0	0	1	1	1	0	0
I2C Rd	GND	4Eh	9Dh	1	0	0	1	1	1	0	1

Table 9: I^{2}C Slave Addresses for KXG03

I^{2}C Operation

Transactions on the I^{2}C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KXG03's Slave Address is comprised of a programmable part and a fixed part, which allows for connection of multiple KXG03's to the same I^{2}C bus. The Slave Address associated with the KXG03 is 100111X, where the programmable bit X is determined by the assignment of ADDR (pin 7) to GND or IO_VDD. The Figure 4 shows how two KXG03's would be implemented on an I^{2}C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free. Note that if the KXG03 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.

Writing to 8-bit Register

Upon power up, the Master must write to the KXG03's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXG03 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXG03 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KXG03 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXG03 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXG03 is now stored in the appropriate register. The KXG03 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.
Note** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers.

Reading from 8-bit Register

When reading data from a KXG03 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXG03 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXG03 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXG03 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXG03 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 below. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command. Note, accelerometer's and/or gyroscope's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^{2}C bus and how the Master and Slave interact during these transfers. The table below defines the I^{2}C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 10: I^{2}C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

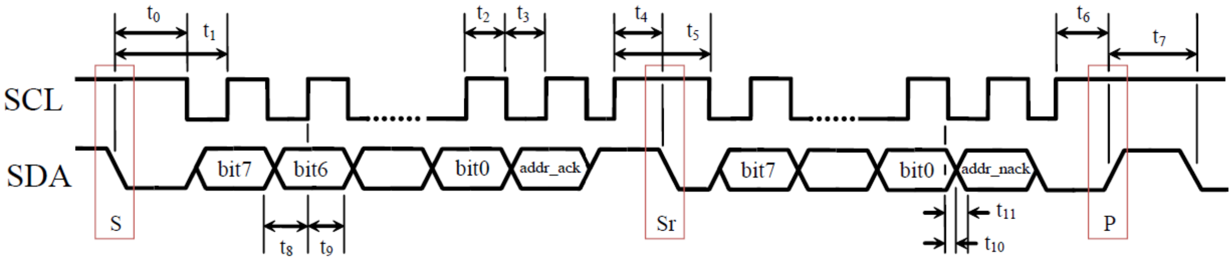
Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes + ack.

I^{2}C Timing Diagram



I^{2}C Timing Specifications (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I^{2}C CLK	2.5	-	us

Table 11: I^{2}C Timing Specifications (Fast Mode)

Auxiliary I^{2}C Operation

The KXG03 has an auxiliary I^{2}C bus for communicating to external I^{2}C-supported sensors. This bus has an I^{2}C Host Mode where the KXG03 acts as a host to external sensors, and a Bypass Mode where the KXG03 directly connects the primary and auxiliary I^{2}C buses together. This allows the system processor to directly communicate with the external sensors. Maximum data rate for this bus is 400KHz Fast Mode. With the auxiliary I^{2}C enabled the AUX_CL pin operates as an output-only pin. The auxiliary I2C hence does not support clock stretching and KXG03 should not be mated with external devices using clock stretching

Auxiliary I^{2}C Host Mode

This mode allows the KXG03 to directly access the data registers of any external sensors connected to the auxiliary I^{2}C bus. In this mode, the KXG03 directly obtains data from the auxiliary sensors and packages them with its own sensor data inside the internal FIFO buffer.

In Host Mode the KXG03 is easily configured to read up to six successive registers from up to two different auxiliary devices. The user simply configures KXG03 control registers with up to two different I^{2}C SAD's, starting register addresses and the number of bytes to be read back via auto-increment.

Auxiliary I^{2}C Bypass Mode

This mode allows an external processor to act as host and directly communicate to the auxiliary devices. This allows the host to initialize the auxiliary sensors for operation, or to access them directly while the KXG03 is disabled. The AUX_CL and AUX_DA pins can be operated in bypass mode shorted to SCLK_SCL and the MOSI_SDA pins, respectively. When operated in bypass mode the connection to the main I2C pins is broken while nCS is low (i.e. while the main interface is operating in SPI mode).

Internal Pull-up Resistor

The auxiliary I^{2}C interface can be operated with external or internal pull up devices. Internal pull up devices are automatically disabled in bypass mode to prevent pulling up the main I^{2}C /SPI interface. The KXG03 AUX_CL pin is driven by as a rail-to-rail (push-pull) CMOS output. The AUX_CL pin hence does not require external (or internal) pull ups.

SPI Communications

4-Wire SPI Interface

The KXG03 also utilizes an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KXG03 always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in the figure below.

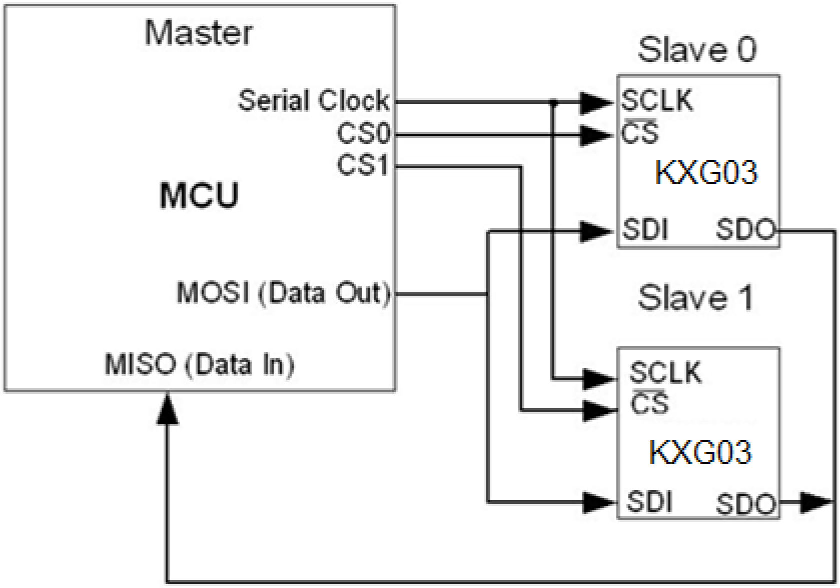
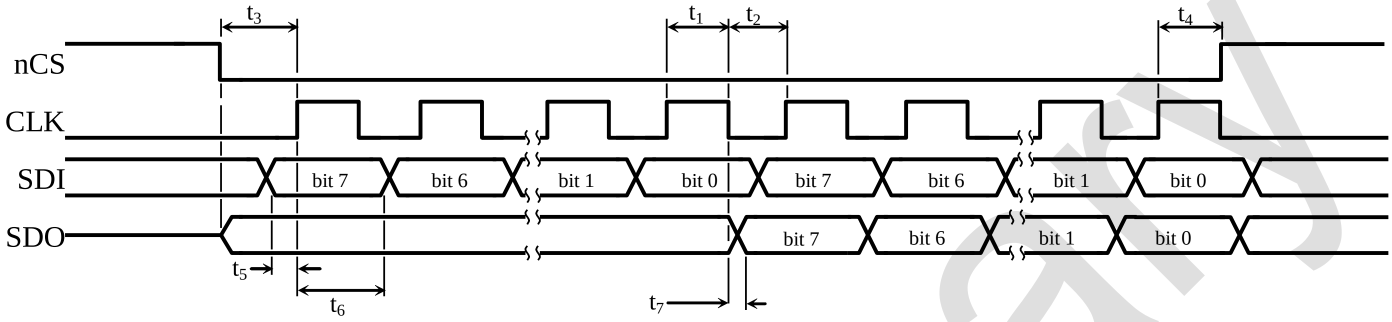


Figure 5: 4-wire SPI Connections

4-Wire SPI Timing Diagram



Number	Description	MIN	MAX	Units
t_1	CLK pulse width: high	40		ns
t_2	CLK pulse width: low	40		ns
t_3	nCS low to first CLK rising edge	20		ns
t_4	nCS low after the final CLK rising edge	30		ns
t_5	SDI valid to CLK rising edge	10		ns
t_6	CLK rising edge to SDI invalid	10		ns
t_7	CLK falling edge to SDO valid		35	ns

Table 12: 4-Wire SPI Timing

Notes:
1. t_7 is only present during reads.
2. Timings are for VDD of 1.8V to 3.6V with 1KΩ pull-up resistor and maximum 20pF load capacitor on SDO.

4-Wire Read and Write Registers

The registers embedded in the KXG03 have 8-bit addresses. Upon power up, the Master must write to the sensor's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. This operation occurs over 16 clock cycles. All commands are sent MSB first. The host must return nCS high for at least one clock cycle before the next data request. However, when data is being read from a buffer read register (BUF_READ), the nCS signal can remain low until the buffer is read. The Figure 6 shows the timing diagram for carrying out an 8-bit register write operation.

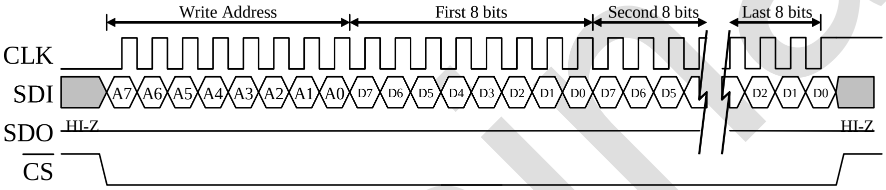


Figure 6: Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the sensor to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the sensor returns the 8-bit data stored in the addressed register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. The Figure 7 shows the timing diagram for an 8-bit register read operation.

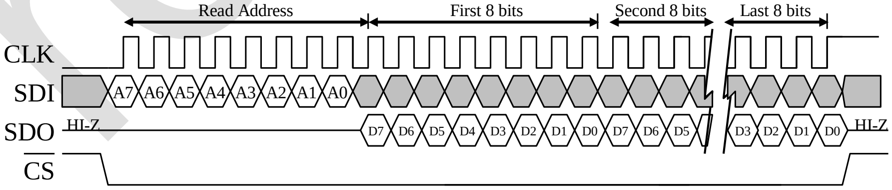


Figure 7: Timing Diagram for 8-Bit Register Read Operation

Power Modes

The KXG03 has three power modes: Off, Stand-by, and Active. The part exists in one of these three modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	IO_VDD	VDD	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
Off	-	ON	OFF	No sensor activity	Not available
Off	-	OFF	ON	No sensor activity	Not available
Stand-by	Active	ON	ON	Waiting activation command	Not available
Active - WUF	Active	ON	ON	Accelerometer active looking for motion Wake-up	Accelerometer registers, buffer, and DRDY
Active	Active	ON	ON	All functionalities available	All sensors available

Off mode

One or both of the power supplies (VDD or IO_VDD) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on IO_VDD before VDD, but if VDD is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power-On Reset (POR) is performed every time when:

1. IO_VDD supply is valid
2. VDD power supply is going to valid level

OR

1. IO_VDD power supply is going to valid level
2. VDD supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command from the external application processor via the I^2C bus.

Active WUF mode

While in Active WUF mode, the accelerometer is periodically taking a measurement to detect if there is any motion. Data in the accelerometer registers is being updated and can be sent to the buffer, and data ready interrupt can be reported.

Active Wake and Sleep mode

Stand-by-mode can be changed to Active mode by writing to register STBY_REG or by use of the WUF.

Active mode engages the full functionality of accelerometer and/or gyroscope measurements in two possible configurations, one is named Wake the other Sleep. The user can select separate configurations for each mode such as ODR, BW, FS-range and even Standby bits for each mode. For example, the user could enable all sensors in Wake state and only the Aux sensor in Sleep state. Or the user could enable the accelerometer in low power mode during Wake state and both the gyroscope and accelerometer in sleep state

The WUF and BTS functions can be used to automatically switch between the two modes based on measured accelerometer activity. The user can select which functions and sensors are enabled for each mode.

Embedded Wake-up and Back-to-Sleep Function

The KXG03 contains an interrupt engine that can be configured by the user to report when qualified changes detected by the acceleration occur, using the accelerometer. The user has the option to enable or disable specific accelerometer axes and specific directions, as well as to specify the delay time. An example use case for the engine would be to detect motion on any axis to signal an event and wake up or put back to sleep the KXG03 or other devices. For Wake-up (WUF), this can be achieved by configuring the engine to detect when the acceleration on any axis is *greater* than the user-defined threshold for a user-defined amount of time. For Back-To-Sleep (BTS), this can be achieved by configuring the engine to detect when the acceleration on any axis is *less* than the user-defined threshold for a user-defined amount of time. The KXG03 will change modes when the WUF or BTS functions trigger. The user can manually force the KXG03 into Wake or Sleep modes using the MAN_WAKE and MAN_SLEEP bits. The equations below show how to calculate the engine threshold and delay time register values for the desired result.

$$\text{Wake-up Threshold (counts)} = \text{Desired Threshold (g)} \times 16 \text{ (counts/g)}$$

Equation 1: Wake-up Threshold

$$\text{Back-To-Sleep Threshold (counts)} = \text{Desired Threshold (g)} \times 16 \text{ (counts/g)}$$

Equation 2: Back-To-Sleep Threshold

$$\text{Back-To-Sleep Threshold (counts)} = \text{Desired Delay Time (sec)} \times \text{OWUF (Hz)}$$

Equation 3: Wake-up Delay Time

$$\text{Back-To-Sleep Delay Time (counts)} = \text{Desired Delay Time (sec)} \times \text{OSA (Hz)}$$

Equation 4: Back-To-Sleep Delay Time

Embedded Registers

The KXG03 has embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. The table below provides a listing of the accessible 8-bit registers and their addresses.

Register Name	R/W	I^{2}C Add
TEMP_OUT_L	R	00h
TEMP_OUT_H	R	01h
GYRO_XOUT_L	R	02h
GYRO_XOUT_H	R	03h
GYRO_YOUT_L	R	04h
GYRO_YOUT_H	R	05h
GYRO_ZOUT_L	R	06h
GYRO_ZOUT_H	R	07h
ACC_XOUT_L	R	08h
ACC_XOUT_H	R	09h
ACC_YOUT_L	R	0Ah
ACC_YOUT_H	R	0Bh
ACC_ZOUT_L	R	0Ch
ACC_ZOUT_H	R	0Dh
AUX1_OUT1	R	0Eh
AUX1_OUT2	R	0Fh
AUX1_OUT3	R	10h
AUX1_OUT4	R	11h
AUX1_OUT5	R	12h
AUX1_OUT6	R	13h
AUX2_OUT1	R	14h
AUX2_OUT2	R	15h
AUX2_OUT3	R	16h
AUX2_OUT4	R	17h
AUX2_OUT5	R	18h
AUX2_OUT6	R	19h
WAKE_CNT_L	R	1Ah
WAKE_CNT_H	R	1Bh
SLEEP_CNT_L	R	1Ch
SLEEP_CNT_H	R	1Dh
BUF_SMPLEV_L	R	1Eh
BUF_SMPLEV_H	R	1Fh
BUF_PAST_L	R	20h
BUF_PAST_H	R	21h
AUX_STATUS	R	22h
RESERVED	R	23h-2Fh
WHO_AM_I	R	30h
SN1_MIR	R	31h
SN2_MIR	R	32h
SN3_MIR	R	33h
SN4_MIR	R	34h
RESERVED	R	35h
STATUS1	R/W	36h
INT1_SRC1	R	37h
INT1_SRC2	R	38h
INT1_L	R	39h
STATUS2	R/W	3Ah
INT2_SRC1	R	3Bh
INT2_SRC2	R	3Ch
INT2_L	R	3Dh
ACCEL_ODR_WAKE	R/W	3Eh
ACCEL_ODR_SLEEP	R/W	3Fh
ACCEL_CTL	R/W	40h
GYRO_ODR_WAKE	R/W	41h
GYRO_ODR_SLEEP	R/W	42h
STDBY	R/W	43h
CTL_REG_1	R/W	44h
INT_PIN_CTL	R/W	45h
INT_PIN1_SEL	R/W	46h
INT_PIN2_SEL	R/W	47h
INT_MASK1	R/W	48h
INT_MASK2	R/W	49h
FSYNC_CTL	R/W	4Ah
WAKE_SLEEP_CTL1	R/W	4Bh
WAKE_SLEEP_CTL2	R/W	4Ch
WUF_TH	R/W	4Dh
WUF_COUNTER	R/W	4Eh
BTS_TH	R/W	4Fh
BTS_COUNTER	R/W	50h
AUX_I2C_CTL_REG	R/W	51h
AUX_I2C_SAD1	R/W	52h
AUX_I2C_REG1	R/W	53h
AUX_I2C_CTL1	R/W	54h
AUX_I2C_BIT1	R/W	55h
AUX_I2C_ODR1_W	R/W	56h
AUX_I2C_ODR1_S	R/W	57h
AUX_I2C_SAD2	R/W	58h
AUX_I2C_REG2	R/W	59h
AUX_I2C_CTL2	R/W	5Ah
AUX_I2C_BIT2	R/W	5Bh
AUX_I2C_ODR2_W	R/W	5Ch
AUX_I2C_ODR2_S	R/W	5Dh
RESERVED	R/W	5Eh -
BUF_WMITH_L	R/W	75h
BUF_WMITH_H	R/W	76h
BUF_TRIGTH_L	R/W	77h
BUF_TRIGTH_H	R/W	78h
BUF_CTL2	R/W	79h
BUF_CTL3	R/W	7Ah
BUF_CTL4	R/W	7Bh
BUF_EN	R/W	7Ch
BUF_STATUS	R	7Dh
BUF_CLEAR	R/W	7Eh
BUF_READ	R	7Fh

Table 13: I2C Register Map

Gyroscope Outputs

These registers contain 16-bits of valid angular rate data for each axis. The data is protected from overwrite during each read, and can be converted from digital counts to angular rate (deg/sec) per the table below.

16-bit Data (2's complement)	Equivalent Counts in decimal	Range = ±2048 deg/sec	Range = ±1024 deg/sec	Range = ±512 deg/sec	Range = ±256 deg/sec
0111 1111 1111 1111	32767	+2047.9375	+1023.9688	+511.9844	+255.9922
0111 1111 1111 1110	32766	+2047.8750	+1023.9376	+511.9688	+255.9844
…	…	…	…	…	…
0000 0000 0000 0001	1	+0.0625	+0.0312	+0.0156	+0.0078
0000 0000 0000 0000	0	0 deg/sec	0 deg/sec	0 deg/sec	0 deg/sec
1111 1111 1111 1111	-1	-0.0625	-0.0312	-0.0156	-0.0078
…	…	…	…	…	…
1000 0000 0000 0001	-32767	-2047.9375	-1023.9688	-511.9844	-255.9922
1000 0000 0000 0000	-32768	-2048.0000	-1024.0000	-512.0000	-256.0000

Table 14: Angular Rate (deg/sec) Calculation

Accelerometer Outputs

These registers contain 16-bits of valid angular rate data for each axis. The data is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per the table below.

16-bit Data (2's complement)	Equivalent Counts in decimal	Range = ±2g	Range = ±4g	Range = ±8g	Range = ±16g
0111 1111 1111 1111	32767	+2.0000g	+3.9999g	+7.9998g	+15.9996g
0111 1111 1111 1110	32766	+1.9999g	+3.9998g	+7.9995g	+15.9992g
…	…	…	…	…	…
0000 0000 0000 0001	1	+0.00006g	+0.0001g	+0.0002g	+0.0004g
0000 0000 0000 0000	0	0.000g	0.0000g	0.0000g	0.0000g
1111 1111 1111 1111	-1	-0.00006g	-0.0001g	-0.0002g	-0.0004g
…	…	…	…	…	…
1000 0000 0000 0001	-32767	-1.9999g	-3.9999g	-7.9998g	-15.9996g
1000 0000 0000 0000	-32768	-2.0000g	-4.0000g	-8.000g	-15.000g

Table 15: Acceleration (g) Calculation

Temperature Sensor Outputs

The temperature registers contain up to 16-bits of temperature data. Sensitivity can be considered as 128 counts/°C, or 7.8mC/LSB.

16-bit Register Data (2's complement)	Equivalent Counts in decimal	Temperature (°C)
0010 1010 1000 0000	10880	+85.000 °C
…	…	…
0000 0000 1000 0000	128	+1.0000 °C
…	…	…
0000 0000 0000 0001	1	+0.0078 °C
0000 0000 0000 0000	0	0.0000 °C
1111 1111 1111 1111	-1	-0.0078 °C
…	…	…
1111 1111 1000 0000	-128	-1.0000 °C
…	…	…
1110 1100 0000 0000	-5120	-40.000 °C

Table 16: Temperature (C) Calculation

Register Descriptions

TEMP_OUT

Temperature Output least and most significant bytes TEMP_OUT_L and TEMP_OUT_H

R	R	R	R	R	R	R	R
TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0
TEMP15	TEMP14	TEMP13	TEMP12	TEMP11	TEMP10	TEMP9	TEMP8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address: 0x00h,0x01h		

GYRO_XOUT

X-axis gyroscope output least and most significant bytes GYRO_XOUT_L and GYRO_XOUT_H

R	R	R	R	R	R	R	R
GYRO_X7	GYRO_X6	GYRO_X5	GYRO_X4	GYRO_X3	GYRO_X2	GYRO_X1	GYRO_X0
GYRO_X15	GYRO_X14	GYRO_X13	GYRO_X12	GYRO_X11	GYRO_X10	GYRO_X9	GYRO_X8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address:		0x02h,0x03h

GYRO_YOUT

Y-axis gyroscope output least and most significant bytes GYRO_YPUT_L and GYRO_YOUT_H

R	R	R	R	R	R	R	R
GYRO_Y7	GYRO_Y6	GYRO_Y5	GYRO_Y4	GYRO_Y3	GYRO_Y2	GYRO_Y1	GYRO_Y0
GYRO_Y15	GYRO_Y14	GYRO_Y13	GYRO_Y12	GYRO_Y11	GYRO_Y10	GYRO_Y9	GYRO_Y8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address: 0x04h,0x05h		

GYRO_ZOUT

Z-axis gyroscope output least and most significant bytes GYRO_ZOUT_L and GYRO_ZOUT_H

R	R	R	R	R	R	R	R
GYRO_Z7	GYRO_Z6	GYRO_Z5	GYRO_Z4	GYRO_Z3	GYRO_Z2	GYRO_Z1	GYRO_Z0
GYRO_Z15	GYRO_Z14	GYRO_Z13	GYRO_Z12	GYRO_Z11	GYRO_Z10	GYRO_Z9	GYRO_Z8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address: 0x06h,0x07h		

ACCEL_XOUT

X-axis accelerometer output least and most significant byte ACCEL_XOUT_L and ACCEL_XOUT_H

R	R	R	R	R	R	R	R
ACCEL_X7	ACCEL_X6	ACCEL_X5	ACCEL_X4	ACCEL_X3	ACCEL_X2	ACCEL_X1	ACCEL_X0
ACCEL_X11	ACCEL_X10	ACCEL_X9	ACCEL_X8	ACCEL_X7	ACCEL_X6	ACCEL_X5	ACCEL_X4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x08h,0x09h		

ACCEL_YOUT

Y-axis accelerometer output least and most significant byte ACCEL_YOUT_L and ACCEL_YOUT_H

R	R	R	R	R	R	R	R
ACCEL_Y7	ACCEL_Y6	ACCEL_Y5	ACCEL_Y4	ACCEL_Y3	ACCEL_Y2	ACCEL_Y1	ACCEL_Y0
ACCEL_Y11	ACCEL_Y10	ACCEL_Y9	ACCEL_Y8	ACCEL_Y7	ACCEL_Y6	ACCEL_Y5	ACCEL_Y4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x0Ah,0x0Bh		

ACCEL_ZOUT

Z-axis accelerometer output least and most significant byte ACCEL_ZOUT_L and ACCEL_ZOUT_H

R	R	R	R	R	R	R	R
ACCEL_Z7	ACCEL_Z6	ACCEL_Z5	ACCEL_Z4	ACCEL_Z3	ACCEL_Z2	ACCEL_Z1	ACCEL_Z0
ACCEL_Z11	ACCEL_Z10	ACCEL_Z9	ACCEL_Z8	ACCEL_Z7	ACCEL_Z6	ACCEL_Z5	ACCEL_Z4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x0Ch,0x0Dh		

AUX1_OUT

Auxiliary Sensor #1 output data bytes AUX1_OUT1 through AUX1_OUT6

R	R	R	R	R	R	R	R	Reset Value
AUX1_1_7	AUX1_1_6	AUX1_1_5	AUX1_1_4	AUX1_1_3	AUX1_1_2	AUX1_1_1	AUX1_1_0	0000
AUX1_2_7	AUX1_2_6	AUX1_2_5	AUX1_2_4	AUX1_2_3	AUX1_2_2	AUX1_2_1	AUX1_2_0	0000
AUX1_3_7	AUX1_3_6	AUX1_3_5	AUX1_3_4	AUX1_3_3	AUX1_3_2	AUX1_3_1	AUX1_3_0	0000
AUX1_4_7	AUX1_4_6	AUX1_4_5	AUX1_4_4	AUX1_4_3	AUX1_4_2	AUX1_4_1	AUX1_4_0	0000
AUX1_5_7	AUX1_5_6	AUX1_5_5	AUX1_5_4	AUX1_5_3	AUX1_5_2	AUX1_5_1	AUX1_5_0	0000
AUX1_6_7	AUX1_6_6	AUX1_6_5	AUX1_6_4	AUX1_6_3	AUX1_6_2	AUX1_6_1	AUX1_6_0	0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					I²C Address: 0x0Eh to 0x13h			

AUX2_OUT

Auxiliary Sensor #2 output data bytes AUX2_OUT1 through AUX2_OUT6

R	R	R	R	R	R	R	R	Reset Value
AUX2_1_7	AUX2_1_6	AUX2_1_5	AUX2_1_4	AUX2_1_3	AUX2_1_2	AUX2_1_1	AUX2_1_0	0000
AUX2_2_7	AUX2_2_6	AUX2_2_5	AUX2_2_4	AUX2_2_3	AUX2_2_2	AUX2_2_1	AUX2_2_0	0000
AUX2_3_7	AUX2_3_6	AUX2_3_5	AUX2_3_4	AUX2_3_3	AUX2_3_2	AUX2_3_1	AUX2_3_0	0000
AUX2_4_7	AUX2_4_6	AUX2_4_5	AUX2_4_4	AUX2_4_3	AUX2_4_2	AUX2_4_1	AUX2_4_0	0000
AUX2_5_7	AUX2_5_6	AUX2_5_5	AUX2_5_4	AUX2_5_3	AUX2_5_2	AUX2_5_1	AUX2_5_0	0000
AUX2_6_7	AUX2_6_6	AUX2_6_5	AUX2_6_4	AUX2_6_3	AUX2_6_2	AUX2_6_1	AUX2_6_0	0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					I^{2}C Address: 0x14h to 0x19h			

WAKE_CNT

Number of ODR cycles spent in wake state as measured in accelerometer ODRa_wake/ODRa_sleep periods. Data byte WAKE_CNT_L and WAKE_CNT_H.

R	R	R	R	R	R	R	R	Reset Value
WAKE_C7	WAKE_C6	WAKE_C5	WAKE_C4	WAKE_C3	WAKE_C2	WAKE_C1	WAKE_C0	0000
WAKE_C15	WAKE_C14	WAKE_C13	WAKE_C12	WAKE_C11	WAKE_C10	WAKE_C9	WAKE_C8	0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					I^{2}C Address: 0x1Ah,0x1Bh			

SLEEP_CNT

Number of ODR cycles spent in sleep state as measured in accelerometer ODRa_wake/ODRa_sleep periods. Data byte SLEEP_CNT_L and SLEEP_CNT_H.

R	R	R	R	R	R	R	R	Reset Value
SLEEP_C7	SLEEP _C6	SLEEP _C5	SLEEP _C4	SLEEP _C3	SLEEP _C2	SLEEP _C1	SLEEP _C0	0000
SLEEP _C15	SLEEP _C14	SLEEP _C13	SLEEP _C12	SLEEP _C11	SLEEP _C10	SLEEP _C9	SLEEP _C8	0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					I^{2}C Address: 0x1Ch,0x1D			

BUF_SMPLEV

Reports the number of data packets (ODR cycles) currently stored in the buffer. Reading the buffer contents, BUF_SMPLEV or BUF_PAST within 10 us from enabling or clearing the buffer is not permitted to avoid corrupted data. Data bytes BUF_SMPLEV_L and BUF_SMPLEV_H

R	R	R	R	R	R	R	R	Reset Value
BUFSLEV1	BUFSLEV0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0000
BUFSLEV9	BUFSLEV8	BUFSLEV7	BUFSLEV6	BUFSLEV5	BUFSLEV4	BUFSLEV3	BUFSLEV2	0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					I^{2}C Address:		0x1Eh,0x1Fh	

BUF_PAST

Reports the number of data packets lost since buffer has been filled. Reading the buffer contents, BUF_SMPLEV or BUF_PAST within 10 us from enabling or clearing the buffer is not permitted to avoid corrupted data. Data bytes BUF_PAST_L and BUF_PAST_H

R	R	R	R	R	R	R	R	Reset Value
BUFPAST1	BUFPAST0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0000
BUFPAST9	BUFPAST8	BUFPAST7	BUFPAST6	BUFPAST5	BUFPAST4	BUFPAST3	BUFPAST2	0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					I^{2}C Address:		0x20h,0x21h	

AUX_STATUS

Reports the status of Auxiliary Sensors AUX1 and AUX2.

R	R	R	R	R	R	R	R	
AUX2FAIL	AUX2ERR	AUX2ST1	AUX2ST0	AUX1FAIL	AUX1ERR	AUX1ST1	AUX1ST0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address:		0x22h	

AUX1ST[1:0] *- Detailed aux1 communication status.*

2'b00: Aux1 sensor is disabled.

Aux1 has not been enabled or ASIC has successfully sent disable cmd.

2'b01: Aux1 sensor is waiting to be enabled.

ASIC is attempting to enable aux sensor via enable sequence.

2'b10: Aux1 sensor is waiting to be disabled.

ASIC is attempting to disable aux sensor via disable sequence.

2'b11: Aux1 sensor is running.

ASIC has successfully sent aux enable cmd.

AUX1ERR *- Aux1 data read error flag.*
0: No error detected.
1: Missing ACK detected during aux1 polling. ASIC will retry polling aux device at next scheduled ODR period.
Flag is cleared by writing (any value) into AUX_STATUS register.

AUX1FAIL *- Aux1 command sequence failure flag.*
0: No failure detected.
1: Missing ACK detected after writing control register address to aux1 device during enable/disable command sequence. ASIC will suspend aux1 communications until AUX1FAIL bit is cleared by user.
Flag is cleared by writing (any value) into AUX_STATUS register.

AUX2ST[1:0] *- Detailed aux2 communication status.*
2'b00: Aux2 sensor is disabled.
Aux2 has not been enabled or ASIC has successfully sent disable cmd.
2'b01: Aux2 sensor is waiting to be enabled.
ASIC is attempting to enable aux sensor via enable sequence.
2'b10: Aux2 sensor is waiting to be disabled.
ASIC is attempting to disable aux sensor via disable sequence.
2'b11: Aux2 sensor is running.
ASIC has successfully sent aux enable cmd.

AUX2ERR *– Aux2 data read error flag.*
0: No error detected.
1: Missing ACK detected during aux2 polling. ASIC will retry polling aux device at next scheduled ODR period.
Flag is cleared by writing (any value) into AUX_STATUS register.

AUX2FAIL *– Aux2 command sequence failure flag.*
0: No failure detected.
1: Missing ACK detected after writing control register address to aux2 device during enable/disable command sequence. ASIC will suspend aux1 communications until AUX2FAIL bit is cleared by user.
Flag is cleared by writing (any value) into AUX_STATUS register.

WHO_AM_I
This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x24h.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100100
						I^{2}C Address:	0x30h	

SN
Individual Identification (serial number). Data bytes SN_1, SN_2, SN_3, SN_4.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8
SN23	SN22	SN21	SN20	SN19	SN18	SN17	SN16
SN31	SN30	SN29	SN28	SN27	SN26	SN25	SN24
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						I^{2}C Address:	0x31h – 0x34

STATUS1
Status register 1. GYRO_START = 1 and GYRO_RUN = 0 at system startup and go to GYRO_START = 0 and GYRO_RUN = 1 as the output rate signals become valid; permanent GYRO_START = 1 and GYRO_RUN = 0 indicate a damage in the device.

R	R	R	R	R	R	R	R	
INT1	POR	AUX2_ACT	AUX1_ACT	AUX_ERR	WAKE/SLEEP	GYRO_RUN	GYRO_START	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01000000
						I^{2}C Address:	0x36h	

INT1 *- reports Logical OR of non-masked interrupt sources sent to INT1 pin.*
0: No interrupt event.
1: Interrupt event.

POR *- Reset indicator.*
0: No reset has occurred since register was last read.
1: ASIC has exited reset phase.
This bit is automatically cleared when the status register is read.

AUX2_ACT *- Auxiliary sensor #2 active flag.*
0:Aux2 is not active. Aux2 has completed its disable sequence and is in standby mode.
1: Aux2 active. Aux2 has completed its enable sequence and is in active mode.

AUX1_ACT *- Auxiliary sensor #1 active flag.*
0:Aux1 is not active. Aux1 has completed its disable sequence and is in standby mode.
1: Aux1 active. Aux1 has completed its enable sequence and is in active mode.

AUX_ERR *- Auxiliary communications error.*
0: No aux communication error detected.
1: Aux communication error (missing ACK) detected.
Note:

- *The user should read aux_stat register to determine state of aux sensors upon aux error detection.*
- *The flag can be cleared through writing any value to AUX_STATUS register*

WAKE/SLEEP *- Wake/sleep status flag.*
0: Sleep mode.
1: Wake mode.

GYRO_START *- Gyroscope start-up flag.*
0: Gyro not in start-up mode.
1: Start-up mode.

GYRO_RUN *- Gyroscope run flag.*
0: control loop has not locked.
1: control loop has locked and gyroscope is active.

INT1_SRC1
Interrupt 1 source register 1

R	R	R	R	R	R	R	R	
INT1_BFI	INT1_WMI	INT1_WUFS	INT1_BTS	INT1_DRDY_AUX2	INT1_DRDY_AUX1	INT1_DRDY_ACC	INT1_DRDY_GYRO	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x37h			

***INT1_BFI** - Buffer full interrupt.*
0: Buffer is not full.
1: Buffer is full.
This bit is cleared when the int1_l register is read or when the buffer full condition ceases to exist.

***INT1_WMI** - Buffer water mark interrupt.*
0: Watermark has not been reached.
1: Watermark has been reached.
This bit is cleared when the int1_l register is read or when the water mark condition ceases to exist.

***INT1_WUFS** - Wake-up function interrupt.*
0: No Wake-up event detected.
1: Wake-up event detected.
This bit is cleared when the int1_l register is read.

***INT1_BTS** – Back-to-sleep interrupt.*
0: No back-to-sleep event detected.
1: Back-to-sleep event detected.
This bit is cleared when the int1_l register is read.

***INT1_DRDY_AUX2** - Aux2 data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int1_l register or when the aux2_out1 register is read.

***INT1_DRDY_AUX1** – Aux1 data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int1_l register or when the aux1_out1 register is read.

INT1_DRDY_ACC – *Accelerometer data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int1_l register or when the acc_xout_l register (x06) is read.

INT1_DRDY_GYRO – *Gyro data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int1_l register or when the gyro_xout_l register (x00) is read.

INT1_SRC2
Interrupt 1 source register 2

R	R	R	R	R	R	R	R	
Reserved	Reserved	INT1_XNWU	INT1_XPWU	INT1_YNWU	INT1_YPWU	INT1_ZNWU	INT1_ZPWU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x38h			

INT1_XNWU - *WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on x-axis, negative direction.

INT1_XPWU - *WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on x-axis, positive direction.

INT1_YNWU - *WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on y-axis, negative direction.

INT1_YPWU – *WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on y-axis, positive direction.

INT1_ZNWU - *WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on z-axis, negative direction.

***INT1_ZPWU** – WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on z-axis, positive direction.

INT1_L
Interrupt 1 Latch Release – Reading the interrupt1 latch release register clears the interrupt1 source (int1_src1 and int1_src2) registers. Reading int1_l returns x00 in user mode.

R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x39h		

STATUS2
Status register 2. GYRO_START = 1 and GYRO_RUN = 0 at system startup and go to GYRO_START = 0 and GYRO_RUN = 1 as the output rate signals become valid; permanent GYRO_START = 1 and GYRO_RUN = 0 indicate a damage in the device.

R	R	R	R	R	R	R	R	
INT2	POR	AUX2_ACT	AUX1_ACT	AUX_ERR	WAKE/SLEEP	GYRO_RUN	GYRO_START	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01000000
					I^2C Address:			0x3Ah

***INT2** - reports Logical OR of non-masked interrupt sources sent to INT2 pin.*
0: No interrupt event.
1: Interrupt event.

***POR** - Reset indicator.*
0: No reset has occurred since register was last read.
1: ASIC has exited reset phase.
This bit is automatically cleared when the status register is read.

***AUX2_ACT** - Auxiliary sensor #2 active flag.*
0:Aux2 is not active. Aux2 has completed its disable sequence and is in standby mode.
1: Aux2 active. Aux2 has completed its enable sequence and is in active mode.

***AUX1_ACT** - Auxiliary sensor #1 active flag.*
0:Aux1 is not active. Aux1 has completed its disable sequence and is in standby mode.
1: Aux1 active. Aux1 has completed its enable sequence and is in active mode.

AUX_ERR *- Auxiliary communications error.*
0: No aux communication error detected.
1: Aux co communication mm error (missing ACK) detected.
Note: The user should read aux_stat register to determine state of aux sensors upon aux error detection.

WAKE/SLEEP *- Wake/sleep status flag.*
0: Sleep mode.
1: Wake mode.

GYRO_START *- Gyroscope start-up flag.*
0: Gyro not in startup mode.
1: Start up mode.

GYRO_RUN *- Gyroscope run flag.*
0: control loop has not locked.
1: control loop has locked and gyroscope is active.

INT2_SRC1
Interrupt 2 source register 1

R	R	R	R	R	R	R	R	
INT2_BFI	INT2_WMI	INT2_WUFS	INT2_BTS	INT2_DRDY_AUX2	INT2_DRDY_AUX1	INT2_DRDY_ACC	INT2_DRDY_GYRO	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x3Bh			

INT2_BFI *- Buffer full interrupt.*
0: Buffer is not full.
1: Buffer is full.
This bit is cleared when the int2_l register is read or when the buffer full condition ceases to exist.

INT2_WMI *- Buffer water mark interrupt.*
0: Watermark has not been reached.
1: Watermark has been reached.
This bit is cleared when the int2_l register is read or when the water mark condition ceases to exist.

INT2_WUFS *- Wake-up function interrupt.*
0: No Wake-up event detected.
1: Wake-up event detected.
This bit is cleared when the int2_l register is read.

INT2_BTS *– Back-to-sleep interrupt.*
0: No back-to-sleep event detected.
1: Back-to-sleep event detected.
This bit is cleared when the int2_l register is read.

INT2_DRDY_AUX2 *- Aux2 data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int2_l register or when the aux2_out1 register is read.

INT2_DRDY_AUX1 *– Aux1 data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int2_l register or when the aux1_out1 register is read.

***INT2_DRDY_ACC** – Accelerometer data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int2_l register or when the acc_xout_l register (x06) is read.

***INT2_DRDY_GYRO** – Gyro data ready interrupt.*
0: New sensor data is not ready.
1: New sensor data is ready.
This bit is cleared when the int2_l register or when the gyro_xout_l register (x00) is read.

INT2_SRC2
Interrupt 2 source register 2

R	R	R	R	R	R	R	R	
Reserved	Reserved	INT2_XNWU	INT2_XPWU	INT2_YNWU	INT2_YPWU	INT2_ZNWU	INT2_ZPWU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x3Ch			

INT2_XNWU *- WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on x-axis, negative direction.

INT2_XPWU *- WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on x-axis, positive direction.

INT2_YNWU *- WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on y-axis, negative direction.

INT2_YPWU *– WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on y-axis, positive direction.

INT2_ZNWU *- WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on z-axis, negative direction.

INT2_ZPWU *– WUF directional indicator bit.*
0: no interrupt event.
1: Wake-up event detected on z-axis, positive direction.

INT2_L
Interrupt 2 Latch Release – Reading the interrupt2 latch release register clears the interrupt2 source (int1_src2 and int2_src2) registers. Reading int2_l returns x00 in user mode.

R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I²C Address: 0x3Dh		

ACCEL_ODR_WAKE
Accelerometer Wake Mode Control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
LPMODE_W	NAVG_W2	NAVG_W1	NAVG_W0	ODRA_W3	ODRA_W2	ODRA_W1	ODRA_W0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11010110
					I²C Address: 0x3Eh			

LPMODE_W *- Accelerometer wake state low power mode enable.*
0: Accelerometer low power mode is disabled in wake state.
Accelerometer operates at max sampling rate and navg_wake is ignored.
1: Accelerometer low power mode is enabled in wake state.
Accelerometer operates in duty cycle mode with number of samples set by navg_wake
Note: The LPMODE_W = 1 setting would be ignored and device would not operate in duty cycle mode when ODR for either accelerometer or gyro is set for 400Hz or higher.

NAVG_W[2:0]: *Accelerometer wake mode OSR control. The max over sampling rate (or max number of samples averaged) varies with ODR.*

[2]	[1]	[0]	Number of Averages
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ODRA_W[3:0]: *Determines accelerometer ODR in wake mode*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	3200Hz
1	1	0	1	6400Hz
1	1	1	0	12800Hz
1	1	1	1	51200Hz

ACCEL_ODR_SLEEP
Accelerometer Wake Mode Control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
LPMODE_S	NAVG_S2	NAVG_S1	NAVG_S0	ODRA_S3	ODRA_S2	ODRA_S1	ODRA_S0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11010110
						I^2C Address:	0x3Fh	

LPMODE_S *- Accelerometer sleep state low power mode enable.*
0: Accelerometer low power mode is disabled in sleep state.
Accelerometer operates at max sampling rate and navg_sleep is ignored.
1: Accelerometer low power mode is enabled in sleep state.
Accelerometer operates in duty cycle mode with number of samples set by navg_sleep.
Note: The LPMODE_S = 1 setting would be ignored and device would not operate in duty cycle mode when ODR for either accelerometer or gyro is set for 400Hz or higher.

NAVG_S[2:0]: *Accelerometer sleep mode OSR control. The max over sampling rate (or max number of samples averaged) varies with ODR.*

[2]	[1]	[0]	Number of Averages
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ODRA_S[3:0]: *Determines accelerometer ODR in sleep mode*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	3200Hz
1	1	0	1	6400Hz
1	1	1	0	12800Hz
1	1	1	1	51200Hz

ACCEL_CTL
Accelerometer range control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ACC_FS_S1	ACC_FS_S0	Reserved	Reserved	ACC_FS_W1	ACC_FS_W0	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x40h			

ACC_FS_S[1:0] *Accelerometer sleep mode full scale range select.*
2'b00: ± 2 g
2'b01: ± 4 g,
2'b10: ± 8 g,
2'b11: ± 16 g

ACC_FS_W[1:0] *Accelerometer wake mode full scale range select.*
2'b00: ± 2 g
2'b01: ± 4 g,
2'b10: ± 8 g,
2'b11: ± 16 g

GYRO_ODR_WAKE
Gyroscope Wake Mode Control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
GYRO_FS_W1	GYRO_FS_W0	GYRO_BW_W1	GYRO_BW_W0	ODRG_W3	ODRG_W2	ODRG_W1	ODRG_W0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
					I²C Address: 0x41h			

GYRO_FS_W[1:0]: *Gyroscope angular velocity range wake mode*
.

[1]	[0]	Range
0	0	±256
0	1	±512
1	0	±1024
1	1	±2048

GYRO_BW_W[1:0]: *Gyroscope bandwidth selection in wake mode.*

[1]	[0]	BW
0	0	10 Hz
0	1	20 Hz
1	0	40 Hz
1	1	160 Hz

ODRG_W[3:0]: *Determines gyroscope ODR in wake mode*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	1600Hz
1	1	0	1	1600Hz
1	1	1	0	1600Hz
1	1	1	1	1600Hz

GYRO_ODR_SLEEP

Gyroscope Sleep Mode Control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
GYRO_FS_S1	GYRO_FS_S0	GYRO_BW_S1	GYRO_BW_S0	ODRG_S3	ODRG_S2	ODRG_S1	ODRG_S0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
					I²C Address: 0x42h			

***GYRO_FS_S[1:0]:** Gyroscope angular velocity range in sleep mode.*

[1]	[0]	Range
0	0	±256
0	1	±512
1	0	±1024
1	1	±2048

***GYRO_BW_S[1:0]:** Gyroscope bandwidth selection in sleep mode.*

[1]	[0]	BW
0	0	10 Hz
0	1	20 Hz
1	0	40 Hz
1	1	160 Hz

ODRG_S[3:0]: *Determines gyroscope ODR in sleep mode*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	1600Hz
1	1	0	1	1600Hz
1	1	1	0	1600Hz
1	1	1	1	1600Hz

STDBY

Stand-by and operational control register. KXG03 register settings can be applied prior to enabling the Accel or Gyro. Enabling the sensor “locks in” the user register settings. Altering register settings after enable is not recommended.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
AUX2_STDBY_S	AUX1_STDBY_S	GYRO_STDBY_S	Reserved	AUX2_STDBY_W	AUX1_STDBY_W	GYRO_STDBY_W	ACC_STDBY	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11101111
				I^{2}C Address: 0x43h				

AUX2_STDBY_S *- Active low aux2 sensor enable.*
0: Aux2 sensor is enabled in sleep state.
1: Aux2 sensor is disabled in sleep state.

AUX1_STDBY_S *- Active low aux1 sensor enable.*
0: Aux1 sensor is enabled in sleep state.
1: Aux1 sensor is disabled in sleep state

GYRO_STDBY_S *- Active low gyroscope sensor enable.*
0: Gyro sensor is enabled in sleep state.
1: Gyro sensor is disabled in sleep state.

AUX2_STDBY_W *- Active low aux2 sensor enable.*
0: Aux2 sensor is enabled in wake state.
1: Aux2 sensor is disabled in wake state.

AUX1_STDBY_W *- Active low aux1 sensor enable.*
0: Aux1 sensor is enabled in wake state.
1: Aux1 sensor is disabled in wake state.

GYRO_STDBY_W *- Active low gyroscope sensor enable.*
0: Gyro sensor is enabled in wake state.
1: Gyro sensor is disabled in wake state.

ACC_STDBY *- Active low Accelerometer sensor enable.*
0: Accelerometer sensor is enabled.
1: Accelerometer sensor is disabled.

CTL_REG_1

Special control register 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RST	Reserved	Reserved	TEMP_STDBY_S	TEMP_STDBY_W	Reserved	ACC_STPOL	ACC_ST	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00011000
					I^2C Address: 0x44h			

***RST** - Active high soft reset.*
0: No reset.
1: ASIC enters reset sequence. All registers are cleared. ASIC may initiate power up sequence.
This bit is self-clearing.

***TEMP_STDBY_S** - Sleep mode temperature output standby bit.*
0: Temperature output is enabled in sleep mode.
1: Temperature output is disabled in sleep mode.

***TEMP_STDBY_W** - Wake mode temperature output standby bit.*
0: Temperature output is enabled in wake mode.
1: Temperature output is disabled in wake mode.

***ACC_STPOL** - Defines accelerometer self-test polarity.*
0: Accelerometer self-test polarity is not inverted.
1: Accelerometer self-test polarity is inverted.

***ACC_ST** - Active high accelerometer self-test enable.*
0: Accelerometer self-test is disabled.
1: Accelerometer self-test is enabled.

INT_PIN_CTL

This register controls the settings for the physical interrupt pins INT1 and INT2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
IEN2	IEA2	IEL2_1	IEL2_0	IEN1	IEA1	IEL1_1	IEL1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01000100
					I^{2}C Address: 0x45h			

IEN2 - *Active high enable for INT2 pin.*
0: INT2 pin is disabled and output is forced to non-asserted state.
1: INT2 pin is enabled. Output state is either high or low depending on status of selected interrupt sources.

IEA2 - *Interrupt polarity select for INT2 pin.*
0: INT2 is active low. Pin pulls low during interrupt event.
1: INT2 is active high. Pin pulls high during interrupt event.

IEL2[1:0]: *Interrupt latch mode select for INT2 pin.*
2'b00: Latched. Once an interrupt has triggered INT2 remains in its interrupt state defined by IEA2 until the interrupt source has been cleared.
2'b01: Pulsed. Once an interrupt has triggered INT2 remains in its interrupt state defined by IEA2 for a period of 50 us before returning to the non-interrupt state.
2'b10: Pulsed. Once an interrupt has triggered INT2 remains in its interrupt state defined by IEA2 for a period of 200 us before returning to the non-interrupt state.
2'b11: Real time mode. INT2 only remains asserted as long as underlying interrupt conditions exist.

IEN1 - *Active high enable for INT1 pin.*
0: INT1 pin is disabled and output is forced to non-asserted state.
1: INT1 pin is enabled. Output state is either high or low depending on status of selected interrupt sources.

IEA1 - *Interrupt polarity select for INT1 pin.*
0: INT1 is active low. Pin pulls low during interrupt event.
1: INT1 is active high. Pin pulls high during interrupt event.

IEL1[1:0]: *Interrupt latch mode select for INT1 pin.*
2'b00: Latched. Once an interrupt has triggered INT1 remains in its interrupt state defined by IEA2 until the interrupt source has been cleared.

2'b01: Pulsed. Once an interrupt has triggered INT1 remains in its interrupt state defined by IEA2 for a period of 50 us before returning to the non-interrupt state.
2'b10: Pulsed. Once an interrupt has triggered INT1 remains in its interrupt state defined by IEA2 for a period of 200 us before returning to the non-interrupt state.
2'b11: Real time mode. INT1 only remains asserted as long as underlying interrupt conditions exist.

INT_PIN1_SEL
Physical interrupt pin INT1 select register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BFI_P1	WMI_P1	WUF_P1	BTS_P1	DRDY_AUX2_ P1	DRDY_AUX1_ P1	DRDY_ACC_ P1	DRDY_GYRO_ P1	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11111111
					I²C Address: 0x46h			

***BFI_P1** – Buffer Full Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

***WMI_P1** – Water Mark Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

***WUF_P1** – Wake-up Function Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

***BTS_P1** – Back-to-sleep Function Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

***DRDY_AUX2_P1** – Data Ready Aux2 Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

***DRDY_AUX1_P1** – Data Ready AUX1 Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

DRDY_ACC_P1 *– Data Ready Accelerometer Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

DRDY_GYRO_P1 *– Data Ready Gyroscope Interrupt for INT1 pin.*
0: Corresponding interrupt is not routed to INT1 pin.
1: Corresponding interrupt is routed to INT1 pin.

INT_PIN2_SEL
Physical interrupt pin INT2 select register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BFI_P2	WMI_P2	WUF_P2	BTS_P2	DRDY_AUX2_P2	DRDY_AUX1_P2	DRDY_ACC_P2	DRDY_GYRO_P2	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x47h			

BFI_P2 *– Buffer Full Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

WMI_P2 *– Water Mark Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

WUF_P2 *– Wake-up Function Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

BTS_P2 *– Back-to-sleep Function Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

DRDY_AUX2_P2 *– Data Ready Aux2 Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

DRDY_AUX1_P2 *– Data Ready AUX1 Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

DRDY_ACC_P2 *– Data Ready Accelerometer Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

DRDY_GYRO_P2 *– Data Ready Gyroscope Interrupt for INT2 pin.*
0: Corresponding interrupt is not routed to INT2 pin.
1: Corresponding interrupt is routed to INT2 pin.

INT_MASK1

Interrupt mask register 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BFIE	WMIE	WUFE	BTSE	DRDY_AUX2	DRDY_AUX1	DRDY_ACC	DRDY_GYRO	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11000000
					I^{2}C Address: 0x48h			

BFIE *– Buffer Full Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

WMIE *– Water Mark Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

WUFE *– Wake-up Function Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

BTSE *– Back-to-sleep Function Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked). 1: Corresponding interrupt is routed to INT1 pin.

DRDY_AUX2 *– Data Ready Aux2 Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

DRDY_AUX1 *– Data Ready AUX1 Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

***DRDY_ACC** – Data Ready Accelerometer Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

***DRDY_GYRO** – Data Ready Gyroscope Interrupt enable/mask bit.*
0: Corresponding interrupt is disabled (masked).
1: Corresponding interrupt is enabled.

INT_MASK2

Interrupt mask register 2. This register controls which axis and direction of detected motion can cause an interrupt.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					I^{2}C Address: 0x49h			

***NXWUE** - x negative (x-) mask for WUF/BTS, 0=disable, 1=enable.*
***PXWUE** - x positive (x+) mask for WUF/BTS, 0=disable, 1=enable.*
***NYWUE** - y negative (y-) mask for WUF/BTS, 0=disable, 1=enable.*
***PYWUE** - y positive (y+) mask for WUF/BTS, 0=disable, 1=enable.*
***NZWUE** - z negative (z-) mask for WUF/BTS, 0=disable, 1=enable.*
***PZWUE** - z positive (z+) mask for WUF/BTS, 0=disable, 1=enable.*

FSYNC_CNT

External Synchronous control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	FSYNC_ MODE1	FSYNC_ MODE2	Reserved	FSYNC_SEL2	FSYNC_SEL1	FSYNC_SEL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x4Ah			

***FSYNC_MODE[1:0]:** FSYNC enable and mode select.*
2'b00: FSYNC is disabled. SYNC pin is tri-stated.
2'b01: FSYNC is enabled. Sync pin is configured as input pin.
Buffer is updated in sync with external clock applied at SYNC pin.
2'b10: FSYNC is enabled. Sync pin is configured as input pin.
State of SYNC pin is stored in selected sensor's LSB bit.
2'b11: FSYNC is disabled. SYNC pin is configured as output pin.

FSYNC_SEL[2:0]: *FSYNC sensor select bits.*
if(fsync_mode=2'b10)
3'b000: SYNC function disabled.
3'b001: State of SYNC pin is stored in gyroscope's x LSB bit.
3'b010: State of SYNC pin is stored in gyroscope's y LSB bit.
3'b011: State of SYNC pin is stored in gyroscope's z LSB bit
3'b100: State of SYNC pin is stored in accelerometer's x LSB bit.
3'b101: State of SYNC pin is stored in accelerometer's y LSB bit.
3'b110: State of SYNC pin is stored in accelerometer's z LSB bit.
3'b111: State of SYNC pin is stored in temperature LSB bit
if(fsync_mode=2'b11)
3'b000: SYNC pin outputs gyroscope ODR clock.
3'b001: SYNC pin outputs accelerometer's ODR clock.
3'b010: SYNC pin outputs aux1 ODR clock.
3'b011: SYNC pin outputs aux2 ODR clock.
3'b1xx: SYNC pin disabled.

WAKE_SLEEP_CTL1
Wake and Sleep control register 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BTS_EN	WUF_EN	MAN_SLEEP	MAN_WAKE	Reserved	OWUF2	OWUF1	OWUF0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x4Bh			

BTS_EN *- Active high back-to-sleep function enable.*
0: Back-to-sleep transition for all sensors is not controlled by BTS function.
1: Back-to-sleep transition for all sensors is controlled by BTS function.

WUF_EN *- Active high wake-up function enable.*
0: Sleep-to-wake transition for all sensors is not controlled by BTS function.
1: Sleep-to-wake transition for all sensors is controlled by BTS function.

MAN_SLEEP *- Active high manual sleep trigger.*
0: No impact.
1: Forces transition to sleep state.
Please note:
Man_sleep is a self-clearing bit. The bit is cleared automatically after transition to sleep state.
Forcing a manual sleep state does not trigger WUFS or BTS interrupts.
Setting both man_sleep=1 and man_wake=1 is ignored.

MAN_WAKE *- Active high manual wake trigger.*
0: No impact.
1: Forces transition to wake state.

Please note:
Man_sleep is a self-clearing bit. The bit is cleared automatically after transition to sleep state.
Forcing a manual sleep state does not trigger WUFS or BTS interrupts.
Setting both man_sleep=1 and man_wake=1 is ignored.

OWUF[2:0]: *sets the Output Data Rate for the Wake-up (motion detection).*

[2]	[1]	[0]	Output Data Rate (Hz)
0	0	0	0.781
0	0	1	1.563
0	1	0	3.125
0	1	1	6.25
1	0	0	12.5
1	0	1	25
1	1	0	50
1	1	1	100

WAKE_SLEEP_CTL2
Wake and Sleep control register 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TH_MODE	C_MODE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000010
					I²C Address: 0x4Ch			

TH_MODE *- Defines WUF and BTS threshold mode.*
0: Absolute threshold. ASIC compares current output to threshold.
1: Relative threshold. ASIC compares difference between current output and previous output to threshold.

C_MODE *- Defines de-bounce counter clear mode.*
0: Counter is cleared once activity level is outside the threshold.
1: Counter is decremented by one when activity level is outside the threshold.

WUF_TH

This register sets the Active Threshold for wake-up (motion detect) interrupt. The KXG03 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g.
Resolution = 62.5 mg/LSB for FS < ± 16 g.
Resolution =125 mg/LSB for FS = ± 16 g.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ATH_7	ATH_6	ATH_5	ATH_4	ATH_3	ATH_2	ATH_1	ATH_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001000
					I²C Address: 0x4Dh			

WUF_COUNTER

This register sets the time motion must be present before a wake-up interrupt is set. Every count is calculated as 1/OWUF delay period. OWUF is set in WAKE_SLEEP_CTL1.
Note: Setting the register to 0xFF disables the WUF_COUNTER.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
WUTH7	WUTH6	WUTH5	WUTH4	WUTH3	WUTH2	WUTH1	WUTH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x4Eh			

BTS_TH

This register sets the threshold for Back-to-sleep (motion detect) interrupt. The KXG03 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g.
Resolution = 62.5 mg/LSB for FS < ± 16 g.
Resolution = 125 mg/LSB for FS = ± 16 g.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BTH_7	BTH_6	BTH_5	BTH_4	BTH_3	BTH_2	BTH_1	BTH_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001000
					I²C Address: 0x4Fh			

BTS_COUNTER

This register sets the time motion must be present before a Back-to-sleep interrupt is set. Every count is calculated as 16/ OWUF delay period. OWUF is set in WAKE_SLEEP_CTL1.
Note: Setting the register to 0xFF disables the BTS_COUNTER.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BTSC7	BTSC6	BTSC5	BTSC4	BTSC3	BTSC2	BTSC1	BTSC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x50h			

AUX_I2C_CTRL_REG
Read/Write control register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	AUX_CTL_POL2	AUX_CTL_POL1	AUX_BUS_SPD	AUX_PULL_UP	AUX_BYPASS	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000001
					I^2C Address: 0x51h			

AUX_CTL_POL2 *- Defines control bit polarity for aux2 enable/disable command sequences.*
0: ASIC clears selected control bits when enabling auxilary-2 sensor and ASIC sets to 1 selected control bits when disabling aux2 sensor.
1: ASIC sets to 1 selected control bits when enabling auxilary-2 sensor and ASIC clears selected control bits when disabling aux2 sensor.

AUX_CTL_POL1 *- Defines control bit polarity for aux1 enable/disable command sequences.*
0: ASIC clears selected control bits when enabling auxilary-1 sensor and ASIC sets to 1 selected control bits when disabling aux1 sensor.
1: ASIC sets to 1 selected control bits when enabling auxilary-1 sensor and ASIC clears selected control bits when disabling aux1 sensor.

AUX_BUS_SPD*- Sets I2C bus speed.*
0: 100 kHz,
1: 400 kHz

AUX_PULL_UP *- Active high pull up enable.*
0: Pull up disabled.
1: 1.5KΩ pull up resistor enabled.
Please not the pull up resistor is automatically disabled when aux_bypass=1 even though aux_pull_up may be set to 1.

AUX_BYPASS – *Active high bypass enable.*
0: Aux I2C not bypassed.
1: Aux I2C pins shorted to main (slave) I2C pins. Pull up disabled.

AUX_I2C_SAD1

Read/Write that should be used to store the SAD for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SAD1_6	SAD1_5	SAD1_4	SAD1_3	SAD1_2	SAD1_1	SAD1_0	-	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x52h			

AUX_I2C_REG1

Read/Write that should be used to store the starting data register address for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
REG1_7	REG1_6	REG1_5	REG1_4	REG1_3	REG1_2	REG1_1	REG1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x53h			

AUX_I2C_CTL1

Register address for enable/disable control register for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
CNTL1_7	CNTL1_6	CNTL1_5	CNTL1_4	CNTL1_3	CNTL1_2	CNTL1_1	CNTL1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x54h			

AUX_I2C_BIT1

Defines bits to toggle in the control register for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BIT1_7	BIT1_6	BIT1_5	BIT1_4	BIT1_3	BIT1_2	BIT1_1	BIT1_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x55h			

AUX_I2C_ODR1_W

Defines register read controls for auxiliary I^{2}C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	AUX1_D2	AUX1_D1	AUX1_D0	AUX1ODRW3	AUX1ODRW2	AUX1ODRW1	AUX1ODRW0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
					I^{2}C Address: 0x56h			

AUX1_D[2:0]: *Number of bytes read back via Auxiliary I^{2}C bus from device 1*

[2]	[1]	[0]	No. of
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	DNE

AUX1ODRW[3:0]: *Determines rate at which aux1 output is polled by ASIC in aux1 wake state*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	1600Hz
1	1	0	1	1600Hz
1	1	1	0	1600Hz
1	1	1	1	1600Hz

AUX_I2C_ODR1_S

Defines register read controls for auxiliary I^2C device 1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	Reserved	Reserved	AUX1ODRS3	AUX1ODRS2	AUX1ODRS1	AUX1ODRS0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
				I^2C Address: 0x57h				

***AUX1ODRS[3:0]:** Determines rate at which aux1 output is polled by ASIC in aux1 sleep state*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	1600Hz
1	1	0	1	1600Hz
1	1	1	0	1600Hz
1	1	1	1	1600Hz

AUX_I2C_SAD2

Read/Write that should be used to store the SAD for auxiliary I^2C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SAD2_6	SAD2_5	SAD2_4	SAD2_3	SAD2_2	SAD2_1	SAD2_0	-	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x58h			

AUX_I2C_REG2
Read/Write that should be used to store the starting data register address for auxiliary I^{2}C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
REG2_7	REG2_6	REG2_5	REG2_4	REG2_3	REG2_2	REG2_1	REG2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x59h			

AUX_I2C_CTL2
Register address for enable/disable control register for auxiliary I^{2}C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
CNTL2_7	CNTL2_6	CNTL2_5	CNTL2_4	CNTL2_3	CNTL2_2	CNTL2_1	CNTL2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x5Ah			

AUX_I2C_BIT2
Defines bits to toggle in the control register for auxiliary I^{2}C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BIT2_7	BIT2_6	BIT2_5	BIT2_4	BIT2_3	BIT2_2	BIT2_1	BIT2_0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x5Bh			

AUX_I2C_ODR2_W
Defines register read controls for auxiliary I^{2}C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	AUX2_D2	AUX2_D1	AUX2_D0	AUX2ODRW3	AUX2ODRW2	AUX2ODRW1	AUX2ODRW0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
				I^{2}C Address: 0x5Ch				

AUX2_D[2:0]: *Number of bytes read back via Auxiliary I²C bus from device 2*

[2]	[1]	[0]	No. of Bytes
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	DNE

AUX2ODRW[3:0]: *Determines rate at which aux2 output is polled by ASIC in aux2 wake state*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	1600Hz
1	1	0	1	1600Hz
1	1	1	0	1600Hz
1	1	1	1	1600Hz

AUX_I2C_ODR2_S
Defines register read controls for auxiliary I²C device 2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	Reserved	Reserved	AUX2ODRS3	AUX2ODRS2	AUX2ODRS1	AUX2ODRS0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
					I²C Address: 0x5Dh			

***AUX2ODRS[3:0]:** Determines rate at which aux2 output is polled by ASIC in aux2 sleep state*

[3]	[2]	[1]	[0]	Output Data Rate
0	0	0	0	0.781Hz
0	0	0	1	1.563Hz
0	0	1	0	3.125Hz
0	0	1	1	6.25Hz
0	1	0	0	12.5Hz
0	1	0	1	25Hz
0	1	1	0	50Hz
0	1	1	1	100Hz
1	0	0	0	200Hz
1	0	0	1	400Hz
1	0	1	0	800Hz
1	0	1	1	1600Hz
1	1	0	0	1600Hz
1	1	0	1	1600Hz
1	1	1	0	1600Hz
1	1	1	1	1600Hz

BUF_WMITH_L
Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SMP_TH1	SMP_TH0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x75h			

BUF_WMITH_H
Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SMP_TH9	SMP_TH8	SMP_TH7	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x76h			

SMP_TH[9:0] Sample Threshold*; determines the number of data packets (ODR cycles) in a watermark interrupt in FIFO, Stream, FILO, or TRIGGER mode.*

BUF_TRIGTH_L
Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TRIG_TH1	TRIG_TH0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x77h			

BUF_TRIGTH_H
Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TRIG_TH9	TRIG_TH8	TRIG_TH7	TRIG_TH6	TRIG_TH5	TRIG_TH4	TRIG_TH3	TRIG_TH2	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x78h			

TRIG_TH[9:0] Trigger Threshold*; determines the number of data packets (ODR cycles) that will trigger an interrupt in Trigger mode.*

BUF_CTL2
Read/write control register that controls sample buffer input in wake mode.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	BUF_TEMP_W	BUF_ACC_W_X	BUF_ACC_W_Y	BUF_ACC_W_Z	BUF_GYR_W_X	BUF_GYR_W_Y	BUF_GYR_W_Z	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x79h			

***BUF_TEMP_W** controls the Temperature input into the sample buffer.*
BUF_TEMP_W = 0 – Temperature data is not input into the sample buffer
BUF_TEMP_W = 1 – Temperature data is input into the sample buffer

***BUF_ACC_W[XYZ]** controls the Accelerometer axis input into the sample buffer.*
BUF_ACC_W = 0 – Accelerometer data is not input into the sample buffer
BUF_ACC_W = 1 – Accelerometer data is input into the sample buffer

***BUF_GYR_W[XYZ]** controls the Gyroscope axis input into the sample buffer.*
BUF_GYR_W = 0 – Gyroscope data is not input into the sample buffer
BUF_GYR_W = 1 – Gyroscope data is input into the sample buffer

BUF_CTL3
Read/write control register that controls sample buffer input in sleep mode.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	BUF_TEMP_S	BUF_ACC_S_X	BUF_ACC_S_Y	BUF_ACC_S_Z	BUF_GYR_S_X	BUF_GYR_S_Y	BUF_GYR_S_Z	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I²C Address: 0x7Ah			

***BUF_TEMP_S** controls the Temperature input into the sample buffer.*
BUF_TEMP_S = 0 – Temperature data is not input into the sample buffer
BUF_TEMP _S= 1 – Temperature data is input into the sample buffer

***BUF_ACC_S[XYZ]** controls the Accelerometer axis input into the sample buffer.*
BUF_ACC_S = 0 – Accelerometer data is not input into the sample buffer
BUF_ACC_S = 1 – Accelerometer data is input into the sample buffer

***BUF_GYR_S[XYZ]** controls the Gyroscope axis input into the sample buffer.*
BUF_GYR_S = 0 – Gyroscope data is not input into the sample buffer
BUF_GYR_S = 1 – Gyroscope data is input into the sample buffer

BUF_CTL4
Read/write control register that controls aux1 and aux2 buffer input.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	Reserved	Reserved	BUF_AUX2_S	BUF_AUX1_S	BUF_AUX2_W	BUF_AUX1_W	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x7Bh			

BUF_AUX2_S *controls the aux2 input into the sample buffer in sleep mode.*
BUF_AUX2_S = 0 – aux2 data is not input into the sample buffer
BUF_AUX2 _S= 1 – aux2 data is input into the sample buffer

BUF_AUX1_S *controls the aux1 axis input into the sample buffer in sleep mode.*
BUF_AUX1_S = 0 – aux1 data is not input into the sample buffer
BUF_AUX1_S = 1 – aux1 data is input into the sample buffer

BUF_AUX2_W *controls the aux2 input into the sample buffer in wake mode.*
BUF_AUX2_W = 0 – aux2 data is not input into the sample buffer
BUF_AUX2 _W= 1 – aux2 data is input into the sample buffer

BUF_AUX1_W *controls the aux1 axis input into the sample buffer in wake mode.*
BUF_AUX1_W = 0 – aux1 data is not input into the sample buffer
BUF_AUX1_W = 1 – aux1 data is input into the sample buffer

BUF_EN
Read/write control register that controls sample buffer operation.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BUFE	Reserved	Reserved	Reserved	BUF_SYM1	BUF_SYM0	BUF_M1	BUF_M0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^{2}C Address: 0x7Ch			

BUFE *– controls activation of the sample buffer.*
BUFE = 0 – sample buffer inactive
BUFE = 1 – sample buffer active

***BUF_SYM1, BUF_SYM0** – Symbol mode select.*

BUF_SYM1	BUF_SYM0	Description
0	0	Symbol mode disabled. ASIC does not insert symbols into buffer output data stream.
0	1	Single symbol mode enabled. ASIC inserts x8000 between complete data sets whenever wake/sleep mode changes. ASIC replaces x8000 in gyroscope, accelerometer and die temp data with x8001 codes.
1	0	Dual symbol mode enables. ASIC inserts x8000 between complete data sets to indicate wake-to-sleep transitions, and x8001 to indicate sleep-to-wake transitions. Symbols are only inserted when wake/sleep state changes. ASIC replaces x8000 and x8001 gyroscope, accelerometer, and die temperature output data codes with x8002.
1	1	Dual symbol mode for every frame. ASIC inserts x8000 or x8001 symbols between every complete data set (frame) according to the current wake/sleep state.

***BUF_M1, BUF_M0** selects the operating mode of the sample buffer.*

BUF_M1	BUF_M0	Mode	Description
0	0	FIFO	The buffer collects 1024 bytes of data until full, collecting new data only when the buffer is not full.
0	1	Stream	The buffer holds the last 1024 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data.
1	0	Trigger	When a trigger event occurs (logic high input on TRIG pin), the buffer holds the last data set of SMP[6:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.
1	1	FILO	The buffer holds the last 1024 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first.

BUF_STATUS

This register reports the status of the sample buffer trigger function.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BUF_TRIG	0	0	0	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address: 0x7Dh		

***BUF_TRIG** reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.*

BUF_CLEAR

Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address: 0x7Eh		

BUF_READ

Data from the buffer should be read using a single SAD+R command. The auto-increment feature of the buffer will continue to increment the read pointer to the next data in the buffer until the specified number of bytes is read. Output data is in 2's Complement format.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^{2}C Address: 0x7Fh		

Sample Buffer Feature Description

The 1024 byte sample buffer feature of the KXG03 accumulates and outputs data based on how it is configured. There are 4 buffer modes available. Data is collected at the ODR specified by the corresponding Wake and Sleep mode registers. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or reading greater than SMPX.

BUF_RES=0:

$$SMPX = SMP\_LEV[9:0] - SMP\_TH[9:0]$$

Equation 5: Samples above Sample Threshold

Stream Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 5).

Trigger Mode

<u>Data Accumulation</u>

When a logic high signal occurs on the TRIG pin, the trigger event is asserted and TRIG[9:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

<u>Data Reporting</u>

Data is reported with the <u>oldest</u> sample first (uses FIFO read pointer).

<u>Status Indicators</u>

When a physical interrupt occurs and there are at least TRIG[9:0] samples in the buffer, BUF_TRIG in BUF_STATUS is asserted.

FILO Mode

<u>Data Accumulation</u>

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

<u>Data Reporting</u>

Data is reported with the <u>newest</u> byte of the <u>newest</u> sample first (Z_H or Z based on resolution).

<u>Status Indicators</u>

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 5).

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Figure 8 represents a high-resolution 3-axis sample within the buffer. Figure 9 through Figure 17 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Regardless of the selected mode, the buffer fills sequentially, one byte at a time. Figure 8 shows one 6-byte data sample. Note the location of the FILO read pointer versus that of the FIFO read pointer.

	Index	Byte	
	0	X_L	←-- FIFO read pointer
	1	X_H	
	2	Y_L	
	3	Y_H	
	4	Z_L	
	5	Z_H	←-- FILO read pointer
buffer write pointer --→	6		

Figure 8: One Buffer Sample

Regardless of the selected mode, the buffer fills sequentially, one sample at a time. Note in Figure 9 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

	Index	Sample	
	0	Data0	⟵ FIFO read pointer
	1	Data1	
	2	Data2	⟵ FILO read pointer
buffer write pointer ⟶	3		
	4		
	5		
	6		
	7		⟵ Sample Threshold
	8		
	9		

Figure 9: Buffer Filling

The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 10 the location of the FILO read pointer versus that of the FIFO read pointer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	← FILO read pointer
buffer write pointer →	7		← Sample Threshold
	8		
	9		

Figure 10: Buffer Approaching Sample Threshold

In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold/FILO read pointer
buffer write pointer →	8		
	9		

Figure 11: Buffer at Sample Threshold

In trigger mode, data is accumulated in the buffer sequentially until the Trigger Threshold is reached. Once the Trigger Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 12 how Data0 was thrown out to make room for Data8.

	Index	Sample	
	0	Data1	⟵ Trigger read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
Trigger write pointer ⟶	7	Data8	⟵ Trigger Threshold
	8		
	9		

Figure 12: Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 13. This results in the buffer holding TRIG_TH[9:0] samples prior to the trigger event, and TRIGX samples after the trigger event.

Index	Sample	
0	Data1	⟵ Trigger read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	⟵ Trigger Threshold
8	Data9	
9	Data10	

Figure 13: Additional Data after Trigger Event

In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	← FILO read pointer

Figure 14: Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 15 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	← FILO read pointer

Figure 15: Buffer Full – Additional Sample Accumulation in Stream or FILO Mode

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 16.

	Index	Sample	
	0	Data1	⟵ FIFO read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
	7	Data8	⟵ Sample Threshold
	8	Data9	⟵ FILO read pointer
buffer write pointer ⟶	9		

Figure 16: FIFO Read from Full Buffer

In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 17.

	Index	Sample	
	0	Data0	⟵ FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	⟵ Sample Threshold
	8	Data8	⟵ FILO read pointer
buffer write pointer ⟶	9		

Figure 17: FILO Read from Full Buffer

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Revision History

REVISION	DESCRIPTION	DATE
0.1	Initial preliminary release	26 Mar 2015
0.4	Updated user register information	22 Apr 2015
0.5	3-wire SPI support removed, added power mode details, minor updates	06 Jun 2015
0.6	Updated POR section including plot, I2C Timing Diagram, minor typos + formatting (Figure captions, headings)	01 Jul 2015
0.7	Changed INS to INT for both interrupts source registers	20 Jul 2015
0.8	Changed BUF_CTRL in the register description section to BUF_CTL to align with ASIC spec (and Register Map).	25 Aug 2015
0.9	Fixed bit names for I_CTL (0 vs. 1 and W vs. S)	27 Aug 2015
0.10	Synchronize with SharePoint update	31 Aug 2015
0.11	Updated RoHS and REACH compliance Formatting Updates	31 Aug 2015
0.12	Updated Application Schematic and Pin Descriptions table	01 Sep 2015
0.13	Updated Package Dimensions figure 2	23 Sep 2015
0.14	Fixed Temp_Out register I2C address value Added note that AUX_ERR can be cleared through writing any value to AUX_STATUS register Added note that LPMODE_W =1 (I_ODR_WAKE) and LPMODE_S = 1 (I_ODR_SLEEP) is ignored if I or Gyro ODR ≥ 400Hz. Added Trigger mode in the BUF_WMI_TH description. Revised description that BUFE = 1 (BUF_EN) can be used independent of RES. Added note that setting WUFC = 0xFF disables the wake up engine, and setting BTSC = 0xFF disables the BTS engine Added Product Notice section	10 Oct 2015
0.15	Updated AUX_CNT_POL1/2 bit description. Added Accelerometer Current over ODR. Accelerometer high resolution current changed. Gyro Start up time description updated. 1034 I2C and 1047 SPI versions. Mechanical specs at 2.5V. Added Table 14 Temperature Calculation.	24 Nov 2015
0.16	Revised BUF_READ register description. Revised Reading from 8-bit Register section. Revised 4-Wire Read and Write Registers section.	25 Nov 2015

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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