POWER FACTOR CORRECTION CONTROLLER AP1661

General Description

The AP1661 is an active power factor control IC which is designed mainly for use as pre-converter in electronic ballast, AC-DC adapters and off-line SMPS applications.

The AP1661 includes an internal start-up timer for stand-alone applications, a one-quadrant multiplier to realize near unity power factor and a zero current detector to ensure DCM boundary conduction operation. The totem pole output stage is capable of driving power MOSFET with 600mA source current and 800mA sink current.

Designed with advanced BiCMOS process, the AP1661 features low start-up current, low operation current and low power dissipation. The AP1661 also has rich protection features including over-voltage protection, input under-voltage lockout with hysteresis and multiplier output clamp to limit maximum peak current.

This IC is available in SOIC-8 and DIP-8 packages.

Features

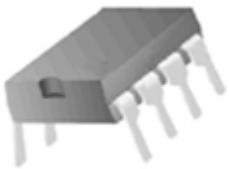
- Zero Current Detection Control for DCM Boundary Conduction Mode
- Adjustable Output Voltage with Precise Over-Voltage Protection
- Low Start-up Current with 50μA Typical Value
- Low Operating Supply Current with 4mA Typical Value
- 1% Precision Internal Reference Voltage
- Internal Start-up Timer
- Disable Function for Reduced Current Consumption
- Totem Pole Output with 600mA Source Current and 800mA Sink Current Capability
- Under-Voltage Lockout with 2.5V of Hysteresis

Applications

- AC-DC Adapter
- Off-line SMPS
- Electronic Ballast



SOIC-8



DIP-8

Figure 1. Package Types of AP1661

Pin Configuration

M Package/P Package
(SOIC-8/DIP-8)

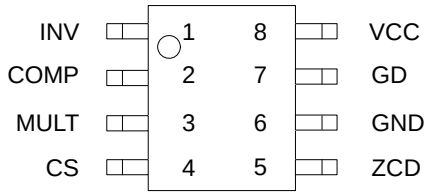


Figure 2. Pin Configuration of AP1661 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	INV	Inverting input of the error amplifier
2	COMP	Output of the error amplifier
3	MULT	Input of the multiplier
4	CS	Input of the current control loop comparator
5	ZCD	Zero current detection input. If it is connected to GND, the device is disabled
6	GND	Ground. Current return for gate driver and control circuits of the IC
7	GD	Gate driver output
8	VCC	Supply voltage of gate driver and control circuits of the IC

Functional Block Diagram

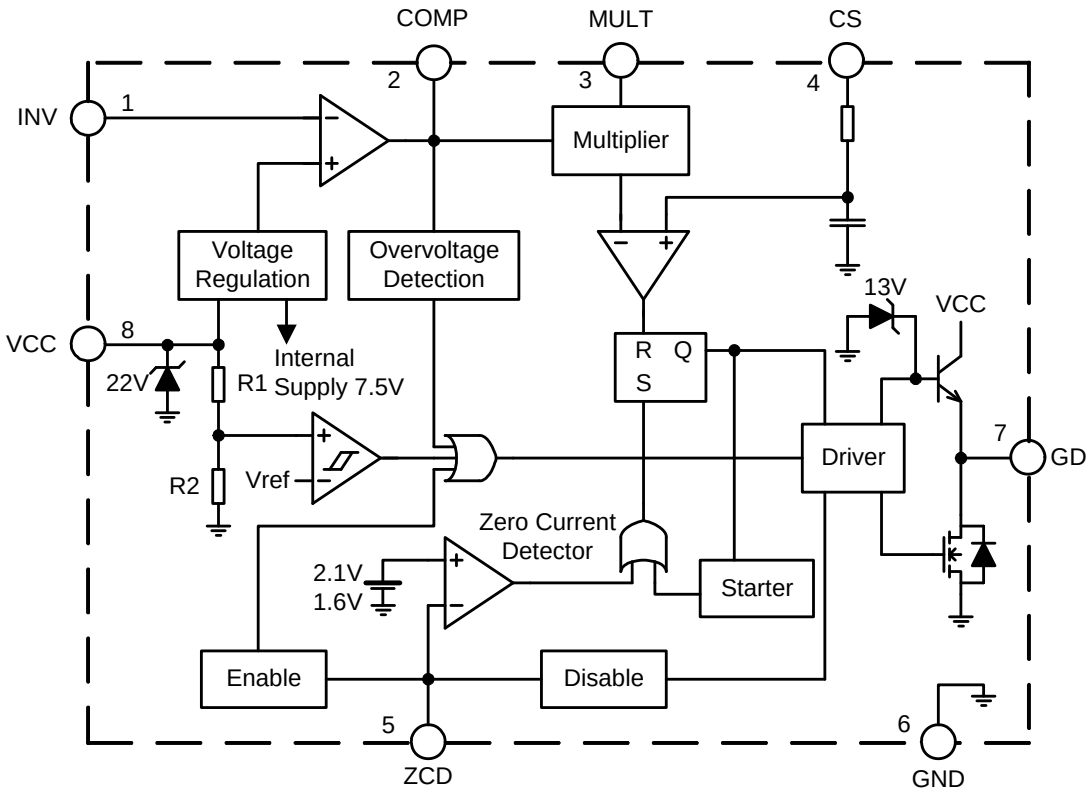
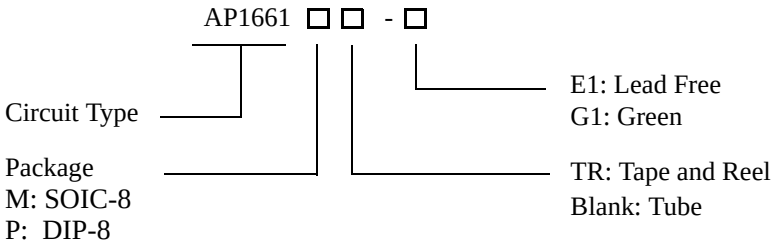


Figure 3. Functional Block Diagram of AP1661

Ordering Information



Package	Temperature Range	Part Number		Marking ID		Packing Type
		Lead Free	Green	Lead Free	Green	
SOIC-8	-40 to 85°C	AP1661M-E1	AP1661M-G1	1661M-E1	1661M-G1	Tube
		AP1661MTR-E1	AP1661MTR-G1	1661M-E1	1661M-G1	Tape & Reel
DIP-8	-40 to 85°C	AP1661P-E1	AP1661P-G1	AP1661P-E1	AP1661P-G1	Tube

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant. Products with "G1" suffix are available in green packages.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value		Unit
Power Supply Voltage	V_{CC}	20		V
Operating Supply Current	I_{CC}	30		mA
Driver Output Current	I_{OUT}	±800		mA
Input/Output of Error Amplifier, Input of Multiplier	V_{INV}, V_{COMP}, V_{MULT}	-0.3 to 7		V
Current Sense Input	V_{CS}	-0.3 to 7		V
Zero Current Detector Input	I_{ZCD}	Source	-50	mA
		Sink	10	
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	DIP-8	100	°C/W
		SOIC-8	150	
Power Dissipation and Thermal Characteristics @ T_A=50°C	P_{TOT}	DIP-8	1	W
		SOIC-8	0.65	
Operating Junction Temperature	T_J	-40 to150		°C
Storage Temperature Range	T_{STG}	-65 to 150		°C
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260		°C
ESD (Human Body Model)		3000		V
ESD (Machine Model)		300		V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Electrical Characteristics

V_{CC}=14.5V, T_A=-25°C to 125°C, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Lockout Section							
Turn-on Threshold		V_{CC-ON}	V_{CC} rising	11	12	13	V
Turn-off Threshold		V_{CC-OFF}	V_{CC} falling	8.7	9.5	10.3	V
Hysterisis		V_{CC-HYS}		2.2	2.5	2.8	V
V_{CC} Operating Range		V_{CC}	After turn-on	10.3		20	V
Total Supply Section							
Start-up Current		$I_{START-UP}$	V_{CC}=11V before turn-on	20	50	90	μA
Operating Supply Current		I_{CC}	C_L=1nF @frequency=70KHz		4	5.5	mA
			In OVP condition Vpin1=2.7V		1.4	2.1	
Quiescent Current		I_Q			2.6	4	mA
Quiescent Current		I_Q	Vpin5≤150mV, V_{CC}>V_{CC-OFF}		1.4	2.1	mA
			Vpin5≤150mV, V_{CC}<V_{CC-OFF}	20	50	90	μA
V_{CC} Zener Voltage		V_Z	I_{CC}=20mA	20	22	24	V
Error Amplifier Section							
Voltage Feedback Input Threshold		V_{INV}	T_A=25 °C	2.465	2.5	2.535	V
			10.3V<V_{CC}<20V	2.44		2.56	
Line Regulation			V_{CC}=10.3V to 20V		2	5	mV
Input Bias Current		I_{INV}	V_{INV}=0V		-0.1	-1	μA
Voltage Gain		G_V	Open Loop	60	80		dB
Gain Bandwidth		GB			1		MHz
Output Voltage	Upper Clamp Voltage	V_{COMP-H}	I_{SOURCE}=0.5mA		5.8		V
	Lower Clamp Voltage	V_{COMP-L}	I_{SINK}=0.5mA		2.25		
Output Current	Source Current	I_{COMP-H}	V_{COMP}=4V, V_{INV}=2.4V	-2	-4	-8	mA
	Sink Current	I_{COMP-L}	V_{COMP}=4V, V_{INV}=2.6V	2.5	4.5		
Enable Threshold		V_{INV-TH}				720	mV
Multiplier Section							
Linear Input Voltage Range		V_{MULT}		0 to 3	0 to 3.5		V
Output Maximum Slope		$\Delta V_{CS}/\Delta V_{MULT}$	V_{MULT}: 0 to 0.5V, V_{COMP}=Upper Clamp Voltage		1.7		
Gain		k	V_{MULT}=1V, V_{COMP}=4V	0.45	0.6	0.75	1/V

Electrical Characteristics (Continued)

V_{CC}=14.5V, T_A=-25°C to 125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sense Section						
Input Bias Current	I_{CS}	V_{CS} =0V		-0.05	-1.0	μA
Current Sense Offset Voltage	$V_{CS-OFFSET}$	V_{MULT}=0V		30		mV
		V_{MULT}=2.5V		5		
Current Sense Reference Clamp	$V_{CS-CLAMP}$	V_{COMP}=Upper Clamp Voltage, V_{MULT}=2.5V	1.6	1.7	1.8	V
Delay to Output	$t_{d(H-L)}$			200	450	ns
Zero Current Detection Section						
Input Threshold Voltage, V_{ZCD} Rising Edge	V_{ZCD-R}	(Note 2)		2.1		V
Hysteresis Voltage	$V_{ZCD-RTH}$	(Note 2)	0.3	0.5	0.7	V
Upper Clamp Voltage	V_{ZCD-H}	I_{ZCD}=20μA	4.5	5.1	5.9	V
		I_{ZCD}=3mA	4.7	5.2	6.1	
Lower Clamp Voltage	V_{ZCD-L}	I_{ZCD}=-3mA	0.3	0.65	1	V
Source Current Capability	I_{ZCD-SR}		-3		-10	mA
Sink Current Capability	I_{ZCD-SN}		3		10	mA
Sink Bias Current	I_{ZCD-B}	1V≤V_{ZCD}≤4.5 V		2		μA
Disable Threshold	$V_{ZCD-DIS}$		150	200	250	mV
Disable Hysterisis	$V_{ZCD-HYS}$			100		mV
Restart Current After Disable	$I_{ZCD-RES}$	V_{ZCD}<V_{DIS}; V_{CC}>V_{CC-OFF}	-100	-200	-300	μA
Drive Output Section						
Dropout Voltage	V_{OH}	$I_{GD-SOURCE}$=200 mA, V_{CC}=12V		2.5	3	V
		$I_{GD-SOURCE}$=20 mA, V_{CC}=12V		2	2.6	
	V_{OL}	$I_{GD-SINK}$=200 mA, V_{CC}=12V		0.9	1.9	V
Output Voltage Rise Time	t_R	C_L=1nF		40	100	ns
Output Voltage Fall Time	t_F	C_L=1nF		40	100	ns
Output Clamp Voltage	$V_{O-CLAMP}$	$I_{GD-SOURCE}$=5 mA, V_{CC}=20V	10	13	15	V
UVLO Saturation	V_{OS}	V_{CC}=0 to V_{CC-ON}, I_{SINK}=10mA			1.1	V
Output Over Voltage Section						
OVP Triggering Current	I_{OVP}		35	40	45	μA
Static OVP Threshold	V_{OVP_TH}		2.1	2.25	2.4	V
Restart Timer						
Restart Timer	t_{START}		70	150	400	μs

Note 2: Limits over the full temperature are guaranteed by design, but not tested in production.

Typical Performance Characteristics

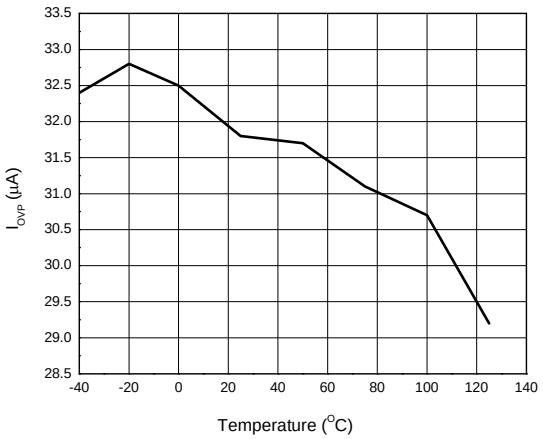


Figure 4. OVP Current Threshold vs. Temperature

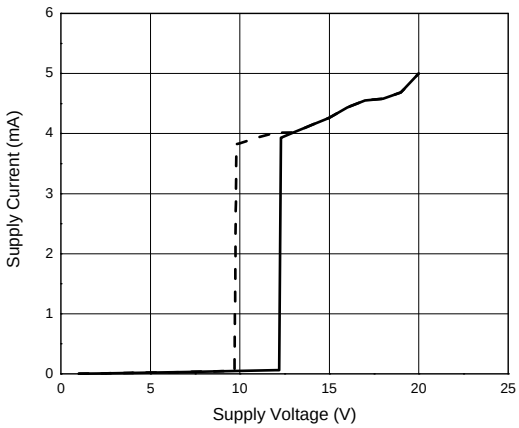


Figure 5. Supply Current vs. Supply Voltage

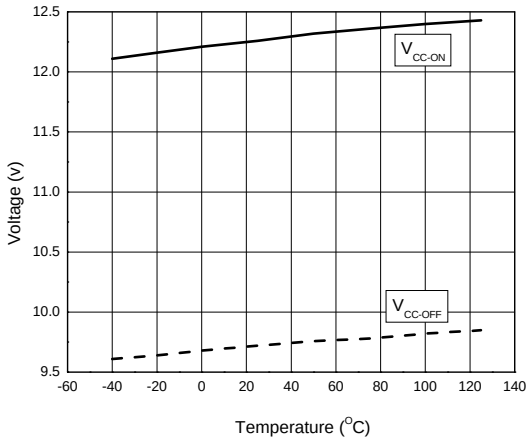


Figure 6. Under Voltage Lockout Threshold vs. Temperature

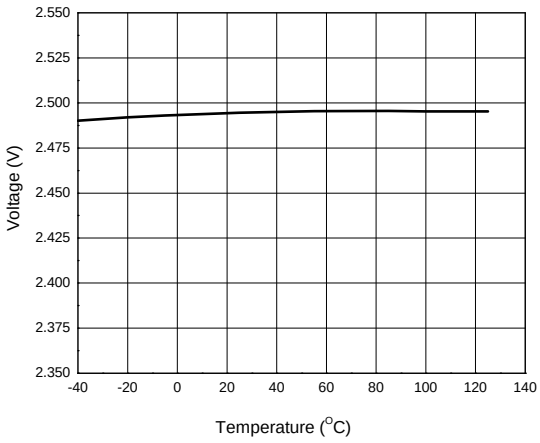


Figure 7. Voltage Feedback Input Threshold vs. Temperature

Typical Performance Characteristics (Continued)

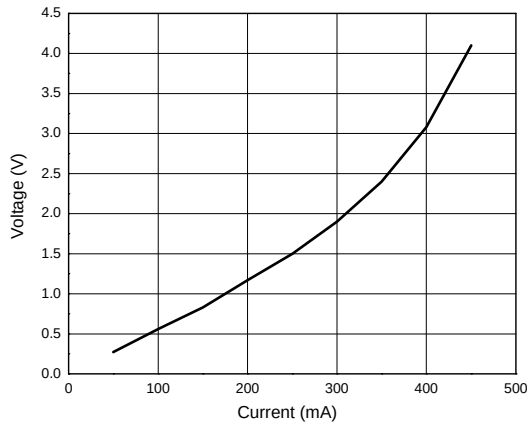


Figure 8. Output Saturation Voltage vs. Sink Current

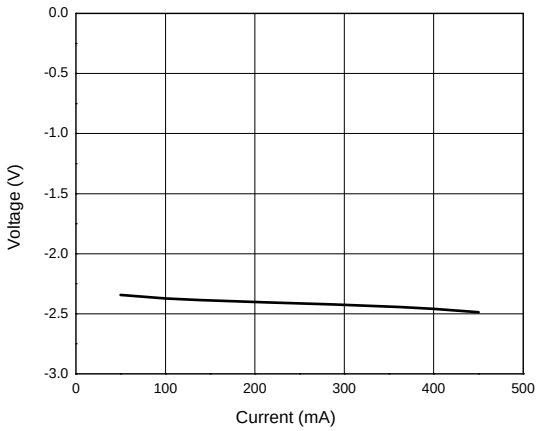


Figure 9. Output Saturation Voltage vs. Source Current

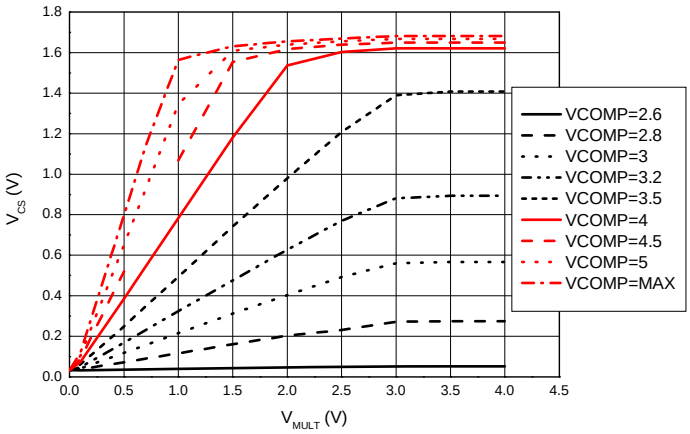


Figure 10. Multiplier Characteristics Family

Functional Block Description

AP1661 is a high performance power factor correction controller which operates in DCM boundary conduction mode. The PFC converter's switch will be turned on when the inductor current reduces to zero and turned off when the sensed inductor current reaches the required reference which is decided by the output of multiplier.

Error Amplifier and Over-Voltage Protection

The error amplifier regulates the PFC output voltage. The internal reference on the non-inverting input of the error amplifier is 2.5V. The error amplifier's inverting input (INV) is connected to an external resistor divider which senses the output voltage. The output of error amplifier is one of the two inputs of multiplier. A compensation loop is connected outside between INV and the error amplifier output. Normally, the compensation loop bandwidth is set very low to realize high power factor for PFC converter.

To make the over voltage protection fast, the internal OVP function is added. If the output over voltage happens, excess current will flow into the output pin of the error amplifier through the feedback compensation capacitor. (see Figure 11) The AP1661 monitors the current flowing into the error amplifier output pin. When the detected current is higher than 40μA, the dynamic OVP is trigged. The IC will be disabled and the drive signal is stopped. If the output over voltage lasts so long that the output of error amplifier goes below 2.25V, static OVP will take place. Also the IC will be disabled until the output of error amplifier goes back to its linear region. R1 and R2 (see Fig. 11) will be selected as below:

$$\frac{R1}{R2} = \frac{Vo}{2.5V} - 1$$

$$R1 = \frac{\Delta V_{OVP}}{40\mu A}$$

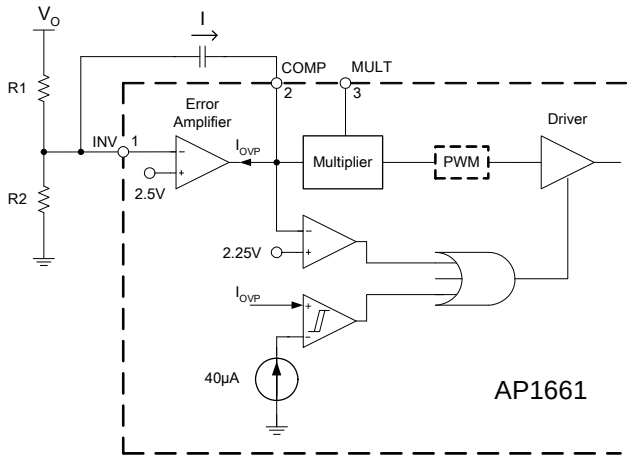


Figure 11. Error Amplifier and OVP Block

Multiplier

The multiplier has two inputs. One (Pin 3) is the divided AC sinusoidal voltage which makes the current sense comparator threshold voltage vary from zero to peak value. The other input is the output of error amplifier (Pin 2). In this way, the input average current wave will be sinusoidal as well as reflects the load status. Accordingly a high power factor and good THD are achieved. The multiplier transfer character is designed to be linear over a wide dynamic range, namely, 0 V to 3V for Pin 3 and 2.0 V to 5.8 V for Pin 2. The relationship between the multiplier output and inputs is described as below equation.

$$V_{CS} = k \times (V_{COMP} - 2.5) \times V_{MULT}$$

where V_{CS} (Multiplier output) is the reference for the current sense, k is the multiplier gain, V_{COMP} is the voltage on pin 2 (error amplifier output) and V_{MULT} is the voltage on pin 3.

Current Sense/Current Sense Comparator

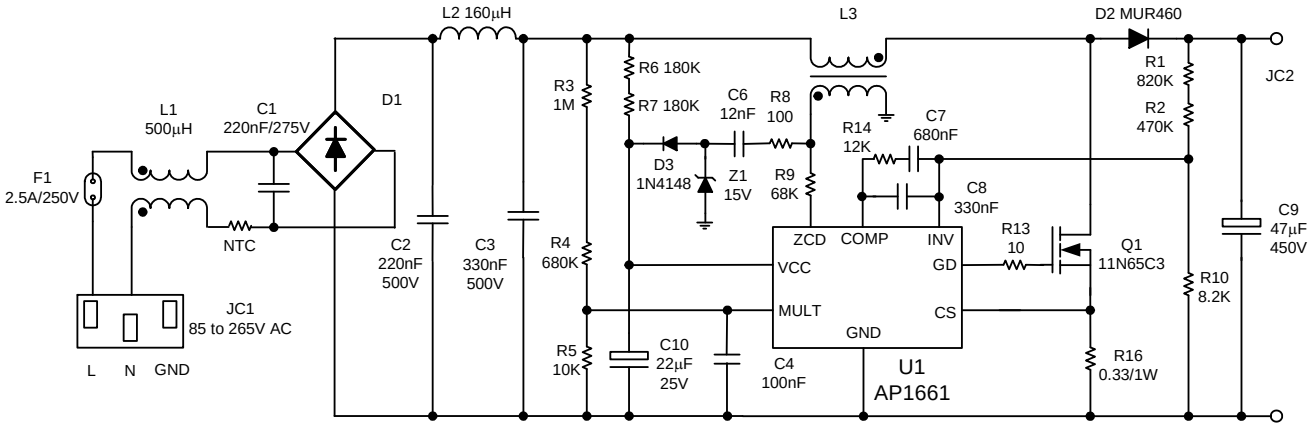
The PFC switch's turn-on current is sensed through an external resistor in series with the switch. When the sensed voltage exceeds the threshold voltage (the multiplier output), the current sense comparator will become low and the external MOSFET will be turned off. This insures a cycle-by-cycle current mode control operation. The maximum current sense reference is 1.8V. The max value usually happens at startup process or abnormal conditions such as short load.

Functional Block Description (Continued)

Zero Current Detection

AP1661 is a DCM boundary conduction current mode PFC controller. Usually, the zero current detection (ZCD) voltage signal comes from the auxiliary winding of the boost inductor. When the ZCD pin voltage decreases below 1.6V, the gate drive signal becomes high to turn on the external MOSFET. 500mV of hysteresis is provided to avoid false triggering. The ZCD pin can be used for disabling the IC. Making its voltage below 0.15V or short to the ground will disable the device thus reduce the IC supply current consumption.

Typical Application

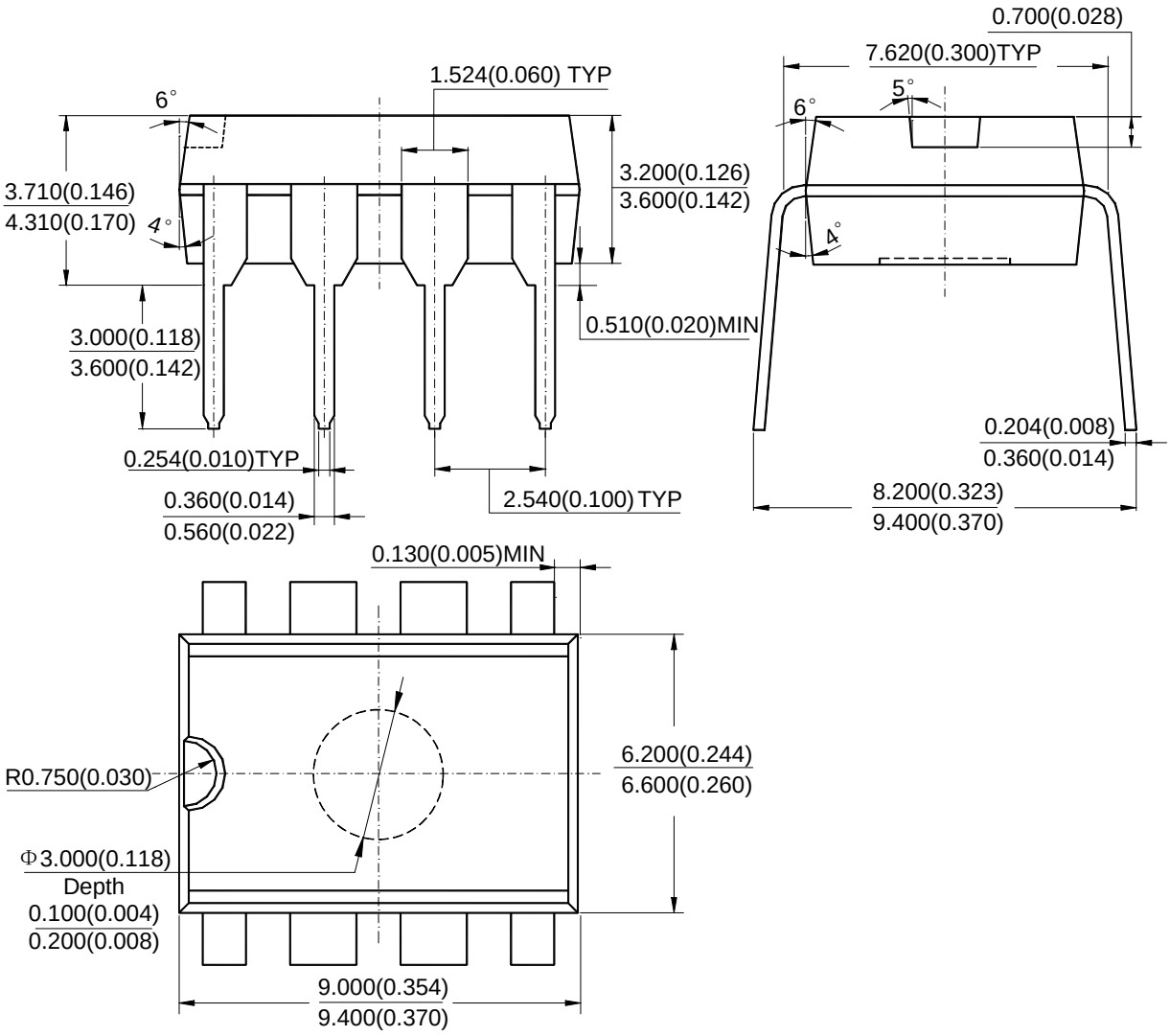


L3:
Core type RM10, material 3C90
primary: 660uH, 66 turns of litze wire 0.1mm*30
secondary: 7 turns wire of 0.2mm

Figure 12. 85 to 265V Wide Range Input 90W PFC Demo Board Electrical Schematic Circuit

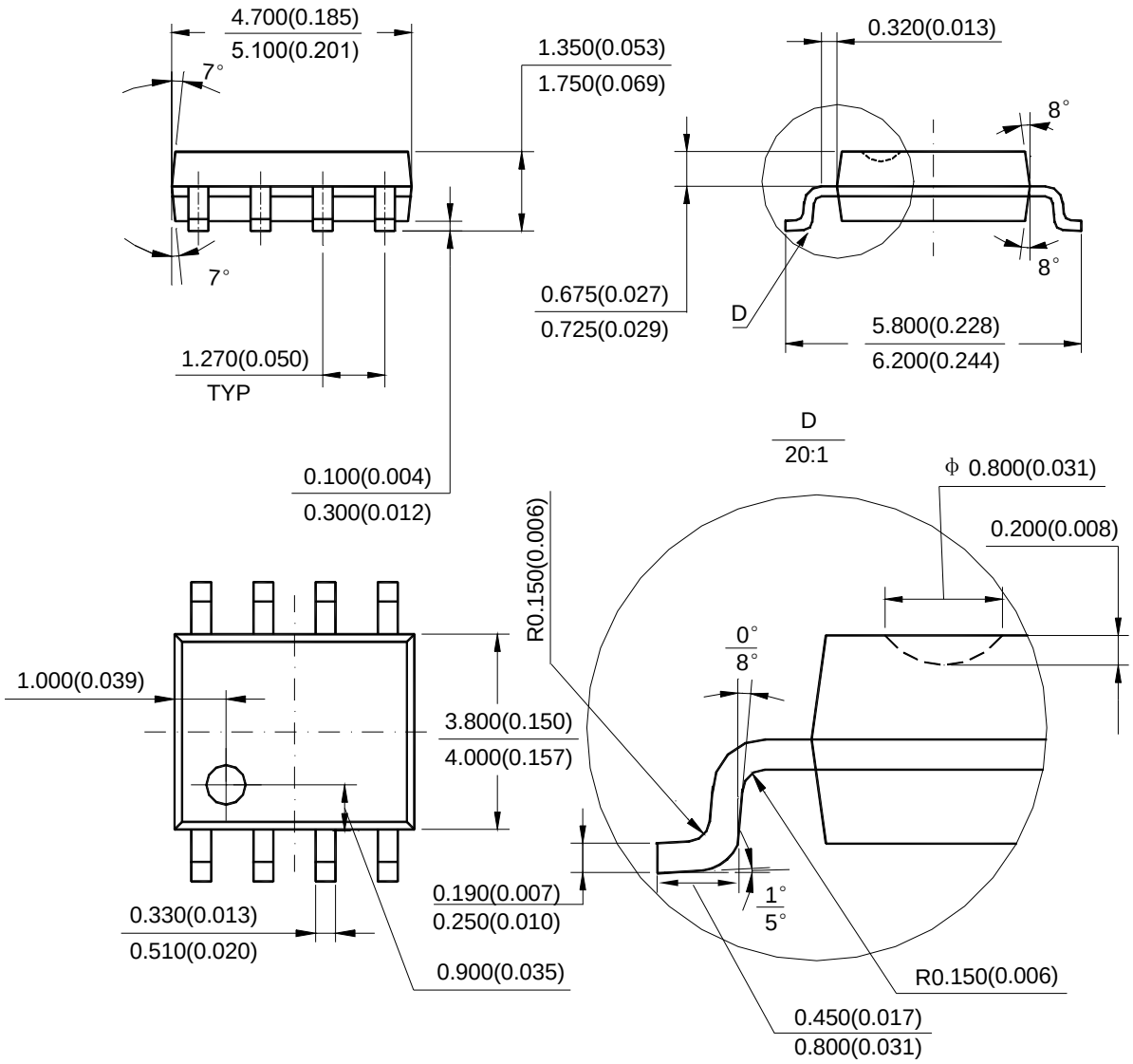
Mechanical Dimensions

DIP-8 **Unit: mm(inch)**



Mechanical Dimensions (Continued)

SOIC-8 **Unit: mm(inch)**





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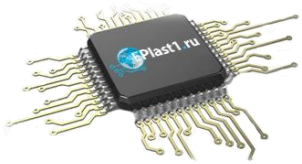
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