STDP4028
DisplayPort transmitter

Datasheet

Rev A

MegaChips

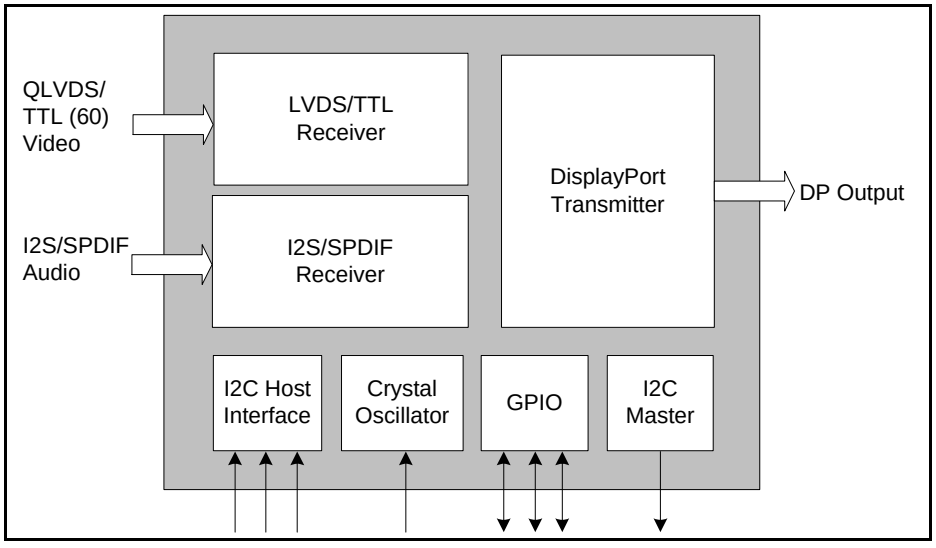
MegaChips' Proprietary Information

Features

- Enhanced DisplayPort® (DP) transmitter
  - DP 1.1a compliant
  - Embedded DisplayPort (eDP) compliant
  - 1, 2, or 4 lanes
- Higher bandwidth “Turbo mode” (3.24 Gbps) per lane, supports:
  - 1920 x 1080 (FHD) 120 Hz/10-bit color video standard timings and 7.1 Ch audio
  - 2560 x 1600 (WQXGA), 2560 x 2048 (QSXGA) 60 Hz/10-bit color graphics and 7.1 Ch audio
- Interface compatibility with wide range of display controller ICs
  - LVTTL (60 wide) and LVDS (quad bus) video interface
  - 8-Ch I2S and SPDIF audio interface
- Robust AUX channel
  - Link service, maintenance
  - I2C-over-AUX (MCCS, DDC)
  - IR, full duplex UART protocol
- Configurable through I2C host interface
- Supports HDCP 1.3 with on-chip keys
- HDCP repeater capability
  - Acts as downstream transmitter
- Spread spectrum on DisplayPort, LVDS, and TTL interfaces for EMI reduction
- Supports deep color and color format conversion
  - RGB/YUV (4:4:4) – 10-bit color
  - YUV (4:2:2/4:2:0) – 12-bit color
  - RGB (4:4:4) to YUV (4:4:4) conversion and vice-versa
- Low power operation; 18 mW standby
- I2C to AUX bridge for EDID, MCCS pass through
- Supports HBR/“Turbo” speed over HBR/RBR-rated long cables (15 m and more)
- Package
  - 164 LFBGA (12 x 12 mm / 0.8 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Digital TV, docking station, STB, game console, etc.



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1. Description

The STDP4028 is a DisplayPort transmitter IC for the secure transmission of high-bandwidth, uncompressed digital audio-video signals targeted for applications such as DTV, LCD monitor, docking station, STB and other types of consumer audio-video systems. STDP4028 is VESA DP 1.1a and eDP compliant device, implementing a single link DisplayPort output port comprising four main lanes, auxiliary channel, and HPD. In addition to the standard HBR (2.7 Gbps) and RBR (1.62 Gbps) speeds, this device supports “turbo” speed of 3.24 Gbps per lane with a total link bandwidth of 12.96 Gbps. The higher bandwidth provides unique benefits to users over other commercial DP transmitters for embedded applications by offering additional margin to support higher color depth, resolution, and refresh rate. For example, STDP4028 supports FHD non-reduced blanking video (1080p 30-bit color per pixel) at 120 Hz, plus 7.1 Ch audio in two-box TV applications. The high-speed auxiliary channel in STDP4028 acts as a bidirectional communication link, supporting application-specific protocols such as MCCS, DDC, UART, IR, as well as, the dedicated DisplayPort link training and device management functions. The STDP4028 supports RGB and YUV video color formats with color depth of 12 (YUV 4:2:2 only), 10, and 8 bits.

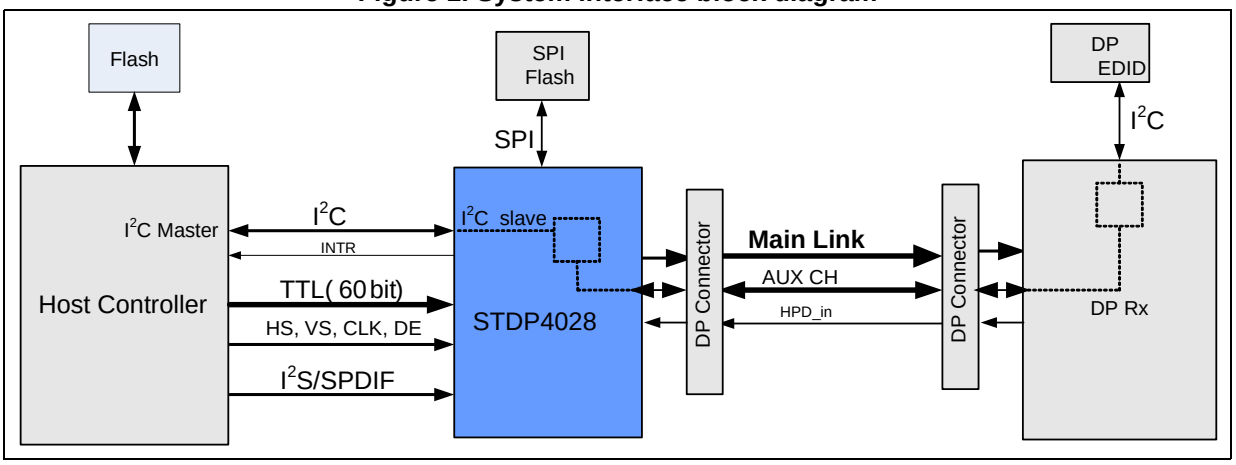
This device offers LVDS and LVTTL input interface configurable to map a wide range of display controller products. The Quad LVDS interface supports video signals up to 400 MHz pixel rate with flexible channel and lane swapping options. The 60-bit LVTTL input ports on STDP4028 can be mapped to transfer video data either in two pixels per clock or single pixel per clock of a chosen color depth. The STDP4028 also supports both compressed and uncompressed audio formats.

This device comprises four I2S audio inputs, supporting up to 8 channels LPCM audio and a single wire SPDIF input for encoded audio. The STDP4028 features HDCP 1.3 content protection scheme with an embedded key option for secure transmission of digital audio-video content. In addition, it supports the HDCP repeater function and, thus acts as a downstream transmitter suitable for two-box TV and HDMI/DVI to DP converter applications.The STDP4028 is configurable from an external host through the I2C host interface. This IC also includes general-purpose inputs/outputs for controlling system components. The STDP4028 features a color space converter (RGB to YUV and YUV to RGB) for flexible interface with external video processing devices.

2. Application overview

The STDP4028 is designed as DisplayPort transmitter device for transferring high bandwidth video and audio in PC and CE applications. Typical audio-video source system has a graphics or video processing device that acts as system master (host). The host controller configures STDP4028 through an I2C host interface. The host and STDP4028 also use interrupt mechanism whenever the slave needs attention. The STDP4028 may require an external SPI Flash to store firmware for supporting custom specific applications. The audio and video signal from the host controller is converted in to DisplayPort streams through STDP4028 and transfer to an external display system over standard DisplayPort cable. The I2C to AUX bypass channel handles the I2C traffic between STDP4028 and host controller as shown in the figure below.

Figure 1. System interface block diagram



3. Feature attributes

- Video
  - Up to 2560 x 2048-60 Hz, 2560 x 1600-60 Hz, FHD 120 Hz at 10-bits per color
  - 8/10/12 bits per color option
  - RGB/YUV color format
- Audio
  - 8-Ch I2S; word length up to 64 x Fs; bit depth up to 24 bits, sample rate up to 192 kHz
  - SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz
- Input interface
  - Video: TTL 60/48 bits wide; QLVDS 8/10 bits per color
  - Audio: I2S 8-Ch, SPDIF x1
- Output interface
  - DP 1.1a (4 lanes, AUX, HPD); supported link speed 3.24 Gbps, 2.7 Gbps, 1.62 Gbps
- Spread spectrum
  - Supported on DP output and LVDS/TTL inputs
- AUX capabilities
  - UART, I2C-over-AUX (MCCS, DDC, etc.) IR
- HDCP
  - On-chip keys, HDCP repeater
- Color format conversion
  - RGB 4:4:4 to YUV 4:4:4 and vice-versa
- System configuration
  - I2C host interface for control by an external system microprocessor
- Package
  - 164 LFBGA (12 x 12 mm), 1 mm thickness, 0.8 pitch
- Power
  - Standby power 18 mW
- ESD
  - 2 KV HBM, 200 V MM, 750 V CDM

4. BGA footprint and pin lists

4.1 Ball grid array diagram

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

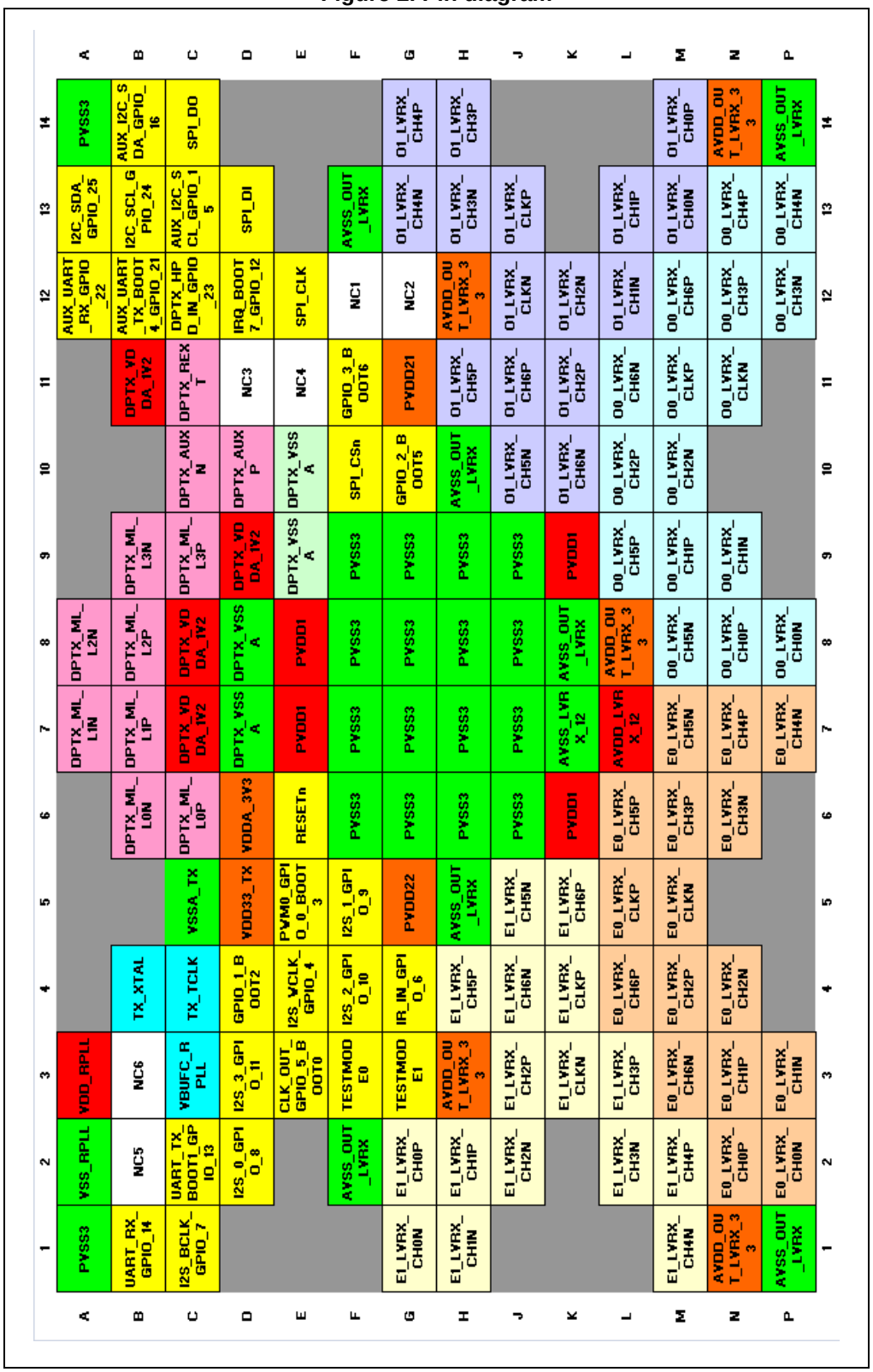
Some signal names in BGA diagrams have been abbreviated. Refer to*Table 2: Pin list on page 11* for full signal names sorted by pin number.

Table 1. Key to BGA diagrams

Function	Type	Key
DisplayPort input	SIG	
Reference clocks	SIG	
System controls	SIG	
Multi-function and system interface connections	SIG	
I2S/SPDIF audio output	SIG	
LVDS/TTL Output_Even-0	SIG	
LVDS/TTL Output_Even-1	SIG	
LVDS/TTL Output_Odd-0	SIG	
LVDS/TTL Output_Odd-1	SIG	
Analog power	VCC/VDD	
Analog ground	VSS/GND	
System power	VCC/VDD	
System ground	VSS/GND	
No connect/Do not connect	NC/DNC	
No ball		

The STDP4028 is available in a 164-pin LFBGA package.

Figure 2. Pin diagram



4.2 Full pin list sorted by pin number

Table 2. Pin list

Pin number	Net name
A1	PVSS3
A2	VSS_RPLL
A3	VDD_RPLL
A7	DPTX_ML_L1N
A8	DPTX_ML_L2N
A12	AUX_UART_RX_GPIO_22
A13	I2C_SDA_GPIO_25
A14	PVSS3
B1	UART_RX_GPIO_14
B2	NC
B3	NC
B4	TX_XTAL
B6	DPTX_ML_L0N
B7	DPTX_ML_L1P
B8	DPTX_ML_L2P
B9	DPTX_ML_L3N
B11	DPTX_VDDA_1V2
B12	AUX_UART_TX_BOOT4_GPIO_21
B13	I2C_SCL_GPIO_24
B14	AUX_I2C_SDA_GPIO_16
C1	I2S_BCLK_GPIO_7
C2	UART_TX_BOOT1_GPIO_13
C3	VBUFC_RPLL
C4	TX_TCLK
C5	VSSA_TX
C6	DPTX_ML_L0P
C7, C8	DPTX_VDDA_1V2
C9	DPTX_ML_L3P
C10	DPTX_AUXN
C11	DPTX_REXT
C12	DPTX_HDP_IN_GPIO_23
C13	AUX_I2C_SCL_GPIO_15
C14	SPI_DO

Table 2. Pin list (continued)

Pin number	Net name
D2	I2S_0_GPIO_8
D3	I2S_3_GPIO_11
D4	GPIO_1_BOOT2
D5	VDD33_TX
D6	VDDA_3V3
D7, D8	DPTX_VSSA
D9	DPTX_VDDA_1V2
D10	DPTX_AUXP
D11	NC
D12	IRQ_BOOT7_GPIO_12
D13	SPI_DI
E3	CLK_OUT_GPIO_5_BOOT0
E4	I2S_WCLK_GPIO_4
E5	PWM0_GPIO_0_BOOT3
E6	RESETn
E7, E8	PVDD1
E9, E10	DPTX_VSSA
E11	NC
E12	SPI_CLK
F2	AVSS_OUT_LVRX
F3	TESTMODE0
F4	I2S_2_GPIO_10
F5	I2S_1_GPIO_9
F6, F7, F8, F9	PVSS3
F10	SPI_CSn
F11	GPIO_3_BOOT6
F12	NC
F13	AVSS_OUT_LVRX
G1	E1_LVRX_CH0N
G2	E1_LVRX_CH0P
G3	TESTMODE1
G4	IR_IN_GPIO_6
G5	PVDD22
G6, G7, G8, G9	PVSS3
G10	GPIO_2_BOOT5

Table 2. Pin list (continued)

Pin number	Net name
G11	PVDD21
G12	NC
G13	O1_LVRX_CH4N
G14	O1_LVRX_CH4P
H1	E1_LVRX_CH1N
H2	E1_LVRX_CH1P
H3	AVDD_OUT_LVRX_33
H4	E1_LVRX_CH5P
H5	AVSS_OUT_LVRX
H6, H7, H8, H9	PVSS3
H10	AVSS_OUT_LVRX
H11	O1_LVRX_CH5P
H12	AVDD_OUT_LVRX_33
H13	O1_LVRX_CH3N
H14	O1_LVRX_CH3P
J2	E1_LVRX_CH2N
J3	E1_LVRX_CH2P
J4	E1_LVRX_CH6N
J5	E1_LVRX_CH5N
J6, J7, J8, J9	PVSS3
J10	O1_LVRX_CH5N
J11	O1_LVRX_CH6P
J12	O1_LVRX_CLKN
J13	O1_LVRX_CLKP
K3	E1_LVRX_CLKN
K4	E1_LVRX_CLKP
K5	E1_LVRX_CH6P
K6	PVDD1
K7	AVSS_LVRX
K8	AVSS_OUT_LVRX
K9	PVDD1
K10	O1_LVRX_CH6N
K11	O1_LVRX_CH2P
K12	O1_LVRX_CH2N
L2	E1_LVRX_CH3N

Table 2. Pin list (continued)

Pin number	Net name
L3	E1_LVRX_CH3P
L4	E0_LVRX_CH6P
L5	E0_LVRX_CLKP
L6	E0_LVRX_CH5P
L7	AVDD_LVRX_12
L8	AVDD_OUT_LVRX_33
L9	O0_LVRX_CH5P
L10	O0_LVRX_CH2P
L11	O0_LVRX_CH6N
L12	O1_LVRX_CH1N
L13	O1_LVRX_CH1P
M1	E1_LVRX_CH4N
M2	E1_LVRX_CH4P
M3	E0_LVRX_CH6N
M4	E0_LVRX_CH2P
M5	E0_LVRX_CLKN
M6	E0_LVRX_CH3P
M7	E0_LVRX_CH5N
M8	O0_LVRX_CH5N
M9	O0_LVRX_CH1P
M10	O0_LVRX_CH2N
M11	O0_LVRX_CLKP
M12	O0_LVRX_CH6P
M13	O1_LVRX_CH0N
M14	O1_LVRX_CH0P
N1	AVDD_OUT_LVRX_33
N2	E0_LVRX_CH0P
N3	E0_LVRX_CH1P
N4	E0_LVRX_CH2N
N6	E0_LVRX_CH3N
N7	E0_LVRX_CH4P
N8	O0_LVRX_CH0P
N9	O0_LVRX_CH1N
N11	O0_LVRX_CLKN
N12	O0_LVRX_CH3P

Table 2. Pin list (continued)

Pin number	Net name
N13	O0_LVRX_CH4P
N14	AVDD_OUT_LVRX_33
P1	AVSS_OUT_LVRX
P2	E0_LVRX_CH0N
P3	E0_LVRX_CH1N
P7	E0_LVRX_CH4N
P8	O0_LVRX_CH0N
P12	O0_LVRX_CH3N
P13	O0_LVRX_CH4N
P14	AVSS_OUT_LVRX

5. Connections

5.1 Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 3. DisplayPort transmitter outputs

Pin	Assignment	I/O	Description
B6	DPTX_ML_L0N	O	Negative output of DPTX Main Link Lane0
C6	DPTX_ML_L0P	O	Positive output of DPTX Main Link Lane0
A7	DPTX_ML_L1N	O	Negative output of DPTX Main Link Lane1
B7	DPTX_ML_L1P	O	Positive output of DPTX Main Link Lane1
A8	DPTX_ML_L2N	O	Negative output of DPTX Main Link Lane2
B8	DPTX_ML_L2P	O	Positive output of DPTX Main Link Lane2
B9	DPTX_ML_L3N	O	Negative output of DPTX Main Link Lane3
C9	DPTX_ML_L3P	O	Positive output of DPTX Main Link Lane3
C10	DPTX_AUXN	I/O	Negative input/output of DPTX Aux Channel
D10	DPTX_AUXP	I/O	Positive input/output of DPTX Aux Channel
C12	DPTX_HPD_IN/GPIO_23	I/O	DisplayPort Receiver Hot Plug Detect Input General Purpose Schmitt Trigger Input / Tri-state Output 26 [5V Tolerant]
C11	DPTX_REXT	I	Termination calibration reference resistor; 240 ohm 1% resistor should be connected from this pin to 1.2 V analog power supply.

Table 4. Reference clocks

Pin	Assignment	I/O	Description
B4	TX_XTAL	I/O	Crystal Oscillator Input. Connect to external crystal.
C4	TX_TCLK	I/O	Reference Clock (TCLK) from a 27 MHz Crystal or TTL Oscillator. Connect to external crystal or oscillator.
C3	VBUFC_RPLL	O	Analog Test Pin for Internal Clocks. No connect.

Table 5. Digital video inputs

Pin	Assignment	I/O	Description
K4	E1_LVRX_CLKP	I	Positive input of LVDS RX E1 Clock Channel
			TTL Even Red Channel Data 4
K3	E1_LVRX_CLKN	I	Negative input of LVDS RX E1 Clock Channel
			TTL Even Red Channel Data 7
G2	E1_LVRX_CH0P	I	Positive input of LVDS RX E1 Channel 0
			TTL VSYNC
G1	E1_LVRX_CH0N	I	Negative input of LVDS RX E1 Channel 0
			TTL HSYNC
H2	E1_LVRX_CH1P	I	Positive input of LVDS RX E1 Channel 1
			TTL Even Red Channel Data 1
H1	E1_LVRX_CH1N	I	Negative input of LVDS RX E1 Channel 1
			TTL Even Red Channel Data 0
J3	E1_LVRX_CH2P	I	Positive input of LVDS RX E1 Channel 2
			TTL DE
J2	E1_LVRX_CH2N	I	Negative input of LVDS RX E1 Channel 2
			TTL Even Red Channel Data 9
L3	E1_LVRX_CH3P	I	Positive input of LVDS RX E1 Channel 3
			TTL Even Red Channel Data 6
L2	E1_LVRX_CH3N	I	Negative input of LVDS RX E1 Channel 3
			TTL Even Red Channel Data 5
M2	E1_LVRX_CH4P	I	Positive input of LVDS RX E1 Channel 4
			TTL Even Red Channel Data 2
M1	E1_LVRX_CH4N	I	Negative input of LVDS RX E1 Channel 4
			TTL Even Red Channel Data 3
J5	E1_LVRX_CH5N	I	TTL Even Red Channel Data 8
H4	E1_LVRX_CH5P	I	TTL Even Blue Channel Data 0
K5	E1_LVRX_CH6P	I	TTL Odd Red Channel Data 0
J4	E1_LVRX_CH6N	I	TTL Even Blue Channel Data 1
J12	O1_LVRX_CLKN	I	Negative input of LVDS RX O1 Clock Channel
			TTL Odd Blue Channel Data 8
J13	O1_LVRX_CLKP	I	Positive input of LVDS RX O1 Clock Channel
			TTL Odd Blue Channel Data 7

Table 5. Digital video inputs

Pin	Assignment	I/O	Description
M14	O1_LVRX_CH0P	I	Positive input of LVDS RX O1 Channel 0
			TTL Odd Green Channel Data 6
M13	O1_LVRX_CH0N	I	Negative input of LVDS RX O1 Channel 0
			TTL Odd Green Channel Data 5
L13	O1_LVRX_CH1P	I	Positive input of LVDS RX O1 Channel 1
			TTL Odd Green Channel Data 3
L12	O1_LVRX_CH1N	I	Negative input of LVDS RX O1 Channel 1
			TTL Odd Blue Channel Data 0
K11	O1_LVRX_CH2P	I	Positive input of LVDS RX O1 Channel 2
			TTL Odd Green Channel Data 4
K12	O1_LVRX_CH2N	I	Negative input of LVDS RX O1 Channel 2
			TTL Odd Green Channel Data 2
H14	O1_LVRX_CH3P	I	Positive input of LVDS RX O1 Channel 3
			TTL Odd Blue Channel Data 4
H13	O1_LVRX_CH3N	I	Negative input of LVDS RX O1 Channel 3
			TTL Odd Blue Channel Data 5
G14	O1_LVRX_CH4P	I	Positive input of LVDS RX O1 Channel 4
			TTL Odd Blue Channel Data 2
G13	O1_LVRX_CH4N	I	Negative input of LVDS RX O1 Channel 4
			TTL Odd Blue Channel Data 3
J10	O1_LVRX_CH5N	I	TTL Odd Green Channel Data 8
H11	O1_LVRX_CH5P	I	TTL Odd Blue Channel Data 6
K10	O1_LVRX_CH6N	I	TTL Odd Green Channel Data 9
J11	O1_LVRX_CH6P	I	TTL Odd Blue Channel Data 9
M5	E0_LVRX_CLKN	I	Negative input of LVDS RX E0 Clock Channel
			TTL Even Green Channel Data 2
L5	E0_LVRX_CLKP	I	Positive input of LVDS RX E0 Clock Channel
			TTL Even Green Channel Data 3
P2	E0_LVRX_CH0N	I	Negative input of LVDS RX E0 Channel 0
			TTL Even Green Channel Data 0
N2	E0_LVRX_CH0P	I	Positive input of LVDS RX E0 Channel 0
			TTL Even Green Channel Data 1
P3	E0_LVRX_CH1N	I	Negative input of LVDS RX E0 Channel 1
			TTL Even Green Channel Data 6

Table 5. Digital video inputs

Pin	Assignment	I/O	Description
N3	E0_LVRX_CH1P	I	Positive input of LVDS RX E0 Channel 1
			TTL Even Green Channel Data 7
N4	E0_LVRX_CH2N	I	Negative input of LVDS RX E0 Channel 2
			TTL Even Green Channel Data 4
M4	E0_LVRX_CH2P	I	Positive input of LVDS RX E0 Channel 2
			TTL Even Green Channel Data 5
N6	E0_LVRX_CH3N	I	Negative input of LVDS RX E0 Channel 3
			TTL Even Blue Channel Data 7
M6	E0_LVRX_CH3P	I	Positive input of LVDS RX E0 Channel 3
			TTL Even Blue Channel Data 8
P7	E0_LVRX_CH4N	I	Negative input of LVDS RX E0 Channel 4
			TTL Odd Red Channel Data 1
N7	E0_LVRX_CH4P	I	Positive input of LVDS RX E0 Channel 4
			TTL DCLK
M7	E0_LVRX_CH5N	I	TTL Even Blue Channel Data 6
L6	E0_LVRX_CH5P	I	TTL Even Blue Channel Data 9
M3	E0_LVRX_CH6N	I	TTL Even Green Channel Data 9
L4	E0_LVRX_CH6P	I	TTL Even Green Channel Data 8
N11	O0_LVRX_CLKN	I	Negative input of LVDS RX O0 Clock Channel
			TTL Odd Red Channel Data 8
M11	O0_LVRX_CLKP	I	Positive input of LVDS RX O0 Clock Channel
			TTL Odd Red Channel Data 7
P8	O0_LVRX_CH0N	I	Negative input of LVDS RX O0 Channel 0
			TTL Odd Green Channel Data 0
N8	O0_LVRX_CH0P	I	Positive input of LVDS RX O0 Channel 0
			TTL Odd Green Channel Data 1
N9	O0_LVRX_CH1N	I	Negative input of LVDS RX O0 Channel 1
			TTL Even Blue Channel Data 4
M9	O0_LVRX_CH1P	I	Positive input of LVDS RX O0 Channel 1
			TTL Even Blue Channel Data 3
M10	O0_LVRX_CH2N	I	Negative input of LVDS RX O0 Channel 2
			TTL Even Blue Channel Data 2
L10	O0_LVRX_CH2P	I	Positive input of LVDS RX O0 Channel 2
			TTL Odd Red Channel Data 2

Table 5. Digital video inputs

Pin	Assignment	I/O	Description
P12	O0_LVRX_CH3N	I	Negative input of LVDS RX O0 Channel 3
			TTL Odd Red Channel Data 6
N12	O0_LVRX_CH3P	I	Positive input of LVDS RX O0 Channel 3
			TTL Odd Red Channel Data 5
P13	O0_LVRX_CH4N	I	Negative input of LVDS RX O0 Channel 4
			TTL Odd Red Channel Data 4
N13	O0_LVRX_CH4P	I	Positive input of LVDS RX O0 Channel 4
			TTL Odd Blue Channel Data 1
M8	O0_LVRX_CH5N	I	TTL Even Blue Channel Data 5
L9	O0_LVRX_CH5P	I	TTL Odd Red Channel Data 9
L11	O0_LVRX_CH6N	I	TTL Odd Green Channel Data 7
M12	O0_LVRX_CH6P	I	TTL Odd Red Channel Data 3

Table 6. Multi-function - digital audio output, general purpose input/output, bootstrap pins

Pin	Assignment	I/O	Description
E4	I2S_WCLK_GPIO_4	I/O	I2S_WCLK
			GPIO_4
C1	I2S_BCLK_GPIO_7	I/O	I2S_BCLK
			GPIO_7
D2	I2S_0_GPIO_8	I/O	I2S_0
			GPIO_8
F5	I2S_1_GPIO_9	I/O	I2S_1
			GPIO_9
F4	I2S_2_GPIO_10	I/O	I2S_2
			GPIO_10
D3	I2S_3_GPIO_11	I/O	I2S_3
			GPIO_11

Table 7. Multi-function and system interface connections

Pin	Assignment	I/O	Description
E6	RESETn	I/O	Reset (active low) signal. Connect to digital 3.3 V with a 2.7 K ohm pull-up resistor.
F3	TESTMODE0	I	Reserve for testing. Must be connected to system ground (GND)
G3	TESTMODE1	I	
D13	SPI_DI	I/O	SPI ROM Data Input.

Table 7. Multi-function and system interface connections

Pin	Assignment	I/O	Description
C14	SPI_DO	I/O	SPI ROM Data Output.
E12	SPI_CLK	I/O	SPI ROM Clock
F10	SPI_CSn	I/O	SPI ROM Chip Select.
E5	PWM0_GPIO_0_BOOT3	I/O	PWM0
			BOOTSTRAP[3] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 0 [5V Tolerant]
D4	GPIO_1_BOOT2	I/O	General Purpose Schmitt Trigger Input / Tri-state Output 1 [5V Tolerant]
			BOOTSTRAP[2] Please refer to Bootstrap configuration table for description
G10	GPIO_2_BOOT5	I/O	General Purpose Schmitt Trigger Input / Tri-state Output 2 [5V Tolerant]
			BOOTSTRAP[5] Please refer to Bootstrap configuration table for description
F11	GPIO_3_BOOT6	I/O	BOOTSTRAP[6] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 3 [5V Tolerant]
E3	CLK_OUT_GPIO_5_BOOT0	I/O	CLK_OUT
			General Purpose Schmitt Trigger Input / Tri-state Output 5 [5V Tolerant]
			BOOTSTRAP[0] Please refer to Bootstrap configuration table for description
G4	IR_IN_GPIO_6	I/O	Infra-red Receiver Data Input
			General Purpose Schmitt Trigger Input / Tri-state Output 6 [5V Tolerant]
D12	IRQ_BOOT7_GPIO_12	I/O	IRQ
			BOOTSTRAP[7] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 12 [5V Tolerant]
C2	UART_TX_BOOT1_GPIO_13	I/O	UART Transmit Data Output.
			BOOTSTRAP[1] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 13 [5V Tolerant]

Table 7. Multi-function and system interface connections

Pin	Assignment	I/O	Description
B1	UART_RX_GPIO_14	I/O	UART Receive Data Input. Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 14 [5V Tolerant]
C13	AUX_I2C_SCL_GPIO_15	I/O	I²C Serial Clock for DP AUX channel. This pin, along with AUX_I2C_SDA, creates external serial interface for DP AUX channel. Connect to digital 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 15 [5V Tolerant]
B14	AUX_I2C_SDA_GPIO_16	I/O	I²C Data Clock for DP AUX channel. This pin, along with AUX_I2C_SCL, creates external serial interface for DP AUX channel. Connect to digital 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 16 [5V Tolerant]
B12	AUX_UART_TX_BOOT4_GPIO_21	I/O	UART Transmit Data Output for DP AUX channel
			BOOTSTRAP[4] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 21 [5V Tolerant]
A12	AUX_UART_RX_GPIO_22	I/O	UART Receive Data Input for DP AUX channel. Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 22 [5V Tolerant]
B13	I2C_SCL_GPIO_24	I/O	I²C_SCL. Pull up to 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 24 [5V Tolerant]
A13	I2C_SDA_GPIO_25	I/O	I²C_SDA. Pull up to 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 25 [5V Tolerant]

Table 8. No connects

Pin	Assignment	I/O	Description
F12	NC1	-	No connection.
G12	NC2	-	
D11	NC3	-	
E11	NC4	-	
B2	NC5	-	
B3	NC6	-	

Table 9. System power and ground

Pin	Assignment	I/O	Description
D6	VDDA_3V3	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
E7, E8, K6, K9	PVDD1	P	Digital 1.2V VDD. Connect to digital 1.2V with 0.1µF bypass capacitor.
G11	PVDD21	P	Digital 3.3V VDD. Connect to digital 3.3V with 0.1µF bypass capacitor. Must be connected at same voltage level.
G5	PVDD22		
A1, A14, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	PVSS3	G	Digital Ground. Each pin must be connected directly to digital ground plane.
B11, C7, C8, D9	DPTX_VDDA_1V2	P	DisplayPort Transmitter Analog 1.2V Power Supply. Must be bypassed with a 0.1µF capacitor to analog ground plane on board.
D7, D8, E9, E10	DPTX_VSSA	G	DisplayPort Transmitter VSS. Must be directly connected to analog ground plane on board.
D5	VDD33_TX	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
C5	VSSA_TX	G	Analog ground. Must connect directly to analog ground plane on board
H3, H12, L8, N1, N14	AVDD_OUT_LVRX_33	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
L7	AVDD_LVRX_12	P	Analog 1.2V VDD. Connect to analog 1.2V with 0.1µF bypass capacitor to analog ground plane on board.
K7	AVSS_LVTX	G	Analog ground. Must connect directly to analog ground plane on board.
F2, F13, H5, H10, K8, P1, P14	AVSS_OUT_LVRX	G	Analog ground. Must connect directly to analog ground plane on board.
A2	VSS_RPLL	G	Analog Ground for the DDS Reference PLL and Digital Core. Must be directly connected to analog ground plane on board.
A3	VDD_RPLL	P	Analog 1.2V Power Supply for RCLK PLL and Digital Core. Must be bypassed with a 0.1µF capacitor to analog ground plane on board.

Note: 1 PVDD21 and PVDD22 must be connected to same power supply.
2 Add 47 K pull-down resistor for HPD_IN signal.

5.2 Bootstrap configuration

During hardware reset, on the rising edge of RESETn, logic high or low configuration on Bootstrap pins are latched and stored. 4.7 K pull-up or pull-down resistors must be installed to indicate logic '1' or '0' status on the bootstrap pins. Bootstrap operation is only guaranteed with external pull-up or pull-down resistors. There are eight Bootstrap pins available on STDP4028. Some bootstraps may not be available for normal use.

Table 10. Bootstrap configuration

Pin #	Assignment	Function
E3	BOOT[0]	Set to 1 (Pull High to Vdd)
C2	BOOT[1]	Set to 0 (Pull Low to GND)
D4	BOOT[2]	Set to 0 (Pull Low to GND) for normal operation
E5	BOOT[3]	TTL_LVDS_OUT TTL/LVDS output mode selection 0 = Output is in LVDS format 1 = Output is in TTL format
B12	BOOT[4]	OCM_BOOT_SEL 0 = OCM boot will be from internal ROM code. (Internal ROM is 'ON' and mapped to top 32K of OCM address range) 1 = OCM boot is from external ROM/Flash code (Internal ROM is 'OFF' and external ROM/Flash mapped to top 512K of OCM address range)
G10	BOOT[5]	WIDE_NARROW_BUS Selects wide or narrow LVDS or TTL bus LVDS 0 = DUAL LVDS 1 = QUAD LVDS TTL 0 = Single 1 = Dual
F11	BOOT[6]	ASSR_ENABLE Selects whether ASSR is enabled 0 = Disabled 1 = Enabled
D12	BOOT[7]	I2C_DEV_ID I2C slave Device ID select for RD/WR access. 0: 0xE6, 0xE7 1: 0xE4, 0xE5

5.3 General purpose input/output (GPIO) pins

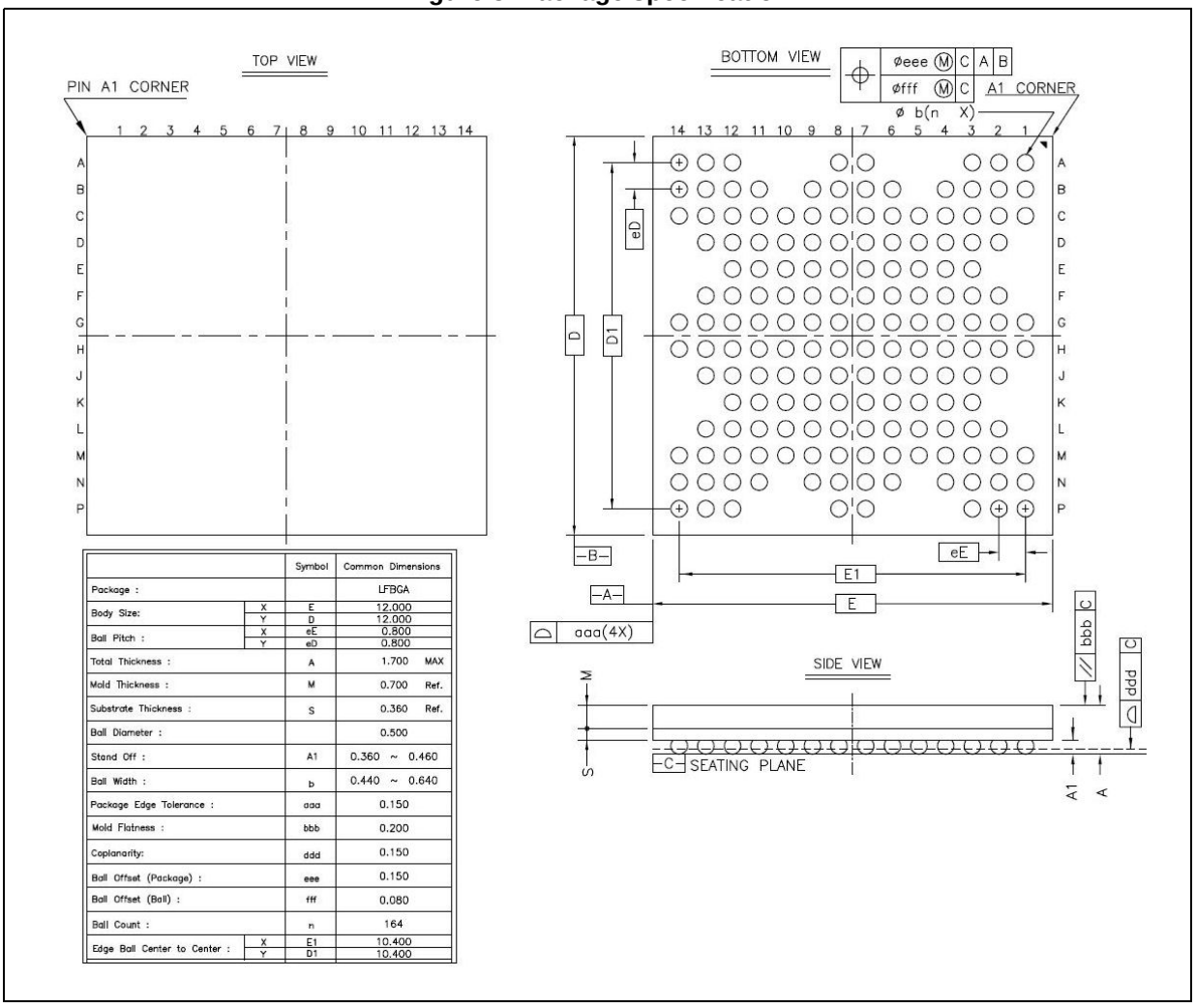
The STDP4028 contains 25 general-purpose input/output (GPIO) pins for system configuration purpose. GPIO_0, GPIO_1 are dedicated general-purpose IO pins and the rest have shared functionality. Each GPIO has independent direction control and open drain enable for reading and writing.

Note: The GPIO functionality is available only for custom applications. Default settings allow configuration of dedicated GPIO pins (GPIO_0 and GPIO_1) through host interface and the rest of the GPIO configuration requires over-riding the default feature using external firmware.

6. Package

Package type: 164 LFBGA (12 x 12 mm / ball pitch 0.8 mm)

Figure 3. Package specification

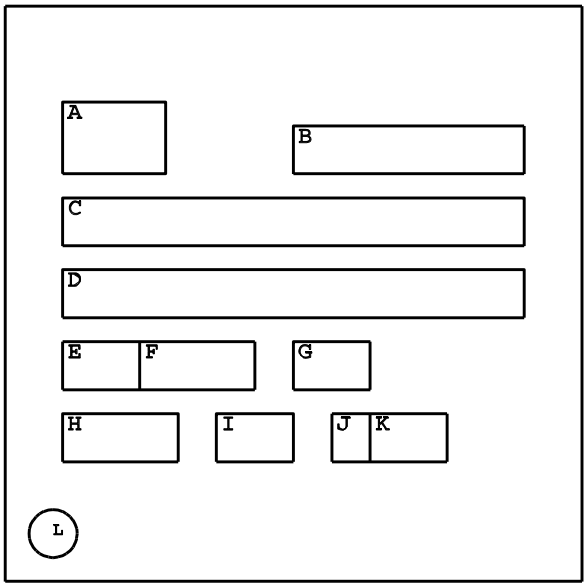


		Symbol	Common Dimensions
Package :			LFBGA
Body Size:	X	E	12.000
	Y	D	12.000
Ball Pitch :	X	eE	0.800
	Y	eD	0.800
Total Thickness :		A	1.700 MAX
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.500
Stand Off :		A1	0.360 ~ 0.460
Ball Width :		b	0.440 ~ 0.640
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.150
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	164
Edge Ball Center to Center :	X	E1	10.400
	Y	D1	10.400

6.1 Marking field template and descriptors

The STDP4028 marking template is shown below.

Figure 4. Marking template



Field descriptors are shown below.

Table 11.Field descriptors

Field	Description	Marking
A	Standard MegaChips logo	M
B	2-character version code	AB
C	Product code	STDP4028
D	8-character diffusion code	9R”ABCDEF”
E	2-character assembly plant code	AA
F	3-character BE sequence code	“XYZ”
G	2-character diffusion plant code	9R
H	3-character country of origin code	TWN
I	2-character test plant code	AA
J	1-digit assembly year	“Y”
K	2-digit assembly week	“WW”
L	Ball A1 identifier	a DOT

7. Electrical specification

7.1 Absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 12. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1,2)	$V_{VDD\_3.3}$	-0.3	3.3	3.6	V
1.2 V supply voltages (1,2)	$V_{VDD\_1.2}$	-0.3	1.2	1.26	V
Input voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3	-	5.5	V
Input voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3	-	3.6	V
ESD - Human Body Model (HBM)(4)	V_{ESD}	-	-	±2.0	kV
ESD - Machine Model (MM)(4)	V_{ESD}	-	-	±200	V
ESD - Charged Device Model (CDM)(4)	V_{ESD}	-	-	±500	V
Latch-up	I_{LA}	-	-	±100	mA
Ambient operating temperature	T_A	0	-	70	°C
Storage temperature	T_{STG}	-40	-	150	°C
Operating junction temperature	T_J	0	-	125	°C
Thermal resistance (Junction to Ambient)(3)	θ_{JA}	-	-	36.6	°C/W
Thermal resistance (Junction to Case)(3)	θ_{JC}	-	-	18.1	°C/W
Peak IR reflow soldering temperature (<10 sec.)	T_{SOL}	-	-	260	°C

Note (1): All voltages are measured with respect to GND.

Note (2): Absolute maximum voltage ranges are for transient voltage excursions.

Note (3): These are simulated results under the following conditions - Four layer JEDEC PCB, no heat spreader, Air flow = 0 m/s

Note (4): The ESD result shown is not applicable for reserved pins.

7.2 Maximum speed of operation

System clocks

Crystal clock = 27 MHz typical

SPI_CLK = 50 MHz

I2C CLK = 400 kHz

Internal OCM clock = 100 MHz max

LVTTL input clocks

Video input: Single bus clocking

165 MHz max

Video input: Dual bus clocking

165 MHz max

LVDS input clocks

Single LVDS channel

Channel E0/O0: 150 MHz

Dual LVDS channel

Channel E0/O0: 150 MHz

Quad LVDS channel

Channel E0/O0/E1/O1: 100 MHz

Audio input

SPDIF LVTTL input = 12.288 MHz

I2S WS input = 192 kHz

I2S SCLK input = 12.288 MHz

DisplayPort transmitter bit rate

Main link

Min: 1.62 Gbps/lane

Max: 3.24 Gbps/lane

Auxiliary channel: 1 Mbps

7.3 DC characteristics

Table 13. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (analog and digital)	$V_{VDD\_3.3}$	3.0	3.3	3.6	V
1.2 V supply voltages (analog and digital)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
Power					
TTL input					
Power consumption: 2560 x 1600 / 60 Hz test pattern: ON-OFF dot Moire	4L	-	330	-	mW
Power consumption: 1920 x 1200 / 60 Hz test pattern: ON-OFF dot Moire	2L	-	270	-	mW
Power consumption: 1440 x 900 / 60 Hz test pattern: ON-OFF dot Moire	1L	-	230	-	mW
Standby		-	18	-	mW
Supply Current					
Measurement conditions: 2560 x 1600 / 60 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3V DDA analog and digital power) =1.2V In all configuration, 8 bits input is used.		-	20 218	-	mA
Power					
LVDS input					
Power consumption: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire	4L	-	604	-	mW
Power consumption: 1920 x 1200 / 60 Hz test pattern: ON-OFF dot Moire	2L	-	400	-	mW
Power consumption: 1440 x 900 / 60 Hz test pattern: ON-OFF dot Moire	1L	-	312	-	mW
Standby		-	18	-	mW
Supply Current					
Measurement conditions: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3V DDA analog and digital power) =1.2V In all configuration, 8 bits input is used.		-	101 226	-	mA
Inputs					
High voltage	V_{IH}	2.0	-	VDD	V
Low voltage	V_{IL}	GND	-	0.8	V
High current (V_{IN} = 5.0 V)	I_{IH}	-25	-	25	µA
Low current (V_{IN} = 0.8 V)	I_{IL}	-25	-	25	µA

Table 13. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Capacitance (V_{IN} = 2.4 V)	C_{IN}	-	-	8	pF
Outputs					
High voltage (I_{OH} = 7 mA)	V_{OH}	2.4	-	VDD	V
Low voltage (I_{OL} = -7 mA)	V_{OL}	GND	-	0.4	V
Tri-state leakage current	I_{OZ}	-25	-	25	µA

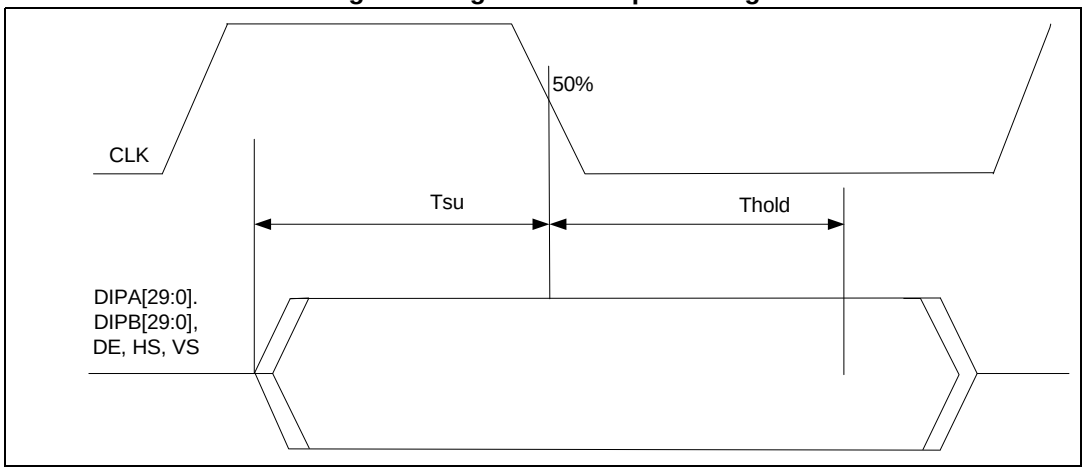
7.4 AC characteristics

7.4.1 Digital video input port DC characteristics

Table 14. Digital video input port DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage		GND	-	+0.8	V
V_{IH}	High level input voltage		2.0	-	$V_{DD\_3.3}$	V
$I_{LI/O}$	I/O leak current		-	-	10	µA
Ci	Input capacitance	I/O at high impedance	-	-	4	pF
tcyc	DIP Clock cycle time		6	-	125	ns
Tsu	DIPE[29:0], DIPO[29:0], HS, VS, DE setup time		2	-	-	ns
Thold	DIPE[29:0], DIPO[29:0], HS, VS, DE hold time		2	-	-	ns

Figure 5. Digital video input timing



7.4.2 LVDS video input DC/AC characteristics

Table 15. LVDS video input DC/AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Differential input high voltage threshold	V_{CM} = 1.2V, *Figure 6*	-	-	100	mV
V_{IL}	Differential input low voltage threshold		-100	-	-	mV
V_{CM}	Common-mode Input voltage	*Note 1*	0.1	-	2.35	V
V_{ID}	Differential Input voltage		200	-	600	mV
$I_{IN-LEAK}$	Input leakage current	V_{IN} = 2.4V or V_{IN} = 0V, termination disabled	-	-	±10	µA
R_{TERM}	Integrated termination resistor		80	100	130	W
t_{TXBIT0}	Receiver LVDS input strobe position	Bit 0, *Figure 7*	0.61	-	1.33	ns
t_{TXBIT1}		Bit 1, *Figure 7*	2.54	-	3.26	ns
t_{TXBIT2}		Bit 2, *Figure 7*	4.47	-	5.19	ns
t_{TXBIT3}		Bit 3, *Figure 7*	6.4	-	7.12	ns
t_{TXBIT4}		Bit 4, *Figure 7*	8.33	-	9.05	ns
t_{TXBIT5}		Bit 5, *Figure 7*	10.26	-	10.98	ns
t_{TXBIT6}		Bit 6, *Figure 7*	12.19	-	12.91	ns
t_{PHD}	Phase delay time		-	241	-	ps
t_{DATA}	Data period	f_{CLOCK} = 74 MHz	-	1.93	-	ns
t_{RCVR_MARGIN}	Receiver margin	*Figure 8*, *Note 2*	-	370	-	ps
t_{STROBE}	Minimum strobe timing	*Figure 8*, f_{CLOCK} = 74 MHz, *Note 2*	720	800	-	ps
$t_{TXBITMIN}$	Clock to data skew margin	*Figure 8*	-200	-	-	ps
$t_{TXBITMAX}$		*Figure 8*	-	-	+200	ps

Note: 1 The common-mode range is guaranteed by design. The LVDS receiver is tested with V_{CM} = 1.2V.

2 The LVDS receiver inputs can tolerate jitter added within the receiver margin (t_{RCVR_MARGIN}) specification.

Figure 6. LVDS single-ended waveform

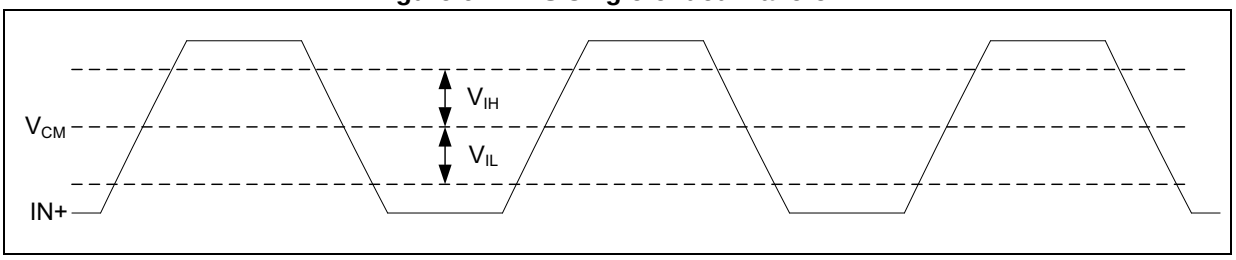


Figure 7. Receiver strobe positions LVDS input

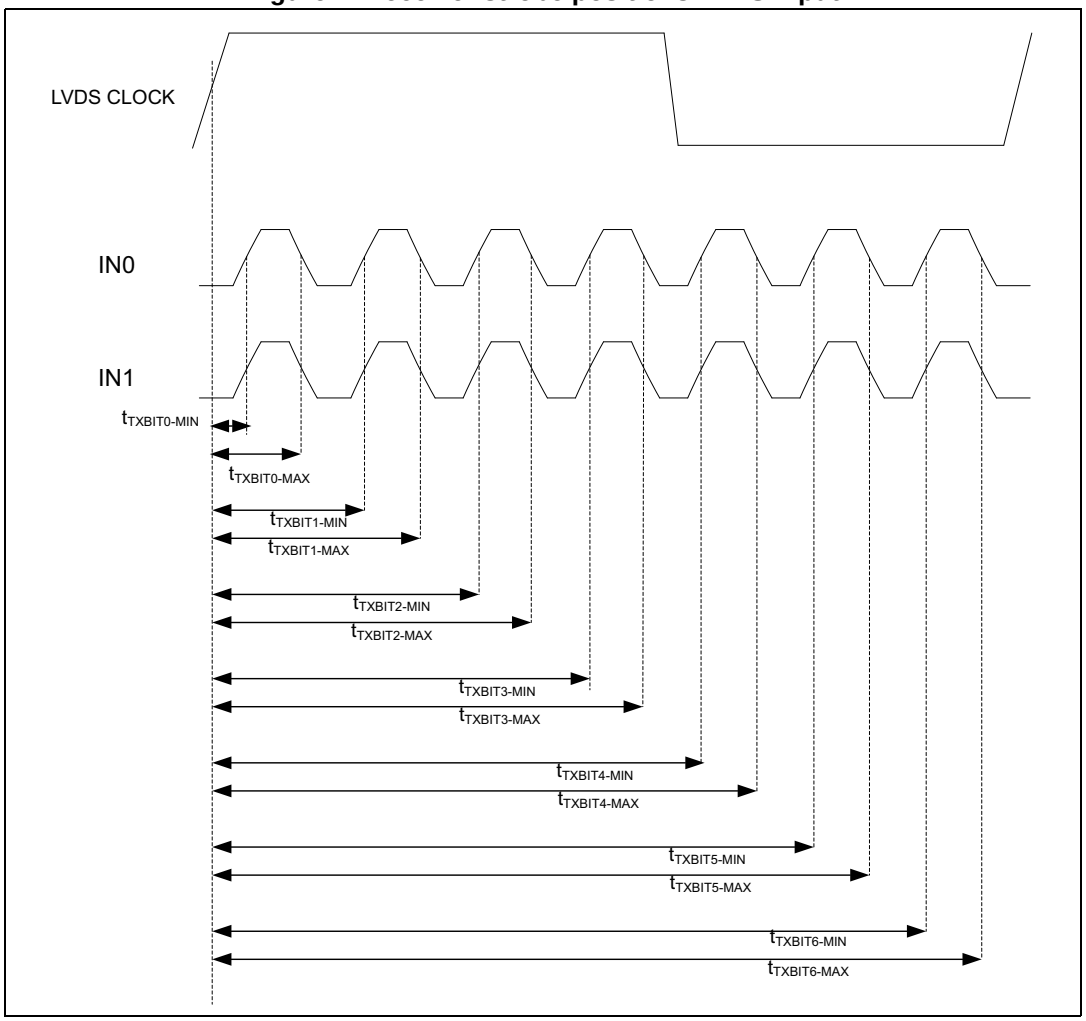
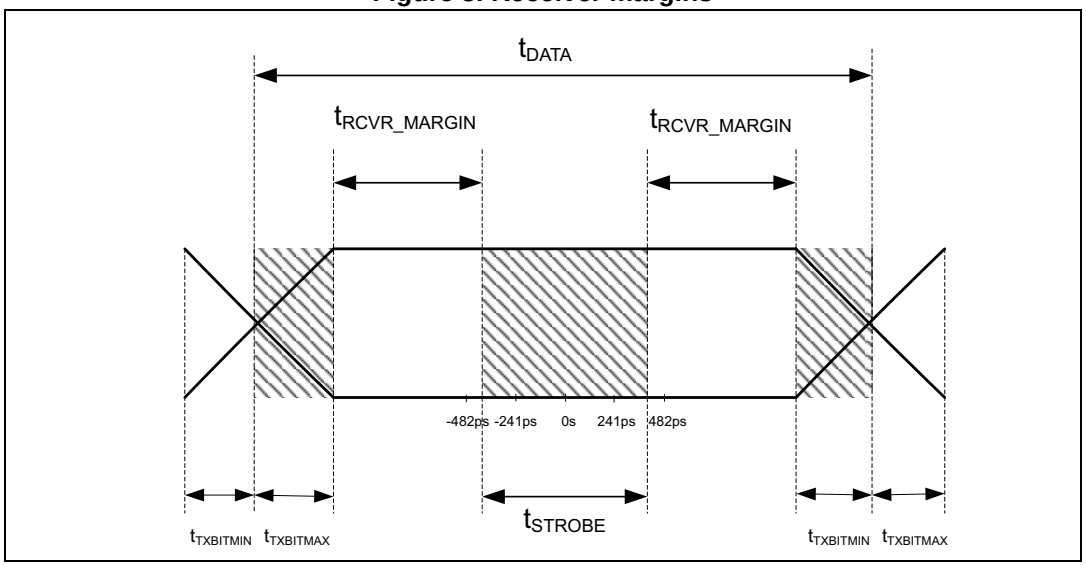


Figure 8. Receiver margins

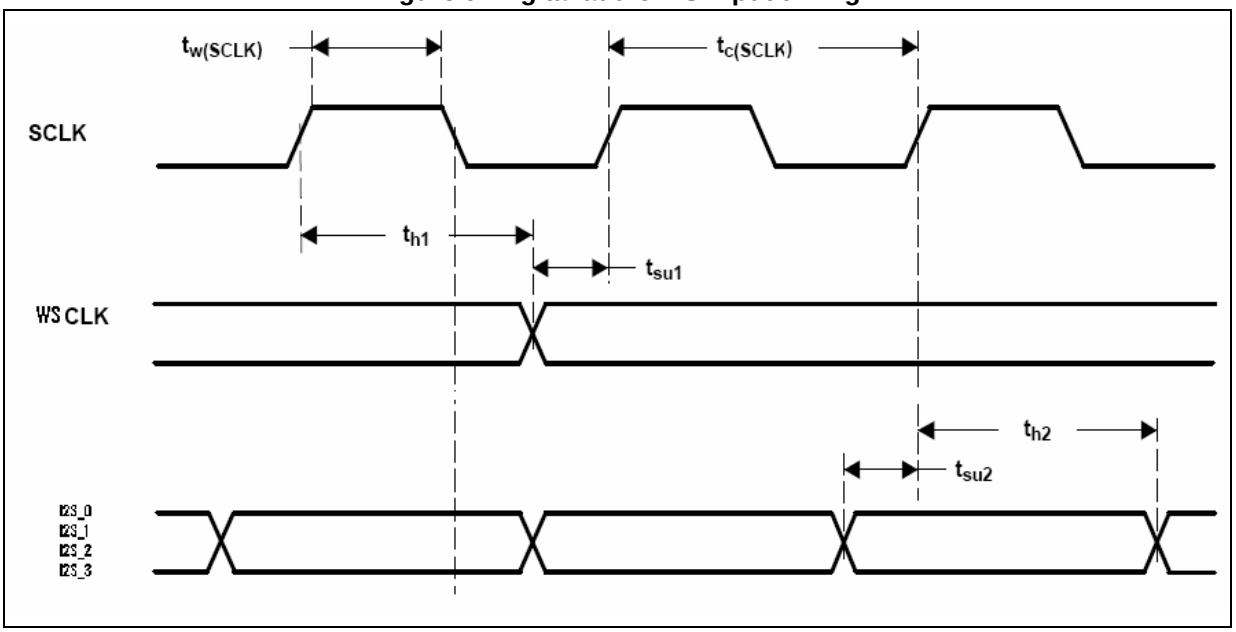


7.4.3 Digital audio input I2S timing

Table 16. Digital audio input I2S timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fs	Sample frequency		32	-	192	kHz
$t_{c(sclk)}$	SCLK cycle time		-	81.38	-	ns
$t_{w(sclk)}$	SCLK pulse duration, SCLK high time		$0.4t_{c(sclk)}$	$0.5t_{c(sclk)}$	$0.6t_{c(sclk)}$	ns
f_{sclk}	SCLK (bit clock) frequency = rate x sample frequency (fs)	Maximum bit clock freq.	-	-	9.216	MHz
		64 x 32 kHz (32 kHz)	-	2.048	-	MHz
		6 4x 44.1 kHz (44.1kHz)	-	2.822	-	MHz
		64 x 48 kHz (48 kHz)	-	3.072	-	MHz
		64 x 96 kHz (96 kHz)	-	6.144	-	MHz
		64 x 192 kHz (192 kHz)	-	12.288	-	MHz
t_{su1}	Hold time, WS clock from SCLK rising edge		$0.5\ t_{c(sclk)}$	-	-	ns
t_{h1}	Setup time, WS clock to SCLK rising edge		10	-	-	ns
t_{su2}	Setup time, I2S data in to SCLK rising edge		10	-	-	ns
t_{h2}	Hold time, I2S data in to SCLK rising edge		10	-	-	ns

Figure 9. Digital audio I2S input timing



7.4.4 DisplayPort transmitter

Table 17. DisplayPort transmitter characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
UI_High_Rate	Unit interval for high bit rate (2.7 Gbps/lane)	-	370	-	ps	Range is nominal +/- 300ppm. UI does not account for down-spread dictated variations.
UI_Low_Rate	Unit interval for reduced bit rate (1.62 Gbps/lane)	-	617	-	ps	
UI_Rate_3.24Gbps	Unit interval for high bit rate (3.24 Gbps/lane)	-	3.24	-	Gbps	
Down_Spread_Amplitude	Link clock down spreading	0	-	0.5	%	
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	
VTX-DIFFp-p-Level1	Differential peak-to-peak output voltage Level 1	0.34	0.4	0.46	V	Refer to DisplayPort Specification for definition of differential voltage.
VTX-DIFFp-p-Level2	Differential peak-to-peak output voltage Level 2	0.51	0.6	0.68	V	
VTX-DIFFp-p-Level3	Differential peak-to-peak output voltage Level 3	0.69	0.8	0.92	V	
VTX-DIFFp-p-Level4	Differential peak-to-peak output voltage Level 4	1.01	1.2	1.38	V	
VTX-PREEMP-RATIO	No pre-emphasis	0.0	-	9.5	dB	Refer to DisplayPort Specification for definition of differential voltage. Support of no pre-emphasis, 3.5- and 6.0-dB pre-emphasis mandatory. 9.5-dB level optional.
	3.5 dB pre-emphasis level	2.8	3.5	4.2	dB	
	6.0 dB pre-emphasis level	4.8	6.0	7.2	dB	
	9.5 dB pre-emphasis level	7.6	9.5	11.4	dB	
Tx horizontal eye specification for high bit rate						
TTX-EYE_CHIP_High_Rate	Minimum transmitter eye width at Tx package pins	0.74	-	-	UI	
TTX-EYE-MEDIAN-to-MAX-JITTER_CHIP_High_Rate	Maximum time between the jitter median and maximum deviation from the median at Tx package pins	-	-	0.13	UI	
Tx horizontal eye specification for reduced bit rate						
TTX-EYE_CHIP_Low_Rate	Minimum transmitter eye width at Tx package pins	0.84	-	-	UI	
TTX-EYE-MEDIAN-to-MAX-JITTER_CHIP_Low_Rate	Maximum time between the jitter median and maximum deviation from the median at Tx package pins	-	-	0.08	UI	

Table 17. DisplayPort transmitter characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
TTX-RISE_CHIP, TTX-FALL_CHIP	D+/D- TX output rise/fall time at Tx package pins	50	-	130	ps	At 20-to-80%
VTX-DC-CM	TX DC common mode voltage	0	-	VDD	V	Common mode voltage is equal to Vbias_Tx voltage. VDD is the output driver power supply voltage and 3.6 V maximum.
ITX-SHORT	TX short circuit current limit	-	-	90	mA	Total drive current of the transmitter when it is shorted to its ground.
RLTX-DIFF	Differential return loss at 0.675 GHz	-	-	12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
	Differential return loss at 1.35 GHz	-	-	9	dB	
LTX-SKEW-INTER_CHIP	Lane-to-lane skew at TX package pins	-	-	2	UI	
LTX-SKEW-INTRA_CHIP	Lane intra-pair output skew at Tx package pins	-	-	20	ps	
CTX	AC coupling capacitor	75	-	200	nF	All DisplayPort Main Link lanes as well as AUX CH shall be AC coupled. AC coupling capacitors shall be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.
FTX-REJECTION-BW	Clock jitter rejection bandwidth	-	-	4	MHz	

7.4.5 I2C interface timing

Table 18. I2C interface timing

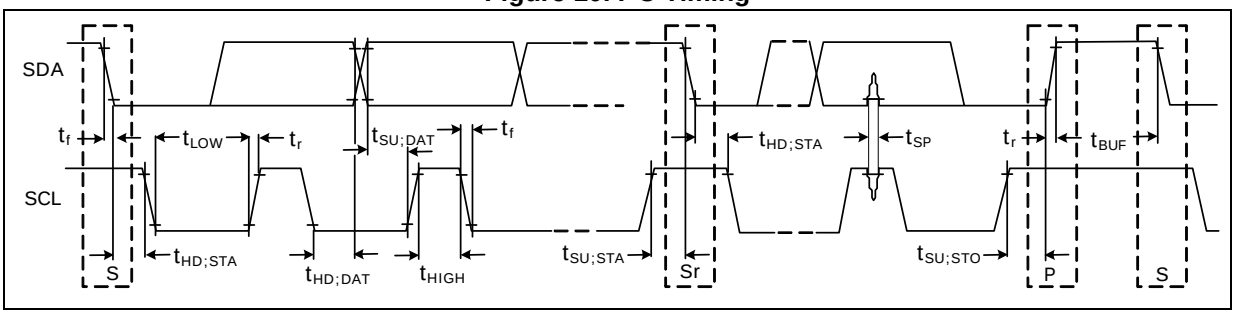
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	-	400	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	0.6	1.1	-	µs
t_{LOW}	Low period of clock	SCL	1.3	1.12	-	µs
t_{HIGH}	High period of clock	SCL	0.6	1.0	-	µs
$T_{su;STA}$	Setup time for a repeated START		0.6	1.4	-	µs
$t_{HD;DAT}$	Data hold time	For master	0	0.72	0.9(1)	µs
$t_{SU;DAT}$	Data setup time		100	400	-	ns

Table 18. I2C interface timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{BUF}	Bus free time between STOP and START		1.3	140	-	µs
C_b	Capacitance load for each bus line		-	-	400	pF
t_r	Rise time		20	195	300	ns
t_f	Fall time		20	10	300	ns
V_{nh}	Noise margin at high level		0.2 VDD	0.34	-	V
V_{nl}	Noise margin at low level		0.1 VDD	0.16	-	

Note: *The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.*

Figure 10. I²C Timing



7.4.6 SPI interface timing

Table 19. SPI interface timing, VDD = 3.3V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial clock frequency	-	50	MHz
T_{SCKH}	Serial clock high time	9	-	ns
T_{SCKL}	Serial clock low time	9	-	ns
T_{SCKR}	Serial clock rise time (slew rate)	0.1	-	V/ns
T_{SCKF}	Serial clock fall time (slew rate)	0.1	-	V/ns
T_{CES}	CE# active setup time	5	-	ns
T_{CEH}	CE# active hold time	5	-	ns
T_{CHS}	CE# not active setup time	5	-	ns
T_{CHH}	CE# not active hold time	5	-	ns
T_{CPH}	CE# high time	50	-	ns
T_{CHZ}	CE# high to high-Z output	-	8	ns
T_{CLZ}	SCK low to low-Z output	0	-	ns
T_{DS}	Data in setup time	5	-	ns
T_{DH}	Data in hold time	5	-	ns
T_{OH}	Output hold from SCK change	0	-	ns
T_V	Output valid from SCK	-	8	ns

Figure 11. SPI output or serial interface SPI ROM input timing

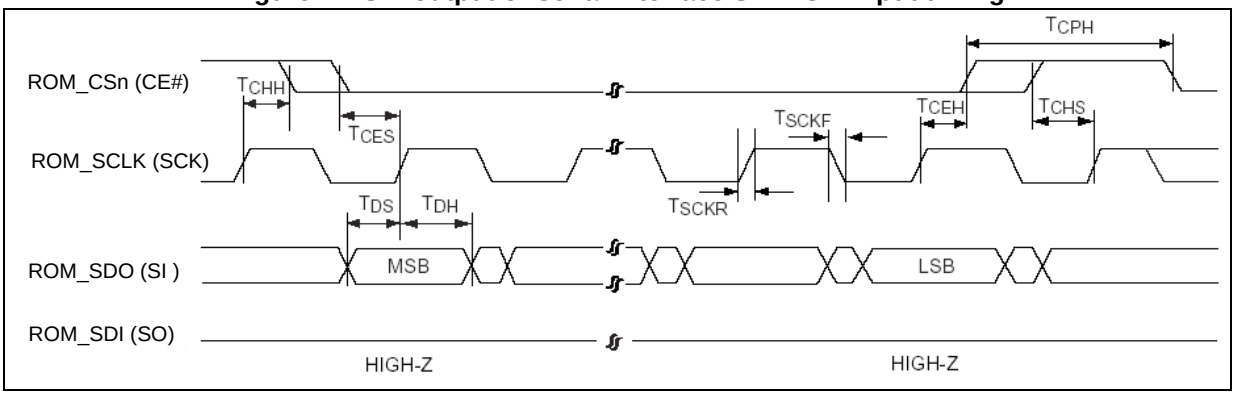
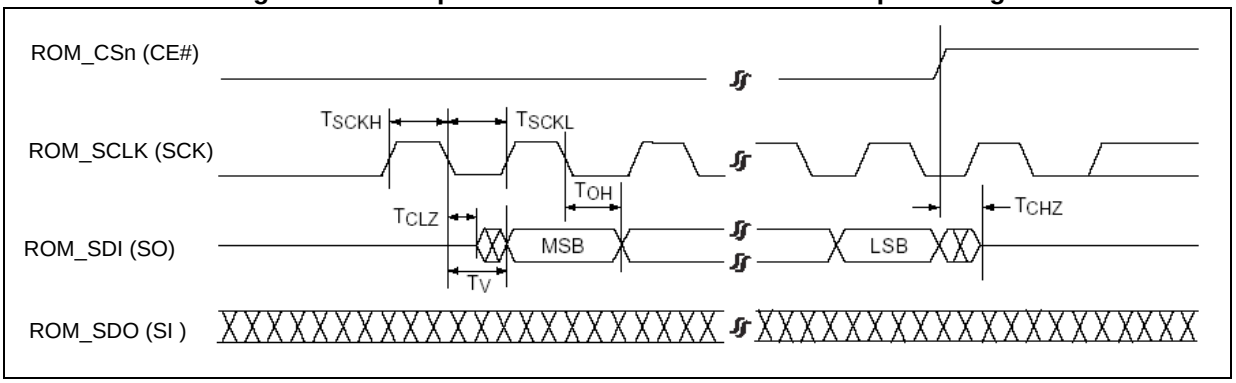


Figure 12. SPI input or serial interface SPI ROM output timing



8. Ordering information

Table 20. Order codes

Part number	Description
STDP4028-AB	164 LFBGA (12 x 12 mm)

9. Revision history

Table 21. Document revision history

Date	Revision	Changes
03-Mar-2016	A	Initial release.

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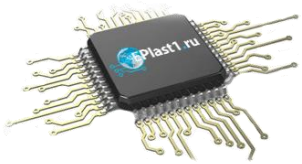
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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