SKY13455-31: 0.4 to 2.7 GHz SP12T Switch with MIPI RFFE Interface

Applications

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM)
- Embedded data cards

Features

- Broadband frequency range: 0.4 to 2.7 GHz
- Low insertion loss
- High isolation and linearity
- Integrated GSM harmonic filter
- Integrated, programmable MIPI interface
- Ten TRX ports, one GSM low band transmit port, and one GSM high band transmit port
- Small MCM (22-pin, 3.2 x 2.5 x 0.8 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

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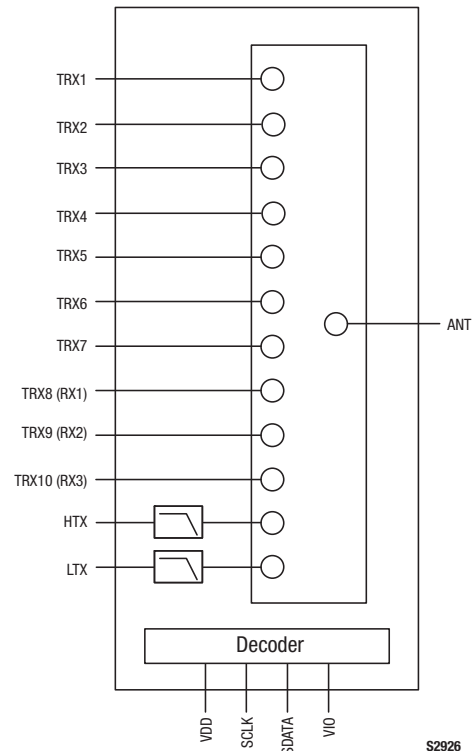

Figure 1. SKY13455-31 Block Diagram
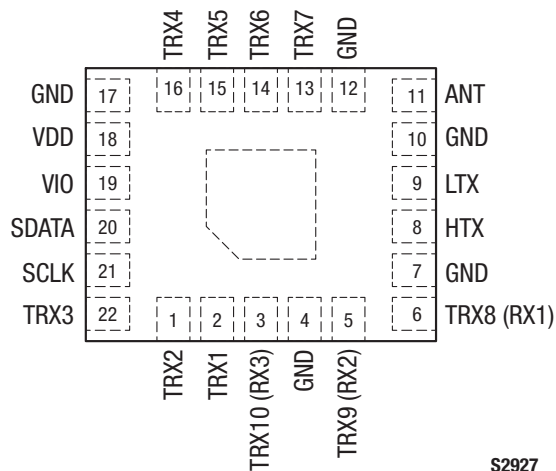
Description

The SKY13455-31 is a Single-Pole, Twelve-Throw (SP12T) antenna switch with integrated GSM transmit harmonic filter. The SKY13455-31 maintains a high linearity, high isolation, and low insertion loss performance, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.

The design features two dedicated GSM transmit ports. The remaining ten ports are suitable for WCDMA transmit/receive and GSM receive functions. Three transmit ports (TRX1, TRX2, and TRX4) have been specifically designed to provide optimal LTE Band 13 performance. The switch exhibits an excellent triple beat ratio and $2^{nd}/3^{rd}$ order modulation distortion performance.

Switching is controlled by an integrated MIPI interface. Depending on the logic applied to the decoder, the antenna pin is connected to one of 12 switched RF ports using a low insertion loss path, while the paths between the antenna pin and the other RF pins are in a high isolation state. No external DC blocking capacitors are required on the RF paths.

The SKY13455-31 is manufactured in a compact, 3.2 x 2.5 x 0.8 mm, 22-pin surface mount Multi-Chip Module (MCM) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Figure 2. SKY13455-31 Pinout – 22-Pin MCM
(Top View)

Table 1. SKY13455-31 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	TRX2	RF input/output port 2 optimzed for LTE Band 13 (704 to 787 MHz)	12	GND	Ground
2	TRX1	RF input/output port 1 optimized for LTE Band 13 (704 to 787 MHz)	13	TRX7	RF input/output port 7
3	TRX10 (RX3)	RF input/output port 10 (receive 3)	14	TRX6	RF input/output port 6
4	GND	Ground	15	TRX5	RF input/output port 5
5	TRX9 (RX2)	RF input/output port 9 (receive 2)	16	TRX4	RF input/output port 4 optimized for LTE Band 13 (704 to 787 MHz)
6	TRX8 (RX1)	RF input/output port 8 (receive 1)	17	GND	Ground
7	GND	Ground	18	VDD	DC power supply
8	HTX	GSM high band transmit RF input port with integrated harmonic filter	19	VIO	Interface supply voltage
9	LTX	GSM low band transmit RF input port with integrated harmonic filter	20	SDATA	Data
10	GND	Ground	21	SCLK	Clock
11	ANT	Antenna RF port	22	TRX3	RF input/output port 3

Note: Bottom ground paddles must be connected to ground.

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Table 2. SKY13455-31 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Power supply	V_{DD}	2.5	5.0	V
Digital control signal	VIO		2	V

RF input power:
    LTX pin
    HTX pin
    All TRXx pins
	P_{IN}		+36
			+34
			+31
				dBm
				dBm
				dBm

Storage temperature	T_{STG}	−55	+150	°C
Operating temperature	T_{OP}	−30	+90	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: *Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13455-31 are provided in Table 2. Electrical specifications are provided in Tables 3, 4, and 5. Figure 3 shows a timing diagram for the SKY13455-31.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 6 and 7, respectively.

Figure 4 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX10 ports, while a −15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting 3rd Order Intermodulation Distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13455-31 exhibits exceptional performance for all TRXx ports.

Table 8 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 5 and 6 provide the timing diagrams for register write commands and read commands, respectively.

Table 9 provides the Register_0 logic. Table 10 describes the register parameters and bit values.

Table 3. SKY13455-31 Electrical Specifications (Note 1) (1 of 4)
(V$_{DD}$ = 2.85 V, T$_{OP}$ = +25 °C, Characteristic Impedance [Z$_0$] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss:	IL					
TXLB		824 to 915 MHz, +35 dBm		1.25	1.45	dB
TXHB		1710 to 1910 MHz, +33 dBm		1.15	1.35	dB
TRX1/2/4		704 to 787 MHz, +25 dBm		0.55	0.70	dB
TRX3/5 to 10		704 to 787 MHz, +25 dBm		0.65	0.80	dB
TRX1/2/3		824 to 960 MHz, +25 dBm		0.60	0.75	dB
TRX4/5/6/7		824 to 960 MHz, +25 dBm		0.70	0.85	dB
TRX8/9/10		824 to 960 MHz, +25 dBm		0.60	0.75	dB
TRX1/2/3		1710 to 1990 Mhz, +25 dBm		0.70	0.85	dB
TRX4/5/6/7		1710 to 1990 Mhz, +25 dBm		0.70	0.85	dB
TRX8/9/10		1710 to 1990 Mhz, +25 dBm		0.70	0.85	dB
TRX1/2/3		2110 to 2170 MHz, +25 dBm		0.70	0.85	dB
TRX4/5/6/7		2110 to 2170 MHz, +25 dBm		0.70	0.85	dB
TRX8,9,10		2110 to 2170 MHz, +25 dBm		0.70	0.85	dB
TRX1/2/3		2300 to 2690 MHz, +25 dBm		0.75	0.90	dB
TRX4/5/6		2300 to 2690 MHz, +25 dBm		0.95	1.10	dB
TRX7		2300 to 2690 MHz, +25 dBm		1.10	1.30	dB
TRX8/9/10		2300 to 2690 MHz, +25 dBm		0.75	0.95	dB

Table 3. SKY13455-31 Electrical Specifications (Note 1) (2 of 4)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

| Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications (continued)						
Return loss	VSWR	TRXx ports, 0.4 to 2.2 GHz	14	18		dB
GSM harmonic attenuation	H2LB	Transmit low band to ANT, 2fo 1648 to 1830 MHz	25	28		dB
	H3LB	Transmit low band to ANT, 3fo 2472 to 2745 MHz	25	28		dB
	H4LB	Transmit low band to ANT, 4fo 3296 to 3660 MHz		25		dB
	H2HB	Transmit high band to ANT, 2fo 3420 to 3820 MHz		25		dB
	H3HB	Transmit high band to ANT, 3fo 5130 to 5730 MHz	25	28		dB
Large signal harmonics, transmit GSM low band	2fo, 3fo	Transmit GSM low band, P_{IN} <+34.5 dBm, VSWR = 1:1		−54	−45	dBm
	2fo, 3fo	Transmit GSM low band, P_{IN} <+34.5 dBm, VSWR = 5:1, all phases		−40	−36	dBm
Large signal harmonics, transmit GSM high band	2fo, 3fo	Transmit GSM high band, P_{IN} <+33 dBm, VSWR = 1:1		−54	−45	dBm
	2fo, 3fo	Transmit GSM high band, P_{IN} <+33 dBm, VSWR = 5:1, all phases		−40	−36	dBm
Large signal harmonics, transmit band 13	2fo	ANT to TRXx ports, @ 777 to 787 MHz, P_{IN} < +25 dBm, VSWR = 1:1		−78		dBm
Large signal harmonics, transmit band 17	3fo	ANT to TRXx ports, @ 704 to 716 MHz, P_{IN} ≤+25 dBm, VSWR = 1:1		−80	−78	dBm
Large signal harmonics, TRXx	2fo, 3fo	Transmit WCDMA 824 to 915 MHz, P_{IN} <+27 dBm, VSWR = 1:1		−72	−66	dBm
	2fo, 3fo	Transmit WCDMA 824 to 915 MHz, P_{IN} <+27 dBm, VSWR = 5:1		−57	−45	dBm

Table 3. SKY13455-31 Electrical Specifications (Note 1) (3 of 4)
(V$_{DD}$ = 2.85 V, T$_{OP}$ = +25 °C, Characteristic Impedance [Z$_0$] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications (continued)						
Large signal harmonics, TRXx	2fo, 3fo	Transmit WCDMA 1710 to 1980 MHz, P$_{IN}$ <+27 dBm, VSWR = 1:1, all phases		–67	–60	dBm
	2fo, 3fo	Transmit WCDMA 1710 to 1980 MHz, P$_{IN}$ <+27 dBm, VSWR = 5:1, all phases		–57	–45	dBm
Isolation (full isolation "on" arms to "off" arms) (see Table 5)	Iso_TX1/2_1800	LTX to HTX, P$_{IN}$ <+35 dBm, @ 1648 to 1830 MHz	28	30.5		dB
	Iso_TX1/TRX_900	LTX to TRXx pins, P$_{IN}$ <+35 dBm, @ 824 to 915 MHz	37	40		dB
	Iso_TX1/RX_900	LTX to receive ports (Note 2), P$_{IN}$ <+35 dBm, @ 869 to 960 MHz	35	43		dB
	Iso_TX2/TRX_1800	HTX to TRXx pins, P$_{IN}$ <+33 dBm, @ 1710 to 1910 MHz	32	35		dB
	Iso_RX2/RX3_1990	TRX9 (RX2) to ANT when TRX10 (RX3) active, P$_{IN}$ <+27 dBm, @ 1805 to 1990 MHz	31	34		dB
	Iso_RX3/RX2_1990	TRX10 (RX3) to ANT when TRX9 (RX2) active, P$_{IN}$ <+27 dBm, @ 1805 to 1990 MHz	31	34		dB
	Iso_TRX/RX	TRXx to receive ports (Note 2), P$_{IN}$ <+27 dBm, @ 1710 to 1910 MHz	25	27		dB
	Iso_TRX/TRX	TRXx to TRXx, P$_{IN}$ <+27 dBm, @ 824 to 1910 MHz, every other pin	26	29		dB
	Iso_TRX/TRX	TRXx to TRXx, P$_{IN}$ <+27 dBm, @ 824 to 1910 MHz, opposite side pins	40	43		dB
	Iso_TRX/TRX	TRXx to TRXx, P$_{IN}$ <+27 dBm, @ 824 to 1910 MHz, adjacent pins	20	22		dB

Table 3. SKY13455-31 Electrical Specifications (Note 1) (4 of 4)
(V$_{DD}$ = 2.85 V, T$_{OP}$ = +25 °C, Characteristic Impedance [Z$_0$] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
DC Specifications						
Triple Beat Ratio (see Table 4)	TBR	650 to 900 MHz	+81	+91		dBc
		1710 to 2155 MHz	+81	+92		dBc
2nd Order Intermodulation Distortion	IMD2	See Table 5		−110	−105	dBm
3rd Order Intermodulation Distortion	IMD3	See Table 6		−110	−105	dBm
Supply voltage	V$_{DD}$		2.50	2.85	3.30	V
Supply current	I$_{DD}$			35	100	µA

Digital data and clock signals:
    High
    Low
    Current
	SDATA, SCLK		0.8 × VIO
			0
					VIO
					0.2 × VIO
					5
						V
						V
						µA

Interface supply voltage level	VIO		1.65	1.80	1.95	V
DC supply turn-on/turn-off time (Note 3)					20	µs
RF path switching time (Note 3)		Between the ANT port and either LTX/HTX or TRXx ports		2	5	µs
Supply ripple					20	mVp-p

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Dedicated receive ports are TRX8 (RX1), TRX9 (RX2), or TRX10 (RX3).

Note 3: Refer to Figure 3.
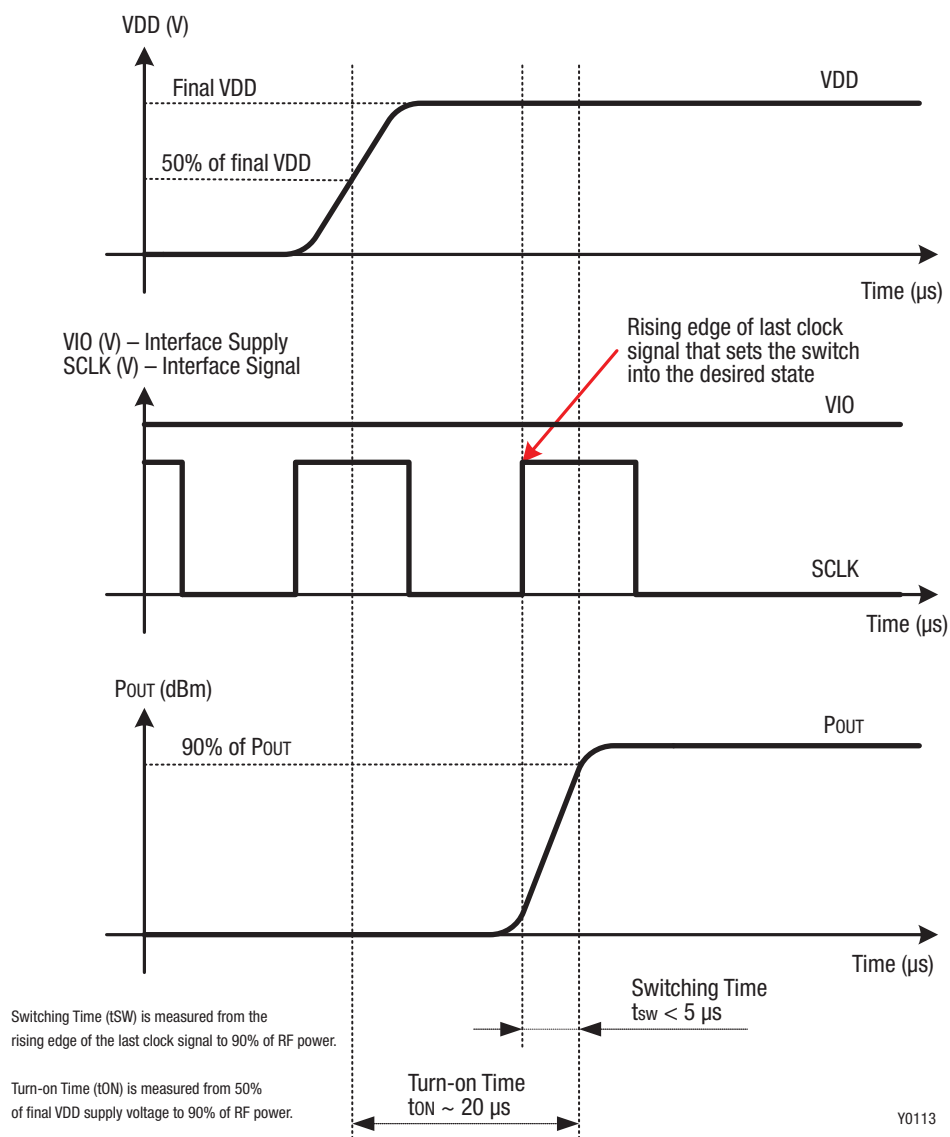
Figure 3. SKY13455-31 Timing Diagram

Table 4. Triple Beat Ratio Frequencies and Power Levels

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker ANT (MHz)	Power Blocker (dBm)	Triple Beat Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	−30	1960.0 ± 1
5	836.5	+21.5	881.5	+21.5	881.5	−30	881.5 ± 1

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Table 5. SKY13455-31 Electrical Specifications: Isolation, "On" Arms to "Off" Arms (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

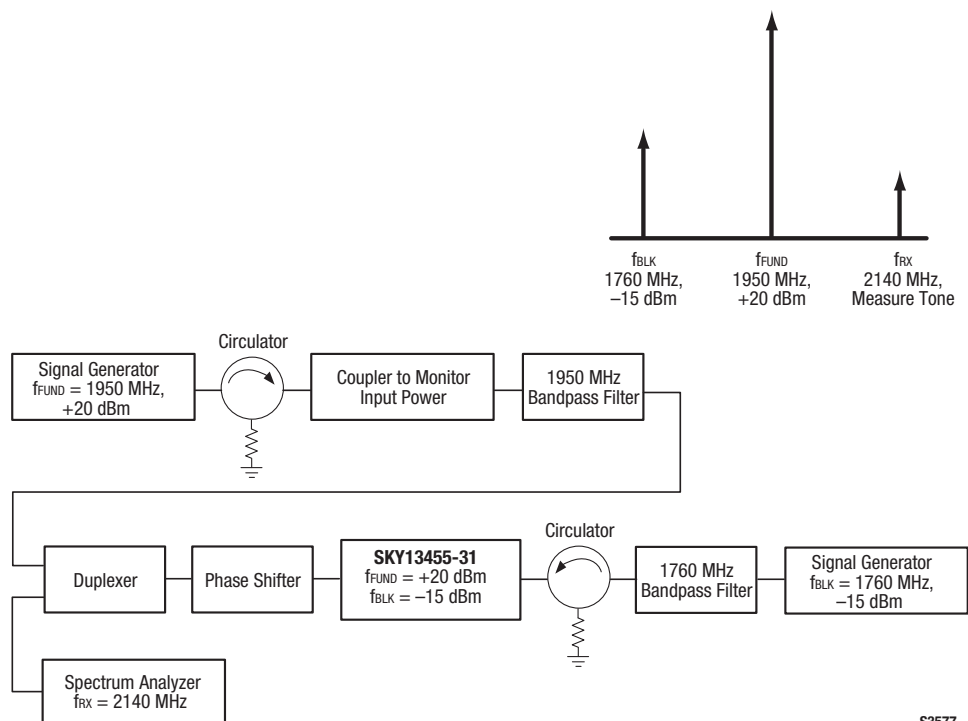| "On" Arm	Freq (MHz)	Isolation (dB)											
		LTX	HTX	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
LTX	915	–	−26	−51	−52	−54	−56	−52	−47	−46	−43	−48	−51
HTX	1910	−25	–	−43	−43	−45	−44	−43	−40	−39	−33	−39	−43
TRX1	915	−34	−66	–	−27	−34	−56	−56	−50	−51	−50	−43	−32
TRX1	1910	−37	−45	–	−22	−28	−45	−45	−42	−41	−43	−37	−27
TRX1	2690	−36	−38	–	−19	−25	−39	−41	−39	−37	−38	−34	−24
TRX2	915	−34	−64	−30	–	−28	−53	−57	−51	−51	−52	−45	−38
TRX2	1910	−37	−44	−24	–	−23	−44	−45	−42	−41	−44	−39	−33
TRX2	2690	−36	−37	−21	–	−20	−38	−41	−39	−37	−39	−36	−30
TRX3	915	−34	−62	−34	−31	–	−50	−57	−52	−52	−54	−47	−41
TRX3	1910	−37	−44	−29	−26	–	−42	−45	−42	−41	−45	−41	−36
TRX3	2690	−36	−37	−26	−22	–	−37	−39	−39	−37	−40	−37	−33
TRX4	915	−34	−57	−49	−48	−47	–	−28	−36	−41	−60	−55	−52
TRX4	1910	−37	−43	−43	−42	−42	–	−22	−30	−33	−47	−47	−45
TRX4	2690	−36	−37	−39	−38	−38	–	−19	−26	−28	−42	−42	−41
TRX5	915	−35	−55	−50	−49	−49	−30	–	−29	−37	−59	−55	−52
TRX5	1910	−38	−43	−44	−43	−43	−25	–	−23	−30	−47	−47	−45
TRX5	2690	−36	−37	−40	−39	−39	−21	–	−19	−26	−42	−42	−41
TRX6	915	−35	−53	−51	−50	−50	−36	−31	–	−30	−58	−55	−52
TRX6	1910	−38	−42	−44	−43	−44	−30	−25	–	−23	−46	−47	−45
TRX6	2690	−36	−37	−40	−39	−40	−26	−22	–	−20	−41	−42	−41
TRX7	915	−37	−51	−51	−50	−51	−39	−38	−32	–	−56	−54	−52
TRX7	1910	−39	−42	−44	−43	−44	−32	−31	−26	–	−45	−46	−45
TRX7	2690	−35	−38	−40	−39	−40	−28	−27	−22	–	−40	−41	−41
TRX8	915	−34	−37	−42	−44	−46	−58	−55	−50	−51	–	−29	−37
TRX8	1910	−42	−29	−37	−39	−41	−45	−45	−42	−41	–	−24	−31
TRX8	2690	−35	−27	−34	−35	−37	−40	−42	−39	−37	–	−21	−28
TRX9	915	−34	−54	−39	−42	−44	−59	−54	−49	−51	−36	–	−32
TRX9	1910	−40	−42	−34	−37	−39	−45	−45	−42	−41	−29	–	−27
TRX9	2690	−36	−39	−31	−34	−36	−40	−42	−39	−37	−25	–	−24
TRX10	915	−34	−65	−29	−36	−40	−58	−55	−49	−51	−44	−38	–
TRX10	1910	−38	−45	−24	−31	−35	−45	−45	−42	−41	−36	−32	–
TRX10	2690	−36	−39	−21	−28	−32	−40	−42	−39	−37	−32	−29	–

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 6. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0		190	4090		2140.0
2	1880.0		80	3840		1960.0
4	1732.0	+20	400	3864	−15	2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 7. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0		1760.0		2140.0
2	1880.0		1800.0		1960.0
4	1732.0	+20	1332.0	−15	2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Figure 4. 3rd Order Intermodulation Test Setup

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Table 8. Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	–	–	–	–	–	–
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
  SSC = Sequence start command   DA = Data/address frame bits   BC = Byte count (# of consecutive addresses)
  C = Command frame bits   BPC = Bus park cycle
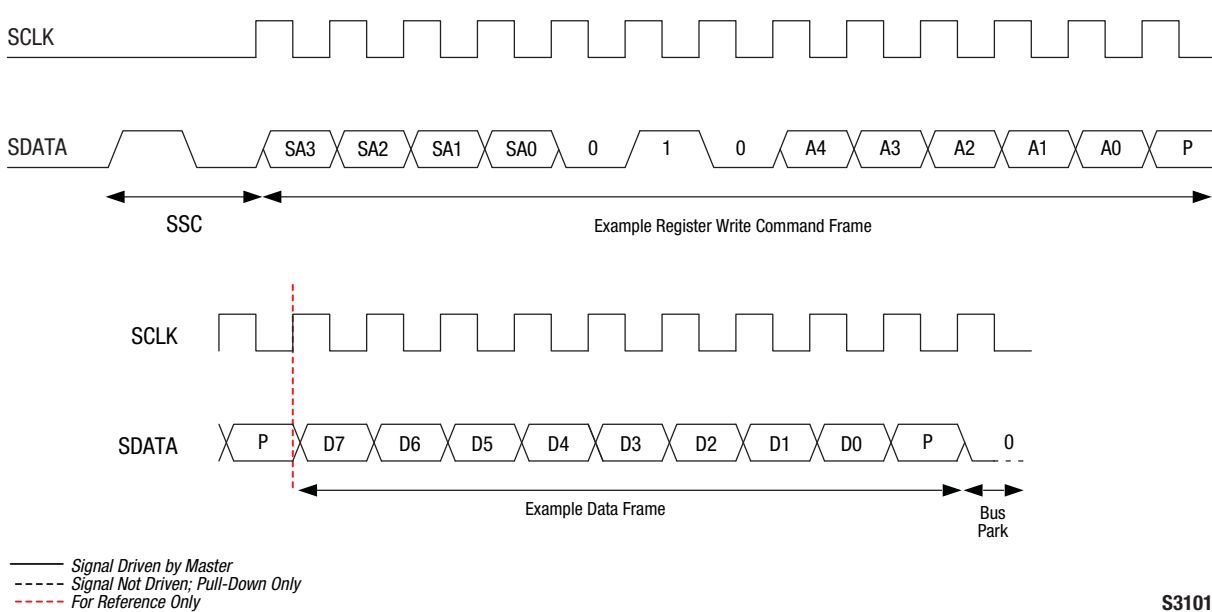
Figure 5. Register Write Command Timing Diagram
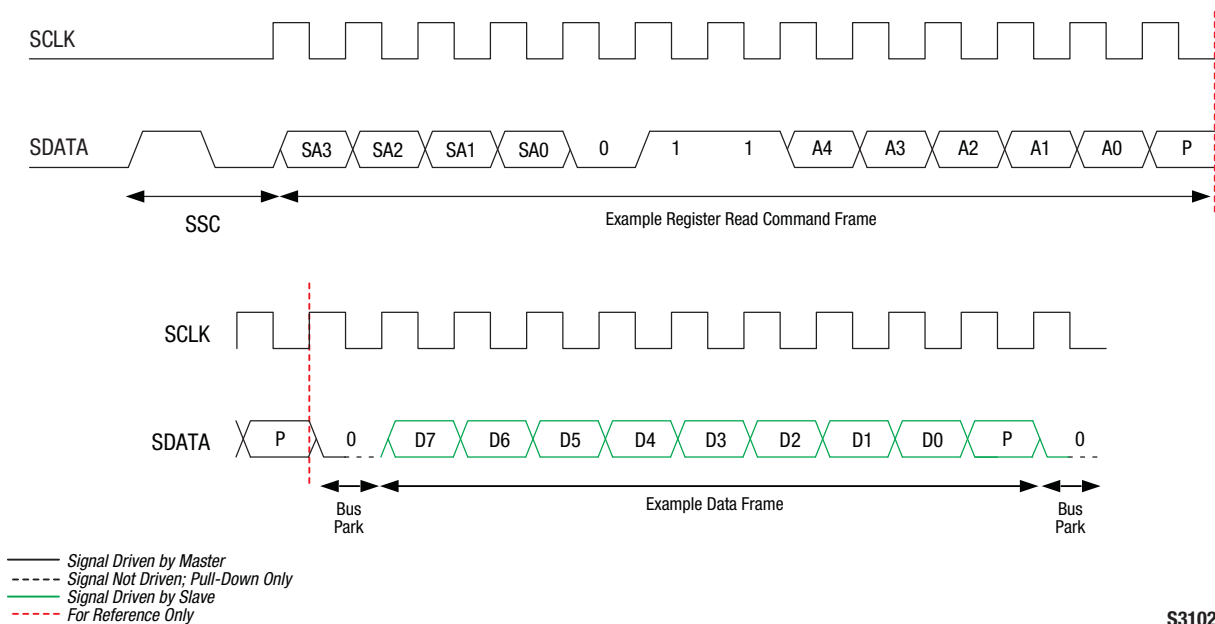
Figure 6. Register Read Command Timing Diagram

Table 9. Register_0 Truth Table

State	Mode	Register 0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	Sleep	x	0	0	0	0	0	0	0
2	LTX	x	0	0	0	1	0	1	0
3	HTX	x	0	0	0	1	0	0	0
4	TRX1	x	0	0	0	0	1	0	0
5	TRX2	x	0	0	0	0	1	0	1
6	TRX3	x	0	0	0	0	1	1	0
7	TRX4	x	0	0	0	0	1	1	1
8	TRX5	x	0	0	0	1	0	0	1
9	TRX6	x	0	0	0	1	0	1	1
10	TRX7	x	0	0	0	1	1	0	0
11	TRX8	x	0	0	0	0	0	0	1
12	TRX9	x	0	0	0	0	0	1	0
13	TRX10	x	0	0	0	0	0	1	1
14	TRX3 + TRX4	x	0	0	0	1	1	0	1
15	TRX5 + TRX10	x	0	0	0	1	1	1	0
16	Warmup (optional)	x	1	1	1	1	1	1	1

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Table 10. Register Description and Programming (1 of 2)

Register		Parameter	Description	Default (Binary)
Name	**Address (Hex)**			
Register_0	0000	MODE_CTRL	Bits[7:0]: Switch control. See Table 8 for logic	–
RFFE_STATUS	001A	SOFTWARE RESET	Bit[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error = 1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the *MIPI Alliance Specification*) or GSID.	0
GROUP_SID	001B	Reserved	Bits[7:4]: Reserved	0000
		GSID	Bits[3:0]: Group slave ID	0000

Table 10. Register Description and Programming (2 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
PM_TRIG (Note 1)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	00
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers (unsupported).	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers (unsupported).	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	01000001
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read-only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read-only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1011

Note 1: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device can be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register is immediately written to the destination register at the conclusion of the RFFE command sequence where the data is written.

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Evaluation Board Description

The SKY13455-31 Evaluation Board is used to test the performance of the SKY13455-31 SP12T Switch. An Evaluation Board schematic diagram is provided in Figure 7. A recommended ESD protection circuit diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9.

Package Dimensions

The PCB layout footprint for the SKY13455-31 is provided in Figure 10. Typical case markings are shown in Figure 11. Package dimensions for the 22-pin MCM are shown in Figure 12, and tape and reel dimensions are provided in Figure 13.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13455-31 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.
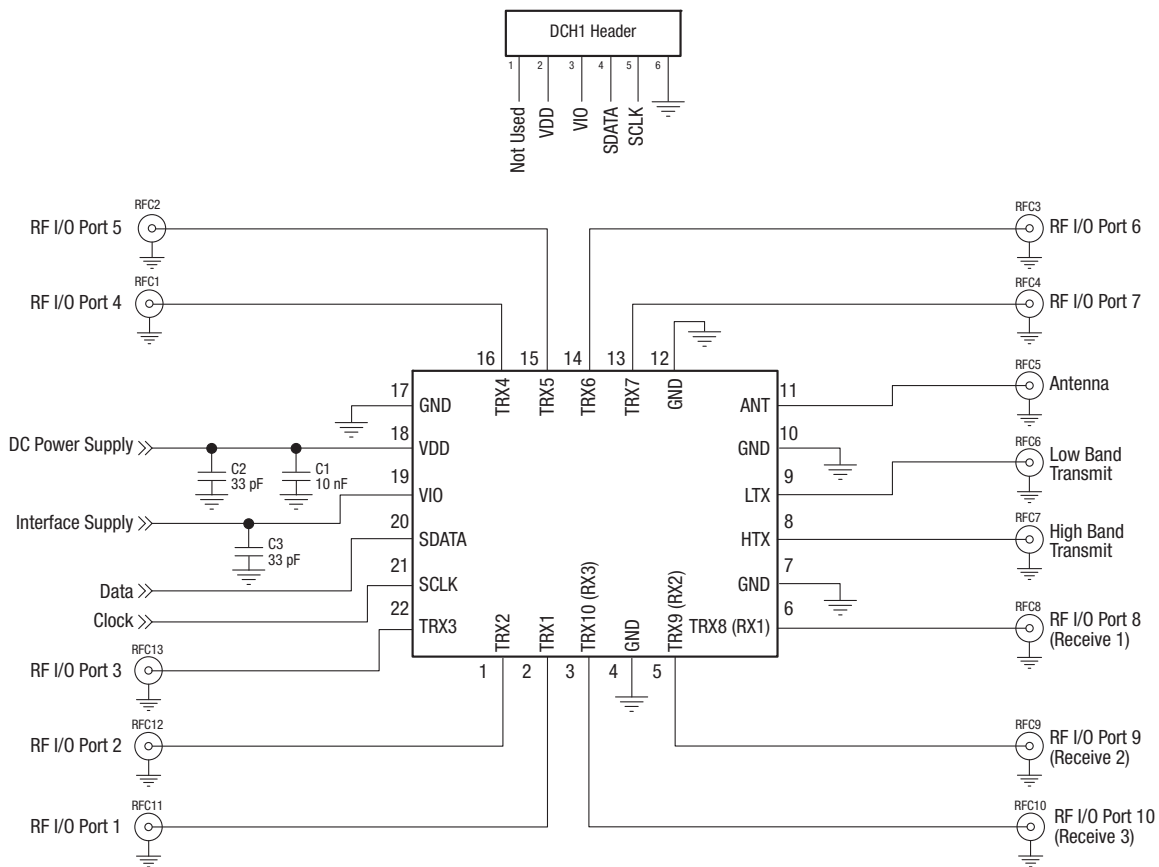
Figure 7. SKY13455-31 Evaluation Board Schematic
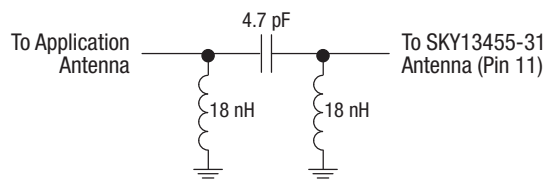
ESD Circuit 1
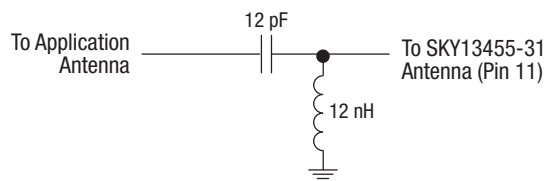
ESD Circuit 2

S3578

Figure 8. SKY13455-31 Recommended ESD Protection Circuits
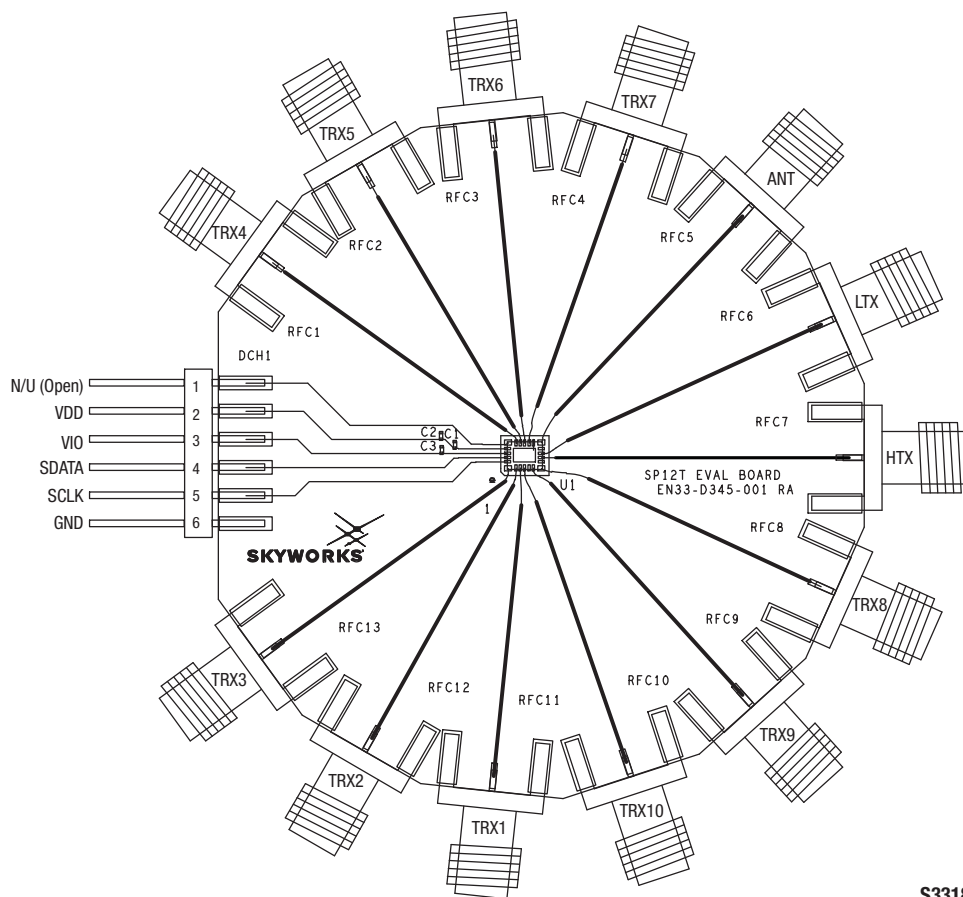
S3318

Figure 9. SKY13455-31 Evaluation Board Assembly Diagram

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Stencil Aperture
Top View

Stencil aperture size for center ground pad should be 80 to 100% (by area) of the solder mask opening.

Metallization
Top View

Thermal via array Ø0.3 mm on 0.6 mm pitch will improve thermal performance.
NOTE: thermal vias should be tented with solder mask, 30-35 μm Cu plating recommended.

Solder Mask Opening
Top View

Opening size of 60 to 100% of exposed center opening shown

All dimensions are in millimeters

S3319

Figure 10. SKY13455-31 PCB Layout Footprint

Pin 1
Indicator

Skyworks Part #

S455

Lot #

XXXX

Date Code:
(YY = Calendar Year
WW = Week)

YYWW
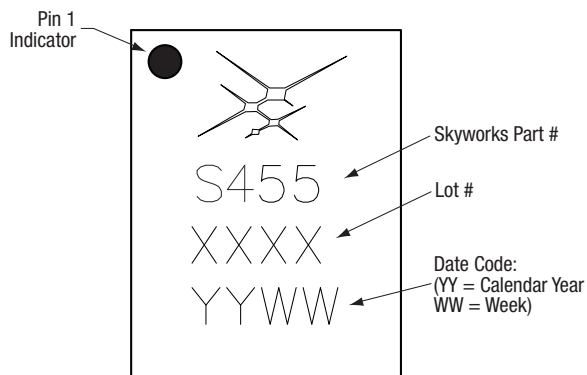
**Figure 11. Typical Part Markings
(Top View)**

Top View

Side View

Bottom View

Detail A
Pad
Scale: 2X
4X This Rotation
4X Rotated 180°
5X Rotated 270°
5X Rotated 90°

Detail B
Pad
Scale: 2X
1X This Rotation
1X Rotated 180°

Detail C
Pad
Scale: 2X
1X This Rotation
1X Rotated 180°

Detail D
Full Scale
1X This Rotation
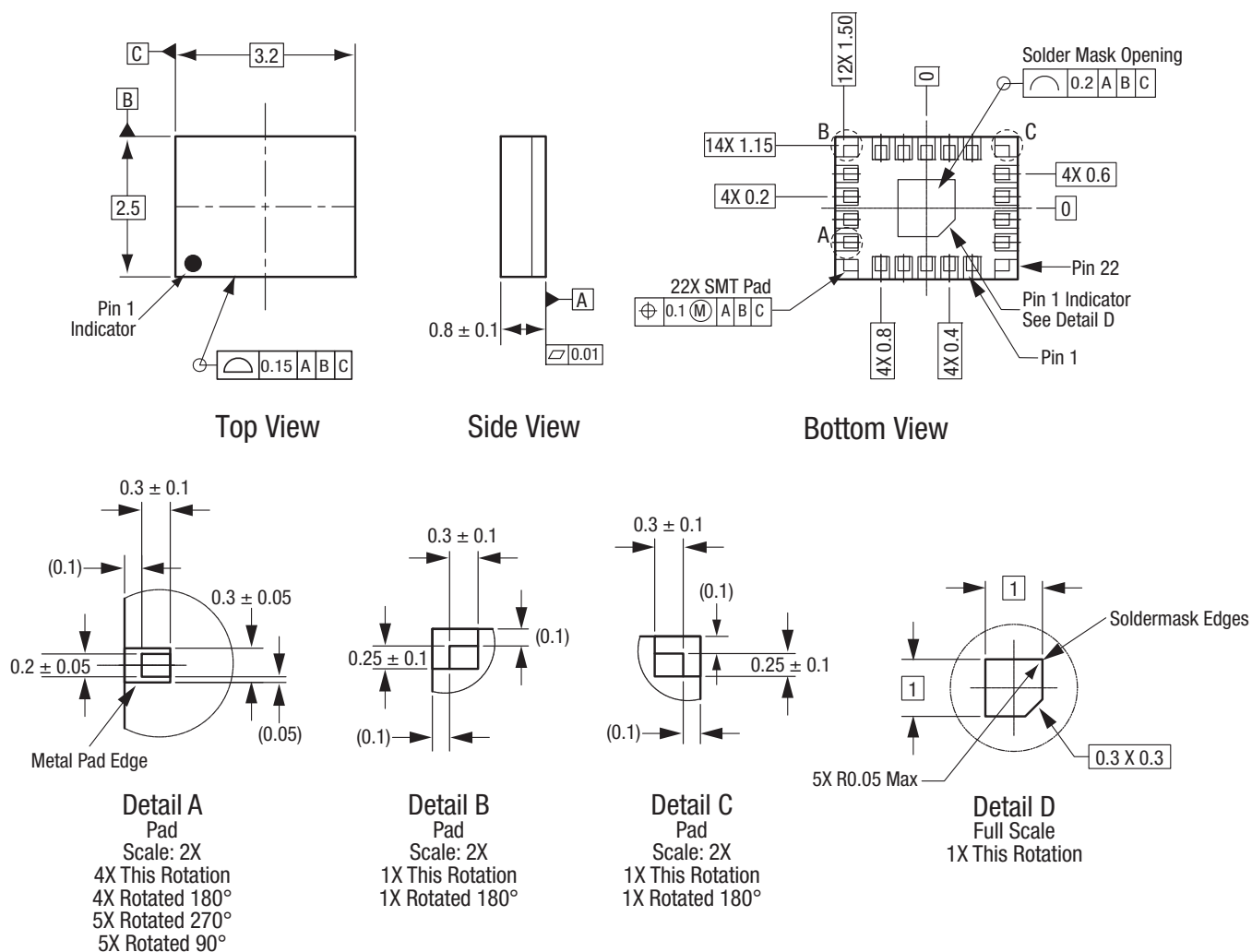
All measurements are in millimeters

Dimensioning and tolerancing according to ASME Y14.5M-1994   **S3579**

Figure 12. SKY13455-31 22-Pin MCM Package Dimensions

Notes:
1. Carrier tape: black conductive polycarbonate.
2. Cover tape material: transparent conductive material.
3. ESD-surface resistivity is ≤1 x 10^{10} Ohms/square per EIA, JEDEC TNR Specification.
4. 10 sprocket hole pitch cumulative tolerance: ±0.20 mm
5. Ao and Bo measusred on plane 0.30 mm above the bottom of the pocket.
6. All measurements are in millimeters.

S2686

Figure 13. SKY13455-31 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13455-31 0.4-2.7 GHz SP12T Switch with MIPI RFFE Interface	SKY13455-31	SKY13455-31-EVB

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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