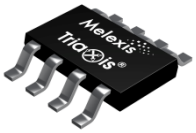
MLX90333 Position Sensor

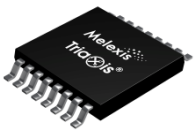
Datasheet

Features and Benefits

- Absolute 3D Position Sensor
- Simple & Robust Magnetic Design
- Tria⊗is® Hall Technology
- Programmable Linear Transfer Characteristics (Alpha, Beta)
- Selectable Analog (Ratiometric), PWM, Serial Protocol
- 12 bit Angular Resolution - 10 bit Angular Thermal Accuracy
- 40 bit ID Number
- Single Die – SOIC-8 Package RoHS Compliant
- Dual Die (Full Redundant) – TSSOP-16 Package RoHS Compliant



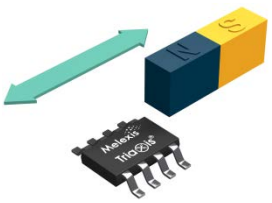
SOIC-8

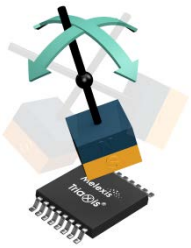


TSSOP-16

Applications

- 3D Position Sensor
- Joystick
- 4-Way Scroll Key
- Joypad
- Man Machine Interface Device
- Linear Position Sensor





Description

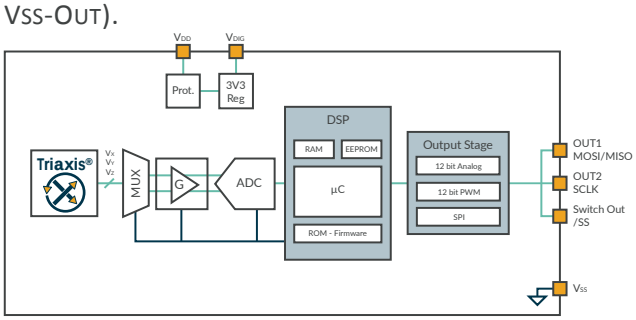
The MLX90333 is a Tria⊗is® Position Sensor able to sense any magnet moving in its surrounding through the measurement and the processing of the 3 spatial components of the magnetic flux density vector (i.e. B_X, B_Y and B_Z).

The horizontal components (B_X and B_Y) are sensed thanks to an Integrated Magneto-Concentrator (IMC) while the vertical component (B_Z) is sensed through conventional Hall plate.

The MLX90333 features a contactless position sensor mode suitable for rotary position sensor (through-shaft magnet), linear stroke position sensor (magnet displacement parallel to the device surface) and for 3D/"Joystick" position sensor.

The processed position information is ultimately reported as a ratiometric analog output or as PWM (Pulse-Width Modulation) signal. In case of 3D/"Joystick" mode, the device features 2 independent outputs. A 3-pin SPI (serial interface) mode is also available to transfer the position information to a host-controller.

The output transfer characteristic is fully programmable (e.g. offset, gain, clamping levels, linearity, thermal drift, filtering, range...) to match any specific requirement through end-of-line calibration. The Melexis programming unit PTC-04 communicates and calibrates the device exclusively through the connector terminals (VDD-VSS-OUT).



Melexis

INSPIRED ENGINEERING

Contents

1. Ordering Information

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90333	S	DC	BCH-000	RE
MLX90333	E	DC	BCH-000	RE
MLX90333	E	DC	BCH-100	RE
MLX90333	E	DC	BCT-000	RE
MLX90333	K	DC	BCH-000	RE
MLX90333	K	DC	BCH-100	RE
MLX90333	K	DC	BCT-000	RE
MLX90333	L	DC	BCH-000	RE
MLX90333	L	DC	BCH-100	RE
MLX90333	L	DC	BCT-000	RE
MLX90333	E	GO	BCH-000	RE
MLX90333	E	GO	BCH-100	RE
MLX90333	E	GO	BCT-000	RE
MLX90333	K	GO	BCH-000	RE
MLX90333	K	GO	BCH-100	RE
MLX90333	K	GO	BCT-000	RE
MLX90333	L	GO	BCH-000	RE
MLX90333	L	GO	BCH-100	RE
MLX90333	L	GO	BCT-000	RE

Legend:

Temperature Code:	S: from -20 Deg.C to 85 Deg.C E: from -40 Deg.C to 85 Deg.C K: from -40 Deg.C to 125 Deg.C L: from -40 Deg.C to 150 Deg.C
Package Code:	"DC" for SOIC-8 package "GO" for TSSOP-16 package (dual die)
Option Code:	AAA-xxx: die version xxx-000: Standard xxx-100: SPI
Packing Form:	"RE" for Reel "TU" for Tube
Ordering Example:	MLX90333LGO-BCH-000-RE

Table 1 - Legend

2. Functional Diagram

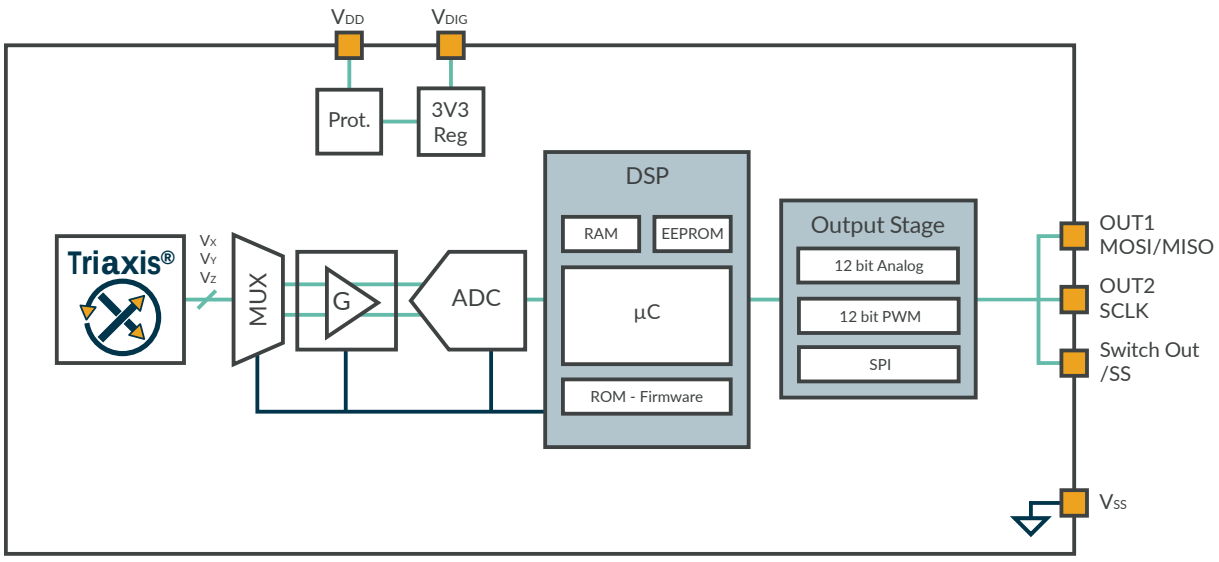


Figure 1 – Block Diagram

3. Glossary of Terms

Gauss (G), Tesla (T)	Units for the magnetic flux density - 1 mT = 10 G
TC	**T**emperature **C**oefficient (in ppm/Deg.C.)
NC	**N**ot **C**onnected
PWM	**P**ulse **W**idth **M**odulation
%DC	**D**uty **C**ycle of the output signal i.e. T_{ON} /(T_{ON} + T_{OFF})
ADC	**A**nalog-to-**D**igital **C**onverter
DAC	**D**igital-to-**A**nalog **C**onverter
LSB	**L**east **S**ignificant **B**it
MSB	**M**ost **S**ignificant **B**it
DNL	**D**ifferential **N**on-**L**inearity
INL	**I**ntegral **N**on-**L**inearity
RISC	**R**educed **I**nstruction **S**et **C**omputer
ASP	**A**nalog **S**ignal **P**rocessing
DSP	**D**igital **S**ignal **P**rocessing
ATAN	Trigonometric function: arctangent (or inverse tangent)
IMC	**I**ntegrated **M**agneto-**C**oncentrator (IMC®)
CoRDiC	**Co**ordinate **R**otation **Di**gital **C**omputer (i.e. iterative rectangular-to-polar transform)
EMC	**E**lectro-**M**agnetic **C**ompatibility

Table 2 – Glossary of Terms

4. Pinout [1]

PIN	SOIC-8		TSSOP-16	
	Analog / PWM	Serial Protocol	Analog / PWM	Serial Protocol
1	VDD	VDD	V_{DIG_1}	V_{DIG_1}
2	Test 0	Test 0	V_{SS_1} ($Ground_1$)	V_{SS_1} ($Ground_1$)
3	Not Used	/SS	V_{DD_1}	V_{DD_1}
4	OUT2	SCLK	$Test\ 0_1$	$Test\ 0_1$
5	OUT1	MOSI / MISO	Not Used	$/SS_2$
6	Test 1	Test 1	$OUT2_2$	$SCLK_2$
7	VDIG	VDIG	$OUT1_2$	$MOSI_2$ / $MISO_2$
8	VSS (Ground)	VSS (Ground)	$Test\ 1_2$	$Test\ 1_2$
9			V_{DIG_2}	V_{DIG_2}
10			V_{SS_2} ($Ground_2$)	V_{SS_2} ($Ground_2$)
11			V_{DD_2}	V_{DD_2}
12			$Test\ 0_2$	$Test\ 0_2$
13			Not Used	$/SS_1$
14			$OUT2_1$	$SCLK_1$
15			$OUT1_1$	$MOSI_1$ / $MISO_1$
16			$Test\ 1_1$	$Test\ 1_1$

For optimal EMC behavior, it is recommended to connect the unused pins (Not Used and Test) to the Ground (see section 16).

[1] *See Section 13.1 for OUT1 and OUT2 configuration*

5. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD} (overvoltage)	+ 20 V
Reverse Voltage Protection	- 10 V
Positive Output Voltage (Analog or PWM) Both Outputs OUT1 and OUT2	+ 10 V + 14 V (200 s max – T_A = + 25 Deg.C)
Output Current (I_{OUT})	± 30 mA
Reverse Output Voltage Both Outputs OUT1 and OUT2	- 0.3 V
Reverse Output Current Both Outputs OUT1 and OUT2	- 50 mA
Operating Ambient Temperature Range, T_A	- 40 Deg.C … + 150 Deg.C
Storage Temperature Range, T_S	- 40 Deg.C … + 150 Deg.C
Magnetic Flux Density	± 4 T

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6. Electrical Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current [2]	I_{DD}	Slow mode [3] Fast mode [3]		8.5 13.5	11 16	mA mA
POR Level	V_{DD} POR	Supply Under Voltage	2	2.7	3	V
Output Current Both Outputs OUT1 and OUT2	I_{OUT}	Analog Output mode PWM Output mode	-8 -20		8 20	mA mA
Output Short Circuit Current Both Outputs OUT1 and OUT2	I_{short}	V_{OUT} = 0 V V_{OUT} = 5 V V_{OUT} = 14 V (T_A = 25 Deg.C)		12 12 24	15 15 45	mA mA mA
Output Load Both Outputs OUT1 and OUT2	R_L	Pull-down to Ground Pull-up to 5V [4]	1 1	10 10	∞ [5] ∞ [5]	kΩ kΩ
Analog Saturation Output Level Both Outputs OUT1 and OUT2	Vsat_lo	Pull-up load $R_L \geq$ 10 kΩ			3	%V_{DD}
	Vsat_hi	Pull-down load $R_L \geq$ 5 kΩ	96			%V_{DD}
Digital Saturation Output Level Both Outputs OUT1 and OUT2	VsatD_lo	Pull-up Low Side $R_L \geq$ 10 kΩ Push-Pull (IOUT = -20mA)			1.5	%V_{DD}
	VsatD_hi	Push-Pull (IOUT = 20mA)	97			%V_{DD}
Active Diagnostic Output Level Both Outputs OUT1 and OUT2	Diag_lo	Pull-down load $R_L \geq$ 5 kΩ Pull-up load $R_L \geq$ 10 kΩ			1 1.5	%V_{DD} %V_{DD}
	Diag_hi	Pull-down load $R_L \geq$ 5 kΩ Pull-up load $R_L \geq$ 5 kΩ	96 98			%V_{DD} %V_{DD}
Passive Diagnostic Output Level	BVSSPD	Broken VSS & Pull-down load $R_L \leq$ 10 kΩ			4[6]	%V_{DD}

[2] Supply current per silicon die. Dual die version will consume twice the current
[3] See section 13.5.1 for details concerning Slow and Fast mode
[4] Applicable for output in Analog and PWM (Open-Drain) mode
[5] $R_L < \infty$ for output in PWM mode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Both Outputs OUT1 and OUT2 (Broken Track Diagnostic) [6]	BVSSPU	Broken VSS & Pull-up load $R_L \geq 1$ kΩ	99	100		%VDD
	BVDDPD	Broken VDD & Pull-down load $R_L \geq 1$ kΩ		0	1	%VDD
	BVDDPU	Broken VDD & Pull-up load to 5 V	No Broken Track diagnostic			%VDD
Clamped Output Level [7] Both Outputs OUT1 and OUT2	Clamp_lo	Programmable	0		100	%VDD
	Clamp_hi	Programmable	0		100	%VDD

As an illustration of the previous table, the MLX90333 fits the typical classification of the output span described on the Figure 2.

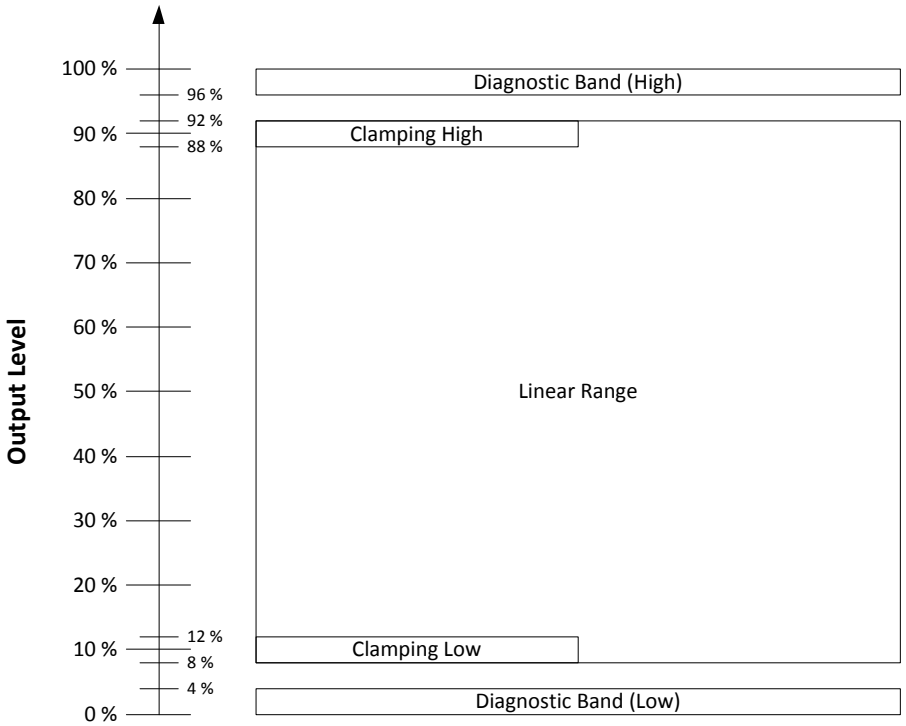


Figure 2 – Output Span Classification

[6] *For detailed information, see also section 14*

[7] *Clamping levels need to be considered vs the saturation of the output stage (see Vsat_lo and Vsat_hi)*

7. Isolation Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L). Only valid for the package code GO i.e. dual die version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Resistance		Between dice	4			MΩ

8. Timing Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck	Slow mode [8] Fast mode [8]		7 20		MHz MHz
Sampling Rate		Slow mode [8] Fast mode [8]		600 200	1000 330	µs µs
Step Response Time	Ts	Slow mode [8], Filter = 5 [9] Fast mode [8], Filter = 0 [9]		 400	4 600	ms µs
Watchdog	Wd	See section 14			5	ms
Start-up Cycle	Tsu	Slow and Fast mode [8]			15	ms
Analog Output Slew Rate		C_{OUT} = 42 nF C_{OUT} = 100 nF		200 100		V/ms V/ms
PWM Frequency	F_{PWM}	PWM Output Enabled	100		1000	Hz
Digital Output Rise Time Both Outputs OUT1 and OUT2		Mode 5 – 10 nF, R_L = 10 kΩ Mode 7 – 10 nF, R_L = 10 kΩ		120 2.2		µs µs
Digital Output Fall Time Both Outputs OUT1 and OUT2		Mode 5 – 10 nF, R_L = 10 kΩ Mode 7 – 10 nF, R_L = 10 kΩ		1.8 1.9		µs µs

[8] *See section 13.5.1 for details concerning Slow and Fast mode*
[9] *See section 13.6 for details concerning Filter parameter*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Maximum Field amplitude Change [10] (%) vs. Field Frequency (Hz)		**AGC 90%** [11]				
		Slow mode [8]				
		Field Freq > 40Hz	-10		10	%
		Field Freq = 20Hz	-30		30	%
		Fast mode [8]				
		Field Freq > 150Hz	-12		12	%
		Field Freq = 50Hz	-30		30	%
		AGC 64% (MLX90333BCT only)				
		Slow mode [8]				
		Field Freq > 80Hz	-22		22	%
		Field Freq = 50Hz	-30		30	%
		Fast mode [8]				
		Field Freq > 250Hz	-30		30	%
		Field Freq = 50Hz	-60		60	%

9. Accuracy Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals X, Y and Z	R_{ADC}	Slow Mode [12]		15		bits
		Fast Mode [12]		14		bits
Offset on the Raw Signals X, Y and Z	X0, Y0, Z0	T_A = 25 Deg.C	-60		60	LSB_{15}
Mismatch on the Raw Signals X, Y and Z		T_A = 25 Deg.C				
	$SMISM_{XY}$	Between X and Y	-1		1	%
	$SMISM_{XZ}$	Between X and Z [13]	-30		30	%
	$SMISM_{YZ}$	Between Y and Z [13]	-30		30	%

[10] Ex.: Magnetic field amplitude change in case of vibration
[11] Automatic Gain Control – see Section 13.5.2 for more information
[12] 15 bits corresponds to 14 bits + sign and 14 bits corresponds to 13 bits + sign. After angular calculation, this corresponds to 0.005Deg./LSB_{15} in Low Speed Mode and 0.01Deg./LSB_{14} in High Speed.
[13] The mismatch between X and Z (Y and Z) can be reduced through the calibration of the 2 parameters k_z and k_t as described in the formulas page 32 in order to take into account the IC mismatch and system tolerances (magnetic and mechanical).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Angle Phase Error		T_A = 25 Deg.C				
	$ORTH_{XY}$	Between X and Y	-0.3		0.3	Deg.
	$ORTH_{XZ}$	Between X and Z	-10		10	Deg.
	$ORTH_{YZ}$	Between Y and Z	-10		10	Deg.
Thermal Offset Drift #1 on the Raw Signals X, Y and Z [14]		Thermal Offset Drift at the DSP input (excl. DAC and output stage)				
		Temperature suffix S, E and K	-60		60	LSB_{15}
		Temperature suffix L	-90		90	LSB_{15}
Thermal Offset Drift #2 (to be considered only for the analog output mode)		Thermal Offset Drift of the DAC and Output Stage				
		Temperature suffix S, E and K	-0.3		0.3	%VDD
		Temperature suffix L	-0.4		0.4	%VDD
Thermal Drift of Sensitivity Mismatch [15]	$\Delta SMISM_{XY}$	Temperature suffix S, E and K	-0.3		0.3	%
		Temperature suffix L	-0.5		0.5	%
	$\Delta SMISM_{XZ}$	Temperature suffix S, E and K	-1		1	%
	$\Delta SMISM_{YZ}$	Temperature suffix L	-1.5		1.5	%
Analog Output Resolution	R_{DAC}	12 bits DAC (Theoretical – Noise free)		0.025		%VDD /LSB
		INL	-4		4	LSB
		DNL	-1		1	LSB
Output stage Noise		Clamped Output		0.05		%VDD
Noise pk-pk [16]		Gain = 14, Slow mode, Filter = 5		5	10	LSB_{15}
		Gain = 14, Fast mode, Filter = 0		10	20	LSB_{15}
Ratiometry Error			-0.1	0	0.1	%VDD
PWM Output Resolution	R_{PWM}	12 bits (Theoretical – Jitter free)		0.025		%DC/ LSB

[14] For instance, Thermal Offset Drift #1 equal ± 60LSB_{15} yields to max. ± 0.3 Deg. angular error for the computed angular information (output of the DSP). See Front End Application Note for more details. This is only valid if automatic gain is set (See section 13.5.2)

[15] For instance, Thermal Drift of Sensitivity Mismatch equal ± 0.4% yields to max. ± 0.1 Deg. angular error for the computed angular information (output of the DSP). See Front End Application Note for more details.

[16] The application diagram used is described in the recommended wiring. For detailed information, refer to section Filter in application mode (Section 13.6).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Jitter [17]	J_{PWM}	Gain = 11, F_{PWM} = 250 Hz – 800Hz			5	LSB_{12}
Serial Protocol Output Resolution	R_{SP}	Theoretical – Jitter free		16		bits

10. Magnetic Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density	B_X, B_Y [18]		20	50	70 [19]	mT
Magnetic Flux Density	B_Z [18]		24		140	mT
IMC Gain in X and Y [20]	$GainIMC_{XY}$		1.2	1.4	1.8	
IMC Gain in Z [20]	$GainIMC_Z$		1.1		1.3	
k factor	k	$GainIMC_{XY}$ / $GainIMC_Z$	1	1.2	1.5	
Magnet Temperature Coefficient	TCm		-2400		0	ppm/ Deg.C

11. CPU & Memory Specification

The DSP is based on a 16 bit RISC µController. This CPU provides 5 MIPS while running at 20 MHz.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				10		KB
RAM				256		B
EEPROM				128		B

[17] Jitter is defined by ± 3 σ for 1000 successive acquisitions and the slope of the transfer curve is 100%DC/360 Deg.
[18] The condition must be fulfilled for at least one field B_X, B_Y or B_Z
[19] Above 70 mT, the IMC starts saturating yielding to an increase of the linearity error.
[20] This is the magnetic gain linked to the Integrated Magneto Concentrator structure. This is the overall variation. Within one lot, the part to part variation is typically ± 10% versus the average value of the IMC gain of that lot.

12. End-User Programmable Items

Parameter	Comments	Default Values			
		BCH STD/IP1	BCH SPI	BCT STD/IP1	# bit
MAINMODE	Select Outputs Configuration	0	0	0	2
Outputs Mode	Output stages mode	2	N/A	2	3
PWMPOL1	PWM Polarity (OUT1)	0	N/A	0	1
PWMPOL2	PWM Polarity (OUT2)	0	N/A	0	1
PWM_Freq	PWM Frequency	1000h	N/A	1000h	16
3-Points	4 segments transfer curve for single angle output	0	0	0	1
ALPHA_POL	Revert the Sign of Alpha	0	0	0	1
ALPHA_MOD180	Modulo Operation (180 Deg) on Alpha	1	1	1	1
ALPHA_DP	Alpha Discontinuity Point	0	0	0	8
ALPHA_DEADZONE	Alpha Dead Zone	0	0	0	6
ALPHA_S0	Alpha Initial Slope	4000h	4000h	4000h	16
ALPHA_X	Alpha X Coordinate	4000h	4000h	4000h	16
ALPHA_Y	Alpha Y Coordinate	8000h	8000h	8000h	16
ALPHA_S1	Alpha S1 Slope	4000h	4000h	4000h	16
BETA_POL	Revert the Sign of Beta	0	0	0	1
BETA_MOD180	Modulo Operation (180 Deg) on Beta	1	1	1	1
BETA_DP	Beta Discontinuity Point	0	0	0	6
BETA_DEADZONE	Beta Dead Zone	0	0	0	8
BETA_S0	Beta Initial Slope	4000h	4000h	4000h	16
BETA_X	Beta X Coordinate	4000h	4000h	4000h	16
BETA_Y	Beta Y Coordinate	8000h	8000h	8000h	16
BETA_S1	Beta S1 Slope	4000h	4000h	4000h	16
CLAMP_LOW	Clamping Low	0%	0%	0%	16
CLAMP_HIGH	Clamping High	100%	100%	100%	16

Parameter	Comments	Default Values			
		BCH STD/IP1	BCH SPI	BCT STD/IP1	# bit
2D		0	0	0	1
XYZ	SPI Only	0	0	0	1
KZ		B3h	B3h		8
KT [21]		80h	80h	N/A	8
FIELDTHRES_LOW		0h	0h	0h	8
FIELDTHRES_HIGH		0h	0h	0h	8
DERIVGAIN		40h	40h	40h	8
FILTER		3	0	3	8
FILTER A1	Filter coefficient A1 for FILTER=6	6600h	6600h	6600h	16
FILTER A2	Filter coefficient A2 for FILTER=6	2A00h	2A00h	2A00h	16
FILTERFIRST		0	0	0	1
FHYST		0	0	0	8
MLXID1 / MLXID2 / MLXID3 [22]		MLX	MLX	MLX	16
CUSTID1		1	1	1	16
CUSTID2		17d [23]	37d	38d	16
CUSTD3		MLX	MLX	MLX	16
HIGHSPEED		0	0	0	1
GAINMIN		0	0	0	8
GAINMAX		41d	41d	41d	8
EEHAMHOLE		3131h	0h	3131h	16
RESONFAULT	Diagnostic mode	1h	N/A	0h	2
MLXLOCK		0h	0h	0h	1

[21] Only applicable for MLX90333BCH
[22] MLXIDs parameters contain unique ID programmed by Melexis to guarantee full part traceability
[23] CUSTID2 might also be 29d for MLX90333SDC–BCH–000

Parameter	Comments	Default Values			
		BCH STD/IP1	BCH SPI	BCT STD/IP1	# bit
LOCK		0h	1h	0h	1
Parameters for MLX90333xxx-BCT only					
AGCRADIUSTARGET [24]	Define Gain target 64% / 90% ADC	N/A	N/A	0	1
SWTHRES	Angle Trigger level for switch on OUT2	N/A	N/A	FFFFh	16
SWLOW	Switch Low level output on OUT2	N/A	N/A	40h	8
SWHIGH	Switch High level output on OUT2	N/A	N/A	FFh	8
SWHYST	Switch hysteresis	N/A	N/A	0	8
CodePWMLATCH	Enable synchronized % DC update	N/A	N/A	1	1
OUT1DIAG	Active Diagnostic Output 1 behavior	N/A	N/A	0	1
OUT2DIAG	Active Diagnostic Output 2 behavior	N/A	N/A	0	1
CodeKTALPHA	"Joystick" ALPHA angle correction parameter	N/A	N/A	80h	8
CodeKTBETA	"Joystick" BETA angle correction parameter	N/A	N/A	80h	8
CodeORTHZXALPHA	Front-end "Joystick" angle correction parameter	N/A	N/A	0	8
CodeORTHZYALPHA	Front-end "Joystick" angle correction parameter	N/A	N/A	0	8
CodeORTHZXBETA	Front-end "Joystick" angle correction parameter	N/A	N/A	0	8
CodeORTHZYBETA	Front-end "Joystick" angle correction parameter	N/A	N/A	0	8
CodeENHORTH	Enable enhanced Front-end "Joystick" angle correction	N/A	N/A	0	1

[24] Option to use the same ADC target as MLX90333BCH. Default value equals lowered % ADC target

13. Description of End-User Programmable Items

13.1. Output Configuration

The parameter MAINMODE defines the output stages configuration

MAINMODE	OUT1	OUT2
0	ALPHA	BETA
1	BETA	ALPHA
2	ALPHA	ALPHA DERIVATE / SWITCH [25]
3	BETA	BETA DERIVATE / SWITCH [25]

13.2. Output Mode

The MLX90333 output type is defined by the Output Mode parameter.

Parameter	Value	Description
Analog Output Mode	2	Analog Rail-to-Rail
PWM Output Mode	5 7	Low Side (NMOS) Push-Pull
Serial Protocol Output Mode	N/A	Low Side (NMOS)

13.2.1. Analog Output Mode

The Analog Output Mode is a rail-to-rail and ratiometric output with a push-pull output stage configuration allows the use of a pull-up or pull-down resistor.

[25] *Derivate = MLX90333BCH, Switch = MLX90333BCT*

13.2.2. PWM Output Mode

If one of the PWM Output mode is selected, the output signal is a digital signal with Pulse Width Modulation (PWM).

In mode 5, the output stage is an open drain NMOS transistor (low side), to be used with a pull-up resistor to VDD.

In mode 7, the output stage is a push-pull stage for which Melexis recommends the use of a pull-up resistor to VDD.

The PWM polarity of the OUT1 (OUT2) is selected by the PWMPOL1 (PWMPOL2) parameter:

- PWMPOL1 (PWMPOL2) = 0 for a low level at 100%
- PWMPOL1 (PWMPOL2) = 1 for a high level at 100%

The PWM frequency is selected by the PWM_Freq parameter.

Oscillator Mode	Pulse-Width Modulation Frequency (Hz)			
	100	200	500	1000
Low Speed	~35000	~17500	~7000	~3500
High Speed	-	~50000	~20000	~10000

Table 3 – PWM Frequency Code (based on typical main clock frequency)

For instance, in Low Speed Mode, set PWM_Freq=7000 (decimal) to set the PWM frequency around 500Hz [(26)].

13.2.3. Serial Protocol Output Mode

The MLX90333 features a digital Serial Protocol mode. The MLX90333 is configured as a Slave node. The frame layer type is defined by the parameter XYZ as described in the next table.

Parameter	Value	Description
XYZ	0	Regular SPI Frame Alpha, Beta
	1	X, Y, Z Frame

See the dedicated Serial Protocol section for a full description (Section 15).

[26] *In order to compensate the lot to lot variation of the main clock frequency (Ck), Melexis strongly recommends trimming the PWM frequency during EOL programming (see the PTC-04 documentation).*

13.2.4. Switch Out

Parameter	Value	Unit
SWTHRES	0 … 100	%
SWHYST	0 … 0.39	%
SWLOW	0 … 100	%
SWHIGH	0 … 100	%

The output level on OUT2 is changed from SWLOW to SWHIGH when the output value is greater than the value stored in the SWTHRES parameter.

The SWHYST defines the hysteresis amplitude around the Switch point. The switch is actually activated if the digital output value is greater than SWTHRES+SWHYST. It is deactivated if the digital output value is less than SWTHRES-SWHYST.

If the Switch feature is not used in the application, the output pin needs to be connected to the ground and disabled in EEPROM.

13.3. Output Transfer Characteristic

Parameter	Value	Description
3-Points	0 1	Regular Alpha, Beta Output (2 times 2 segments) Alpha (or Beta) Single Output (1 time 4 segments)

The 3-Points parameters allow the user to use the 3-points mapping (4 segments). This mode can only be used for Mainmode equals 2 and 3.

- 3-Points = 0, the parameters list is described as bellow (Angle Alpha and Beta):

Parameter	Value	Unit
ALPHA_POL BETA_POL	0, 1	
ALPHA_MOD180 BETA_MOD180	0, 1	
ALPHA_DP BETA_DP	0 … 359.9999	Deg
ALPHA_X BETA_X	0 … 359.9999	Deg
ALPHA_Y BETA_Y	0 … 100	%

Parameter	Value	Unit
ALPHA_S0 ALPHA_S1 BETA_S0 BETA_S1	0 … 17	%/Deg
CLAMP_LOW	0 … 100	%
CLAMP_HIGH	0 … 100	%
ALPHA_DEADZONE BETA_DEADZONE	0 … 359.9999	Deg

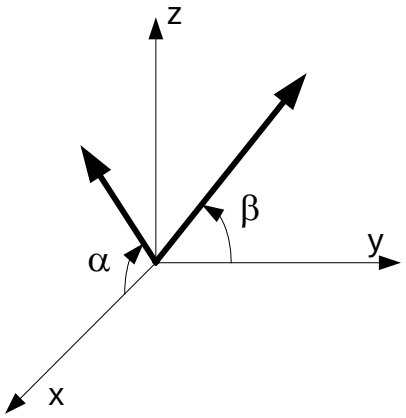
- 3-Points = 1, the parameters list is described as bellow (Angle Alpha or Beta):

Parameter	Value	Unit
ALPHA_POL	0 → CCW 1 → CW	
DP	0 … 359.9999	Deg
LNR_A_X LNR_B_X LNR_C_X	0 … 359.9999	Deg
LNR_A_Y LNR_B_Y LNR_C_Y	0 … 100	%
LNR_S0 LNR_A_S LNR_B_S	0 … 17	%/Deg
LNR_C_S	-17 … 0 … 17	%/Deg
CLAMP_LOW	0 … 100	%
CLAMP_HIGH	0 … 100	%
DEADZONE	0 … 359.9999	Deg

13.3.1. The Polarity and Modulo Parameters

The angle Alpha is defined as the arctangent of Z/X and Beta as the arctangent of Z/Y. It is possible to invert the polarity of these angles via the parameters ALPHA_POL and BETA_POL set to “1”.

The MLX90333 can also be insensitive to the field polarity by setting the ALPHA_MOD180/BETA_MOD180 to “1”.



13.3.2. Alpha/Beta Discontinuity Point (or Zero Degree Point)

The Discontinuity Point (DP) defines the zero point of the circle (Alpha or Beta). The discontinuity point places the origin at any location of the trigonometric circle (see Figure 5).

For a Joystick Application, Melexis recommends to set the DP to zero.

13.3.3. LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angles (Alpha and Beta) and the output signals.

The shape of the MLX90333 transfer function from the digital angle values to the output voltages is described by the drawing below (see Figure 3). Four segments can be programmed but the clamping levels are necessarily flat (3-Points = 0).

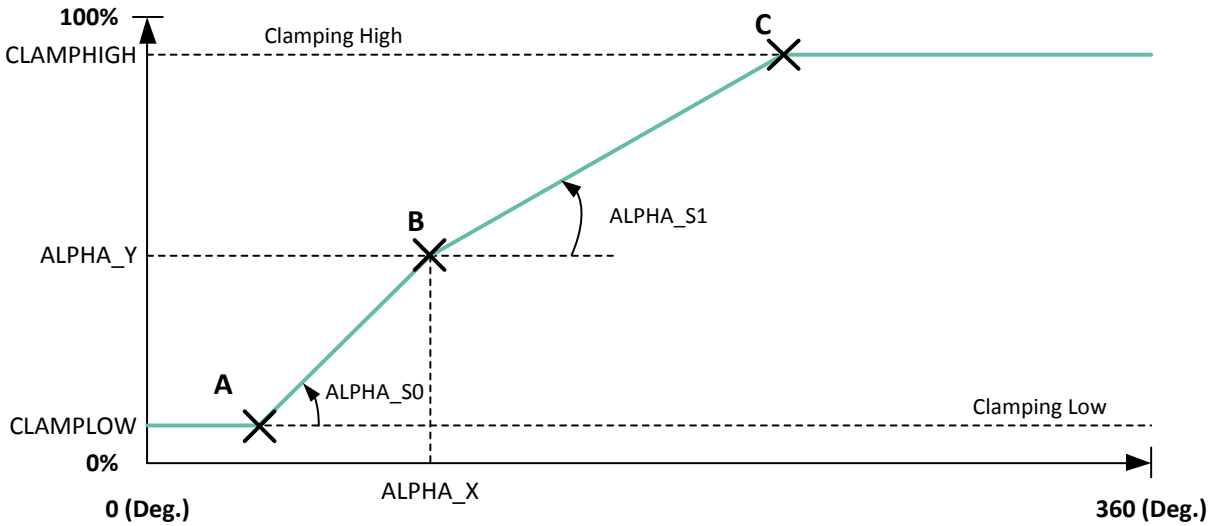


Figure 3 – Digital Angle (Alpha) Transfer Characteristic (Idem ditto for Beta)

In the case of one single angle output (3-Points = 1), the shape of the MLX90333 transfer function from the digital angle values to the output voltage is described by the drawing below (See Figure 4). Six segments can be programmed but the clamping levels are necessarily flat.

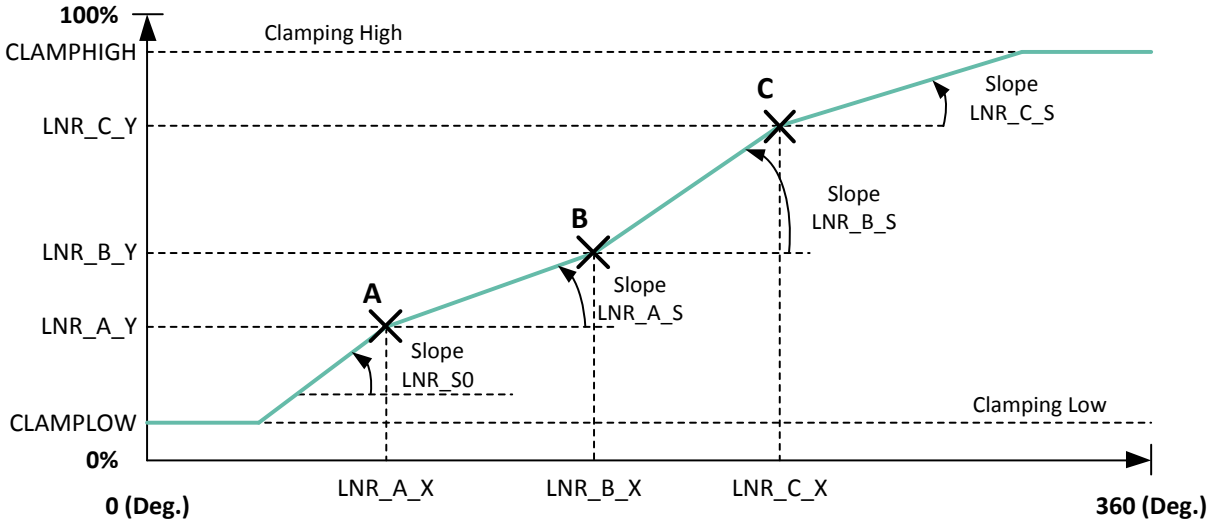


Figure 4 – Digital Angle (Alpha) Transfer Characteristic for Single Angle Output

13.3.4. CLAMPING Parameters

The clamping levels are two independent values to limit the output voltage range in normal operation. The CLAMP_LOW parameter sets the minimum output voltage level while the CLAMP_HIGH parameter sets the maximum output voltage level. Both parameters have 16 bits of adjustment. In analog mode the resolution will be limited by the D/A converter (12 bits) to 0.024%V_{DD}. In PWM mode the resolution will be 0.024%DC. In SPI mode the resolution is 14 bits or 0.022 Deg. over 360 Deg.

13.3.5. DEADZONE Parameter

The dead zone is defined as the angle window between 0 and 359.9999 Deg. (See Figure 5).

When the digital angle (Alpha or Beta) lies in this zone, the IC is in fault mode (RESONFAULT must be set to “1” – See 13.8.2).

In case of ALPHA_MOD180 (or BETA_MOD180) is not set, the angle between 180 Deg. and 360 Deg. will generate a “deadzone” fault, unless DEADZONE = 0.

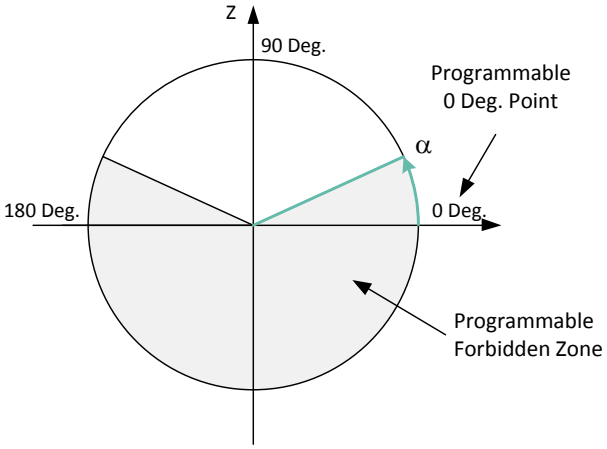


Figure 5 – Discontinuity Point and Dead Zone (Alpha - Idem ditto for Beta)

13.4. Identification

Parameter	Value	Unit
MLXID1	0 … 65535	
MLXID2	0 … 65535	
MLXID3	0 … 65535	
CUSTID1	0 … 65535	
CUSTID2	0 … 65535	
CUSTID3	0 … 65535	

Identification number: 48 bits freely useable by Customer for traceability purpose.

13.5. Sensor Front-End

Parameter	Value	Unit
HIGHSPEED	Slow mode = 0 Fast mode = 1	
GAINMIN	0 … 41	
GAINMAX	0 … 41	
FIELDTHRES_LOW	0 … 100	%
FIELDTHRES_HIGH	0 … 100	%

13.5.1. HIGHSPEED Parameter

The HIGHSPEED parameter defines the main frequency for the DSP:

- HIGHSPEED = 0 selects the Slow mode with a 7 MHz master clock.
- HIGHSPEED = 1 selects the Fast mode with a 20 MHz master clock.

For better noise performance, the Slow Mode must be enabled.

13.5.2. GAINMIN and GAINMAX Parameters

The MLX90333 features an automatic gain control (AGC) of the analog chain. The AGC loop is based on

$$Max(|V_X|, |V_Y|, |V_Z|) = |Amplitude| = Radius$$

and it targets an amplitude of 90% of the ADC input span.

In MLX90333BCT, this default target is changed to 64% but can be set to 90% by enabling the parameter AGCRADIUSTARGET.

The current gain can be read out with the programming unit PTC-04 and gives a rough indication of the applied magnetic flux density (Amplitude).

GAINMIN & GAINMAX define the boundaries within the gain setting is allowed to vary. Outside this range, the outputs are set in diagnostic low.

13.5.3. FIELDTHRES_LOW and FIELDTHRES_HIGH Parameters

The strength of the applied field is constantly calculated in a background process. The value of this field can be read out with the PTC-04 and gives a rough indication of the applied magnetic flux density (Amplitude).

FIELDTHRES_LOW & FIELDTHRES_HIGH define the boundaries within the actual field strength (Radius) is allowed to vary. Outside this range, the outputs are set in diagnostic low.

13.6. FILTER

Parameter	Value	Unit
FHYST	0 … 11; step 0.04	Deg.
FILTER	0 … 6	
FILTERFIRST	0, 1	

The MLX90333 includes 3 types of filters:

- Hysteresis Filter: programmable by the FHYST parameter
- Low Pass FIR Filters controlled with the Filter parameter
- Low Pass IIR Filter controlled with the Filter parameter and the coefficients FILTER A1 and FILTER A2

Note: if the parameter FILTERFIRST is set to “1”, the filtering is active on the digital angle. If set to “0”, the filtering is active on the output transfer function.

13.6.1. Hysteresis Filter

The FHYST parameter is a hysteresis filter. The output value of the IC is not updated when the digital step is smaller than the programmed FHYST parameter value. The output value is modified when the increment is bigger than the hysteresis. The hysteresis filter reduces therefore the resolution to a level compatible with the internal noise of the IC. The hysteresis must be programmed to a value close to the noise level.

13.6.2. FIR Filters

The MLX90333 features 6 FIR filter modes controlled with Filter = 0 … 5. The transfer function is described below:

$$y_n = \frac{1}{\sum_{i=0}^{j} a_i} \sum_{i=0}^{j} a_i x_{n-i}$$

The characteristics of the filters no 0 to 5 is given in the Table 4.

Filter No (j)	0	1	2	3	4	5
Type	Disable	Finite Impulse Response				
Coefficients a_0… a_5	N/A	110000	121000	133100	111100	122210
Title	No Filter	Extra Light		Light		
90% Response Time	1	2	3	4	4	5
99% Response Time	1	2	3	4	4	5

Filter No (j)	0	1	2	3	4	5
Efficiency RMS (dB)	0	2.9	4	4.7	5.6	6.2
Efficiency P2P (dB)	0	2.9	3.6	5.0	6.1	7.0

Table 4 – FIR Filters Selection Table

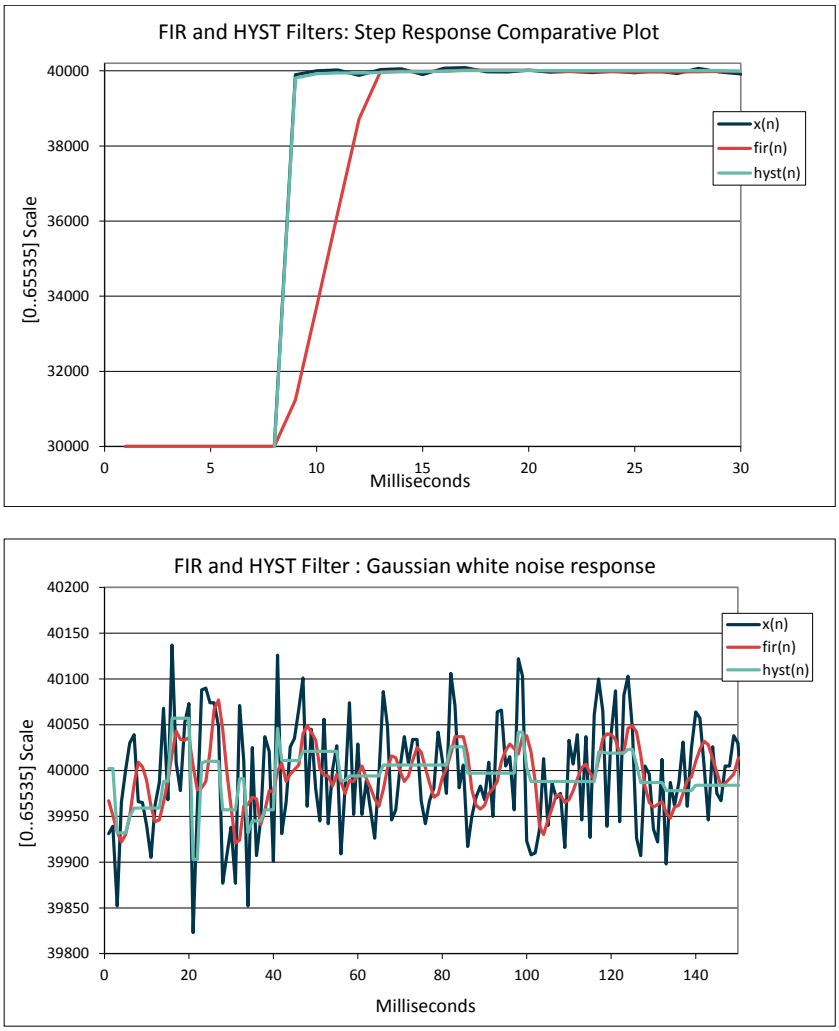


Figure 6 – Step Response and Noise Response for FIR (No 3) and FHYST = 10

13.6.3. IIR Filters

The IIR Filter is enabled with Filter = 6. The diagram of the IIR Filter implemented in the MLX90333 is given in Figure 7. Only the parameters A1 and A2 are configurable (See Table 5).

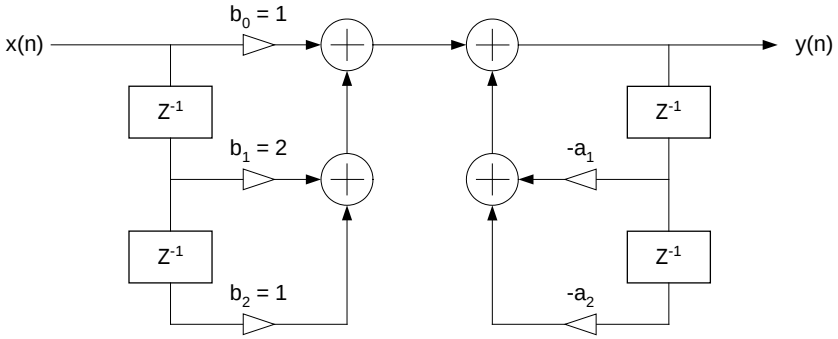


Figure 7 - IIR Diagram

Filter No	6					
Type	2nd Order Infinite Impulse Response (IIR)					
Title	Medium & Strong					
90% Response Time	11	16	26	40	52	100
Efficiency RMS (dB)	9.9	11.4	13.6	15.3	16.2	> 20
Efficiency P2P (dB)	12.9	14.6	17.1	18.8	20.0	> 20
Coefficient A1	26112	28160	29120	30208	31296	31784
Coefficient A2	10752	12288	12992	13952	14976	15412

Table 5 – IIR Filter Selection Table

The Figure 8 shows the response of the filter to a Gaussian noise with default coefficient A1 and A2.

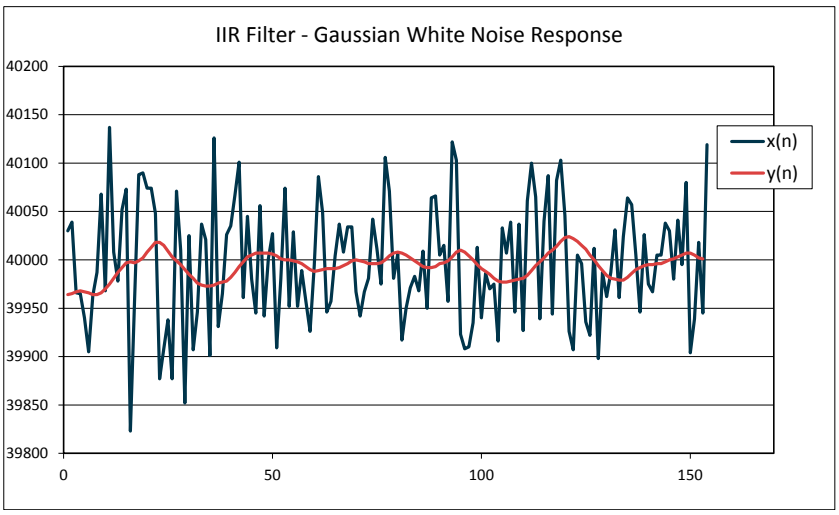


Figure 8 – Noise Response for the IIR Filter

13.7. Programmable Enhanced "Joystick' Angle Correction [27]

Parameter	Value	Unit
KTALPHA KTBETA	[0 … 200] / 128	LSB
ORTHZXALPHA ORTHZYALPHA ORTHZXBETA ORTHZYBETA	[-128 … 127] / 256	LSB
ENHORTH	Disable = 0 Enable = 1	

13.7.1. Enhanced "Joystick" Angle Formula

$$\alpha = ATAN\left(\frac{\sqrt{(k_Z V_Z)^2 + (k_t(V_Y - ORTHzy * V_z))^2}}{V_X - ORTHzx * Vz}\right)$$

$$\beta = ATAN\left(\frac{\sqrt{(k_Z V_Z)^2 + (k_t(Vx - ORTHzx * V_z))^2}}{V_y - ORTHzy * V_z}\right)$$

The enhanced "joystick" angle function is enabled by parameter ENORTH. Parameters are automatically calculated when using the MLX90333BCT/ 9 points solver to optimize the shape of Betaout vs Alphaout in accordance to the mechanical boundaries of the Joystick.

13.8. Programmable Diagnostic Settings

Parameter	Value	Unit
OUT1DIAG OUT2DIAG	DIAGLOW = 0 DIAGHIGH = 1	
RESONFAULT	Disable = 0 Enable = 1	
EEHAMHOLE	Enable = 0 Disable = 3131h	

[27] *Only Applicable for MLX90333BCT*

13.8.1. OUTxDIAG Parameter

This OUT1DIAG, OUT2DIAG parameters define the behavior of the output in case of a diagnostic situation.

13.8.2. RESONFAULT Parameter

The RESONFAULT parameter enables the soft reset when a fault is detected by the CPU when the parameter is set to “1”. It is recommended to set it to “1” to activate the self diagnostic modes (See section 14).

Note that in the User Interface (MLX90333UI), the RESONFAULT is a cluster of the following two bits, i.e. the 2 bits are both disabled or both enabled:

- DRESONFAULT: disable the reset in case of a fault.
- DOUTINFAULT: disable output in diagnostic low in case of fault.

It is recommended to set both EEPROM parameters to “0” to activate the self diagnostic modes.

13.8.3. EEHAMHOLE Parameter

The EEHAMHOLE parameter disables the CRC check and the memory recovery (Hamming code) when it is equal to 3131h. Melexis strongly recommends setting the parameter to “0” (enable memory recovery). The parameter is set automatically to “0” by the solver function “MemLock”.

13.9. Lock

Parameter	Value	Unit
MLXLOCK	0, 1	
LOCK	0, 1	

13.9.1. MLXLOCK Parameter

MLXLOCK locks all the parameters set by Melexis.

13.9.2. LOCK Parameter

LOCK locks all the parameters set by the user. Once the lock is enabled, it is not possible to change the EEPROM values. However it is still possible to read back the memory contents with the PTC-04 programmer.

Note that the lock bit should be set by the solver function “MemLock”.

14. Self Diagnostic

The MLX90333 provides numerous self-diagnostic features. Those features increase the robustness of the IC functionality as it will prevent the IC to provide erroneous output signal in case of internal or external failure modes ("fail-safe").

Fault Mode	Action	Effect on Outputs	Remark
ROM CRC Error at start up (64 words including Intelligent Watch Dog - IWD)	CPU Reset [28]	Diagnostic low [29]	All the outputs are already in Diagnostic low - (start-up)
ROM CRC Error (Operation - Background task)	Enter Endless Loop: - Progress (watchdog Acknowledge) - Set Outputs in Diagnostic low	Immediate Diagnostic low	
RAM Test Fail (Start up)	CPU Reset	Diagnostic low	All the outputs are already in Diagnostic low (start-up)
Calibration Data CRC Error (Start-Up)	Hamming Code Recovery		Start-Up Time is increased by 3 ms if successful recovery
Hamming Code Recovery Error (Start-Up)	CPU Reset	Immediate Diagnostic low	See section 13.8.3
Calibration Data CRC Error (Operation - Background)	CPU Reset	Immediate Diagnostic low	
Dead Zone Alpha Dead Zone Beta	Set Outputs in Diagnostic low. Normal Operation until the "dead zone" is left.	Immediate Diagnostic low	Immediate recovery if the "dead zone" is left
ADC Clipping (ADC Output is 0000h or 7FFFh)	Set Outputs in Diagnostic low. Normal mode and CPU Reset If recovery	Immediate Diagnostic low	

[28] CPU reset means

1. Core Reset (same as Power-On-Reset). It induces a typical start up time.

2. Periphery Reset (same as Power-On-Reset)

3. Fault Flag/Status Lost

4. The reset can be disabled by clearing the RESONFAULT bit (See 13.8.1)

[29] Refer to section 6 for the Diagnostic Output Level specifications

Fault Mode	Action	Effect on Outputs	Remark
Radius Overflow (> 100%) or Radius Underflow (< 50 %)	Set Outputs in Diagnostic low. Normal mode and CPU Reset If recovery	Immediate Diagnostic low	(50 % - 100 %) No magnet / field too high See also section 13.5.2
Field Clipping (Radius < FIELDTHRES_LOW or Radius > FIELDTHRES_HIGH)	Set Outputs in Diagnostic low. Normal mode, and CPU Reset If recovery	Immediate Diagnostic low	See also section 13.5.3
Rough Offset Clipping (RO is < 0d or > 127d)	Set Outputs in Diagnostic low. Normal mode, and CPU Reset If recovery	Immediate Diagnostic low	
Gain Clipping (GAIN < GAINMIN or GAIN > GAINMAX)	Set Outputs in Diagnostic low. Normal mode, and CPU Reset If recovery	Immediate Diagnostic low	See also section 13.5.2
DAC Monitor (Digital to Analog converter)	Set Outputs in Diagnostic low. Normal Mode with immediate recovery without CPU Reset	Immediate Diagnostic low	
ADC Monitor (Analog to Digital Converter)	Set Outputs in Diagnostic low. Normal Mode with immediate recovery without CPU Reset	Immediate Diagnostic low	ADC Inputs are Shorted
Undervoltage Mode	At Start-Up, wait Until V_{DD} > 3V. During operation, CPU Reset after 3 ms debouncing	- V_{DD} < POR level => Outputs high impedance - POR level < V_{DD} < 3 V => Outputs in Diagnostic low	
Firmware Flow Error	CPU Reset	Immediate Diagnostic low	Intelligent Watchdog (Observer)
Read/Write Access out of physical memory	CPU Reset	Immediate Diagnostic low	100% Hardware detection
Write Access to protected area (IO and RAM Words)	CPU Reset	Immediate Diagnostic low	100% Hardware detection
Unauthorized entry in “SYSTEM” Mode	CPU Reset	Immediate Diagnostic low	100% Hardware detection
V_{DD} > 7 V	Set Output High Impedance (Analog)	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High (29)	100% Hardware detection

Fault Mode	Action	Effect on Outputs	Remark
V_{DD} > 9.4 V	IC is switched off (internal supply) CPU Reset on recovery	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High	100% Hardware detection
Broken V_{SS}	CPU Reset on recovery	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High	100% Hardware detection. Pull down load ≤ 10 kΩ to meet Diag Low spec: - < 2% V_{DD} (temperature suffix S and E) - < 4% V_{DD} (temperature suffix K) - contact Melexis for temperature suffix L
Broken V_{DD}	CPU Reset on recovery	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High	No valid diagnostic for V_{PULLUP} = V_{DD}. Pull up load (≤ 10kΩ) to V_{PULLUP} > 8 V to meet Diag Hi spec > 96% V_{DD}.

15. Serial Protocol

15.1. Introduction

The MLX90333 features a digital Serial Protocol mode. The MLX90333 is configured as a Slave node. The serial protocol of the MLX90333 is a three wires protocol (/SS, SCLK, MOSI-MISO):

- /SS pin is a 5 V tolerant digital input
- SCLK pin is a 5 V tolerant digital input
- MOSI-MISO pin is a 5 V tolerant open drain digital input/output

The basic knowledge of the standard SPI specification is required for the good understanding of the present section.

15.2. SERIAL PROTOCOL Mode

- CPHA = 1 → even clock changes are used to sample the data
- CPOL = 0 → active-Hi clock

The positive going edge shifts a bit to the Slave's output stage and the negative going edge samples the bit at the Master's input stage.

15.3. MOSI (Master Out Slave In)

The Master sends a command to the Slave to get the angle information.

15.4. MISO (Master In Slave Out)

The MISO of the slave is an open-collector stage. Due to the capacitive load, a >1 kΩ pull-up is used for the recessive high level (in fast mode). Note that MOSI and MISO use the same physical pin of the MLX90333.

15.5. /SS (Slave Select)

The /SS pin enables a frame transfer (if CPHA = 1). It allows a re-synchronization between Slave and Master in case of communication error.

15.6. Master Start-Up

/SS, SCLK, MISO can be undefined during the Master start-up as long as the Slave is re-synchronized before the first frame transfer.

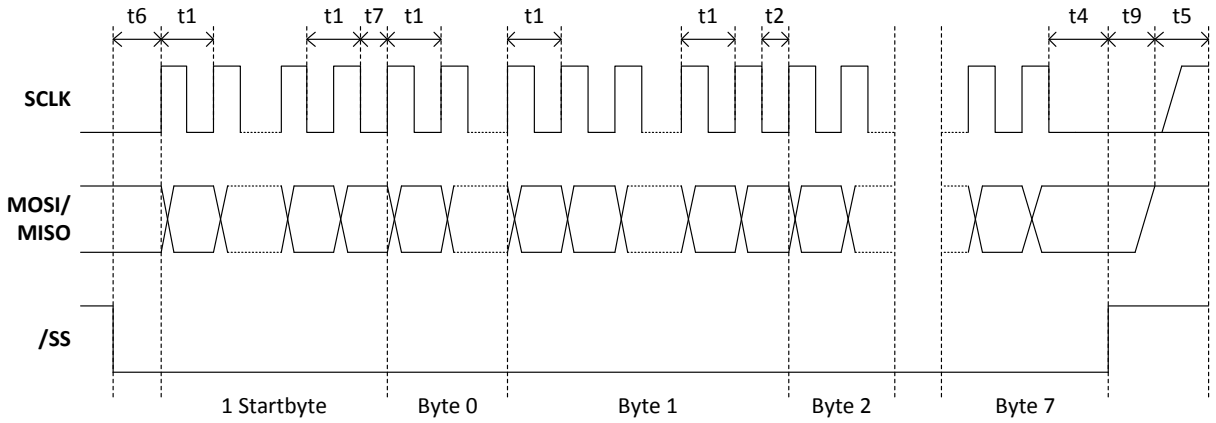
15.7. Slave Start-Up

The slave start-up (after power-up or an internal failure) takes 16 ms. Within this time /SS and SCLK is ignored by the Slave. The first frame can therefore be sent after 16 ms. MISO is Hi-Z (i.e. Hi-Impedance) until the Slave is selected by its /SS input. MLX90333 will cope with any signal from the Master while starting up.

15.8. Timing

To synchronize communication, the Master deactivates /SS high for at least t5 (1.5 ms). In this case, the Slave will be ready to receive a new frame. The Master can re-synchronize at any time, even in the middle of a byte transfer.

Note: Any time shorter than t5 leads to an undefined frame state, because the Slave may or may not have seen /SS inactive.



Timings	Min [30]	Max	Remarks
t1	2.3 µs / 6.9 µs	-	No capacitive load on MISO. t1 is the minimum clock period for any bits within a byte.
t2	12.5 µs / 37.5 µs	-	t2 the minimum time between any other byte
t4	2.3 µs / 6.9 µs	-	Time between last clock and /SS = high = chip de-selection
t5	300 µs / 1500 µs	-	Minimum /SS = Hi time where it's guaranteed that a frame re-synchronizations will be started.
t5	0 µs	-	Maximum /SS = Hi time where it's guaranteed that NO frame re-synchronizations will be started.

[30] *Timings shown for oscillator base frequency of 20MHz (Fast Mode) / 7 MHz (Slow Mode)*

Timings	Min [30]	Max	Remarks
t6	2.3 µs / 6.9 µs	-	The time t6 defines the minimum time between /SS = Lo and the first clock edge
t7	15 µs / 45 µs	-	t7 is the minimum time between the StartByte and the Byte0
t9	-	< 1 µs	Maximum time between /SS = Hi and MISO Bus High-Impedance
$T_{StartUp}$	-	< 10 ms / 16 ms	Minimum time between reset-inactive and any master signal change

15.9. Slave Reset

On internal soft failures the Slave resets after 1 second or after an (error) frame is sent. On internal hard failures the Slave resets itself. In that case, the Serial Protocol will not come up. The serial protocol link is enabled only after the completion of the first synchronization (the Master deactivates /SS for at least t5).

15.10. Frame Layer

15.10.1. Frame Type Selection

See the programmable parameter XYZ in section 13.2.3 to select between the Alpha, Beta Frame and the X, Y, Z Frame.

15.10.2. Data Frame Structure

The Figure 9 gives the timing diagram for the SPI Frame. The latch point for the angle measurement is at the last clock before the first data frame byte.

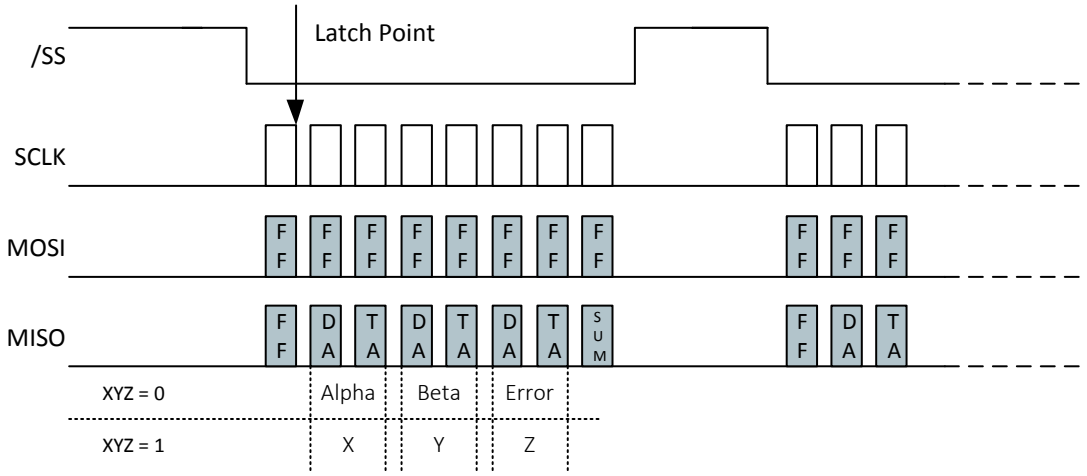


Figure 9 – Timing Diagram for the SPI Frame

A data frame consists of 8 bytes:

Data Frame	XYZ = 0	XYZ = 1
1 start byte	FFh	
2 data bytes (LSByte first)	Alpha	X
2 data bytes (LSByte first)	Beta	Y
2 data bytes (LSByte first)	Error Code	Z
1 SUM byte	8 LSB of the sum of the transmitted bytes	

15.10.3. Timing

There are no timing limits for frames: a frame transmission could be initiated at any time. There is no inter-frame time defined.

15.10.4. Data Structure

The DATA could be a valid angle/field component or an error condition.

DATA: Angle/Field Component A[15:0] with (Span)/2^{16}

Least Significant Byte								Most Significant Byte							
MSB							LSB	MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0	A15	A14	A13	A12	A11	A10	A9	A8

DATA: Error

Least Significant Byte								Most Significant Byte							
MSB							LSB	MSB							LSB
E7	E6	E5	E4	E3	E2	E1	E0	E15	E14	E13	E12	E11	E10	E9	E8

BIT	NAME	Description
E0	-	
E1	-	
E2	F_ADCMONITOR	ADC Failure
E3	F_ADCSATURA	ADC Saturation (Electrical failure or field too strong)
E4	F_GAINTOOLOW	The gain code is strictly less than EE_GAINMIN

BIT	NAME	Description
E5	F_GAINTOOHIGH	The gain code is strictly greater than EE_GAINMAX
E6	F_NORMTOOLOW	Goes high when the fast norm (the max of absolute X,Y,Z) is below 30%
E7	F_FIELDTOOLOW	The norm (Square root) is strictly less than EE_FIELDLOW
E8	F_FIELDTOOHIGH	The norm (Square root) is strictly greater than EE_FIELDHIGH
E9	F_ROCLAMP	Analog Chain Rough Offset Compensation: Clipping
E10	-	
E11	F_DEADZONEALPHA	The angle ALPHA lies in the deadzone
E12	-	
E13	-	
E14	-	
E15	F_DEADZONEBETA	The angle BETA lies in the deadzone

15.10.5. Angle Calculation

All communication timing is independent (asynchronous) of the angle data processing. The angle is calculated continuously by the Slave:

- Slow Mode: every 1.5 ms at most.
- Fast Mode: every 350 µs at most.

The last angle calculated is hold to be read by the Master at any time. Only valid angles are transferred by the Slave, because any internal failure of the Slave will lead to a soft reset.

15.10.6. Error Handling

In case of any errors listed in section 15.10.4, the Serial protocol will be initialized and the error condition can be read by the master.

In case of any other errors (ROM CRC error, EEPROM CRC error, RAM check error, intelligent watchdog error…) the Slave's serial protocol is not initialized. The MOSI/MISO pin will stay Hi-impedant (no error frames are sent).

16. Recommended Application Diagrams

16.1. Analog Output Wiring in SOIC-8 Package

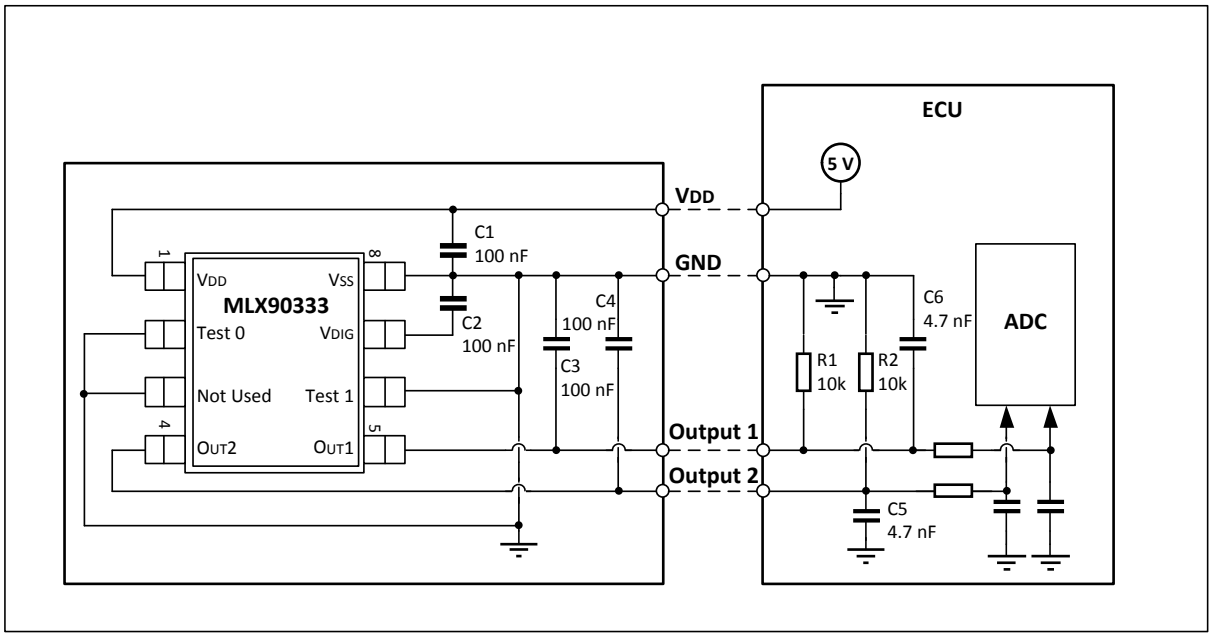


Figure 10 – Recommended wiring in SOIC-8 package

16.2. PWM Low Side Output Wiring

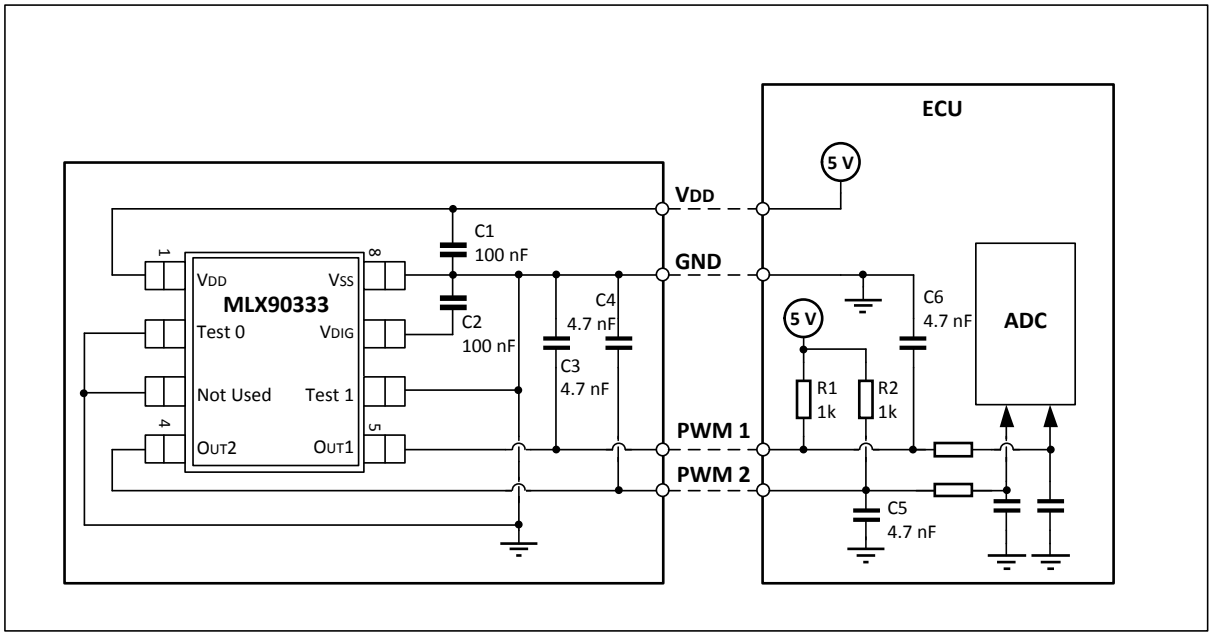


Figure 11 – Recommended wiring for a PWM Low Side Output configuration

16.3. Analog Output Wiring in TSSOP-16 Package

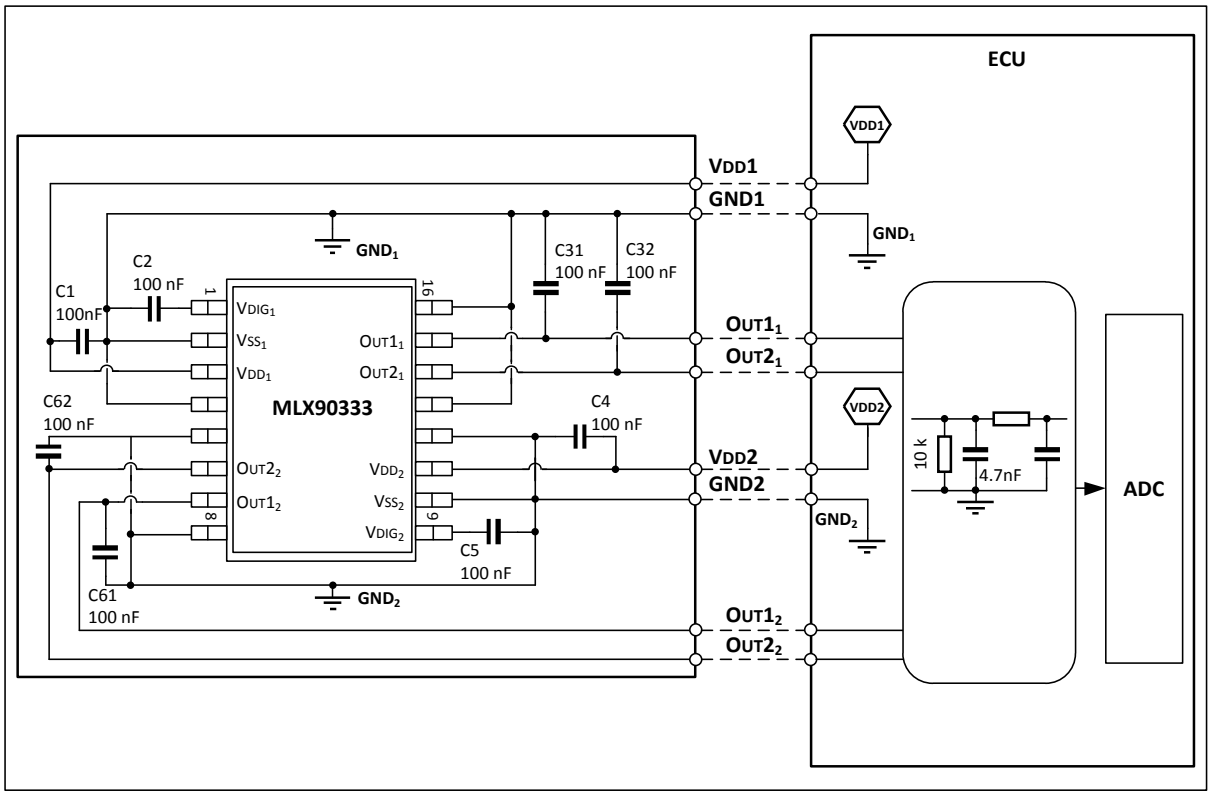


Figure 12 – Recommended wiring in TSSOP-16 package (dual die)

16.4. Serial Protocol

Generic schematics for single slave and dual slave applications are described.

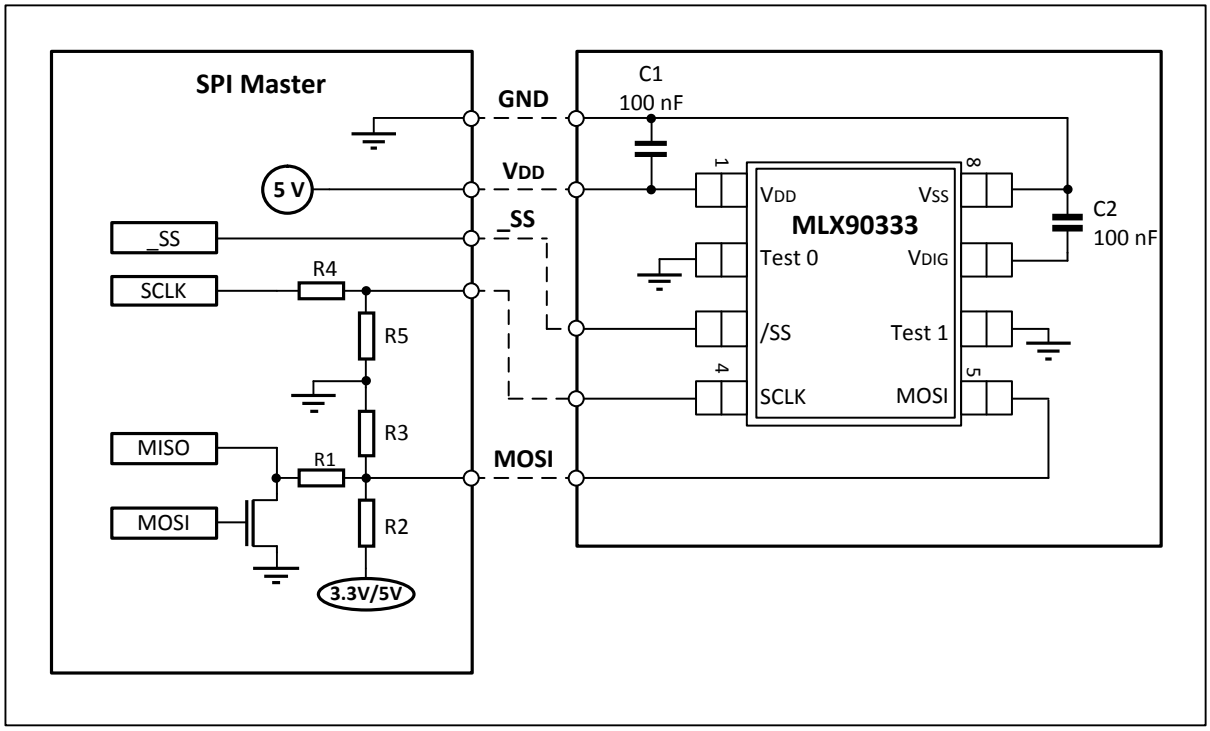


Figure 13 – SPI Version – Single Die – Application Diagram

Application Type	µCtrl Supply (V)	Pull-up Supply (V)	90316 Supply (V)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	MOS Type
5V µCtrl w/o O.D. w/o 3.3V	5V	5V	5V	100	1000	20,000	1000	20,000	BS170
5V µCtrl w/o O.D. w/ 3.3V	5V	3.3V	5V	150	1000	N/A	1000	20,000	BS170
3.3V µCtrl w/o O.D. [31]	3.3V	3.3V	5V	150	1000	N/A	N/A	N/A	BS170
5V µCtrl w/ O.D. w/o 3.3V [32]	5V	5V	5V	100	1000	20,000	1000	20,000	N/A
3.3V µCtrl w/ O.D.	3.3V	3.3V	5V	150	1000	N/A	N/A	N/A	N/A

Table 6 – Resistor Values for Common Specific Applications

[31] *µCtrl w/ O.D. : Micro-controller with open-drain capability (for instance NEC V850ES series)*
[32] *µCtrl w/o O.D. : Micro-controller without open-drain capability (like TI TMS320 series or ATMEL AVR)*

17. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/en/quality-environment/soldering).

For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends consulting the dedicated trim&forming recommendation application note: lead trimming and forming recommendations (http://www.melexis.com/en/documents/documentation/application-notes/lead-trimming-and-forming-recommendations).

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment.

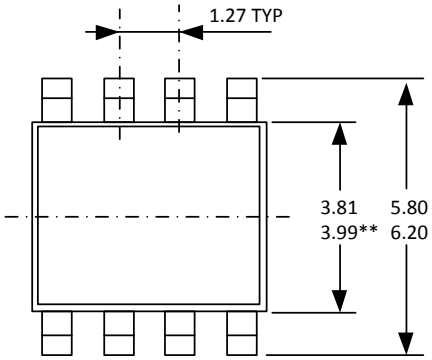
18. ESD Precautions

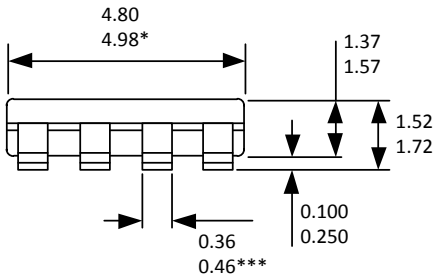
Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

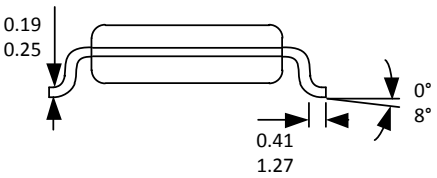
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

19. Package Information

19.1. SOIC-8 - Package Dimensions



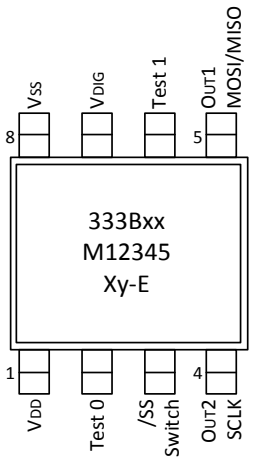




NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

19.2. SOIC-8 - Pinout and Marking



Marking :

Part Number MLX90333 (3 digits)
Die Version (3 digits)

Top 333 Bxx

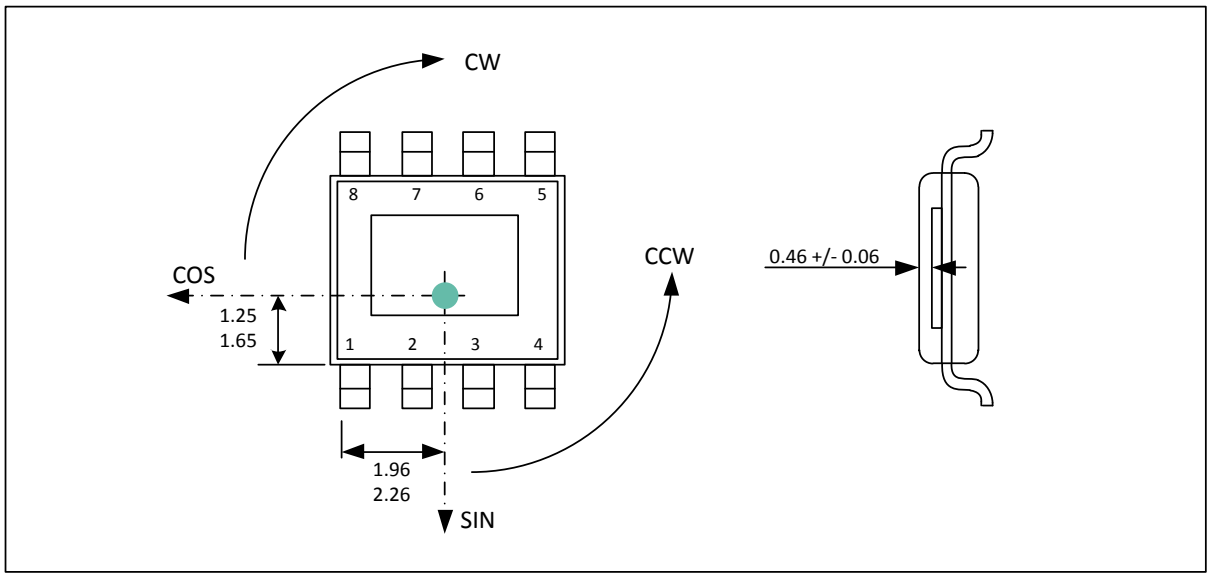
M12345 Lot number: “M” + 5 digits

Xy-E Split lot number + “-E” (Optional)

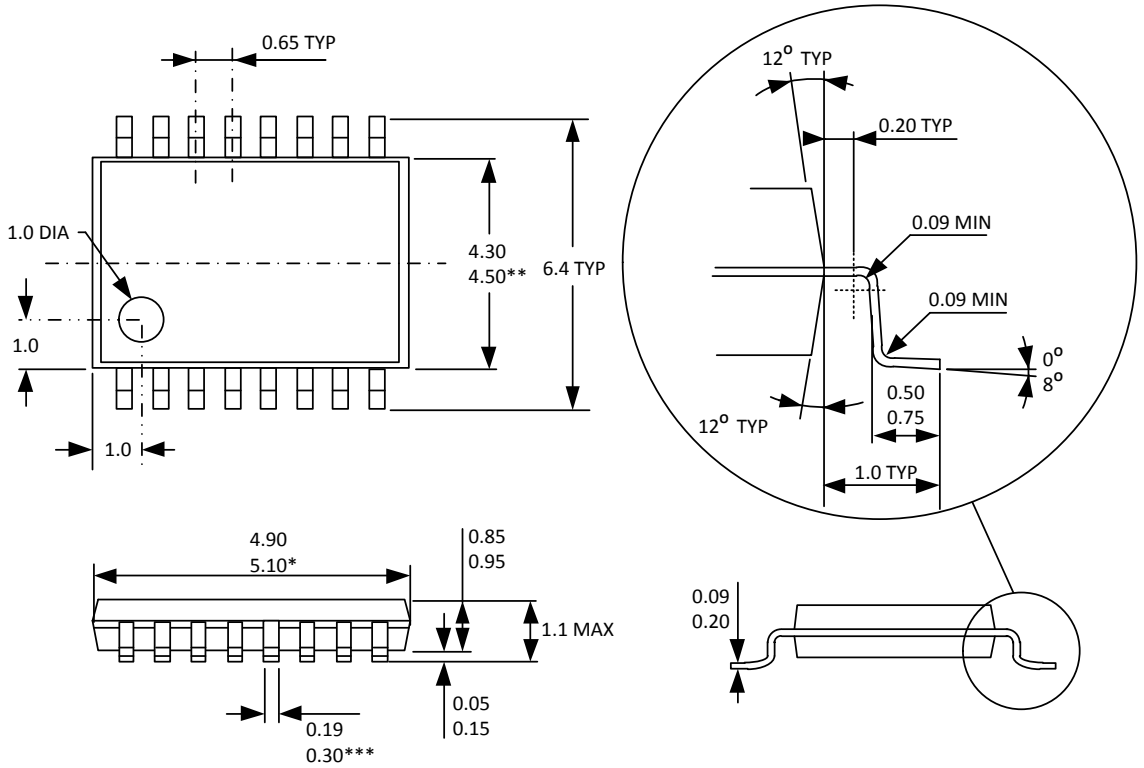
Bottom YY WW

Week Date code (2 digits)
Year Date code (2 digits)

19.3. SOIC-8 - IMC Positionning



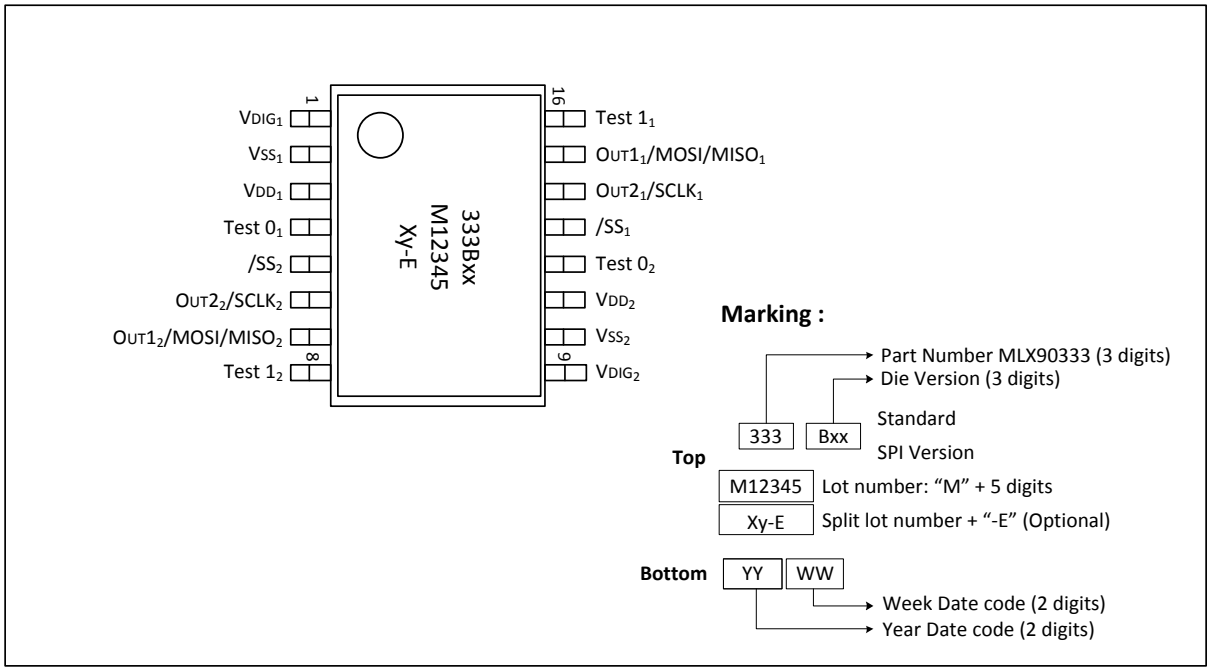
19.4. TSSOP-16 - Package Dimensions



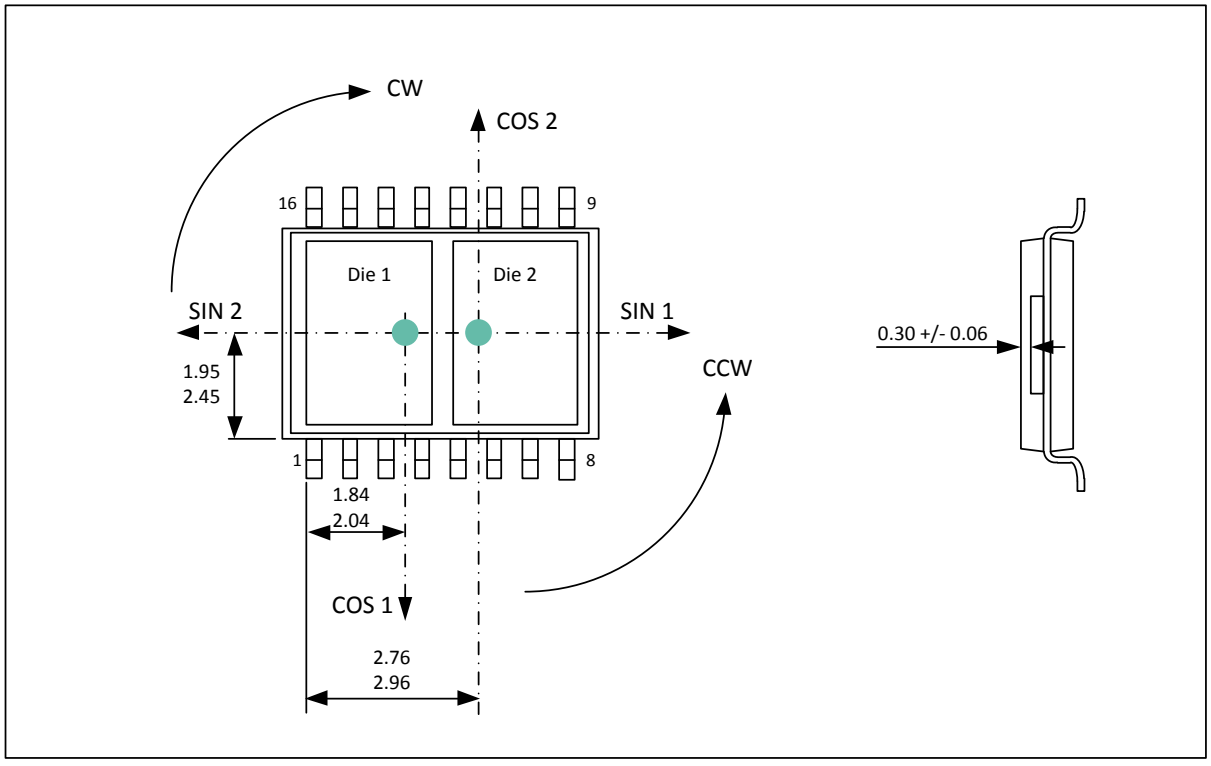
NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

19.5. TSSOP-16 - Pinout and Marking



19.6. TSSOP-16 - IMC Positionning



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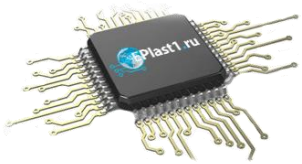

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