ADVANCED LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

Check for Samples: TLC2272-Q1 , TLC2272A-Q1 , TLC2274-Q1, TLC2274A-Q1

FEATURES

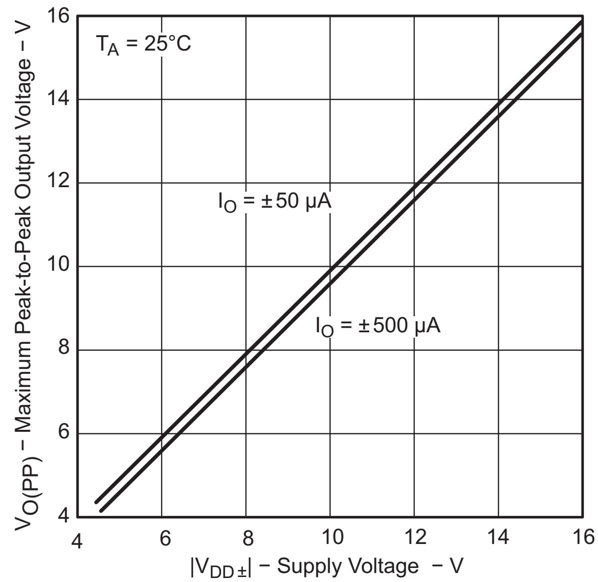
- **Qualified for Automotive Applications**
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Macromodel Included**
- **Performance Upgrades for the TS272, TS274, TLC272, and TLC274**

DESCRIPTION

The TLC2272 and TLC2274 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC227x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE



The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices.

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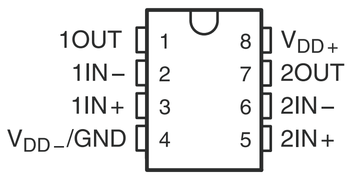
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

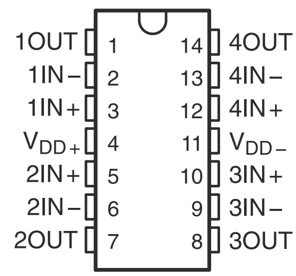
T_A	V_{IO}max At 25°C	PACKAGED DEVICES(1)(2)	
		SMALL OUTLINE (D)	TSSOP (PW)
-40°C to 125°C	950 µV	TLC2272AQDRQ1	TLC2272AQPWRQ1
	2.5 mV	TLC2272QDRQ1	TLC2272QPWRQ1
-40°C to 125°C	950 µV	TLC2274AQDRQ1	TLC2274AQPWRQ1
	2.5 mV	TLC2274QDRQ1	TLC2274QPWRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

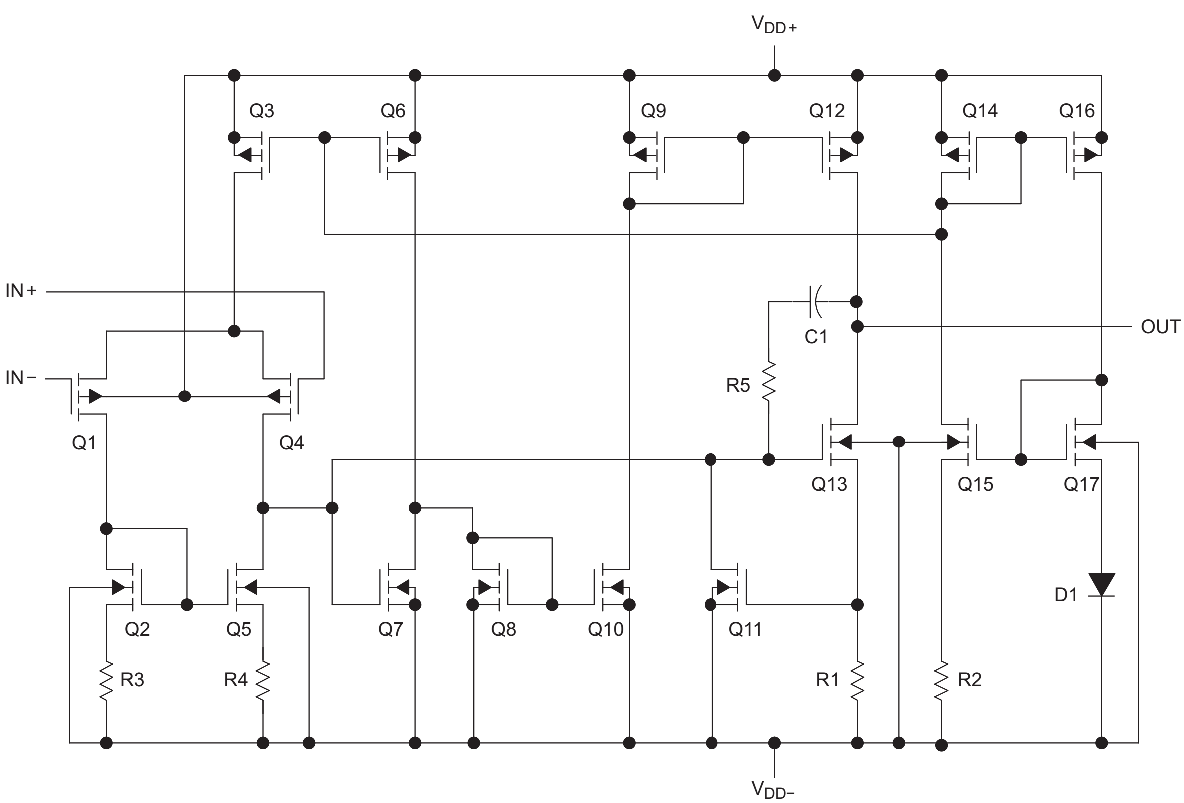
TLC2272
D OR PW PACKAGE
(TOP VIEW)



TLC2274
D OR PW PACKAGE
(TOP VIEW)



Equivalent Schematic (Each Amplifier)



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Actual Device Component Count(1)

COMPONENT	TLC2272	TLC2274
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{DD+}	Supply voltage(2)		8	V
V_{DD-}	Supply voltage(2)		−8	V
V_{ID}	Differential input voltage(3)		±16	V
V_I	Input voltage range(2)	Any input	V_{DD-} − 0.3 to V_{DD+}	V
I_I	Input current	Any input	±5	mA
I_O	Output current		±50	mA
	Total current into V_{DD+}		±50	mA
	Total current out of V_{DD-}		±50	mA
	Duration of short-circuit current at (or below) 25°C(4)		unlimited	
	Continuous total dissipation		See Dissipation Ratings	
T_A	Operating free-air temperature range		-40°C to 125°C	°C
T_{stg}	Storage temperature range		−65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or PW package	260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
(3) Differential voltages are at I_{N+} with respect to I_{N-}. Excessive current will flow if input is brought below V_{DD-} − 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	337 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
D-14	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
D-14	700 mW	5.6 mW/°C	448 mW	364 mW	-

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD\pm}$	Supply voltage	±2.2	±8	V
V_I	Input voltage	V_{DD-}	V_{DD+} −1.5	V
V_{IC}	Common-mode input voltage	V_{DD-}	V_{DD+} −1.5	V
T_A	Operating free-air temperature	−40	125	°C

TLC2272Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLC2272Q			TLC2272AQ			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, $V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500		300	950	μV
			Full range			3000			1600	
αV_{IO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (2)		25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current		25°C		0.5	60		0.5	60	pA
			Full range			800			800	
I_{IB}	Input bias current		25°C		1			1	60	pA
			Full range						800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\|$ ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −200 μA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_{OH} = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ (3)	25°C	10	35		10	35		V/mV
			Full range	10			10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ (3)	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.2	3		2.2	3	mA
			Full range			3			3	

(1) Full range is −40°C to 125°C for Q level part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 2.5 V

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TLC2272Q OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC2272Q			TLC2272AQ			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O =1.25 V to 2.75 V, R_L = 10 kΩ (2)	C_L = 100 pF (2)	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1			1		μV
		f = 0.1 to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5V to 2.5V, R_L = 10 kΩ, f = 20 kHz (2)	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF (2)	R_L = 10 kΩ (2)	25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2V, R_L = 10 kΩ (2)	A_V = 1, C_L = 100 pF (2)	25°C		1			1		MHz
t_s	Settling time	A_V = -1, Step = 0.5V to 2.5V, R_L = 10 kΩ (3) C_L = 100 pF (3)	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ (3),	C_L = 100 pF (3)	25°C		50°			50°		
	Gain margin			25°C		10			10		dB

(1) Full range is −40°C to 125°C for Q level part.
(2) Referenced to 2.5 V
(3) Referenced to 2.5 V

TLC2272Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC2272Q MIN	TLC2272Q TYP	TLC2272Q MAX	TLC2272AQ MIN	TLC2272AQ TYP	TLC2272AQ MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, R_S = 50 Ω	V_O = 0 V	25°C		300	2500		300	950	μV
				Full range			3000			1500	
$αV_{IO}$	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (2)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	$\|V_{IO}\|$ ≤ 5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 μA	25°C		−4.99			−4.99		V
		V_{IC} = 0 V,	I_O = 500 μA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V,	I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V,	R_L = 10 kΩ	25°C	20	50		20	50		V/mV
				Full range	20			20			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	AV = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = -5 V to 2.7 V, V_O = 0 V,	R_S = 50 Ω	25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply voltage rejection ratio ($ΔV_{DD}/ΔV_{IO}$)	V_{DD} = ±2.2 V to ±8 V, V_{IC} = 0V,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V,	No load	25°C		2.4	3		2.4	3	mA
				Full range			3			3	

(1) Full range is −40°C to 125°C for Q level part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2272Q OPERATING CHARACTERISTICS

at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC2272Q MIN	TLC2272Q TYP	TLC2272Q MAX	TLC2272AQ MIN	TLC2272AQ TYP	TLC2272AQ MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ	C_L = 100 pF	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1			1		μV
		f = 0.1 to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, f = 20 kHz, R_L = 10 kΩ	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ	A_V = 1, C_L = 100 pF	25°C		0.54			0.54		MHz
t_s	Settling time	A_V = -1, Step = -2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°			52°		
	Gain margin			25°C		10			10		dB

(1) Full range is −40°C to 125°C for Q level part.

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TLC2274Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC2274Q			TLC2274AQ			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1600	
αV_{IO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (2)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1			1	60	pA
				Full range						800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	$\|V_{IO}\|$ ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V,	R_L = 10 kΩ (3)	25°C	10	35		10	35		V/mV
				Full range	10			10			
			R_L = 1 MΩ (3)	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		4.4	6		4.4	6	mA
				Full range			6			6	

(1) Full range is −40°C to 125°C for Q level part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 2.5 V

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TLC2274Q OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC2274Q			TLC2274AQ			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ (2)	C_L = 100 pF (2)	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1			1		μV
		f = 0.1 to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5V to 2.5V, R_L = 10 kΩ, f = 20 kHz (2)	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF (2)	R_L = 10 kΩ (2)	25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2V, R_L = 10 kΩ (2)	A_V = 1, C_L = 100 pF (2)	25°C		1			1		MHz
t_s	Settling time	A_V = -1, Step = 0.5V to 2.5V, R_L = 10 kΩ (3) C_L = 100 pF (3)	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ (3),	C_L = 100 pF (3)	25°C		50°			50°		
	Gain margin			25°C		10			10		dB

(1) Full range is −40°C to 125°C for Q level part.
(2) Referenced to 2.5 V
(3) Referenced to 2.5 V

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TLC2274Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A (1)	TLC2274Q			TLC2274AQ			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, R_S = 50 Ω	V_O = 0 V	25°C		300	2500		300	950	µV
				Full range			3000			1500	
αV_{IO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (2)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	$\lvert V_{IO}\rvert$ ≤ 5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0 V,	I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V,	I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V,	R_L = 10 kΩ	25°C	20	50		20	50		V/mV
				Full range	20			20			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	AV = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = -5 V to 2.7 V, V_O = 0 V,	R_S = 50 Ω	25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = ±2.2 V to ±8 V, V_{IC} = 0V,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V,	No load	25°C		4.4	6		4.4	6	mA
				Full range			6			6	

(1) Full range is −40°C to 125°C for Q level part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2274Q OPERATING CHARACTERISTICS

at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC2274Q			TLC2274AQ			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ	C_L = 100 pF	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1			1		μV
		f = 0.1 to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, f = 20 kHz, R_L = 10 kΩ	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ	A_V = 1, C_L = 100 pF	25°C		0.54			0.54		MHz
t_s	Settling time	A_V = -1, Step = -2.3 V to 2.3 V, R_L = 10 kΩ C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
φ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°			52°		
	Gain margin			25°C		10			10		dB

(1) Full range is −40°C to 125°C for Q level part.

TYPICAL CHARACTERISTICS

Table of Graphs(1)

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6
αV_{IO}	Input offset voltage temperature coefficient	Distribution	Figure 7,Figure 8, Figure 9, Figure 10
I_{IB} /I_{IO}	Input bias and input offset current	vs Free-air temperature	Figure 11
V_I	Input voltage	vs Supply voltage	Figure 12
		vs Free-air temperature	Figure 13
V_{OH}	High-level output voltage	vs High-level output current	Figure 14
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 15, Figure 16
V_{OM+}	Maximum positive peak output voltage	vs Output current	Figure 17
V_{OM-}	Maximum negative peak output voltage	vs Output current	Figure 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 19
I_{OS}	Short-circuit output current	vs Supply voltage	Figure 20
		vs Free-air temperature	Figure 21
V_O	Output voltage	vs Differential input voltage	Figure 22, Figure 23
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	Figure 24
	Large-signal differential voltage amplification and phase margin	vs Frequency	Figure 25, Figure 26
	Large-signal differential voltage amplification	vs Free-air temperature	Figure 27, Figure 28
zo	Output impedance	vs Frequency	Figure 29, Figure 30
CMRR	Common-mode rejection ratio	vs Frequency	Figure 31
		vs Free-air temperature	Figure 32
kSVR	Supply-voltage rejection ratio	vs Frequency	Figure 33, Figure 34
		vs Free-air temperature	Figure 35
I_{DD}	Supply current	vs Supply voltage	Figure 36, Figure 37
		vs Free-air temperature	Figure 38, Figure 39
SR	Slew rate	vs Load capacitance	Figure 40
		vs Free-air temperature	Figure 41
V_O	Inverting large-signal pulse response		Figure 42, Figure 43
	Voltage-follower large-signal pulse response		Figure 44, Figure 45
	Inverting small-signal pulse response		Figure 46, Figure 47
	Voltage-follower small-signal pulse response		Figure 48, Figure 49
V_n	Equivalent input noise voltage	vs Frequency	Figure 50, Figure 51
	Noise voltage over a 10-second period		Figure 52
	Integrated noise voltage	vs Frequency	Figure 53
THD + N	Total harmonic distortion plus noise	vs Frequency	Figure 54
	Gain bandwidth product Gain-bandwidth product	vs Supply voltage	Figure 55
		vs Free-air temperature	Figure 56
φ_m	Phase margin	vs Load capacitance	Figure 57
	Gain margin	vs Load capacitance	Figure 58

(1) For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE

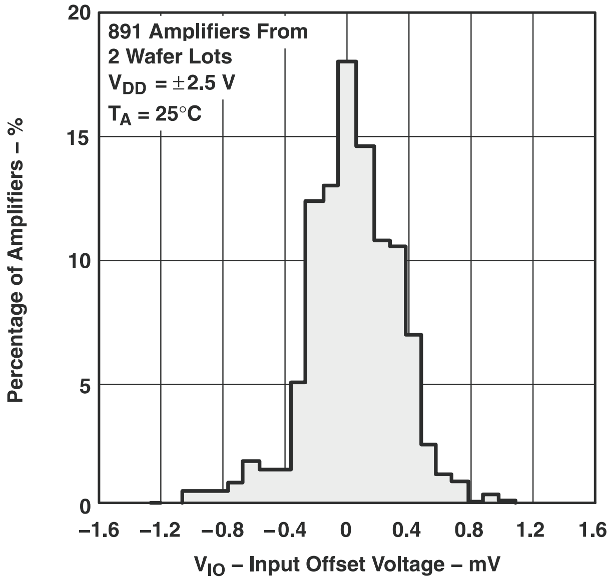

Figure 1.

DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE

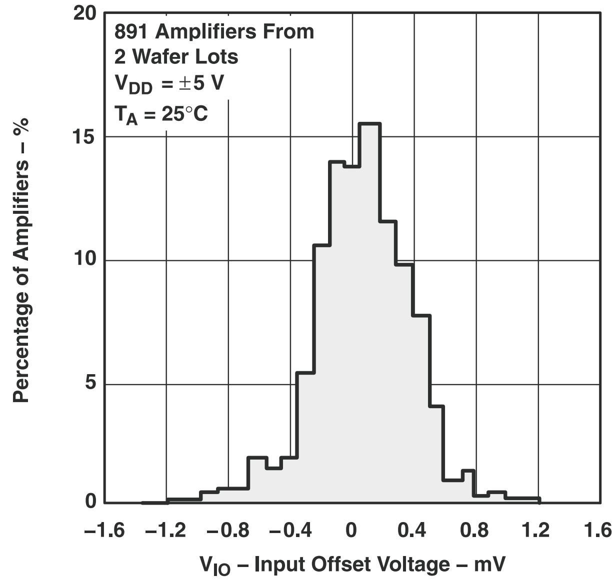

Figure 2.

DISTRIBUTION OF TLC2274 INPUT OFFSET VOLTAGE

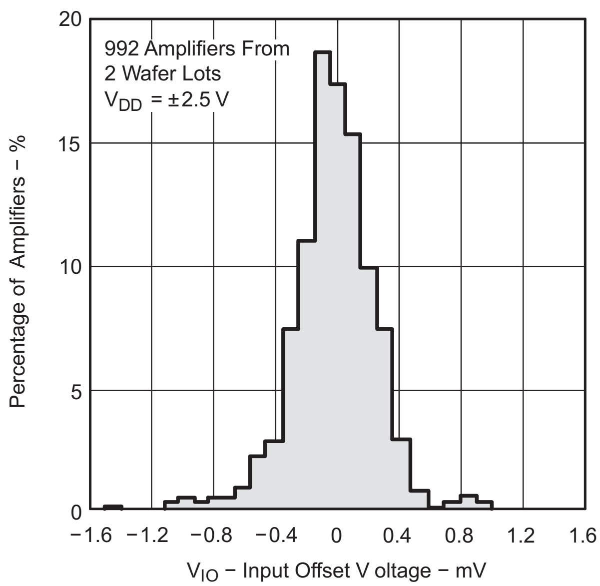

Figure 3.

DISTRIBUTION OF TLC2274A INPUT OFFSET VOLTAGE

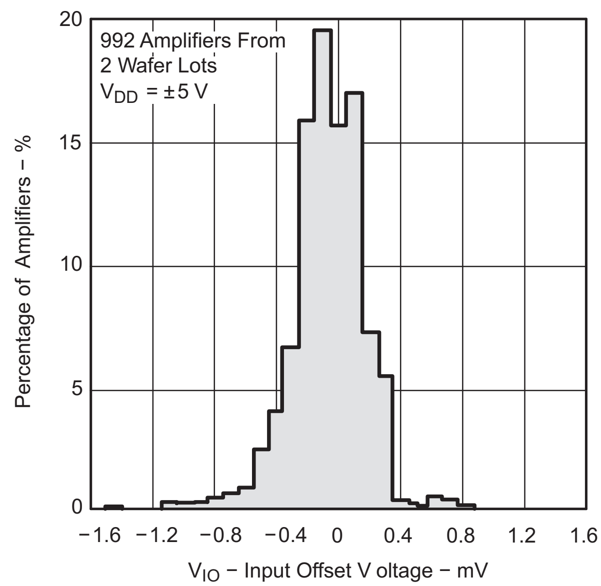

Figure 4.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

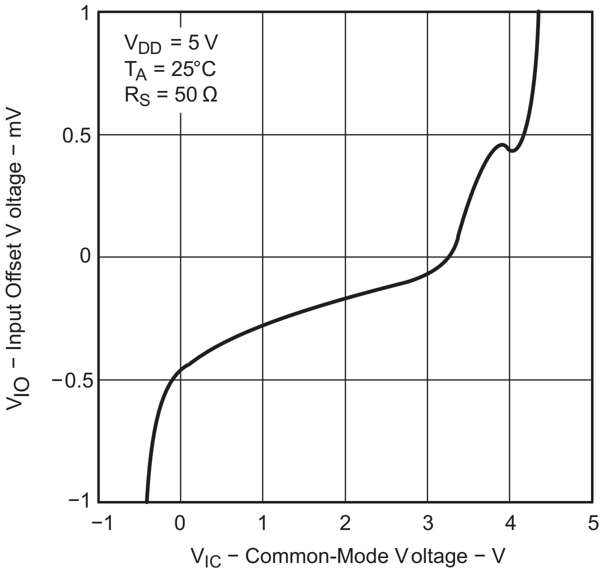

Figure 5.

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

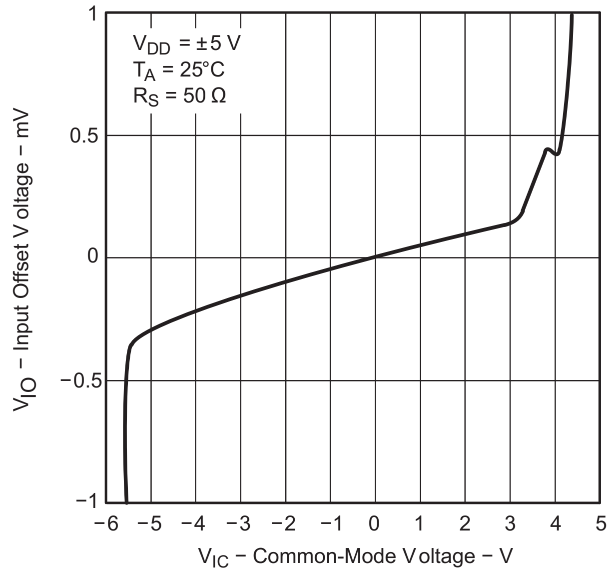

Figure 6.

DISTRIBUTION OF TLC2272
vs
INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

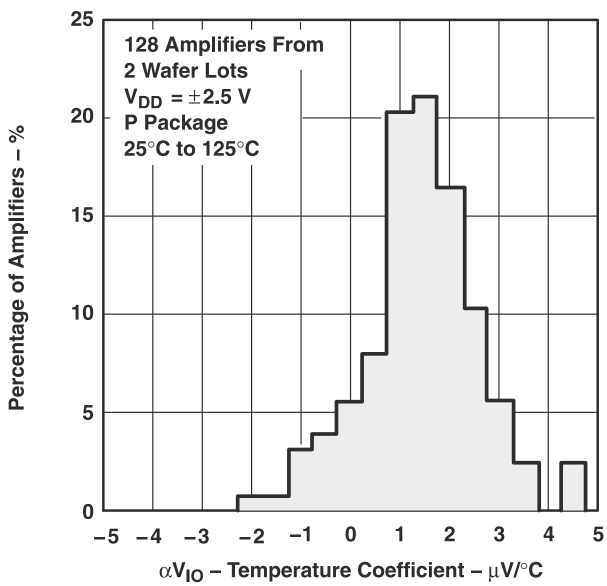

Figure 7.

DISTRIBUTION OF TLC2272
vs
INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

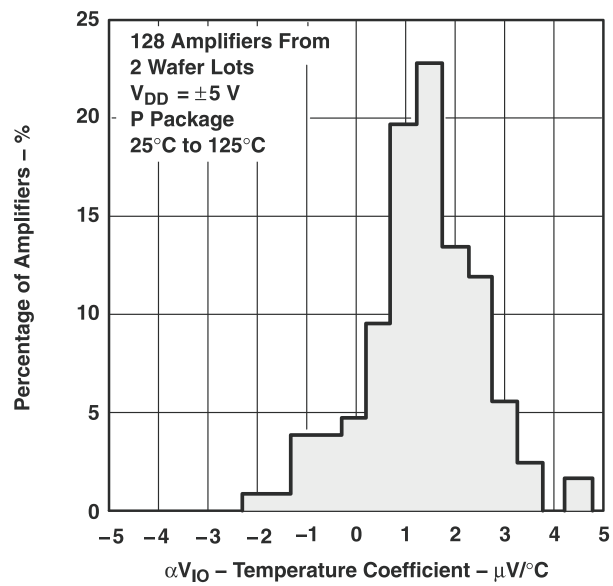

Figure 8.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

DISTRIBUTION OF TLC2274A vs INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

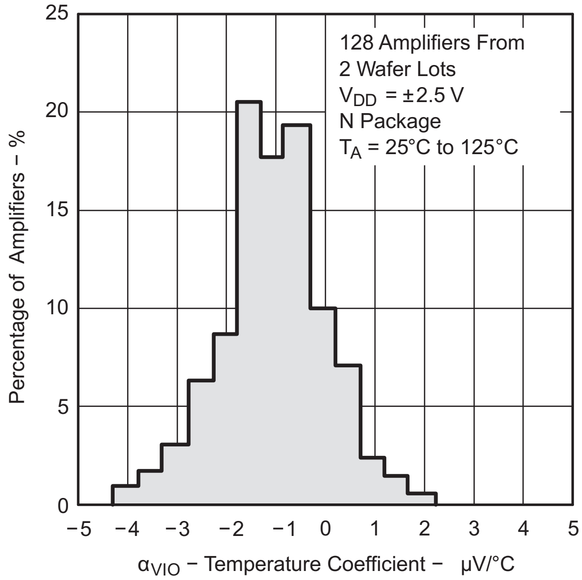

Figure 9.

DISTRIBUTION OF TLC2274A vs INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

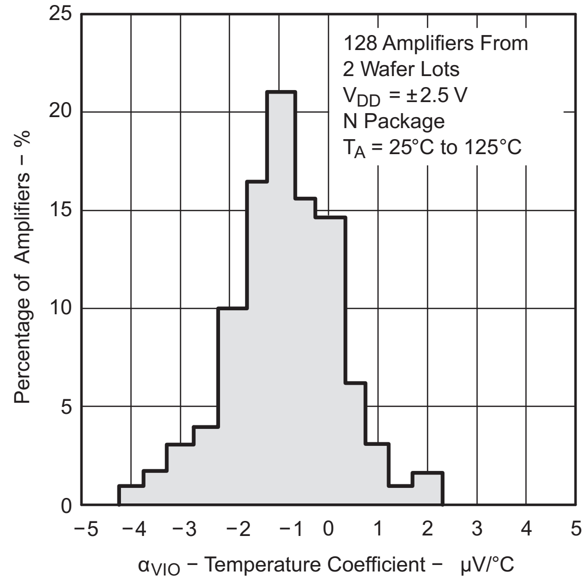

Figure 10.

INPUT BIAS AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

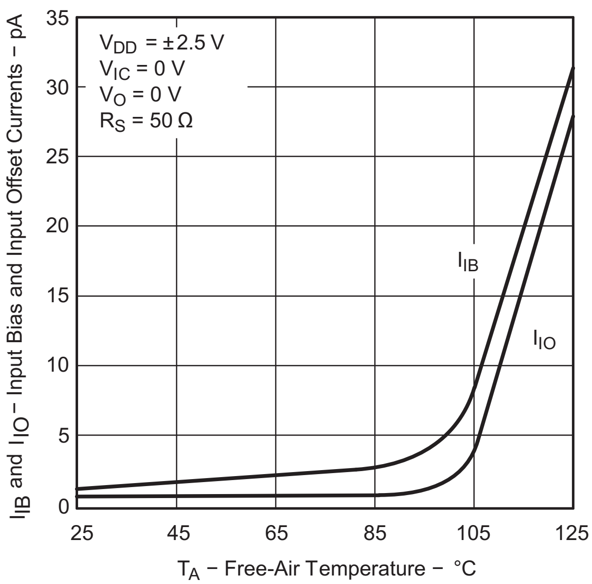

Figure 11.

INPUT VOLTAGE vs SUPPLY VOLTAGE

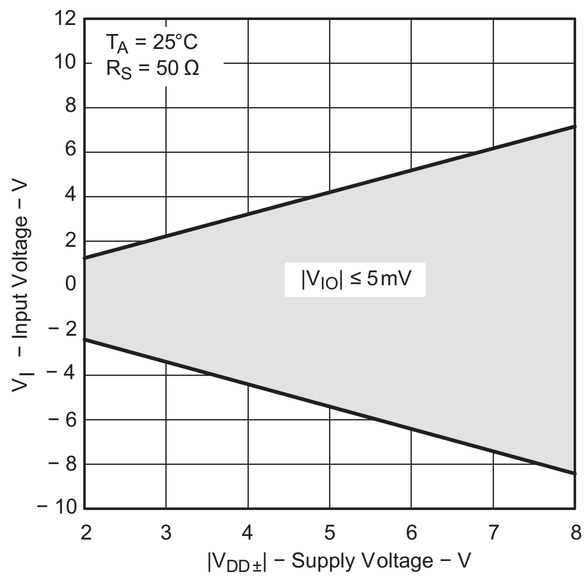

Figure 12.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

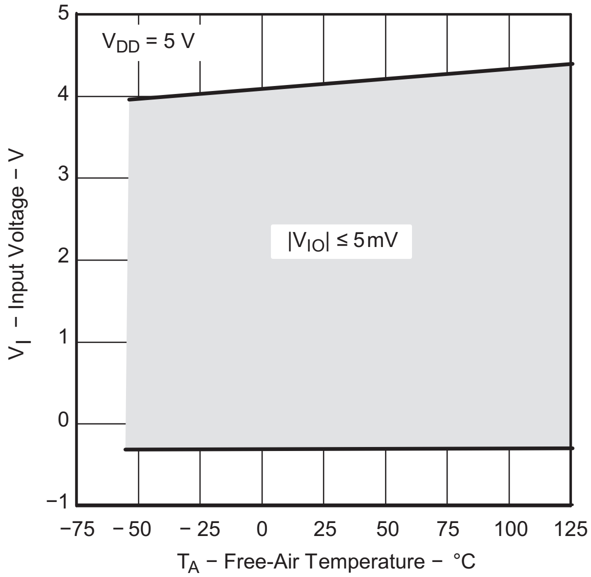

Figure 13.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

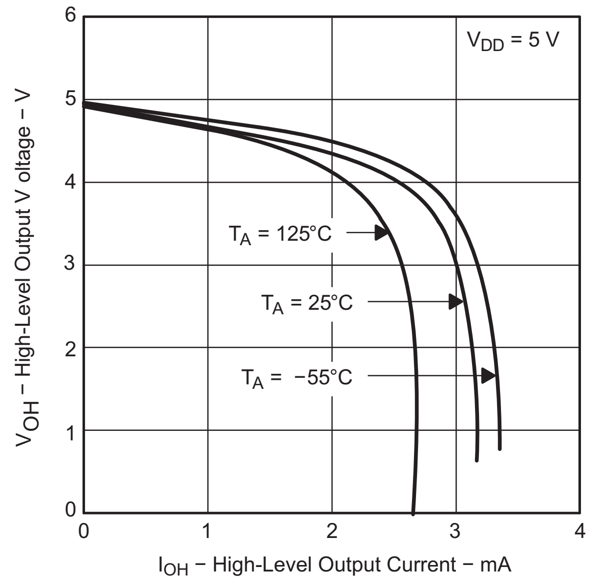

Figure 14.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

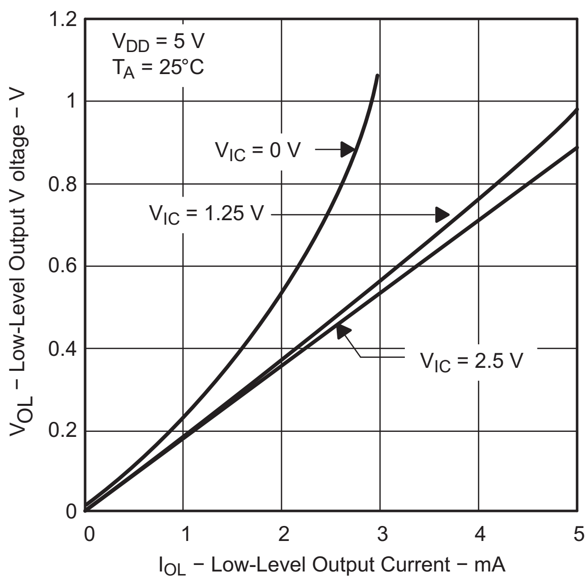

Figure 15.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

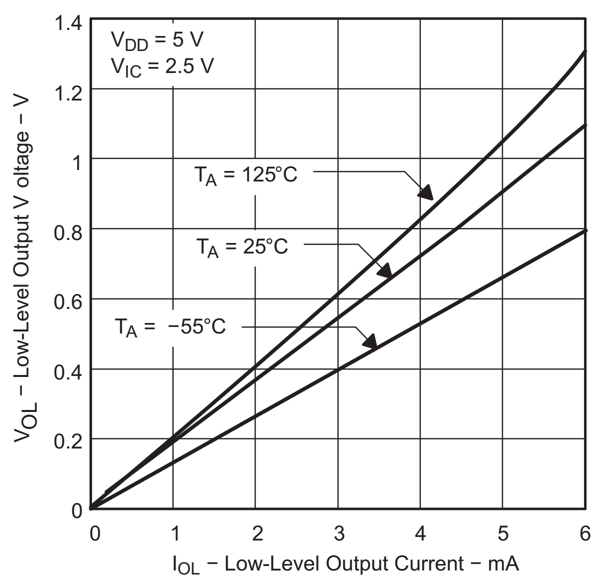

Figure 16.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

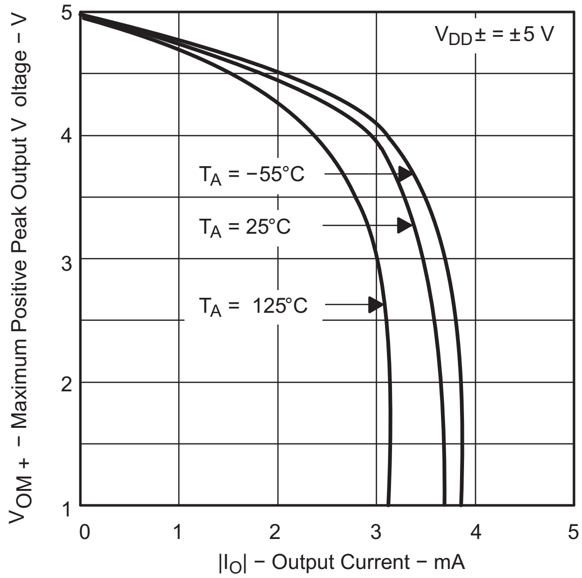

Figure 17.

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

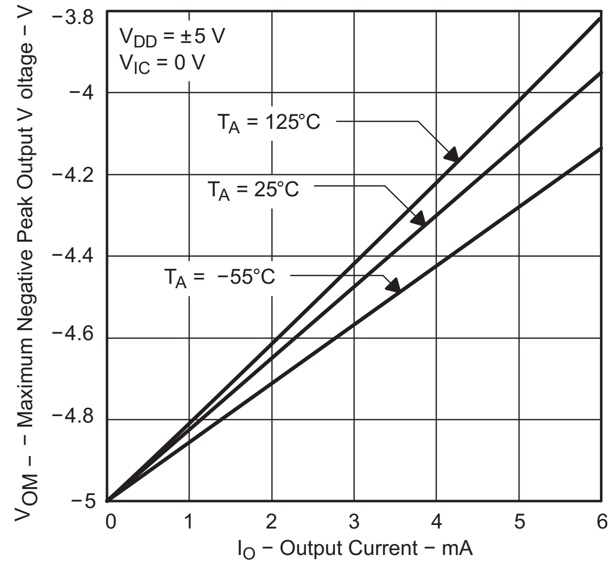

Figure 18.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

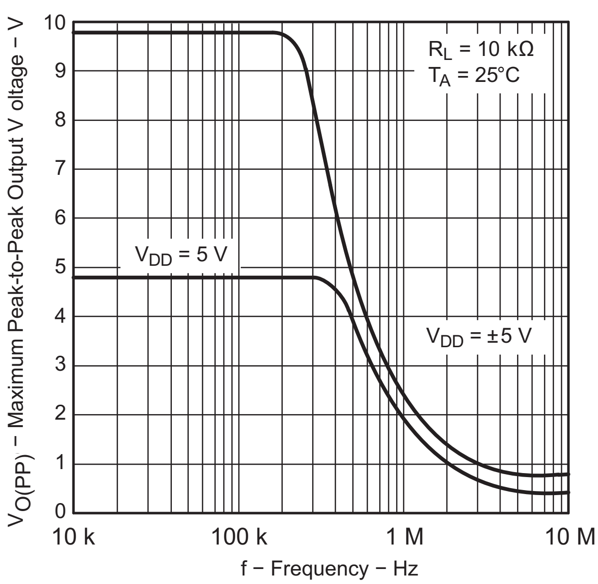

Figure 19.

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

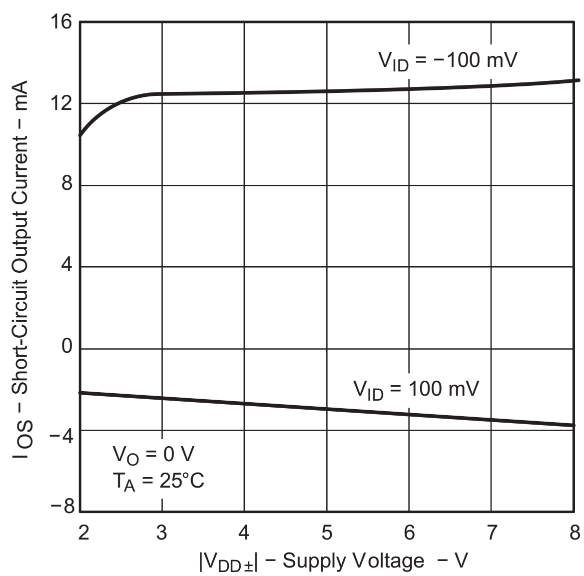

Figure 20.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

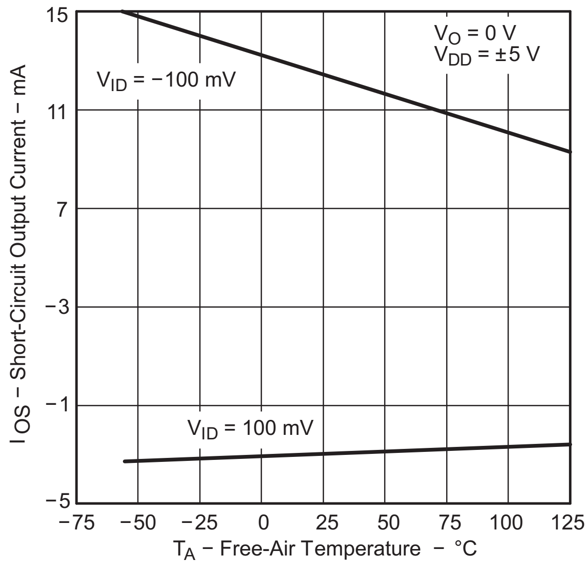

Figure 21.

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

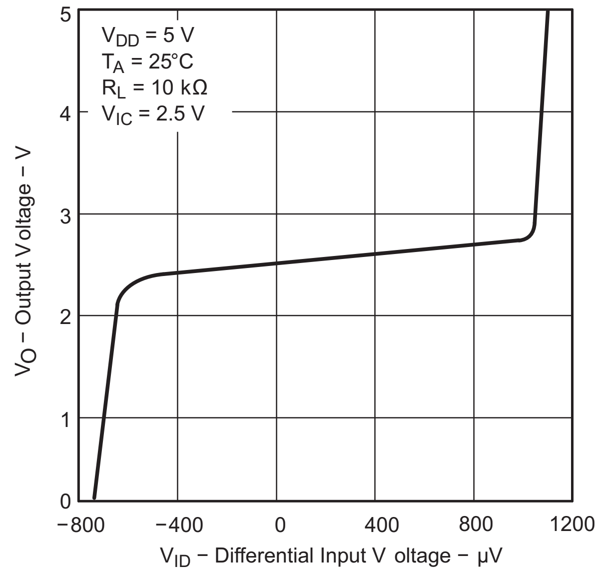

Figure 22.

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

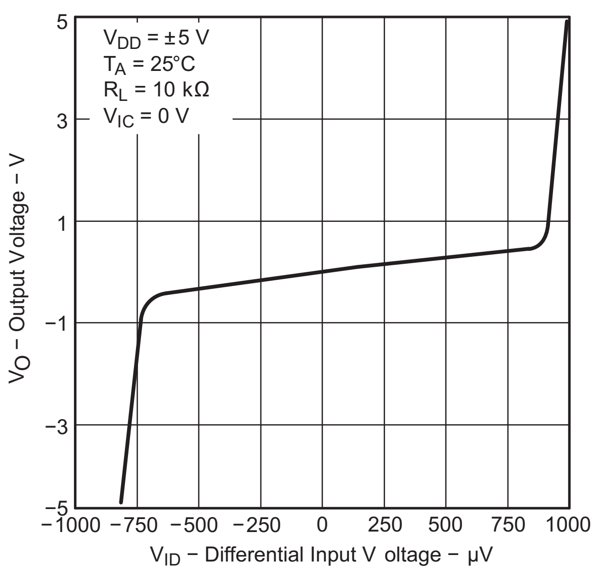

Figure 23.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

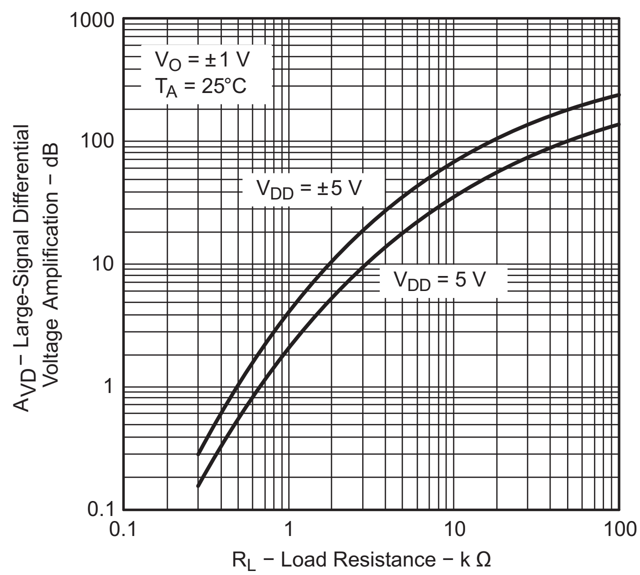

Figure 24.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

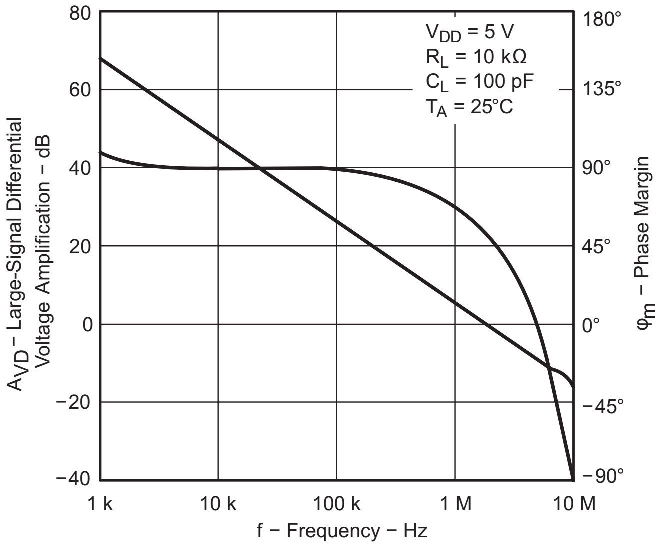

Figure 25.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

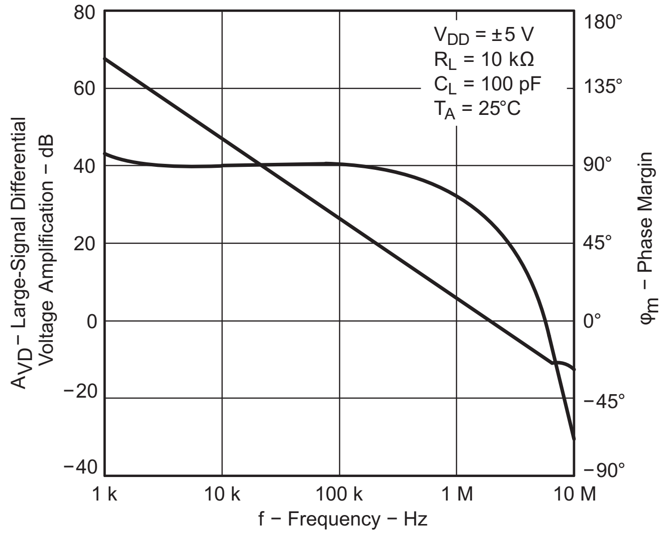

Figure 26.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

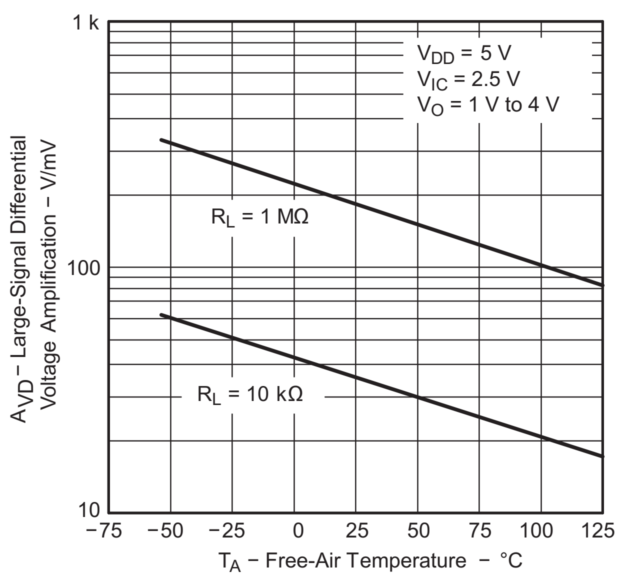

Figure 27.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

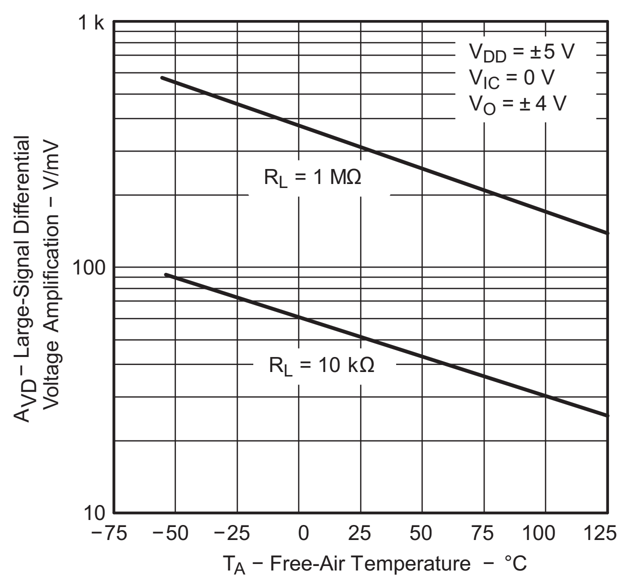

Figure 28.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

OUTPUT IMPEDANCE
vs
FREQUENCY

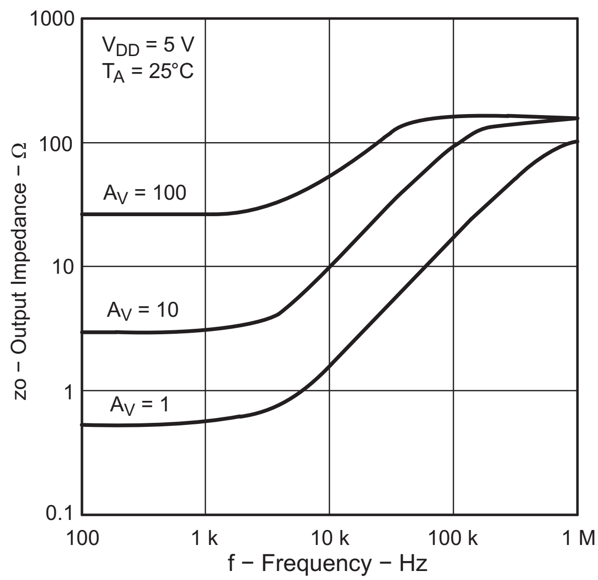

Figure 29.

OUTPUT IMPEDANCE
vs
FREQUENCY

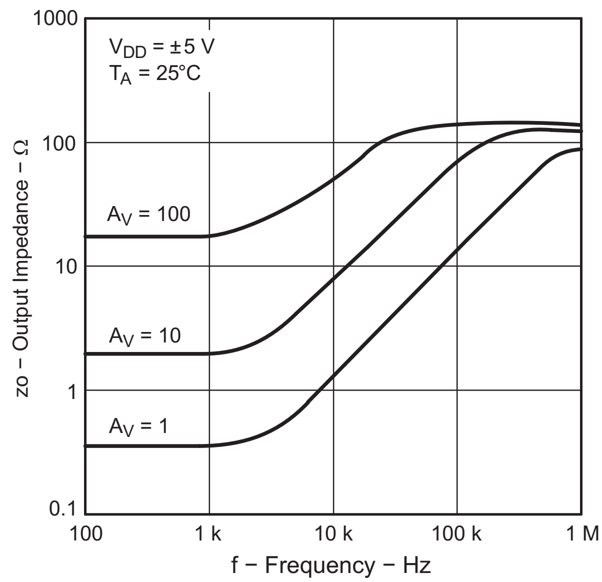

Figure 30.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

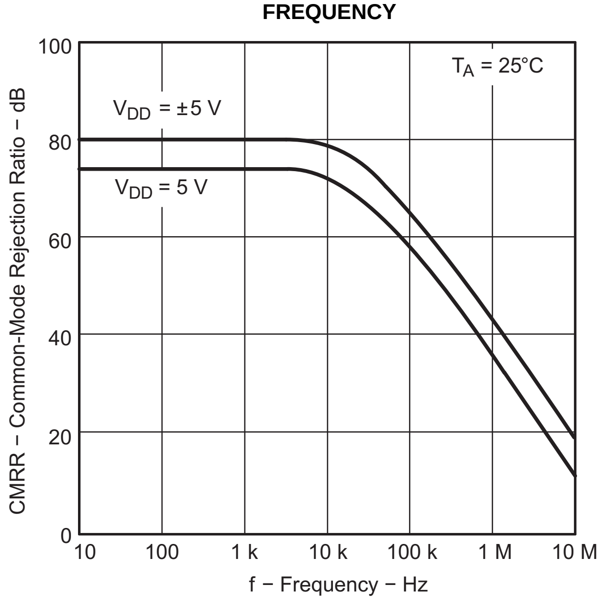

Figure 31.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY-AIR TEMPERATURE

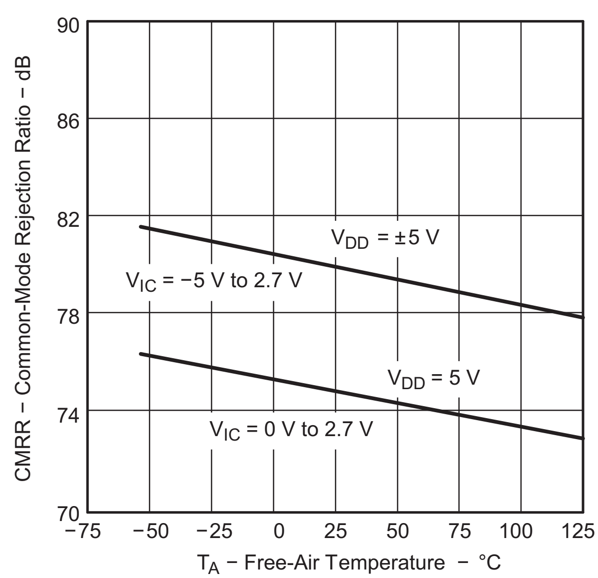

Figure 32.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

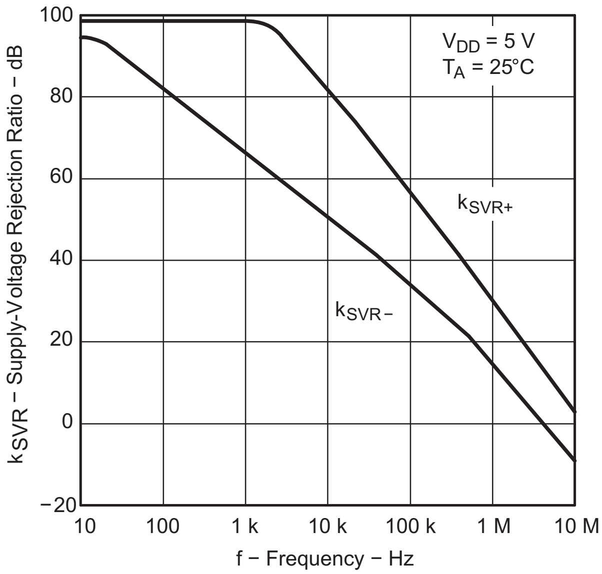

Figure 33.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

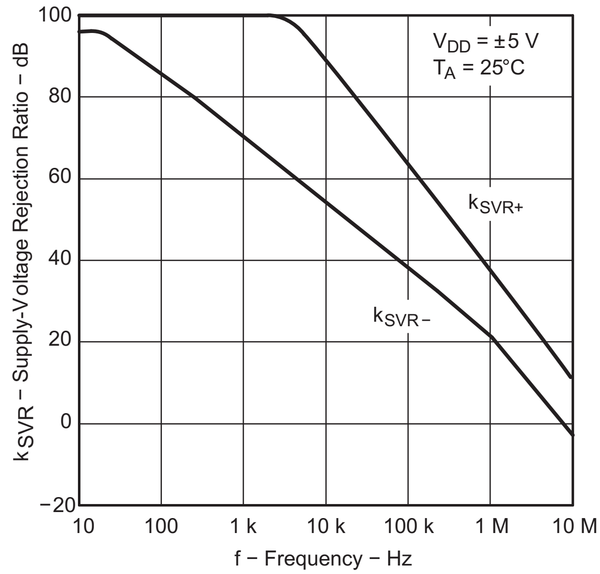

Figure 34.

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

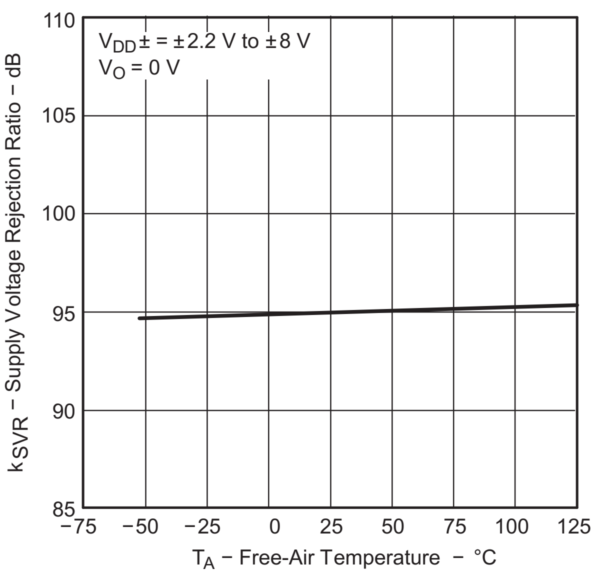

Figure 35.

TLC2272 SUPPLY CURRENT vs SUPPLY VOLTAGE

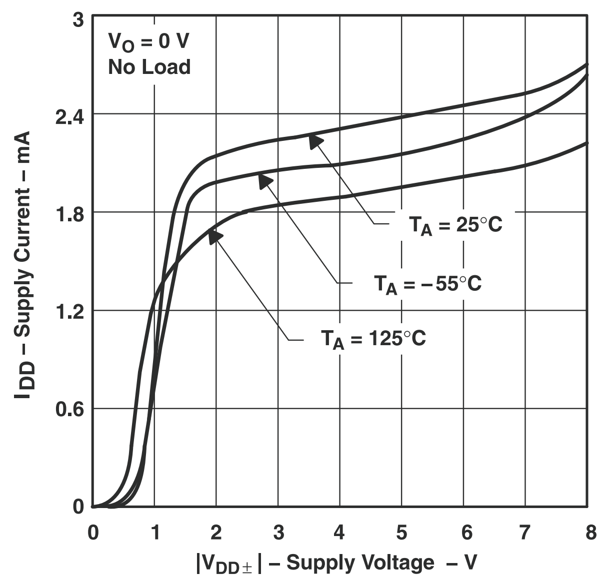

Figure 36.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC2274A SUPPLY CURRENT vs SUPPLY VOLTAGE

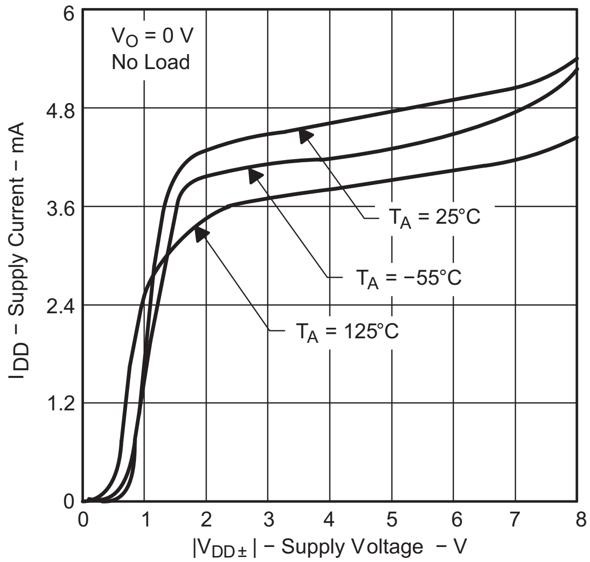

Figure 37.

TLC2272 SUPPLY CURRENT vs FREE-AIR TEMPERATURE

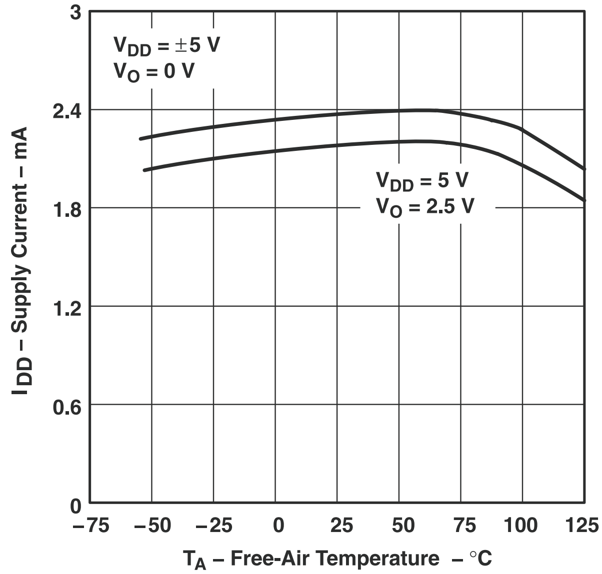

Figure 38.

TLC2274A SUPPLY CURRENT vs FREE-AIR TEMPERATURE

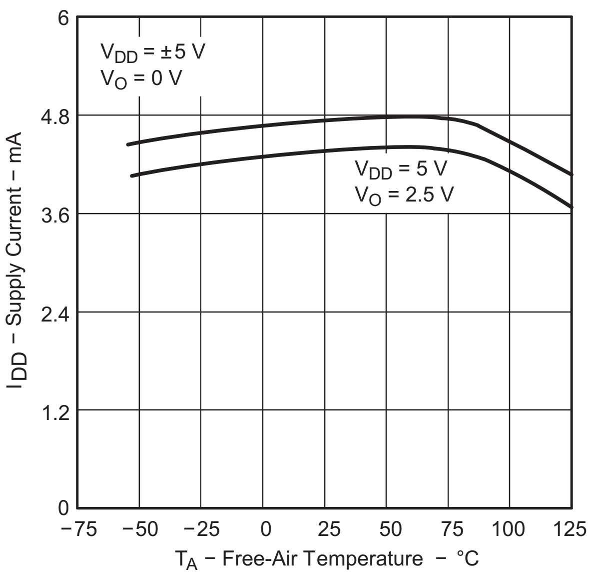

Figure 39.

SLEW RATE vs LOAD CAPACITANCE

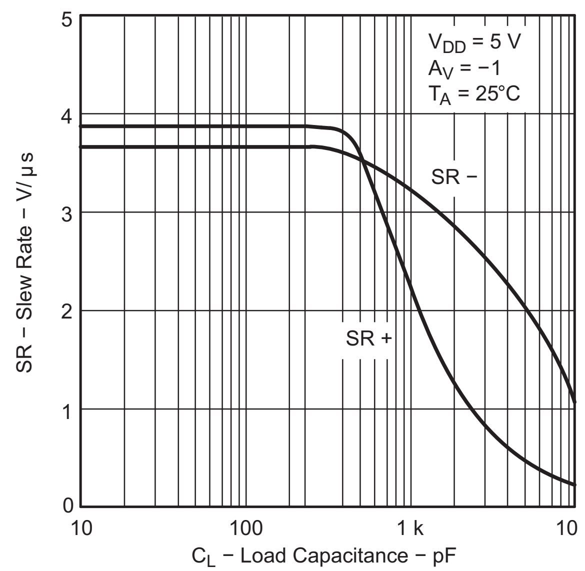

Figure 40.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

SLEW RATE vs FREE-AIR TEMPERATURE

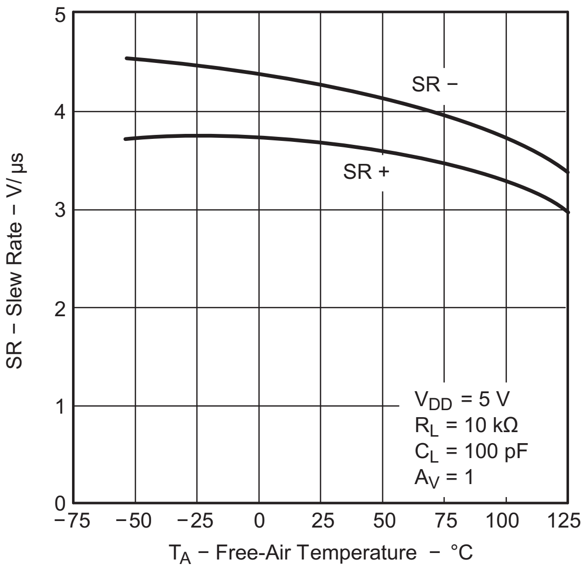

Figure 41.

INVERTING LARGE-SIGNAL PULSE RESPONSE

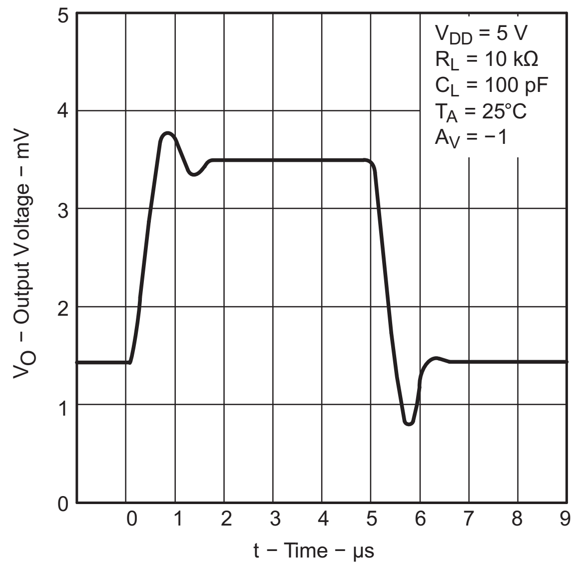

Figure 42.

INVERTING LARGE-SIGNAL PULSE RESPONSE

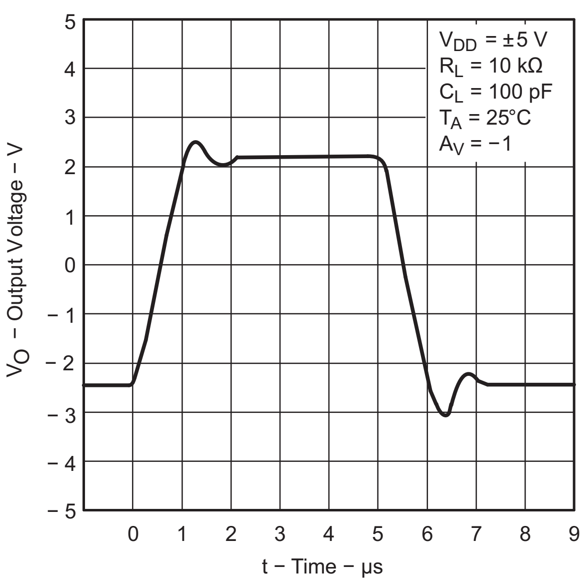

Figure 43.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

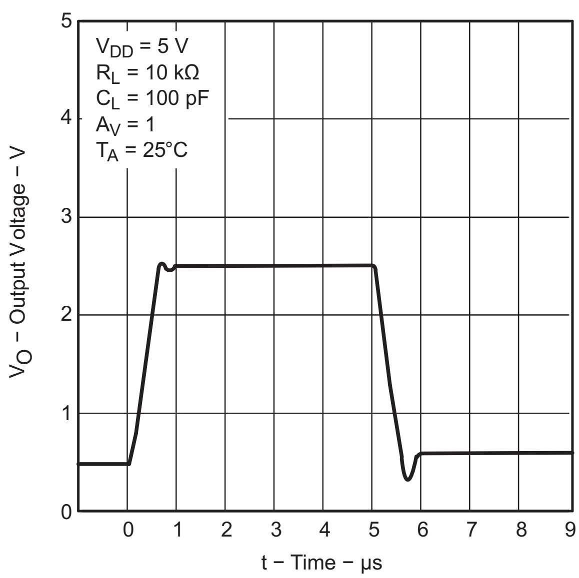

Figure 44.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

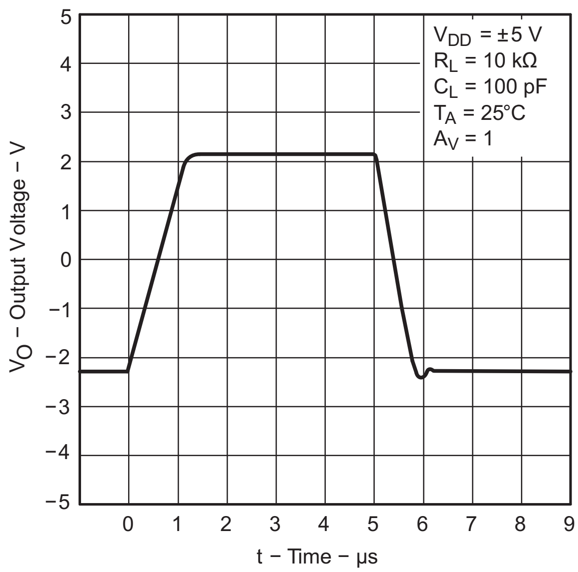

Figure 45.

INVERTING SMALL-SIGNAL PULSE RESPONSE

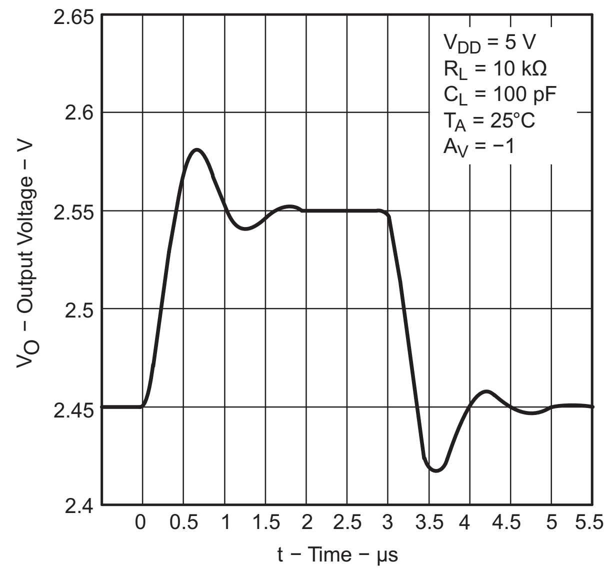

Figure 46.

INVERTING SMALL-SIGNAL PULSE RESPONSE

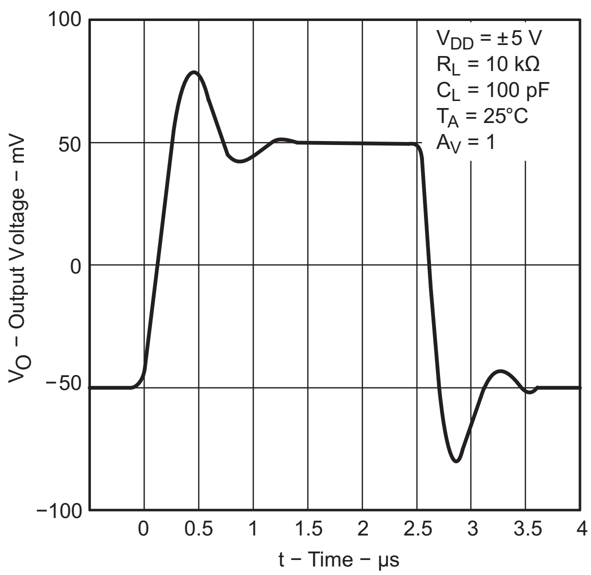

Figure 47.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

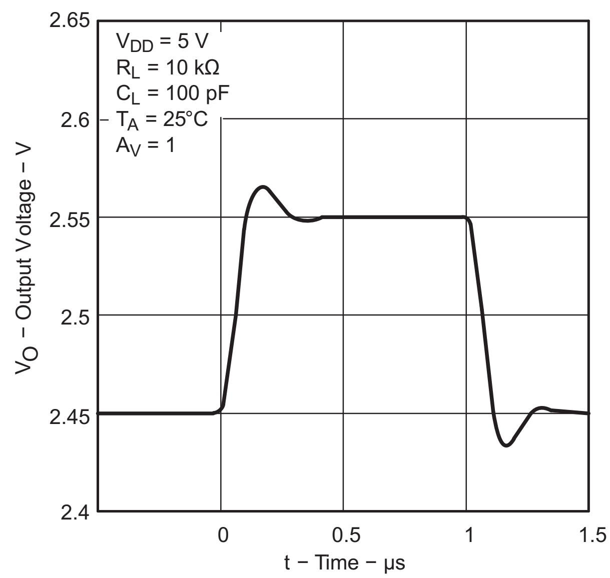

Figure 48.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

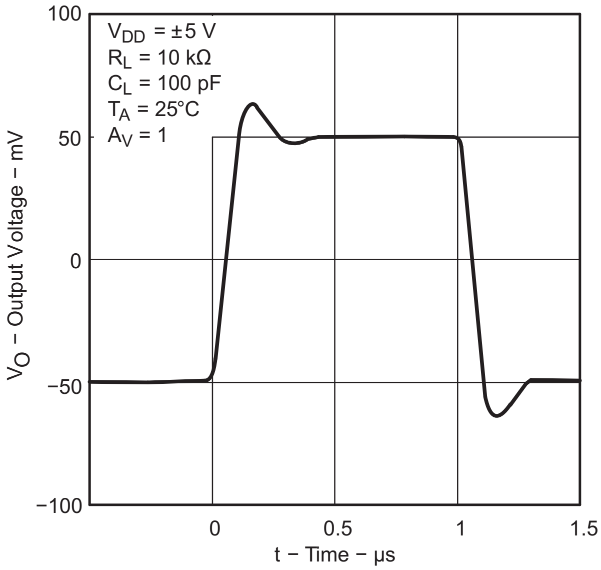

Figure 49.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

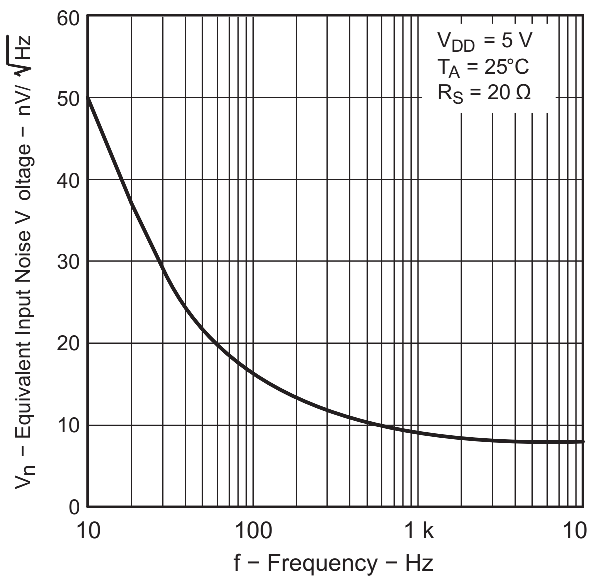

Figure 50.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

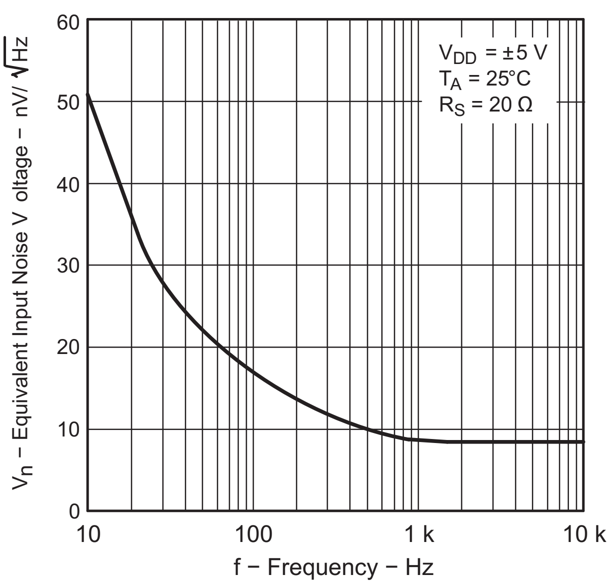

Figure 51.

NOISE VOLTAGE OVER A 10 SECOND PERIOD

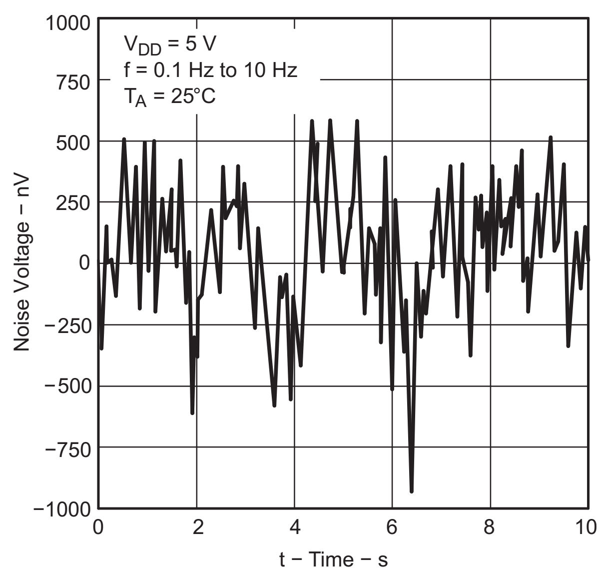

Figure 52.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

INTEGRATED NOISE VOLTAGE vs FREQUENCY

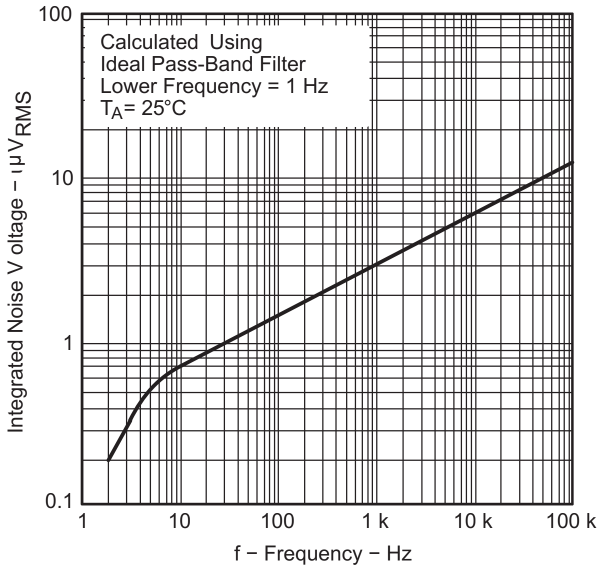

Figure 53.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

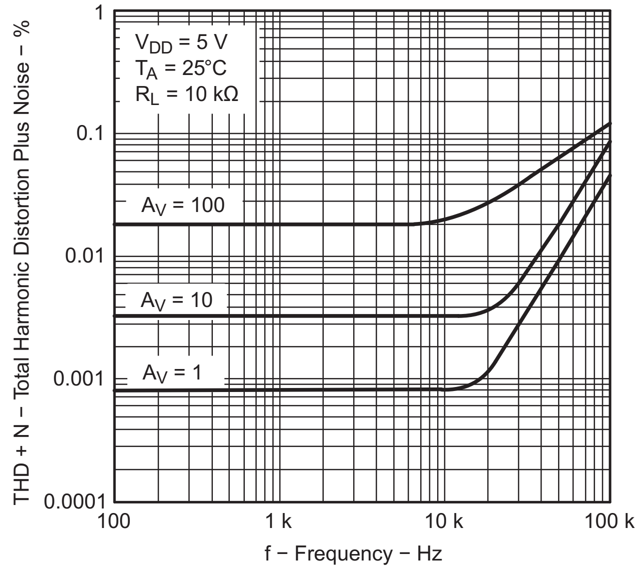

Figure 54.

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

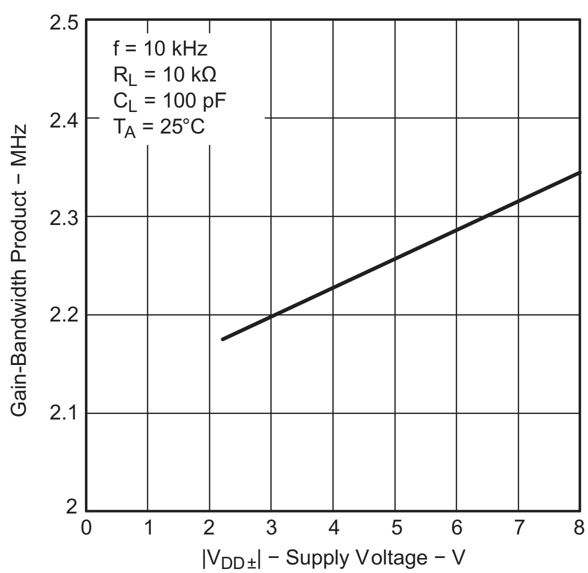

Figure 55.

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

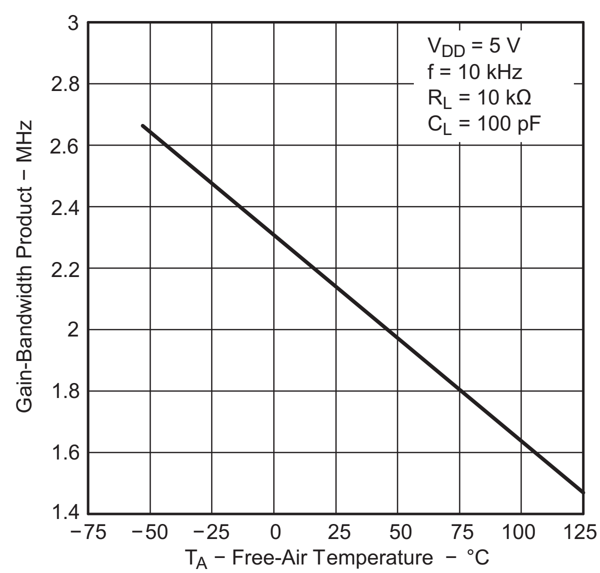

Figure 56.

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PHASE MARGIN vs LOAD CAPACITANCE

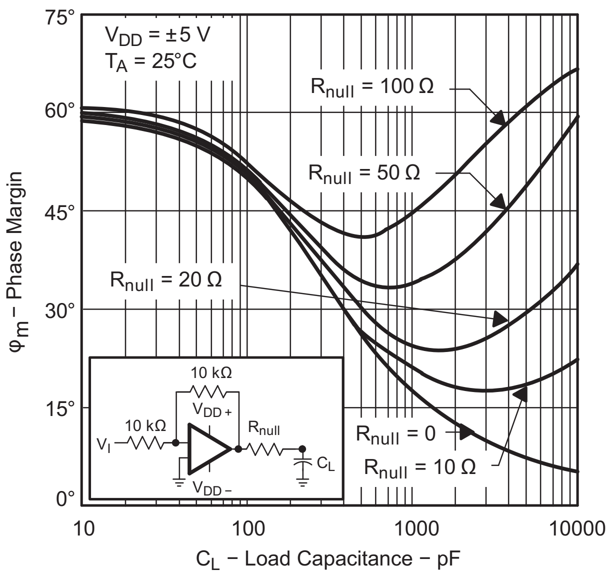


Figure 57.

GAIN MARGIN vs LOAD CAPACITANCE

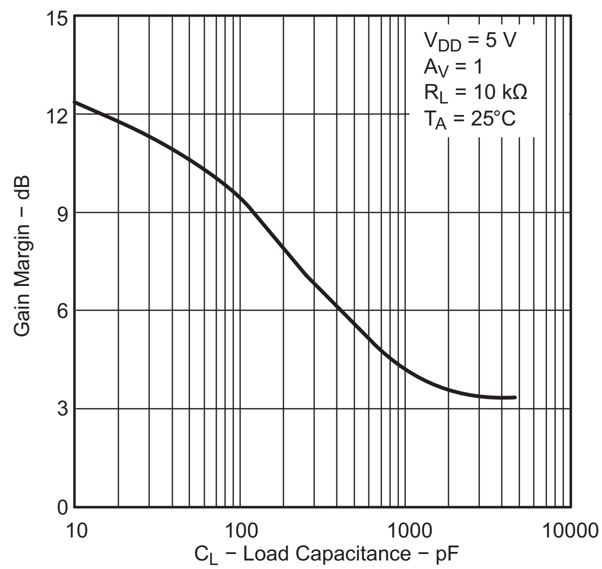


Figure 58.

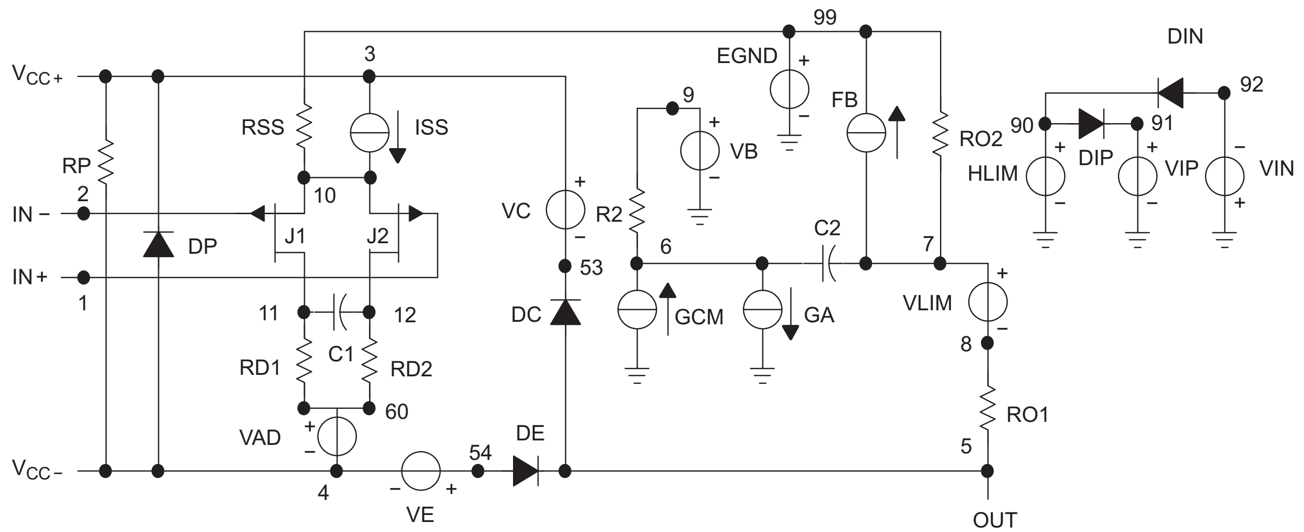
APPLICATION INFORMATION

Macromodel Information

Macromodel information provided was derived using Microsim Parts, the model generation software used with Microsim PSpice. The Boyle macromodel[(2)] and subcircuit in Figure 59 are generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

(2) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLC227x 1 2 3 4 5
        C1      11      1214E−12
        C2      6       760.00E−12
        DC      5       53DX
        DE      54      5DX
        DLP     90      91DX
        DLN     92      90DX
        DP      4       3DX
        EGND    99      0POLY (2) (3,0) (4,) 0 .5 .5
        FB      99      0POLY (5) VB VC VE VLP VLN 0
        + 984.9E3 −1E6 1E6 1E6 −1E6
        GA      6       011 12 377.0E−6
        GCM 0 6 10 99 134E−9
        ISS     3       10DC 216.OE−6
        HLIM    90      0VLIM 1K
        J1      11      210 JX
        J2      12      110 JX
        R2      6       9100.OE3

RD1     60      112.653E3
RD2     60      122.653E3
R01     8       550
R02     7       9950
RP      3       44.310E3
RSS     10      99925.9E3
VAD     60      4−.5
VB      9       0DC 0
VC 3 53 DC .78
VE      54      4DC .78
VLIM    7       8DC 0
VLP     91      0DC 1.9
VLN     0       92DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 59. Boyle Macromodels and Subcircuit

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REVISION HISTORY

Changes from Revision D (March 2009) to Revision E	Page
• Deleted ESD ratings table	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC2272AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2272QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2272QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2272QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2274AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274AQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples
TLC2274QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples
TLC2274QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples
TLC2274QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2272-Q1, TLC2272A-Q1, TLC2274-Q1, TLC2274A-Q1 :

- Catalog: TLC2272, TLC2272A, TLC2274, TLC2274A
- Enhanced Product: TLC2272A-EP, TLC2274-EP, TLC2274A-EP
- Military: TLC2272M, TLC2272AM, TLC2274M, TLC2274AM

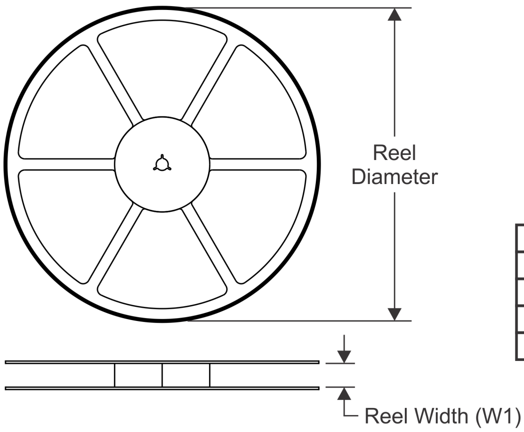
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

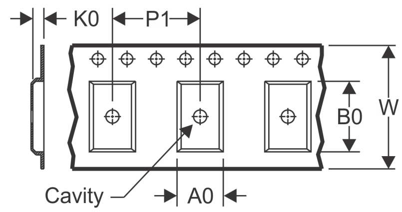
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

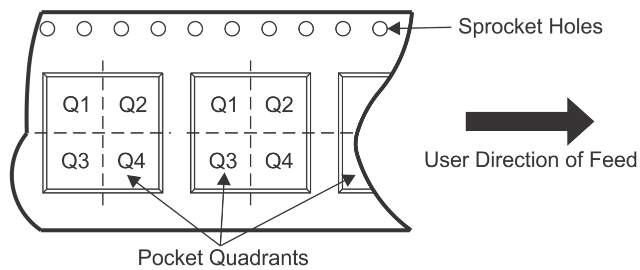


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

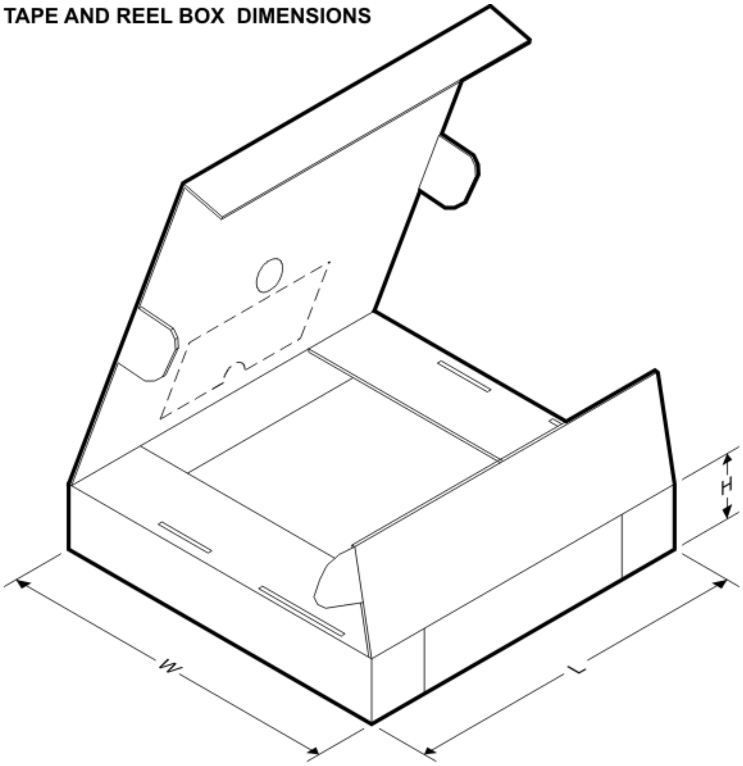
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

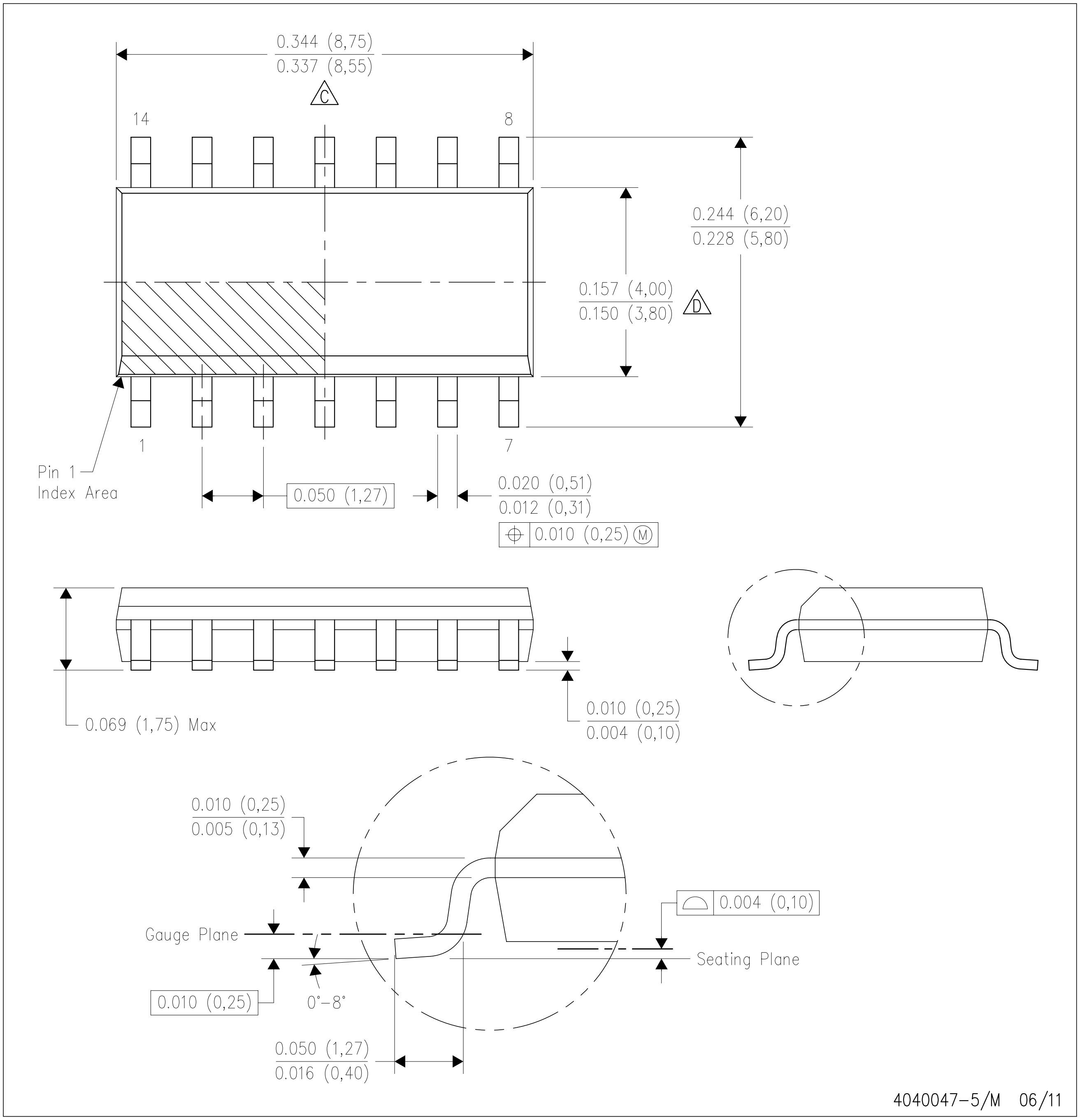
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

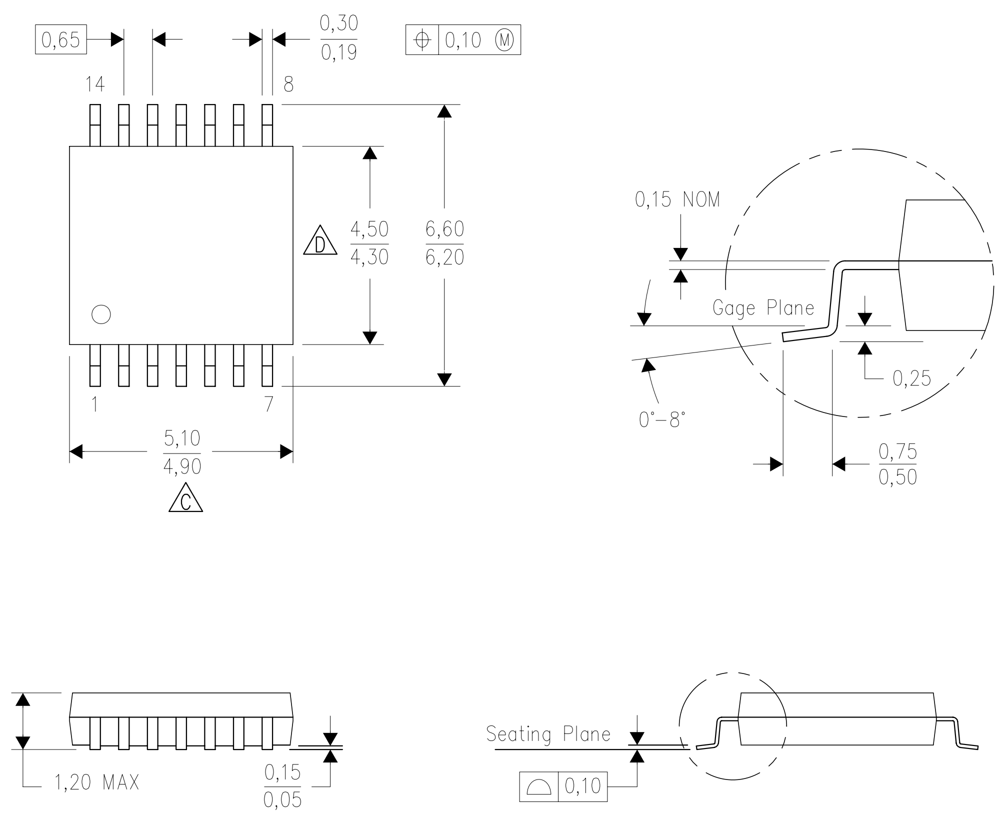
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



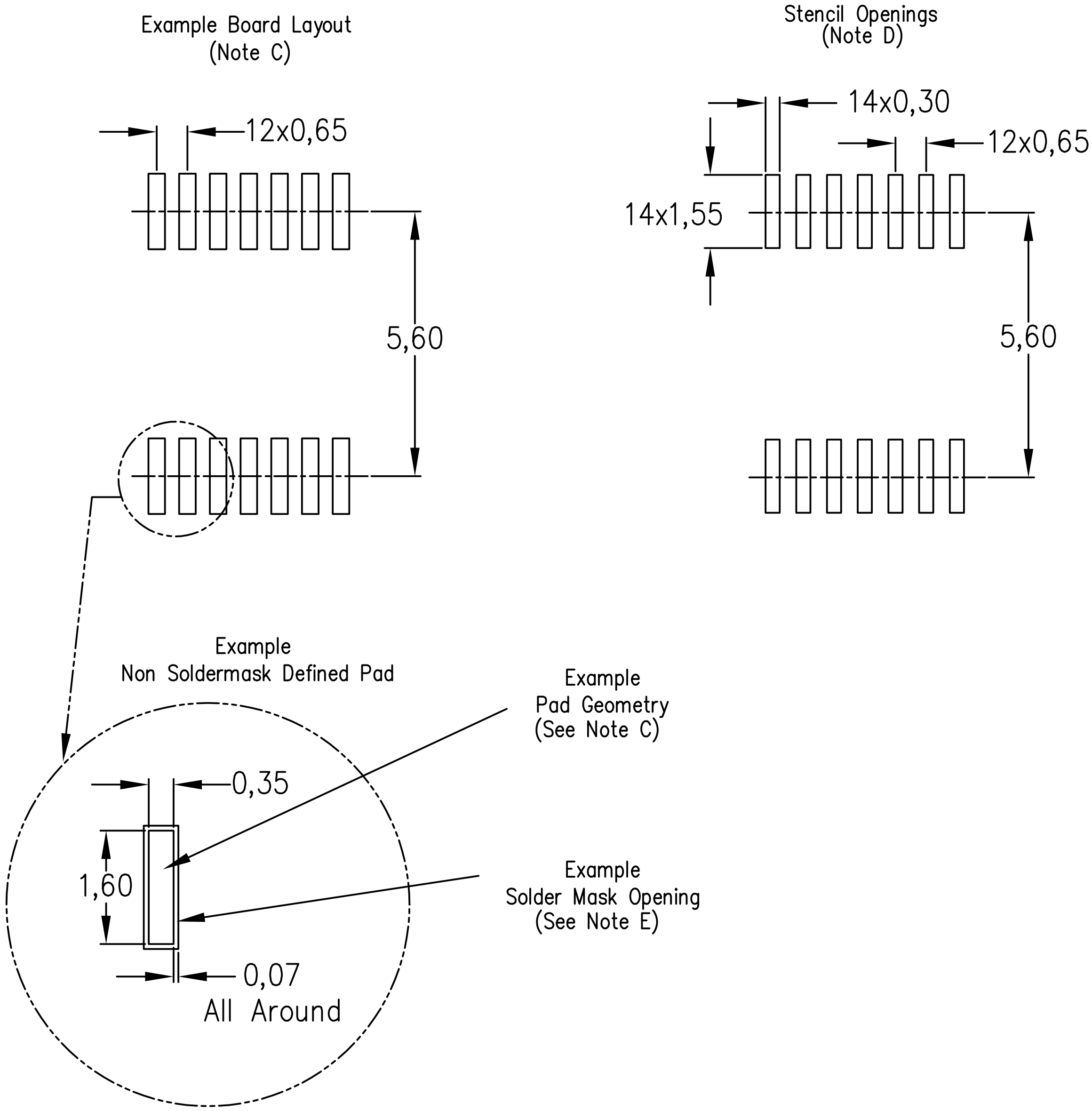
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

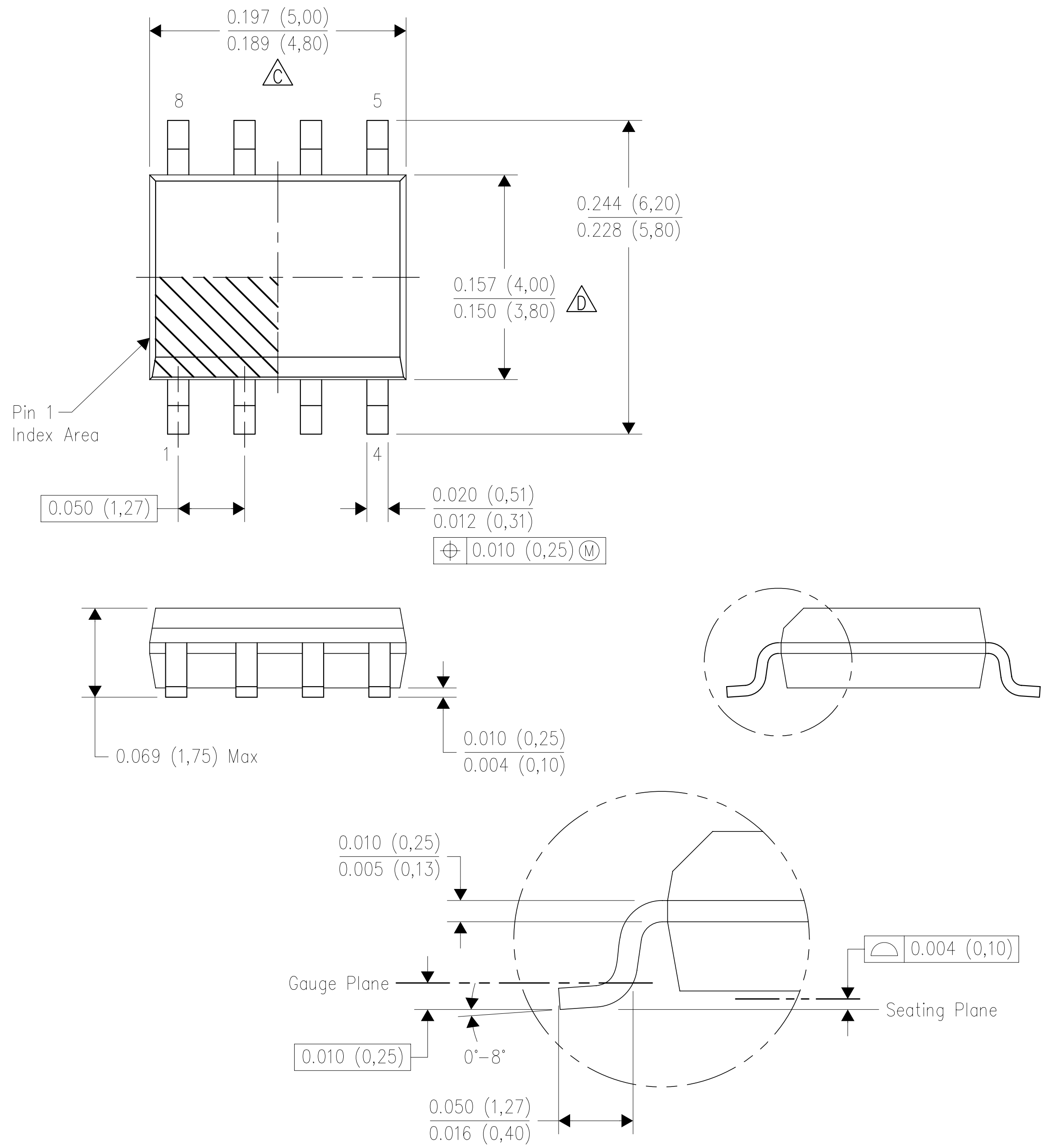
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211284-2/F 12/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

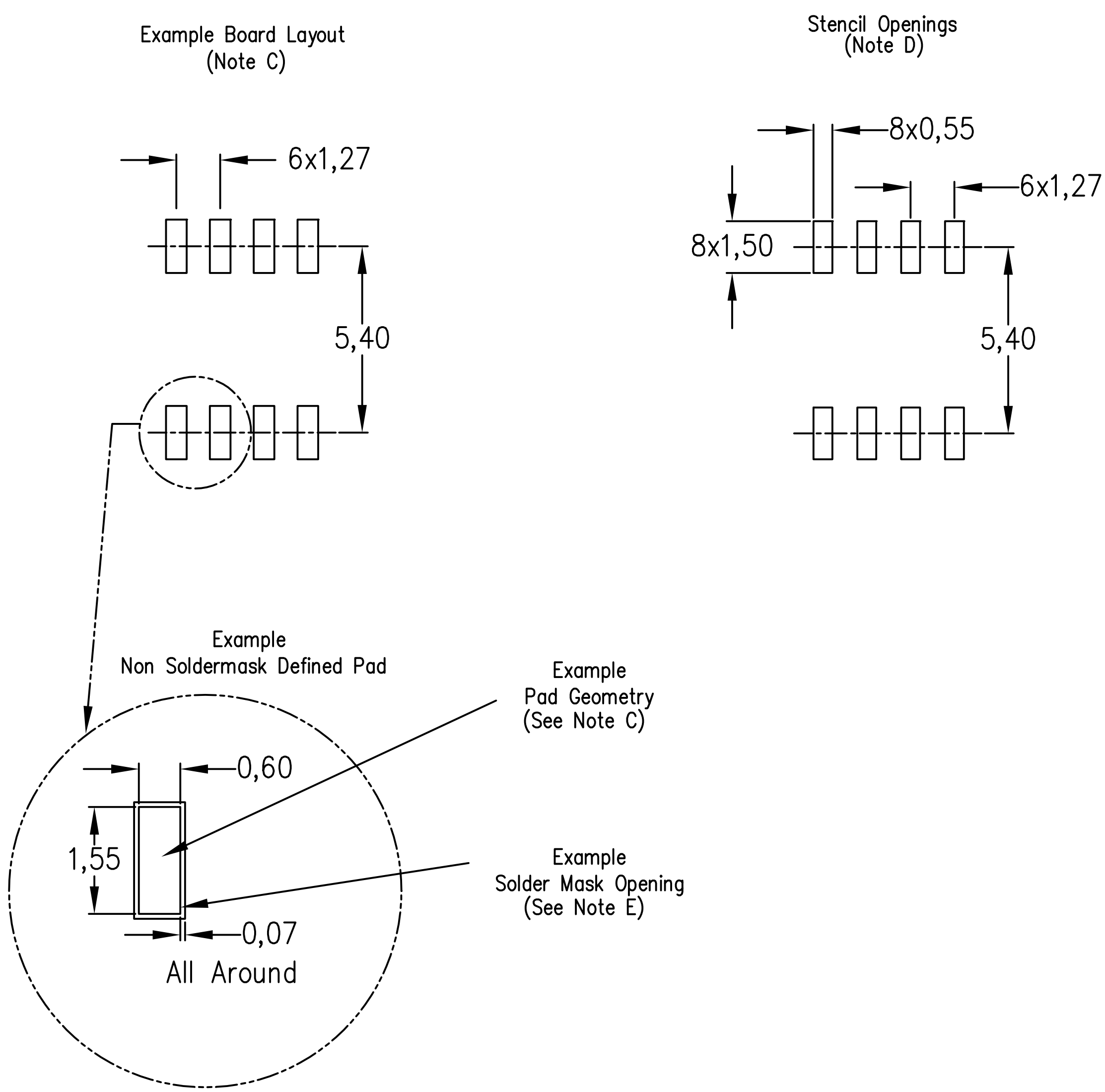
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

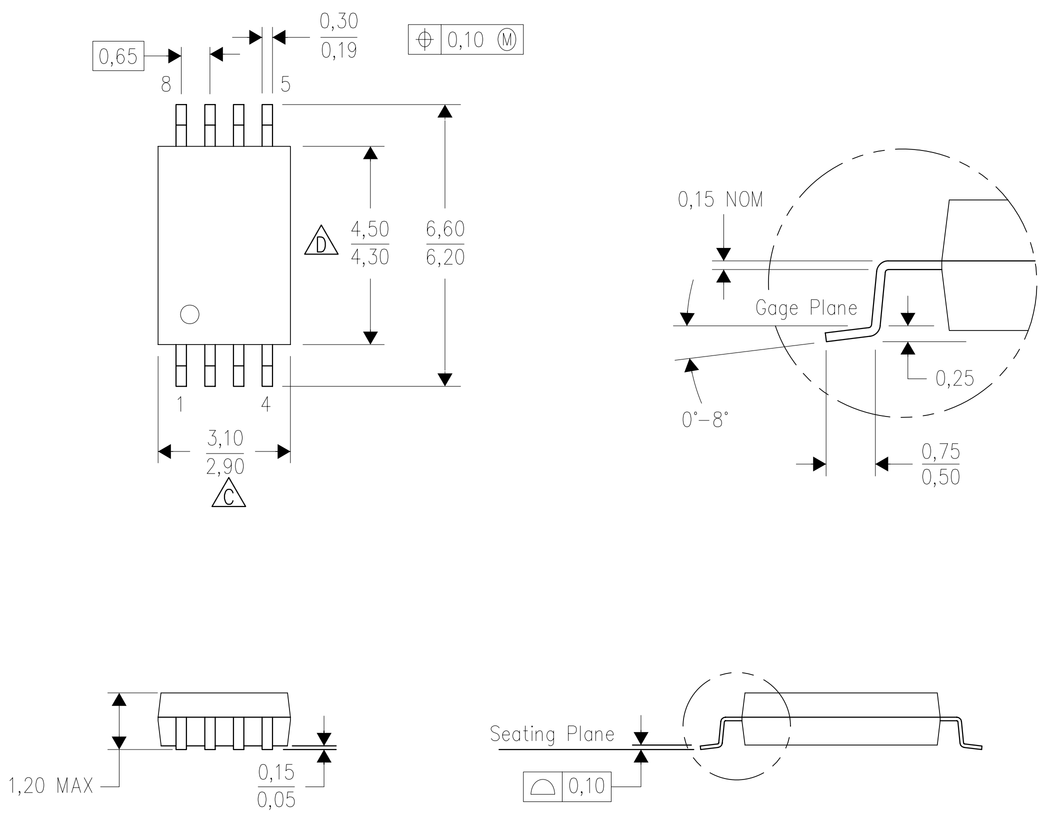
D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8) PLASTIC SMALL OUTLINE



4040064-2/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.