

Sharks Cove

Technical Specifications

Rev. 1.0

Revision History

Version	Changes
1.0	Initial External Release

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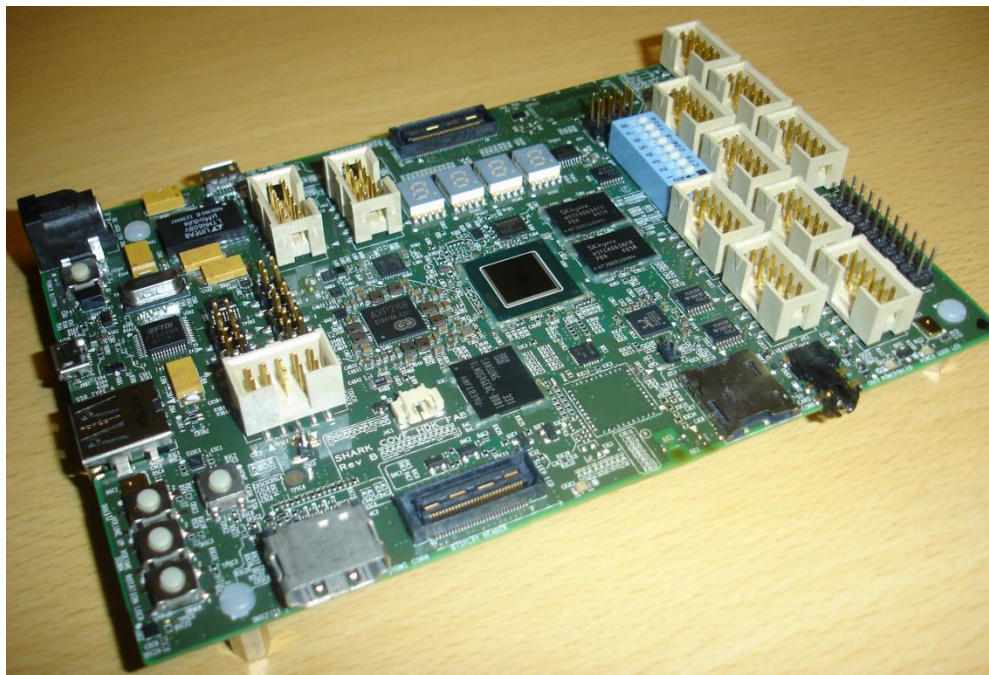
1 Introduction

1.1 Scope

The scope of this document is to illustrate the detailed specifications of the Sharks Cove board. It is intended to be used in conjunction with the Sharks Cove Developer's Guide posted at www.sharkscove.org/docs which describes procedures for powering up the board, updating the latest FW, pointers to OS installation procedures (Windows and Android), tools for system development, and also a troubleshooting table. Please use both documents to assure that board is used properly and best development experience is achieved.

1.2 Overview

The Sharks Cove Development Board is based on the Intel® Atom™ Processor Z3735G SoC that integrates the next generation Intel® processor core, Graphics, Memory Controller, and I/O interfaces into a single system-on-chip solution.



This board is intended for:

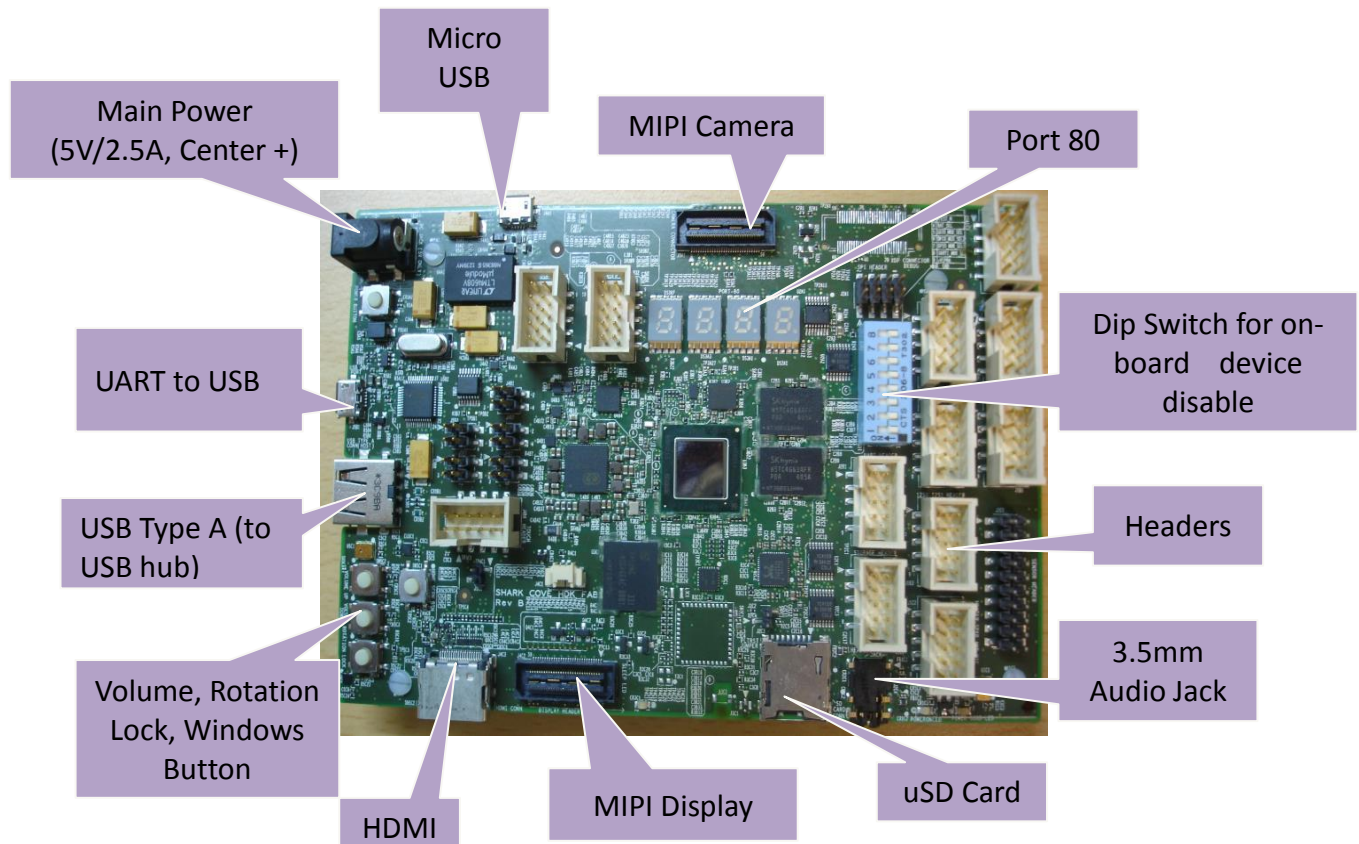
- Hardware developers enabling devices for x86 based tablets

- Developers of new products and market segments for Atom™ products (enabling new OSs, early development for new device types and form factors)

Sharks Cove is based on current Intel® Atom™ Processor based tablet designs and configured as the core of a tablet design, with the additional devices (e.g.: cameras, sensors, display, WiFi/BT) left off so that drivers for new versions of those devices can be developed for x86 compatible, Connected Standby Atom™ based platform designs.

2 Sharks Cove Development Board Snapshot

The heart of the board design is functionally similar to current tablet designs, and is powered by a 5 V / 2.5A wall adapter. Alternately, power can be supplied through Type B Micro-USB connector with a high quality 2.0 A+ rated USB charger. A full size HDMI port enables display connectivity, a 3.5mm stereo/mic. audio jack provides audio, and buttons typical to a tablet design are included. Serial output is converted to USB via the FTDI FT232 <http://www.ftdichip.com/Products/ICs/FT232R.htm>, providing serial debug output when connected to a host system with the proper drivers for your operating system. The board also provides connectivity for the interfaces available for current tablet designs through an array of pin headers.



3 Sharks Cove Development Board Device Key Features

The specifications for the Sharks Cove Development Board follow typical features seen in current tablets. Developers using the Sharks Cove Development Board to bring new devices to market have a flexible and accessible platform to work with that will closely match the configuration of commercial products. Please also refer the Sharks Cove Developers Guide posted the www.sharkscove.org/docs for details regarding bring up and usage of the board.

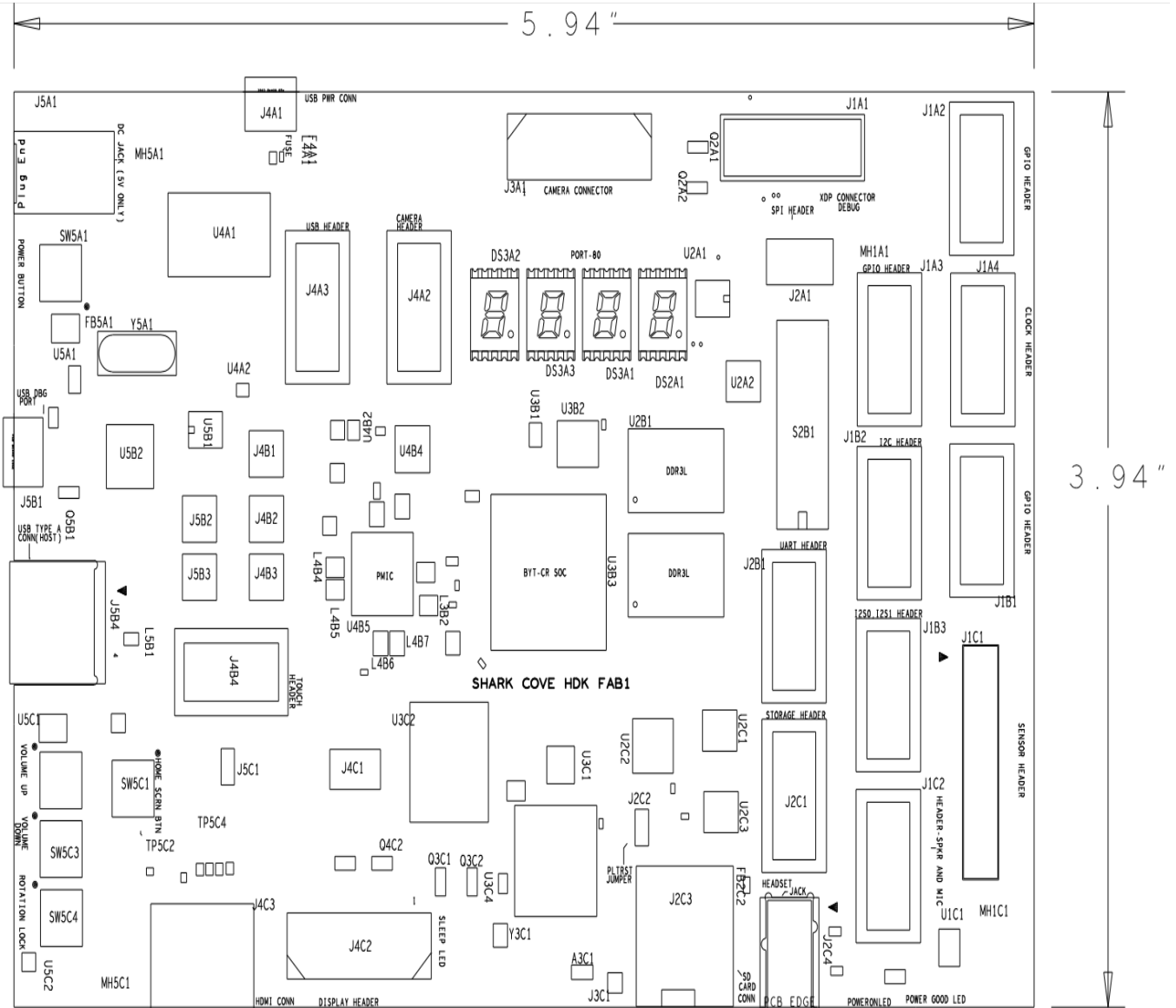
Interface		Feature Supported
SoC		Intel® ATOM™ Processor Z3735G , 2M Cache, 4 Core, 1.33GHz up to 1.88GHz
Memory		1GB DDR3L- Micron MT41K256M16HA-125M:E
eMMC		16GB eMMC 4.5 - KLMBG4GEAC-B001
SPI		2MB SPI NOR
PMIC		XPower PMIC - AXP288
Display	MIPI	Supported via MIPI Connector
	HDMI	Type A HDMI
USB	USB2.0	USB Port1 to full size Type-A connector USB Port2 to header
Audio	On board	Realtek ALC5640
		3.5mm Headset Jack and DMIC
	Header	Speaker and Microphone
Camera	MIPI	Supported through connector
LAN		Supported through USB to Ethernet
Camera		Supported through connector
Low Speed Interfaces	UART	Supported on header
Low Speed Interfaces	I2C	All I2C buses are supported on header
	I2S	Supported on HDR
High Speed Interfaces	SD I/F	microSD card
	SDIO	Supported on header
Debug Ports/ GPIOs	PORT 80/81	LED display
	UART	Supported through microUSB connector
		GPIOs routed to header
Platform Clocks		Supported on Header
S0ix Support		Supported (Virtual Battery Mode selection)
Buttons		Power Button, Rotation, Volume. UP/DN,

Interface		Feature Supported
Buttons, cont'd		Home Screen
LEDs		Power On, Power Good, S0ix
PCB Type		Type-3 6 Layer
Dimension		4x6inch

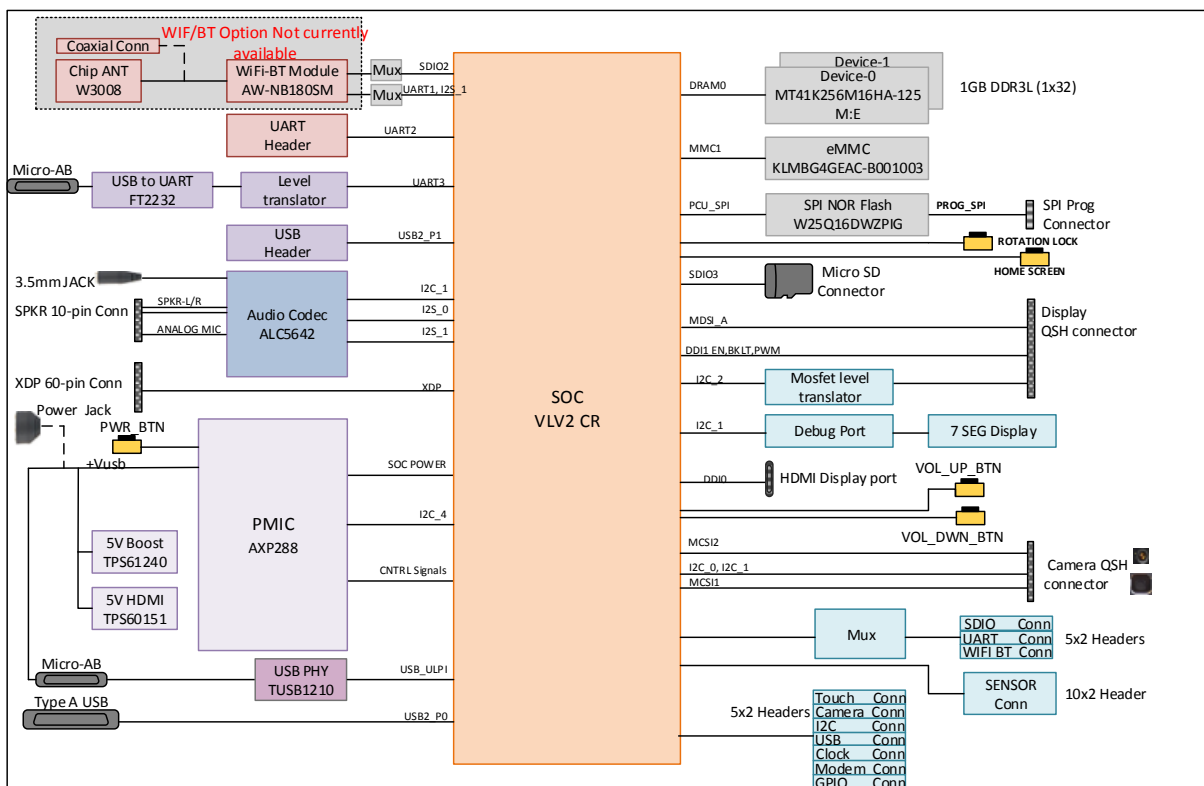
3.1 Limitations

- Two lanes of MIPI CSI Port 1 are supported. Cameras with higher resolution that require additional lanes cannot be supported
- When enabling a MIPI CSI panel, please assure that the main power supply jack is used and not the USB charger, since the MIPI panel may require a higher current rating.

4 Sharks Cove Development Board Layout with Reference designator of major components



5 Block Diagram



Note: WiFi/BT feature is not currently available

6 SoC Features Overview

6.1 Processor Core

- Quad-core SoC
- Up to four IA-compatible low power Intel® processor core
 - One thread per core
- Two-wide instruction decode, out of order execution
- On-die, 32 KB 8-way L1 instruction cache and 24 KB 6-way L1 data cache per core
- On-die, 1MB, 16-way L2 cache, shared per two cores
- 36-bit physical address, 48-bit linear address size support
- Supported C-states: C0, C1, C1E, C4, C6C, C6, C7

6.2 System Memory Controller

- Supports one Channel of DDR3L/L-RS
- 16 bit data bus for each channel
- Supports x32 and x64 DDR3L/L-RS SDRAM device data width

- Supports DDR3L/L-RS with 1333 MT/s data rate
- Memory bandwidth supported is 10.6 GB/s (for x64 data width 1333 MT/s single channel)
- Memory bandwidth supported is 5.3 GB/s (for x32 data width 1333 MT/s single channel)
- Supports different physical mappings of bank addresses to optimize performance
- Out-of-order request processing to increase performance
- Aggressive power management to reduce power consumption
- Proactive page closing policies to close unused pages
- Supports soldered down DRAM devices

6.3 Display Controller

- Support 1 MIPI DSI port
 - MIPI DSI resolution supported: 1920x1200
- Support 2 DDI port to enable HDMI 1.4
 - HDMI resolution supported: 1080p
- Support Audio on HDMI
- Supports Intel® Display Power Saving Technology (DPST) 6.0, Panel Self Refresh (PSR) and Display Refresh Rate Switching Technology (DRRS)

6.4 Graphics and Media Engine

- Intel® 7th generation (Gen 7) graphics and media encode/decode engine
- VED video decoder in addition to Gen 7 Media decoder
- Graphics Burst enabled through energy counters
- Supports DX*11, OpenGL 3.0 (OGL 3.0), OpenCL 1.1 (OCL 1.1), OpenGLES 2.0
- GPU shader is capable of up to 8 gigaflops
- 4x anti-aliasing
- Full HW acceleration for decode of 1080p60 (H.264, VP8, WMV9, VC1)
- Full HW acceleration for encode of 1080p30 (H.264, VP8, WMV9, VC1)
- Intel® Wireless Display (WiDi) support

6.5 Image Signal Processor

- Support up to two MIPI CSI ports
- Support for up to 8MP sensors
- Supports 1080p30 Video recording

6.6 USB xHCI Controller

- Supports 2 USB 2.0/1.1 Host port (Note : Only one host controller (xHCI or EHCI) can be used.)

6.7 USB EHCI Controller

- Supports USB 1.1 to 2.0 Host port.

6.8 USB 2.0 (ULPI)Device Mode

- Supports one USB 2.0 SS port with USB device compatibility

6.9 Audio Controllers

Low Power Engine (LPE) Audio

- LPE is a complete audio solution based on an internal audio processing engine, which
 - Includes 2 I2S Output ports.
- I2S and DDI with dedicated DMA
- MP3, AAC, AC3/DD+, WMA9, PCM (WAV)

6.10 eMMC, SDIO & SD

- Supports one SDIO 3.0 controller
- Supports one eMMC 4.5 controller
- Supports one SDXC controller

6.11 Intel® Trusted Execution Engine (Intel® TXE)

- Intel® TXE system contains a security engine and additional hardware security features that enable a secure and robust platform.
- The major security features are:
 - Isolated execution environment for crypto operations (SKU-enabled)
 - Theft deterrence
 - Supports secure boot - with customer programmable keys to secure code

6.12 Serial I/O (SIO)

- Controller for external devices via SPI, UART, I2C or PWM
- Each port is multiplexed with general purpose I/O for configurations flexibility
- Supports up to 5 I2C, 2 HSUART, 2 PWM, 1 SPI interface

6.13 Platform Control Unit (PCU)

- The platform controller unit is a collection of HW blocks, including UART, debug/boot SPI and Intel® legacy block (iLB), that are critical to implement a Windows* compatible platform.
- Some of its key features are:
 - Universal Asynchronous Receiver/Transmitter (UART) with COM1 interface
 - A Serial Peripheral Interface (SPI) for Flash only - stores boot FW and system configuration data
- Intel® Legacy Block (iLB) supports legacy PC platform features
 - RTC, Interrupts, Timers, General Purpose I/Os (GPIO).

Board Power delivery details:

Supply rail name	Total Current (in mA)	Voltage (in V)	Interface/devices	Individual current (in mA)	Comments
+V2P8_ALDO1	500	2.8	J3A1 Camera connector	500	Maximum current available on these two connector
		2.8	J5B2.1 (Header connector)		
+V3P3SX_DLDO3	300	3.3	J4C2 Display Connector	XX	Current consumed by devices should not exceed 0.3A
		3.3	J5B2.2 (Header connector)		
+V3P3A_PLT	200	3.3	SSD driver (MAX6958)	30	
		3.3	SoC	70	
		3.3	J4B2.1 (Header connector)	100	Remaining current available on the connector
+VSYS (4.2V)	2000	VBAT	J3A1 Camera Connector	XX	Current that can be used from 2A charger
		VBAT	Ext. regulator (TPS6015)	125	
		VBAT	Ext. regulator (TPS61240)	768	
		VBAT	J4C2 Display Connector	XX	Current that can be used from 2A charger
		VBAT	USB PHY (TUSB1210)	65	
		VBAT	Audio codec	700	If speaker is connected or else no current consumed by codec
		VBAT	J4B2.2 (Header	XX	Current that can

		(4.2V)	connector)		be used from 2A charger
+V3P3_GPLDO1	150	3.3	SoC	5	
		3.3	J5B3.1 (Header connector)	145	Remaining current available
+V3P3SX_ALDO2	300	3.3	J4C2 Display connector	Depends on the device connected	Need to ensure the current consumed by devices connected on these headers do not exceed total current
			J4B4.4 Header Connector		
			J5B3.2 (Header connector)		
+V_ELDO1	400	1.8	J4B3.2	400	Available on the connector
+V1P8A	1500	1.8	Display connector	XX	1. Total max current is 1.5A. 2. Interfaces connector to 1.8V and its current required is mention in the table. 3.XX means connector depends on the external devices connected
		1.8	Audio codec	10	
		1.8	USB PHY (TUSB1210)	30	
		1.8	PSS chip	3	
		1.8	SoC chip	34.3	
		1.8	SPI NOR chip	25	
		1.8	MUX TI-TS3A5018	1	
		1.8	EMMC chip	150	
+V3P3_DLDO4	500	3.3	J4B1.1 (Header connector)	XX	Maximum Current available

9 Items in the Package

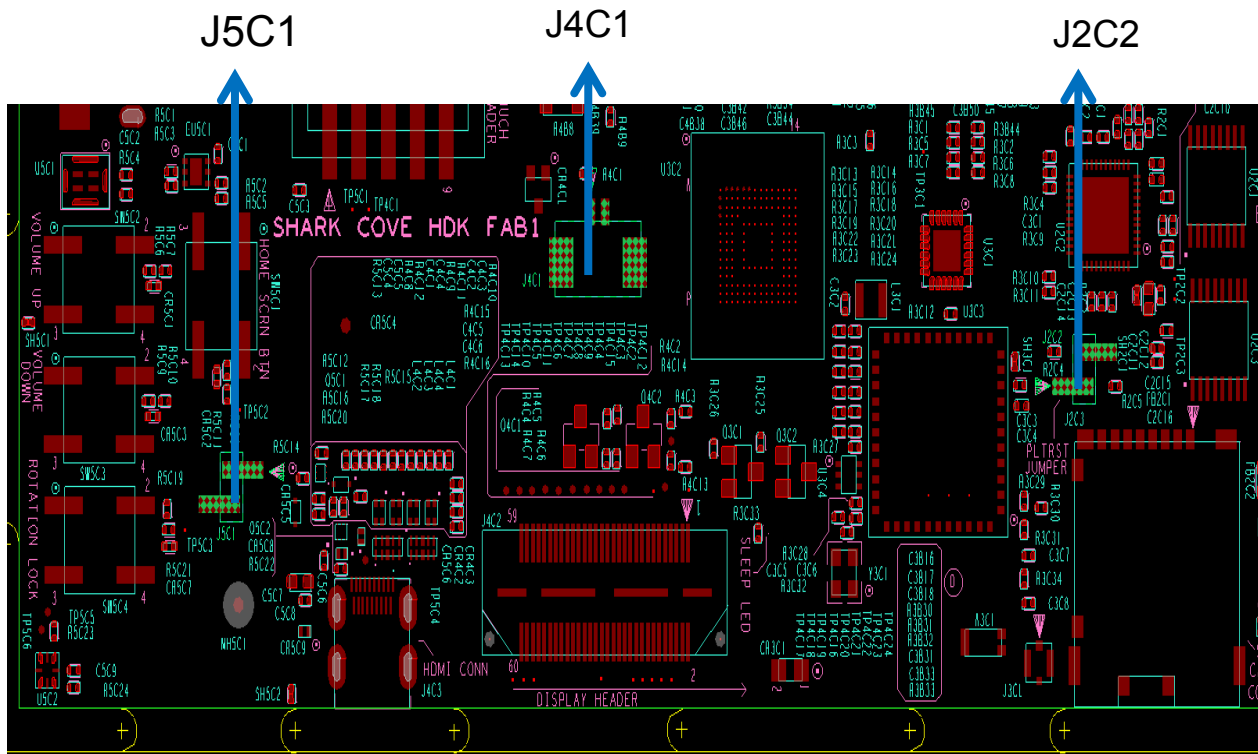
- Sharks Cove development board
- AC/DC Adapter wall Adapter Input: 100-250V Output: 5V, 2.5A, Center +

9.1 Suggested Accessories

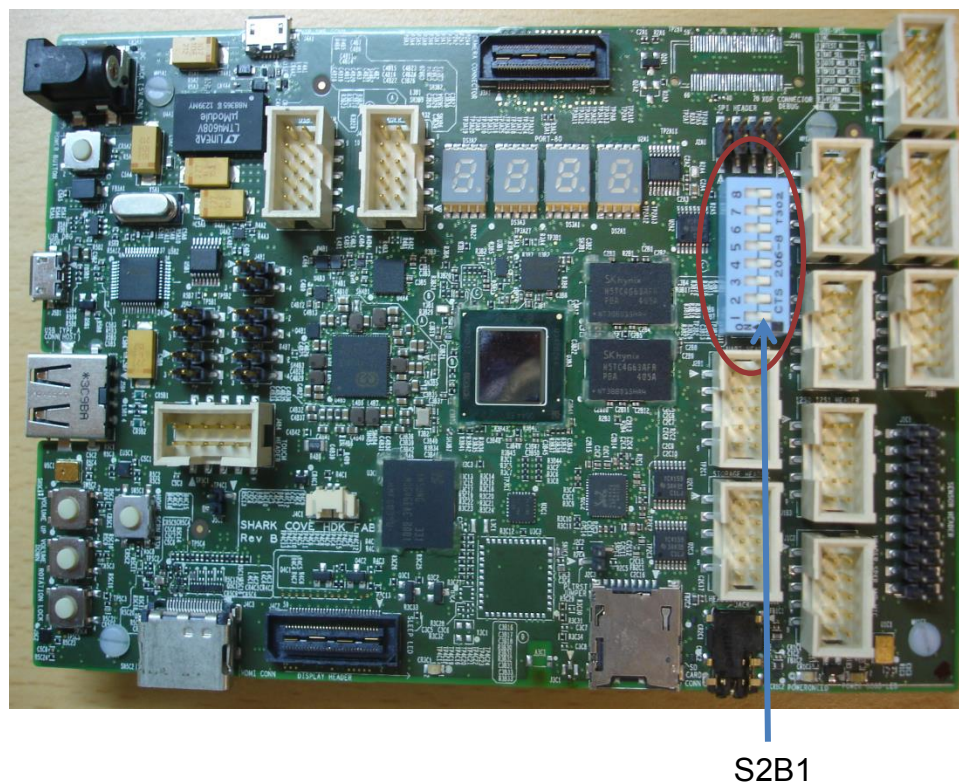
- USB Hub to expand USB port for KB/Mouse, USB to Ethernet or USB WiFi module, and USB thumb drive
- USB to Ethernet Adapter or USB WiFi module for connectivity

10 Jumper settings

Ref Des	Jumper Position	Default	Description
J4C1	1-2	Default	Coin Cell connected
J5C1	1-X	Default	PMU_PWRBTN_N
J2C2	1-X	Default	PLTRST_N



11 Switches

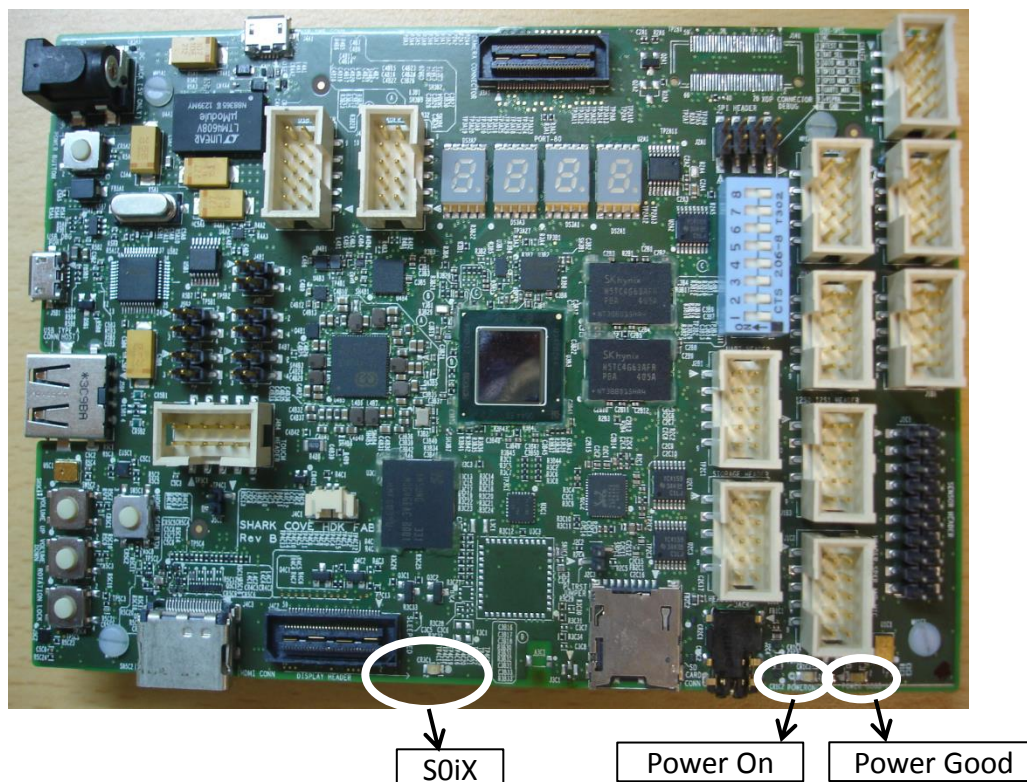


Ref Des	Switch Position	Default	Description
S2B1	2-X	Default	Logic '1' RTEST_N input to SoC
	4-16		Logic '0' RTEST_N input to SoC
	4-X	Default	Logic '1' BAT_SEL input to SoC
	4-13		Logic '0' BAT_SEL input to SoC
	5-X	Default	SDIO_MUX_SEL SET TO '0' SoC SDIO port mapped to WIFI SDIO port
	5-12		GPIO_MUX_SEL1 SET TO '1' SoC SDIO port mapped to External Header J2C1
	6-X	Default	GPIO_MUX_SEL2 SET TO '0' SoC GPIOs drives the WIFI and Audio Codec Control lines
	6-11		GPIO_MUX_SEL1 SET TO '1' SoC GPIOs drives the External Header Ios
	7-X	Default	GPIO_MUX_SEL1 SET TO '0' SoC GPIOs drives the WIFI Control lines
	7-10		GPIO_MUX_SEL1 SET TO '1' SoC GPIOs drives the External Header IOs

8-X	Default	UART1_MUX_SEL SET TO '0' SoC UART1 port mapped to WIFI UART port
8-9		UART1_MUX_SEL SET TO '1' SoC UART1 port mapped to external Header J2B1

Note: Highlighted rows are switch setting when WiFi/BT device is present on the board. Board is not currently shipped with WiFi/BT module.

12 Platform LED Indications

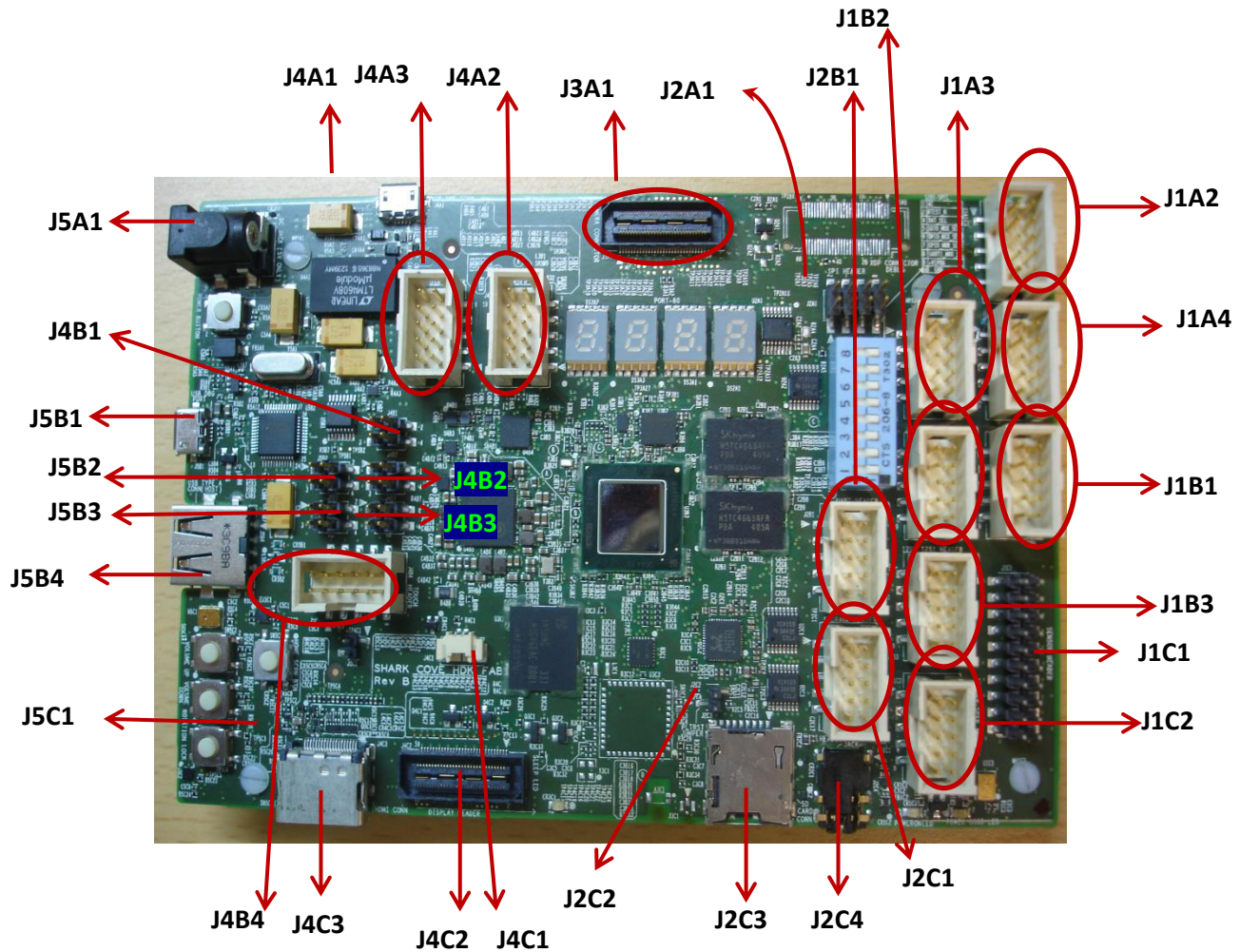


POWER ON LED

- Power on LED is directly connected to main supply. Power on LED will glow when DC adapter or USB based adapter is plugged in.
- POWER GOOD LED
 - Power good LED is connected to the COREPWROK pin of PMIC which is an output. COREPWROK is an active high dedicated output signal. COREPWROK asserts when all voltage rails to the SOC that are supposed to be on in S0 and S0iX states are within 10% of its nominal voltage.
- S0iX LED

- S0IX LED is connected to PMC_SLP_S0IX# pin of SoC.. This pin indicates S0IX state entry upon assertion (SLP_S0IX=LOW) and exit upon de-assertion (SLP_S0IX_B=HIGH)
- Buttons supported on board:
 - Power ON/OFF
 - Home Screen
 - Volume Up
 - Volume Down
 - Rotation Lock

13 SHARKS COVE BOARD CONNECTOR DETAILS



Sl.No.	Connector Refdes	Description
1	J1A2	2x5 Header for MODEM signals
2	J1A3	2x5 Header for audio, volume up/down signals
3	J1A4	2x5 Header for CLOCK signals
4	J1B1	2x5 Header for WIFI BT signals
5	J1B2	2x5 Header for I2C signals
6	J1B3	2x5 Header for I2S signals
7	J1C1	2x10 Header for SENSOR signals
8	J1C2	2x5 Header for MIC and SPEAKER signals
9	J2A1	2x4 Header for SPI Flash program
10	J2B1	2x5 Header for UART signals
11	J2C1	2x5 Header for SDIO signals
12	J2C2	1x2 Header for PLTRST signal

13	J2C3	Micro SDCARD Connector
14	J2C4	6 PIN Audio Jack
15	J3A1	60 PIN Camera connector
16	J4A1	Power Input Micro USB AB connector
17	J4A2	2x5 Header for Camera signals
18	J4A3	2x5 Header for USB signals
19	J4B1	2x2 Header for Power rails
20	J4B2	2x2 Header for Power rails
21	J4B3	2x2 Header for Power rails
22	J4B4	2x5 Header for TOUCH signals
23	J4C1	Coin Cell Header
24	J4C2	60 pin Display Connector
25	J4C3	HDMI Connector
26	J5A1	5V Power Jack
27	J5B1	Debug Connector: Micro USB AB connector
28	J5B2	2x2 Header for Power rails
29	J5B3	2x2 Header for Power rails
30	J5B4	USB Type A Connector
31	J5C1	1x2 Header for power button

Debug Interface:

J5B1 Debug message trace through UART to USB ports. Please refer to Sharks Cove Developer's Guide for more information on operation of the debug interface.

J2C3 – SD card connector

Micro SD card connector is used. SDMMC3 port from VLV2 SOC is used for connecting to a uSD card for external storage, which is powered by PMIC.

J2C4 – Audio headset connector

Headset jack is used that supports LRGM type of headsets. Detection on ring2 and is default OPEN.

14 Headers on the board

GPIO Signals are Brocken out of SoC and connected to headers for Firmware enabling of different interfaces.

J4A2:10 pin Header (Camera sideband signal)

J4A2 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	GPIO_S0_NC[20]	FLASH_TORCH	_SB.GPO1 {0x14}	Camera torch enable signal
2	GPIO_S0_NC[21]	CAMERA_1_PD	_SB.GPO1 {0x15}	Rear camera power down signal
3	GPIO_S0_NC[16]	FLASH_RESET_N	_SB.GPO1 {0x10}	Camera Flash reset signal
4	GPIO_S0_NC[22]	CAMERA_2_PD	_SB.GPO1 {0x16}	Front camera power down signal
5	GPIO_S0_NC[19]	FLASH_TRIGGER_N	_SB.GPO1 {0x13}	Camera Flash trigger signal
6	GPIO_S0_NC[17]	CAM1_RESET_N	_SB.GPO1 {0x11}	Rear camera reset signal
7	NA	OPEN		
8	GPIO_S0_NC[18]	CAM2_RESET_N	_SB.GPO1 {0x12}	Rear camera reset signal
9	NA	GROUND		Ground
10	NA	GROUND		Ground

J1A2: 10 pin Header (Modem signals)

J1A2 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	NA	+V1P8A		1.8V power rail
2	NA	+VSYS (4.2V)		4.2V power rail
3	GPIO_S5[29]	MODEM_BB_RESET_N	_SB.GPO2 {0x1D}	Modem Reset Signal
4	GPIO_S0_NC[23]	MODEM_POWER_ON	_SB.GPO1 {0x17}	Modem Power On Signal
5	GPIO_S5[30]	MODEM_CORE_DUMP	_SB.GPO2 {0x1E}	Modem Core dump
6	PMC_PLT_CLK[4]	MODEM_POWER_OFF		Modem Power Off Signal
7	GPIO_S5[28]	MODEM_RST_OUT	_SB.GPO2 {0x1C}	Modem Reset out Signal
8	GPIO_S5[22]	GPS_WAKEUP	_SB.GPO2 {0x16}	GPS wake up signal
9	NA	GROUND		Ground
10	NA	GROUND		Ground

J4B4: 10 pin Header (Touch Signals)

J4B4 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	NA	+V1P8A		1.8V power rail
2	NA	GROUND		Ground
3	GPIO_S0_NC[26]	TOUCH_RESET_N	_SB.GPO1 {0x1A}	Display Touch reset signal
4	NA	+V3P3SX_ALDO2_HDR		3.3V Analog LDO rail
5	GPIO_S5[3]	TOUCH_INT_N	_SB.GPO2 {0x3}	Display Touch Interrupt signal
6	SIO_I2C3_DATA	I2C_3_SDA	_SB.I2C4	I2C Data line for I2C controller 3
7	PCU_SPI_CS#[1]	GPI_SOC_HOMESCRN		Home screen signal
8	SIO_I2C3_CLK	I2C_3_SCL	_SB.I2C4	I2C Clock line for I2C controller 3
9	NA	GROUND		Ground

J4B4 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
10	NA	GROUND		Ground

J1A4: 10 pin Header (Clocks)

J1A4 pin#	SoC GPIO PIN NAME	SIGNAL NAME	Comments
1	PMC_PLT_CLK[0]	HDR_PLT_CLK0_CAM1	Platform Clock for Camera
2	NA	GROUND	
3	PMC_PLT_CLK[1]	HDR_PLT_CLK0_CAM2	Platform Clock for Camera
4	NA	GROUND	Ground
5	NA	OPEN	
6	PMC_PLT_CLK[4]	MODEM_POWER_OFF	Modem Power Off signal or can be configured as Clock
7	NA	GROUND	
8	PMC_PLT_CLK[3]	HDR_CODEC_MCLK	Audio Codec MCK
9	NA	GROUND	
10	NA	OPEN	

J1C1: 20 pin Header (Sensor signals)

J1C1 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	NA	+V3P3A_PLT		3.3V Power Rail
2	NA	+VSYS (4.2V)		4.2V Power Rail
3	NA	+V2P8_ALDO1		2.8V analog power rail
4	NA	+V1P8A		1.8V Power Rail
5	NA	GROUND		Ground
6	NA	GROUND		Ground
7	GPIO_S5[23]	ACCEL_INT_N	_SB.GPO2 {0x17}	Accelerometer Interrupt signal
8	GPIO_S5[25]	HDR_GYRO_INT1	_SB.GPO2 {0x19}	Gyroscope Interrupt signal
9	GPIO_S5[24]	HDR_COMPASS_DRDY	_SB.GPO2 {0x18}	Ready signal
10	GPIO_S5[26]	HDR_GYRO_INT2	_SB.GPO2 {0x1A}	Gyro Interrupt signal
11	NA	GROUND		Ground
12	NA	GROUND		Ground
13	SIO_I2C2_DATA	HDR_I2C_2_SDA	_SB.I2C3	I2C Data line for I2C controller 2
14	GPIO_S5[6]	HDR_PROX_ALS_INT_N	_SB.GPO2 {0x6}	AMBIENT LIGHT SENSOR Interrupt signal
15	SIO_I2C2_CLK	HDR_I2C_2_SCL	_SB.I2C3	I2C clock line for I2C controller 2
16	USB_OC#[0]	SAR_PROX_INT		If this signal needs to be used for SAR_PROX_INT then need to be configured as Interrupt signal. Rework to

				be done on the board follow note1
17	NA	OPEN		
18	SIO_PWM[1]	SAR_PROX_RST		Proximity Sensor Reset signal
19	NA	OPEN		
20	NA	OPEN		

Note1: Need to install resistor R3A4 and uninstall R3A3

J1A3: 10 pin Header (VOL.BTN/Interrupts/PMU)

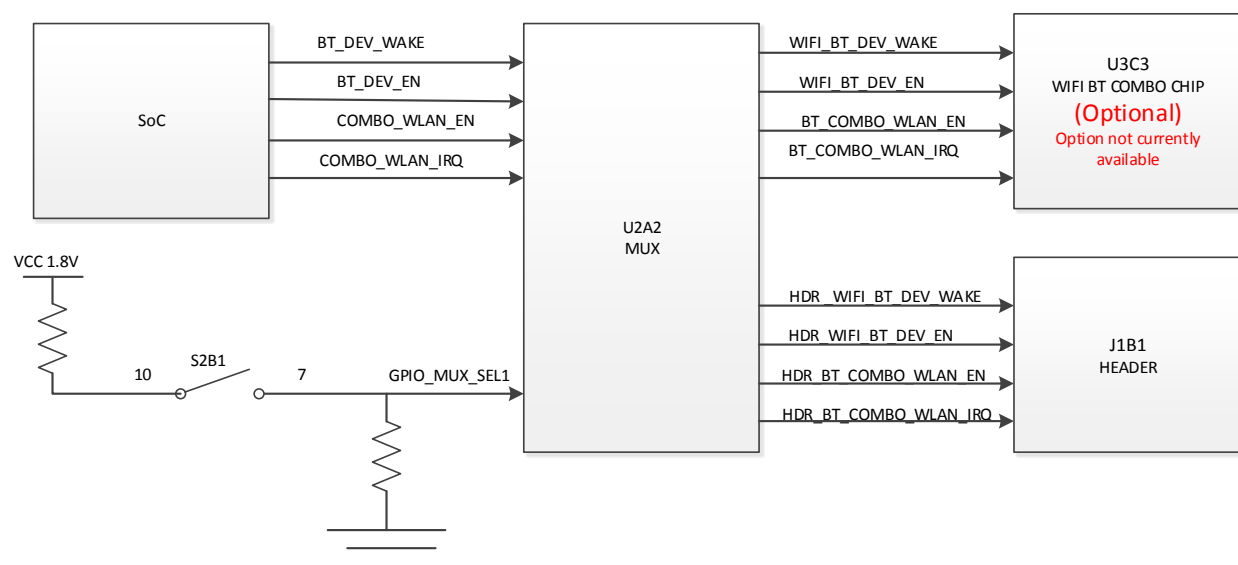
J1A3 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	GPIO_S5[2]	MODEM_SAR	_SB.GPO2 {0x2}	Modem Signal
2	GPIO_S0_SC[0]	GPI_VOLUMEDOWN	_SB.GPO0 {0x0}	Volume down input
3	GPIO_S0_SC[2]	HDR_LID	_SB.GPO0 {0x2}	LID signal
4	PMC_SLP_S0IX#	PMU_SLP_S0IX_N		PMU Sleep signal
5	GPIO_S5[1]	USBMUX_INT_N	_SB.GPO2 {0x1}	USB interrupt signal
6	GPIO_S5[4]	HDR_AUDIO_INT	_SB.GPO2 {0x4}	Audio codec Interrupt signal
7	GPIO_S0_NC[15]	PMIC_USB_EN	_SB.GPO1 {0xF}	PMIC USB Enable signal
8	GPIO_S5[27]	HDR_JACK_DET_N	_SB.GPO2 {0x1B}	Audio Jack Detect signal
9		GROUND		Ground
10	GPIO_S0_SC[1]	GPI_VOLUMEUP	_SB.GPO0 {0x1}	Volume Up input

J1B1: 10 Pin Header (WiFi-BT Signals)

Note: U2A2 and U2C1 are the MUX ICs used to switch WiFi and BT control signals. Switching can be done with the DIP switch (S2B1 ref. des. on the board) by the 7th position switch.

J1B1 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	NA	GROUND		Ground
2	GPIO_S5[5]	WIFI_32K_CLK	_SB.GPO2 {0x5}	WIFI 32KHz Clock
3	GPIO_S5[17]	HDR_BT_HOST_WAKE	_SB.GPO2 {0x11}	BT Host Wake up signal
4	GPIO_S0_NC[24]	HDR_WIFI_BT_DEV_WAKE	_SB.GPO1 {0x18}	BT Device Wake up signal
5	GPIO_S5[7]	GPS_32K_CLK	_SB.GPO2 {0x7}	GPS Clock
6	GPIO_S0_NC[25]	HDR_WIFI_BT_DEV_EN	_SB.GPO1 {0x19}	WIFI BT device Enable signal
7	GPIO_S5[15]	HDR_BT_COMBO_WLAN_IRQ	_SB.GPO2 {0xF}	WLAN Interrupt request
8	USB_OC#[1]	HDR_COMBO_WLAN_EN		WLAN Enable signal. SOC pin need to be configured as GPIO
9	NA	GROUND		Ground
10	NA	GROUND		Ground

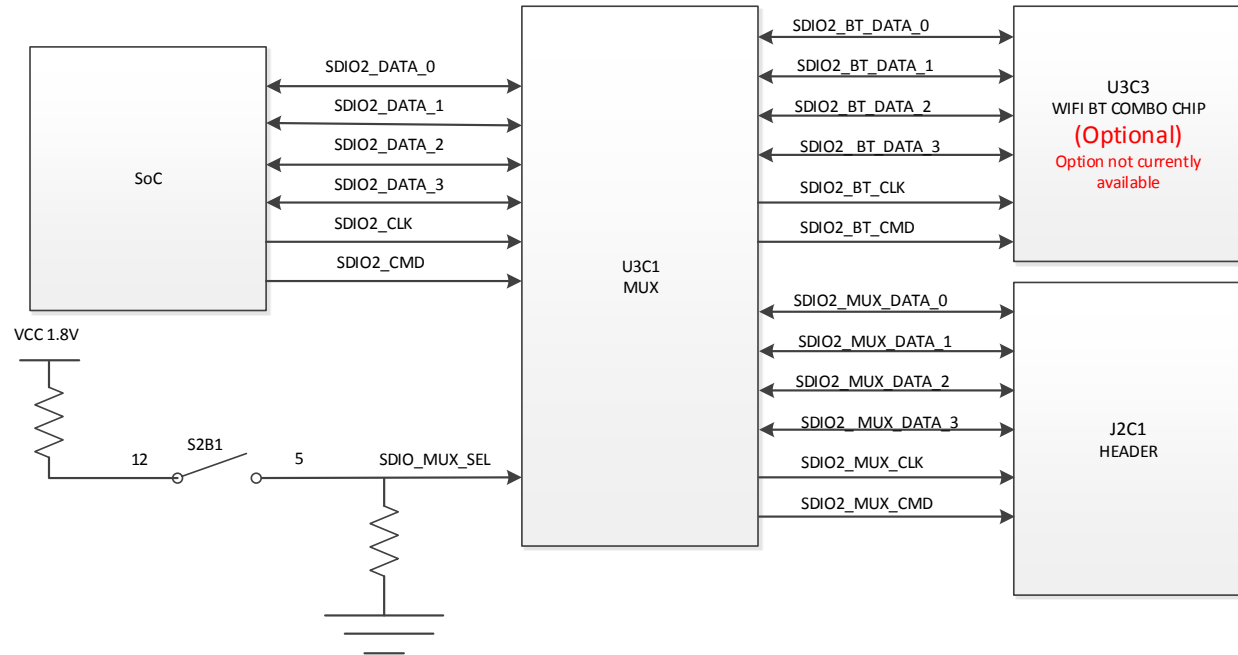
Note: The WiFi header is NOT populated on Sharks Cove at this point. Please use USB WiFi module for connectivity if required. Above data is provided for development of WiFi modules only.



J2C1: 10 Pin Headers (SDIO2 Signals)

Note: U3C1 is the MUX IC used to switch the signals. To switch the signals to BT, use the DIP switch (ref des S2B1) and close the 5th position.

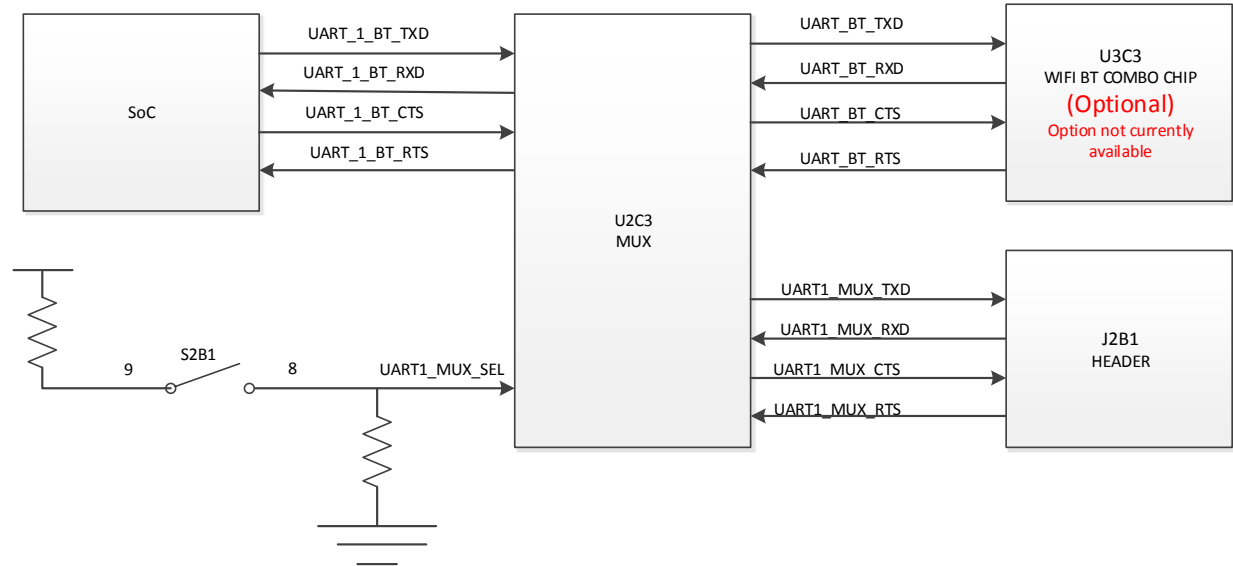
J2C1 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	SD2_CLK	SDIO2_MUX_CLK	_SB.SDHB	SDIO CLOCK
2	SD2_CMD	SDIO2_MUX_CMD	_SB.SDHB	SDIO CMD
3	NA	GROUND		Ground
4	SD2_DATA_2	SDIO2_MUX_DATA_2	_SB.SDHB	SDIO Data 2
5	SD2_DATA_0	SDIO2_MUX_DATA_0	_SB.SDHB	SDIO Data 0
6	NA	GROUND		Ground
7	SD2_DATA_1	SDIO2_MUX_DATA_1	_SB.SDHB	SDIO Data 1
8	SD2_DATA_3	SDIO2_MUX_DATA_3	_SB.SDHB	SDIO Data 3
9	NA	GROUND		Ground
10	NA	OPEN		No Connection



J2B1: 10 Pin Header (UART Signals)

Note: U2C3 U3C1 is the MUX IC used to switch the signals. To route the signals to headers, close the 8th position of DIP switch (ref des S2B1)

J2B1 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	SIO_UART1_RTS#	UART1_MUX_RTS	_SB_.URT1	UART1 RTS signal
2	SIO_UART2_RTS#	UART_GPS_RTS	_SB_.URT2	UART2 RTS Signal
3	SIO_UART1_TXD	UART1_MUX_TXD	_SB_.URT1	UART1 TXD signal
4	SIO_UART2_TXD	UART_GPS_TXD	_SB_.URT2	UART2 TXD signal
5	NA	GROUND		Ground
6	NA	GROUND		Ground
7	SIO_UART1_RXD	UART1_MUX_RXD	_SB_.URT1	UART1 RXD signal
8	SIO_UART2_RXD	UART_GPS_RXD	_SB_.URT2	UART2 RXD signal
9	SIO_UART1_CTS#	UART1_MUX_CTS	_SB_.URT1	UART1 CTS signal
10	SIO_UART2_CTS#	UART_GPS_CTS	_SB_.URT2	UART2 CTS signal



J4A3: 10 Pin Header (USB Signals)

J4A3 pin#	SoC GPIO PIN NAME	SIGNAL NAME	Comments
1		+VSYS(4.2V)	4.2V Power Rail
2		+VSYS(4.2V)	4.2V Power Rail
3	USB_DN[1]	USB2_P1_DN	USB differential line
4		OPEN	No Connection
5	USB_DP[1]	USB2_P1_DP	USB differential line
6		OPEN	No Connection
7		GROUND	Ground
8		OPEN	No Connection
9		GROUND	Ground
10		OPEN	No Connection

J1B2: 10 Pin Header (I2C Signals)

J4A3 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1	SIO_I2C0_CLK	I2C_0_SCL	_SB.I2C1	I2C Clock line for Controller 0
2	SIO_I2C2_CLK	I2C_2_SCL	_SB.I2C3	I2C Clock line for Controller 2
3	SIO_I2C0_DATA	I2C_0_SDA	_SB.I2C1	I2C Data line for Controller 0
4	SIO_I2C2_DATA	I2C_2_SDA	_SB.I2C3	I2C Data line for Controller 2
5	SIO_I2C1_CLK	I2C_1_SCL	_SB.I2C2	I2C Clock line for Controller 1
6	NA	OPEN		No Connection
7	SIO_I2C1_DATA	I2C_1_SDA	_SB.I2C2	I2C Data line for Controller 1
8	NA	OPEN		No Connection
9	NA	GROUND		Ground
10	NA	GROUND		Ground

J1B3: 10 Pin Header (I2S0 and I2S1 Signals)

J1B3 pin#	SoC GPIO PIN NAME	SIGNAL NAME	Comments
1	I2S1_DATAOUT	HDR_I2S_1_TXD	I2S Transmit line1
2	I2S0_DATAOUT	HDR_I2S_0_TXD	I2S Transmit line0
3	I2S1_DATAIN	HDR_I2S_1_RXD	I2S Receive line1
4	I2S0_DATAIN	HDR_I2S_0_RXD	I2S Receive line0
5	NA	GROUND	Ground
6	NA	GROUND	Ground
7	I2S1_L_R	HDR_I2S_1_FS	I2S FS line1
8	I2S0_L_R	HDR_I2S_0_FS	I2S FS line0
9	I2S1_CLK	HDR_I2S_1_CLK	I2S Clock line1
10	I2S0_CLK	HDR_I2S_0_CLK	I2S Clock line0

J4C2: 60 Pin Receptacle (Display Connector)

J4C2 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1		TP4C12		Test Point
2		+V1P8A_DISP		1.8V Power rail for display
3		TP4C12		Test Point
4		+V1P8A_DISP		1.8V Power rail for display
5		TP4C12		Test Point
6		+V1P8A_DISP		1.8V Power rail for display
7		GROUND		Ground
8		GROUND		Ground
9	SIO_I2C2_DATA	DISP_SDA	_SB.I2C3	I2C Data line for Display
10		TP_DISP_PIN_10		Test Point
11	SIO_I2C2_CLK	DISP_SCL	_SB.I2C3	I2C Clock line for Display
12		TP_DISP_PIN_12		Test Point
13		TP_DISP_PIN_13		Test Point
14		TP_DISP_PIN_14		Test Point
15		GROUND		Ground
16	PCU_SPI_CS#[1]	GPI_SOC_HOMESCRN		Home screen Input Signal
17		+VSYS_MIPI_CONN		VSYS MIPI power rail
18		TP_DISP_PIN_18		Test Point
19		+VSYS_MIPI_CONN		VSYS MIPI power rail
20		TP_DISP_PIN_20		Test Point
21		+VSYS_MIPI_CONN		VSYS MIPI power rail
22		GROUND		Ground
23		GROUND		Ground
24		+V3P3_DISP		1.8V Power rail for display
25	DDI1_BKLTCTL	DDI1_PANELEN		Display Panel Enable
26		+V3P3_DISP		1.8V Power rail for display
27	DDI1_BKLTEN	DDI1_BKLTEN		Display Backlight Enable

J4C2 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
28		GROUND		Ground
29		GROUND		Ground
30		TP_DISP_PIN_30		Test Point
31	MDSI_A_CLKP	MDSI_A_CLK_DP		Display Differential Clock P
32	SIO_I2C3_DATA	TOUCH_SDA3	_SB.I2C4	Touch I2C data line
33	MDSI_A_CLKN	MDSI_A_CLK_DN		Display Differential Clock N
34	SIO_I2C3_CLK	TOUCH_SCL3	_SB.I2C4	Touch i2C clock line
35		GROUND		Ground
36		GROUND		Ground
37	MDSI_A_DP[0]	MDSI_A_DATA0_DP		Display Differential Data0_P
38		+V3P3SX_ALDO2_DISP		3.3V Analog LDO power rail
39	MDSI_A_DN[0]	MDSI_A_DATA0_DN		Display Differential Data0_N
40		+V3P3SX_ALDO2_DISP		3.3V Analog LDO power rail
41		GROUND		Ground
42		GROUND		Ground
43	MDSI_A_DP[1]	MDSI_A_DATA1_DP		Display Differential Data1_P
44	MDSI_A_TE_R	MDSI_A_TE		Display TE
45	MDSI_A_DN[1]	MDSI_A_DATA1_DN		Display Differential Data1_N
46	SIO_PWM[0]	DISP_PWM_BKLT_EN		Display PWM signal
47		GROUND		Ground
48	GPIO_S5[3]	TOUCH_INT_N	_SB.GPO2 {0x3}	Touch Interrupt Signal
49	MDSI_A_DP[2]	MDSI_A_DATA2_DP		Display Differential Data2_P
50	DDI1_VDDEN	DDI1_VDDEN		DDI1 VDD Enable
51	MDSI_A_DN[2]	MDSI_A_DATA2_DN		Display Differential Data2_N
52	GPIO_S5[6]	ALS_INT_N	_SB.GPO2 {0x6}	Ambient Light Sensor Interrupt
53		GROUND		Ground
54	GPIO_S0_NC[26]	TOUCH_RESET_N	_SB.GPO1 {0x1A}	Touch Reset Signal
55	MDSI_A_DP[3]	MDSI_A_DATA3_DP		Display Differential Data3_P
56		TP_DISP_PIN_56		Test Point
57	MDSI_A_DN[3]	MDSI_A_DATA3_DN		Display Differential Data3_N
58		TP_DISP_PIN_58		Test Point

J4C2 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
59		GROUND		Ground
60		TP_DISP_PIN_60		Test Point

J3A1: 60-pin Receptacle (Camera Connector)

J3A1 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
1		GROUND		Ground
2		GROUND		Ground
3	MCSI1_CLKP	MCSI_1_CLK_DP		MCSI Differential Clock1_P
4		+V2P8_AVDD_CAM		2.8V power rail for Camera
5	MCSI1_CLKN	MCSI_1_CLK_DN		MCSI Differential Clock1_N
6		+V2P8_AVDD_CAM		2.8V power rail for Camera
7		GROUND		Ground
8		+V2P8_AVDD_CAM		2.8V power rail for Camera
9	MCSI_DP[0]	MCSI_1_DATA0_DP		MCSI Differential Data0_P
10		+V2P8_AVDD_CAM		2.8V power rail for Camera
11	MCSI_DN[0]	MCSI_1_DATA0_DN		MCSI Differential Data0_N
12		GROUND		Ground
13		GROUND		Ground
14		+V2P8_AVDD_CAM		2.8V power rail for Camera
15	MCSI_DP[1]	MCSI_1_DATA1_DP		MCSI Differential Data1_P
16		+V2P8_AVDD_CAM		2.8V power rail for Camera
17	MCSI_DN[1]	MCSI_1_DATA1_DN		MCSI Differential Data1_N
18		I2C_0_SCL	_SB.I2C1	I2C Clock line
19		GROUND		Ground
20		I2C_0_SDA	_SB.I2C1	I2C Data line
21		TP		Test Point
22		CAMERA_PRSENT_N		Camera Present signal
23		TP		Test Point
24		+V1P8_CAMERA		1.8V power rail for Camera
25		GROUND		Ground
26		+V1P8_CAMERA		1.8V power rail for Camera
27		TP		Test Point
28		TP_CAM_PIN_28		Test Point

J3A1 pin#	SoC GPIO PIN NAME	SIGNAL NAME	ACPI Object	Comments
29		TP		Test Point
30		TP_CAM_PIN_30		Test Point
31		GROUND		Ground
32		GROUND		Ground
33	SIO_I2C1_CLK	CAM_I2C_1_SCL	_SB.I2C2	Camera I2C Clock line
34		+VSYS_CAMERA		Camera Power Rail
35	SIO_I2C1_DATA	CAM_I2C_1_SDA	_SB.I2C2	Camera I2C data line
36		+VSYS_CAMERA		Camera Power Rail
37		GROUND		Ground
38		+VSYS_CAMERA		Camera Power Rail
39	MCSI2_CLKN	MCSI_2_CLK_DN		MCSI Differential Clock2_P
40		GROUND		Ground
41	MCSI2_CLKP	MCSI_2_CLK_DP		MCSI Differential Clock2_N
42	PMC_PLT_CLK[0]	CAM1_MCLK		Rear Camera MCLK (Clock)
43		GROUND		Ground
44		CAM1_RESET_N	_SB.GPO1 {0x11}	Rear Camera Reset Signal
45	MCSI2_DN[0]	MCSI_2_DATA_DN		MCSI2 Differential Data2_P
46		TP_CAM_GPIO1_RSVD		Test Point
47	MCSI2_DP[0]	MCSI_2_DATA_DP		MCSI2 Differential Data2_N
48		GROUND		Ground
49		GROUND		Ground
50		CAMERA_2_PD	_SB.GPO1 {0x16}	Front Camera Power Down
51		TP_CAM_RESET		Test Point
52	PMC_PLT_CLK[1]	CAM2_MCLK		Front Camera MCLK (Clock)
53	GPIO_S0_NC[20]	FLASH_TORCH	_SB.GPO1 {0x14}	Camera Flash signal
54	GPIO_S0_NC[18]	CAM2_RESET_N	_SB.GPO1 {0x12}	Front Camera Reset Signal
55	GPIO_S0_NC[16]	FLASH_RESET_N	_SB.GPO1 {0x10}	Camera Flash Reset signal
56		GROUND		Ground
57	GPIO_S0_NC[21]	CAMERA_1_PD	_SB.GPO1 {0x15}	Rear Camera Power Down
58	GPIO_S0_NC[19]	FLASH_TRIGGER_N	_SB.GPO1 {0x13}	Camera Flash Trigger signal
59		TP_CAM_FHLD		Test Point
60		TP_CAM_GPIO2_RSVD		Test Point

15 Power supply connector headers

J4B1: 4 Pin header

J4B1 pin#	PMIC PIN Name	SIGNAL NAME	Comments
1	DLDO4	+V3P3_DLDO4_HDR	3.3V Digital LDO Power rail
2	LX6 (Buck6)	+V1P8A_HDR	1.8V power rail
3		GROUND	Ground
4		GROUND	Ground

J5B2: 4 Pin Header

J5B2 pin#	PMIC PIN Name	SIGNAL NAME	Comments
1	ALDO1	+V2P8_ALDO1_HDR	2.8V Analog LDO Power rail
2	DLDO3	+V3P3SX_DLDO3_HDR	3.3V Digital LDO Power rail
3		GROUND	Ground
4		GROUND	Ground

J4B2: 4 Pin Header

J4B2 pin#	PMIC PIN Name	SIGNAL NAME	Comments
1	ALDO3	+V3P3A_PLT_HDR	3.3V Power rail
2		+V3P3SYS_HDR	Vsys Power rail
3		GROUND	Ground
4		GROUND	Ground

J5B3: 4 Pin Header

J5B3 pin#	PMIC PIN Name	SIGNAL NAME	Comments
1	GPIO1/GPLDO1	+V3P3_GPLDO1_HDR	3.3V Power rail
2	ALDO2	+V3P3SX_ALDO2	3.3V Analog LDO Power rail
3		GROUND	Ground
4		GROUND	Ground

J4B3: 4 Pin Header

J4B3 pin#	PMIC PIN Name	SIGNAL NAME	Comments
1		OPEN	No Connection
2	ELDO1	+V_ELDO1	ELDO power rail
3		GROUND	Ground
4		GROUND	Ground

16 Jumper headers for Board RESET

J2C2: 2 Pin Header (PLTRST Jumper)

Note: This Jumper is used for COLD RESET of platform. You need to short J2C2 pin 1 and pin 2 to assert RESET. Refer the above table for pin definitions.

J2C2 pin#	SoC/PMICPIN Name	SIGNAL NAME	Comments
1	PMC_PLTRST#/PLTRST_B	PLTRST_N	Platform Reset Signal
2		GROUND	Ground

POWER button Jumper

J5C1: 2 pin Header

This Jumper is used to reset the board. You need to short J5C1 pin 1 and pin 2 to assert RESET. Refer the above table for pin definitions. Short press will put the system in S0iX mode. One more short press will take the system out of sleep. Long press will put it into mechanical OFF state.

J5C1 pin#	PMIC PIN Name	SIGNAL NAME	Comments
1	PWRON	PMU_PWRBTN_N	Power Button Signal
2		GROUND	Ground

17 APPENDIX

17.1 Port 80 codes

Power-on self-test (POST) is a process performed by firmware or software routines immediately after many digital electronic devices are powered on. Perhaps the most widely known usage pertains to computing devices (personal computers, PDAs, networking devices such as routers, switches, intrusion detection systems and other monitoring devices). The routines are part of a device's pre-boot sequence. Once POST completes successfully, bootstrap loader code is invoked.

The original IBM BIOS made POST diagnostic information available by outputting a number to I/O port 80 (a screen display was not possible with some failure modes). Both progress indication and error codes were generated; in the case of a failure which did not generate a code, the code of the last successful operation was available to aid in diagnosing the problem

Disclaimer: Port 80 code is subject to change with newer BIOS version

Port 80h Post Code	Comments
0x00B4	Windows boot Mode
0x0034	eMMC loaded with other half of the BIOS file. Status indication that the BIOS load completed
0XFA67	Need to load the remaining part of the BIOS
0x0D67	Intermediate status code indicate the BIOS load from USB

17.2 Troubleshooting Tips

Please refer to the Sharks Cove Developer's Guide on www.sharkscove.org/docs for a complete list of troubleshooting tips.



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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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