Crystal-to-HSTL 100MHz / 200MHz PCI Express™ Clock Synthesizer

ICS842S104E

DATA SHEET

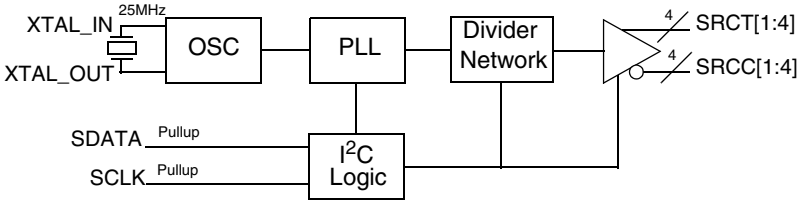
General Description

The ICS842S104E is a PLL-based clock generator specifically designed for PCI Express™ Clock Generation 2 applications. This device generates either a 200MHz or 100MHz differential HSTL clock from an input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference is applied to the XTAL_IN pin with the XTAL_OUT pin left floating.The device offers spread spectrum clock output for reduced EMI applications. An I^2C bus interface is used to enable or disable spread spectrum operation as well as select either a down spread value of -0.35% or -0.5%.The ICS842S104E is available in a lead-free 24-Lead package.

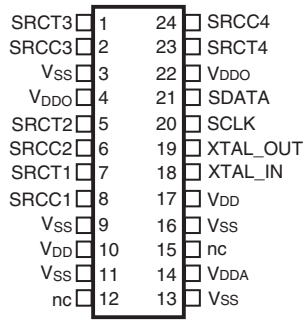
Features

- Four differential HSTL output pairs
- Crystal oscillator interface: 25MHz
- Output frequency: 100MHz or 200MHz
- RMS phase jitter @ 200MHz (12kHz – 20MHz): 1.229ps (typical)
- Cycle-to-cycle jitter: 25ps (maximum)
- I^2C support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V core/1.5V to 2.0V output operating supply
- 0°C to 70°C ambient operating temperature
- Available lead-free (RoHS 6) package
- PCI Express Gen2 Jitter Compliant

Block Diagram



Pin Assignment



ICS842S104E
24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	SRCT3, SRCC3	Output		Differential output pair. HSTL interface levels.
3, 9, 11, 13, 16	V_{SS}	Power		Power supply ground.
4, 22	V_{DDO}	Power		Output power supply pins.
5, 6	SRCT2, SRCC2	Output		Differential output pair. HSTL interface levels.
7, 8	SRCT1, SRCC1	Output		Differential output pair. HSTL interface levels.
10, 17	V_{DD}	Power		Core supply pins.
12, 15	nc	Unused		No connect.
14	V_{DDA}	Power		Analog supply for PLL.
18, 19	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
20	SCLK	Input	Pullup	I^2C compatible SCLK. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.
21	SDATA	I/O	Pullup	I^2C compatible SDATA. This pin has an internal pullup resistor. Open drain. LVCMOS/LVTTL interface levels.
23, 24	SRCT4, SRCC4	Output		Differential output pair. HSTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal I^2C serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the serial interface initialize to their default setting upon power-up, therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 3A.

The block write and block read protocol is outlined in Table 3B, while Table 3C outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3A.Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
6:5	Chip select address, set to “00” to access device.
4:0	Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be “00000”.

Table 3B. Block Read and Block Write Protocol

Bit	Description = Block Write	Bit	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 1 - 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 - 8 bits	30:37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Byte/Slave Acknowledges	39:46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from Slave/Acknowledge
			Data Byte N from slave - 8 bits
			Not Acknowledge

Table 3C. Byte Read and Byte Write Protocol

Bit	Description = Byte Write	Bit	Description = Byte Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data Byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Registers

Table 3D. Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z) 1 = Enable
5	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z) 1 = Enable
4	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z) 1 = Enable
3	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z) 1 = Enable
2	1	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

NOTE: @PUP denotes at power-up.

Table 3E. Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 3F. Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	SRCT/C	Spread Spectrum Selection 0 = -0.35%, 1 = -0.5%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SRC	SRC Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	Reserved	Reserved
0	1	FOUTCTL	Output Frequency Control 0 = 100MHz 1 = 200MHz

Table 3G. Byte 3:Control Register 3

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 3H. Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	1	Reserved	Reserved

Table 3I. Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 3J. Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Hi-Z Select 0 = Hi-Z, 1 = REF/N
6	0	TEST_MODE	TEST Clock Mode Entry Control 0 = Normal Operation, 1 = REF/N or Hi-Z Mode
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

NOTE: @PUP denotes at power-up.

Table 3K. Byte 7: Control Register 7

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	1		Vendor ID Bit 0

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	77.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V to 2.0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.25	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		1.5		2.0	V
I_{DD}	Power Supply Current				106	mA
I_{DDA}	Analog Supply Current				25	mA
I_{DDO}	Output Supply Current				7	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V to 2.0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SDATA, SCLK	V_{DD} = V_{IN} = 3.465V			10	µA
I_{IL}	Input Low Current	SDATA, SCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V to 2.0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		0.9		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40		65	%
V_{SWING}	Peak-to-Peak Output Voltage Swing		40% x (V_{OH} - V_{OL}) + V_{OL}		60% x (V_{OH} - V_{OL}) + V_{OL}	V

NOTE 1: Outputs terminated with 50Ω to GND.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

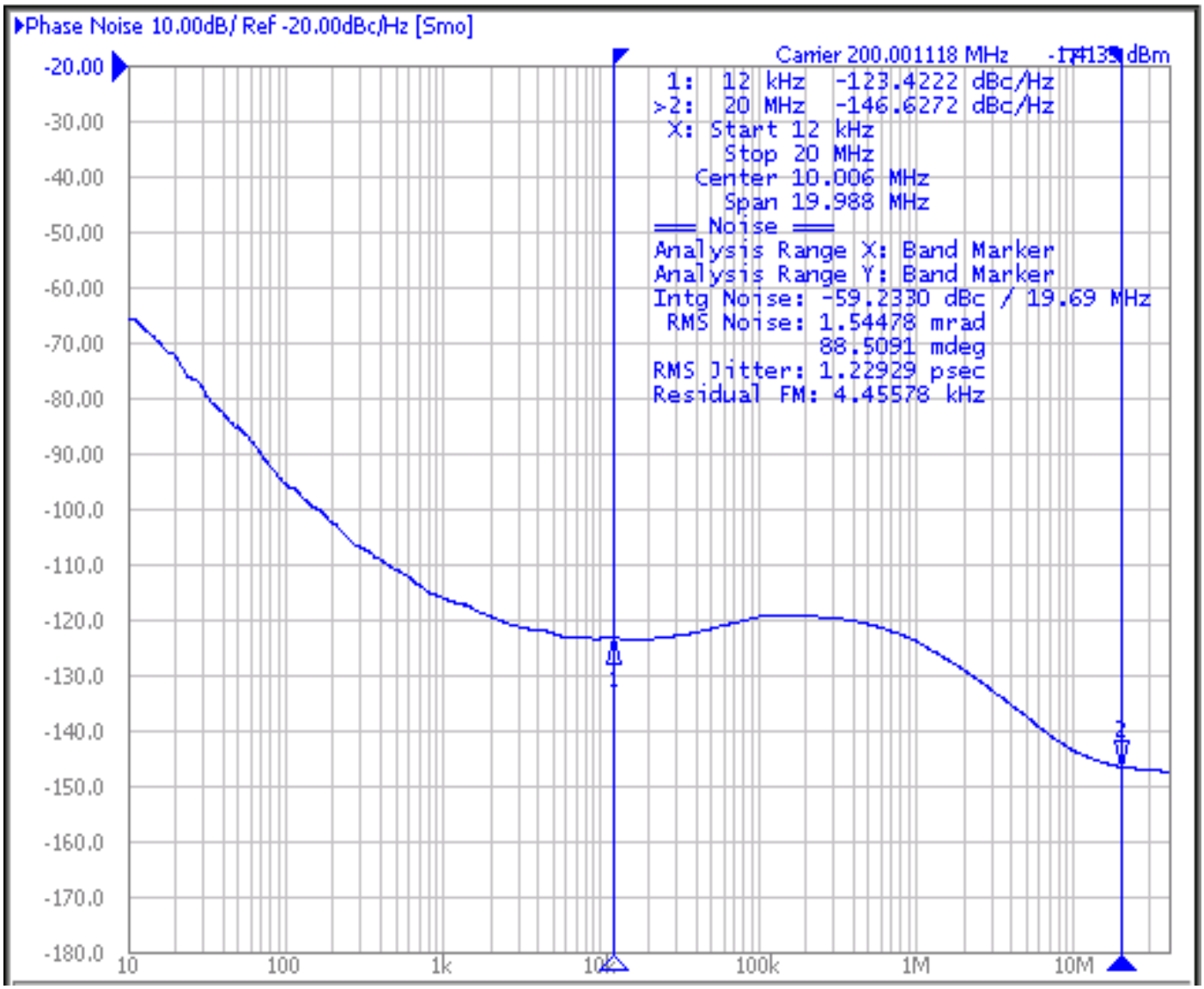
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V to 2.0V, T_A = 0°C to 70°C

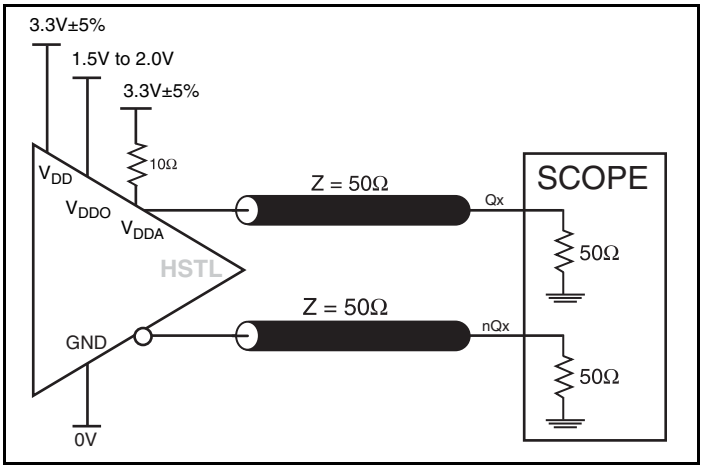
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FOUTCTL = 0		100		MHz
		FOUTCTL = 1		200		
fref	Reference frequency			25		MHz
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 1, 2	f = 200MHz, 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.95		ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 1, 2	f = 200MHz, 25MHz crystal input Low Band: 10kHz - 1.5MHz		0.31		ps
tsk(o)	Output Skew; NOTE 3, 4				55	ps
tjit(Ø)	Phase Jitter, RMS (Random)	200MHz, Integration Range: 12kHz – 20MHz		1.229		ps
tjit(cc)	Cycle-to-Cycle Jitter	PLL Mode			25	ps
t_L	PLL Lock Time				60	ms
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE: 2: This parameter is guaranteed by characterization. Not tested in production.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions.

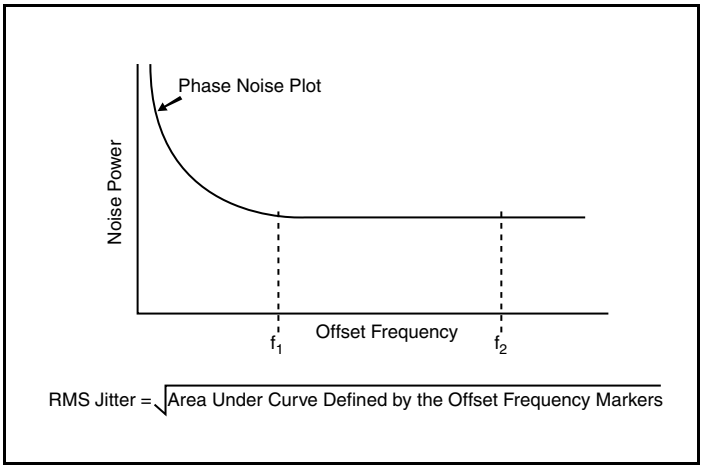
Typical Phase Noise at 200MHz



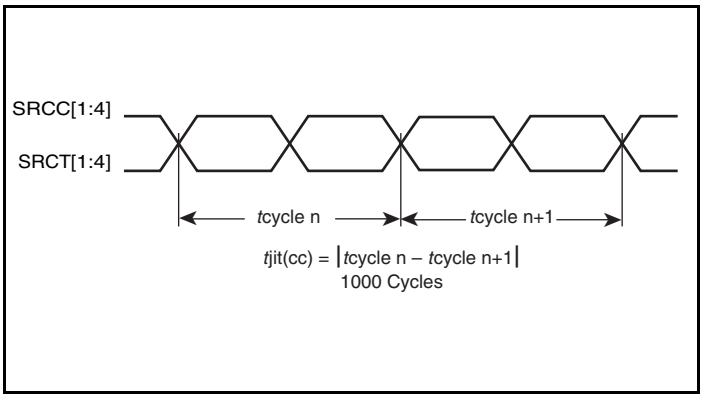
Parameter Measurement Information



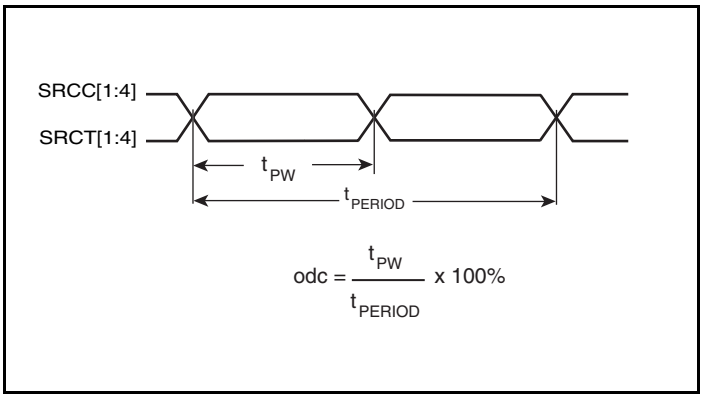
3.3V HSTL Output Load AC Test Circuit



RMS Phase Jitter



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS842S104E provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

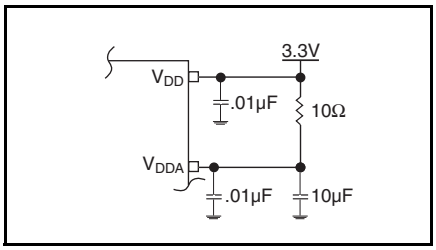


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

HSTL Outputs

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS842S104E has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

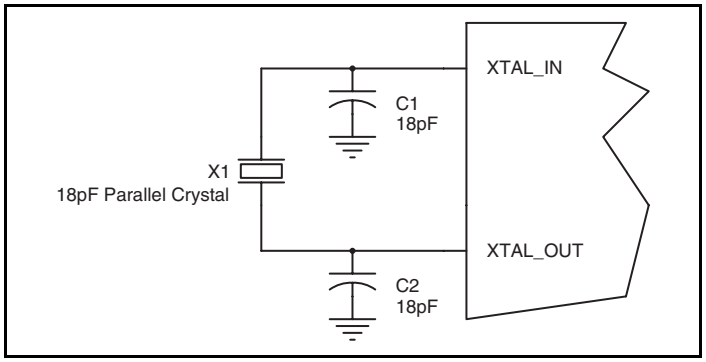


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

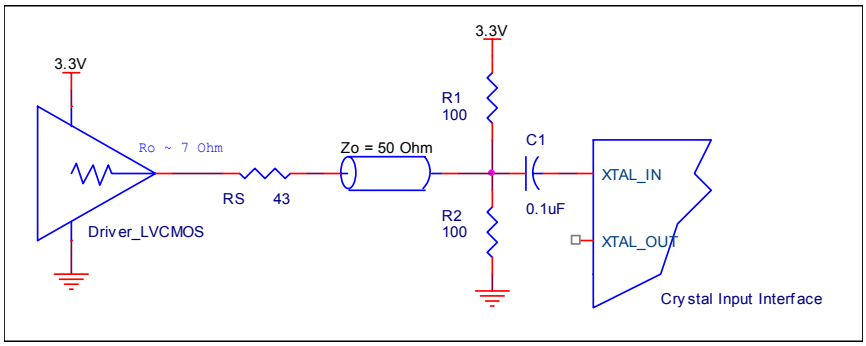


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

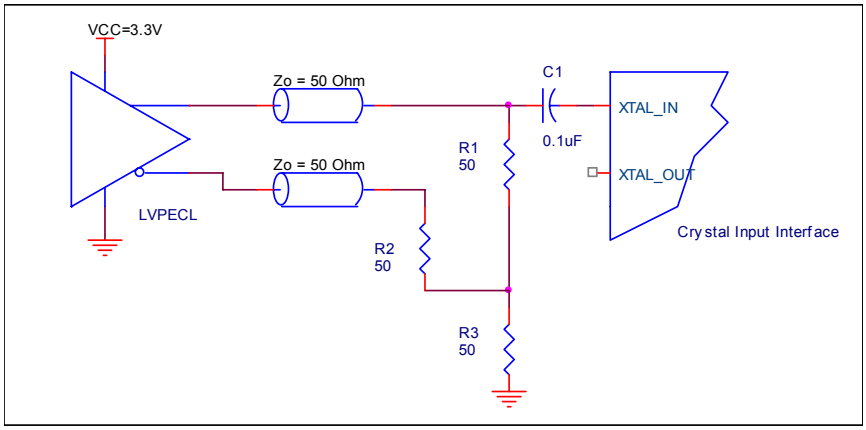


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for HSTL Outputs

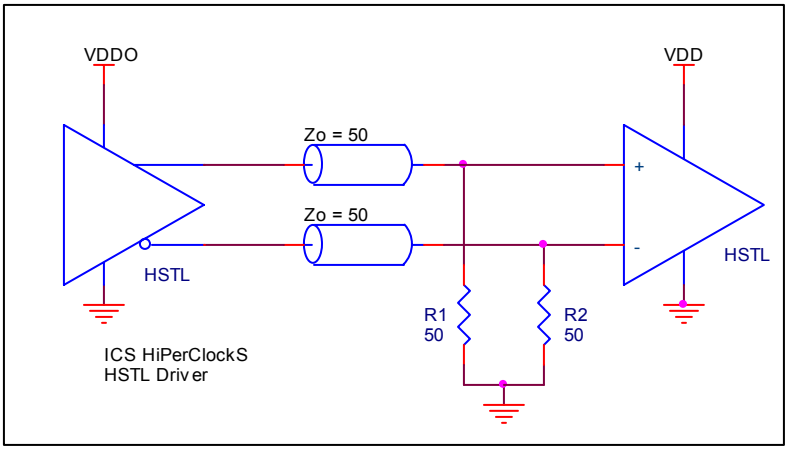


Figure 4. HSTL Output Termination

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 0.6% down-spread (+0.0% / -0.5%) from the nominal output frequency. An example of a triangle frequency modulation profile is shown in *Figure 5A* below. The ramp profile can be expressed as:

? Fnom = Nominal Clock Frequency in Spread Off mode
? Fm = Nominal Modulation Frequency (30kHz)
? δ = Modulation Factor (0.6% down spread)

$$(1-\delta)Fnom + 2Fm \times \delta \times Fnom \times t \text{ when } 0 < t < \frac{1}{2Fm},$$

$$(1-\delta)Fnom - 2Fm \times \delta \times Fnom \times t \text{ when } \frac{1}{2Fm} < t < \frac{1}{Fm}$$

The ICS842S104E triangle modulation frequency deviation will not exceed 0.7% down-spread from the nominal clock frequency (+0.0% / -0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 5B*. The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.7%. The resulting spectral reduction will be greater than 5dB, as shown in Figure 5B. It is important to note the ICS842S104E 5dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

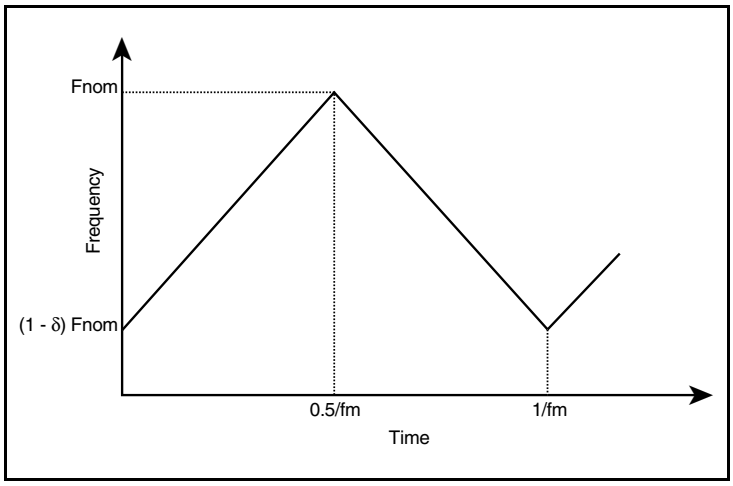


Figure 5A. Triangle Frequency Modulation

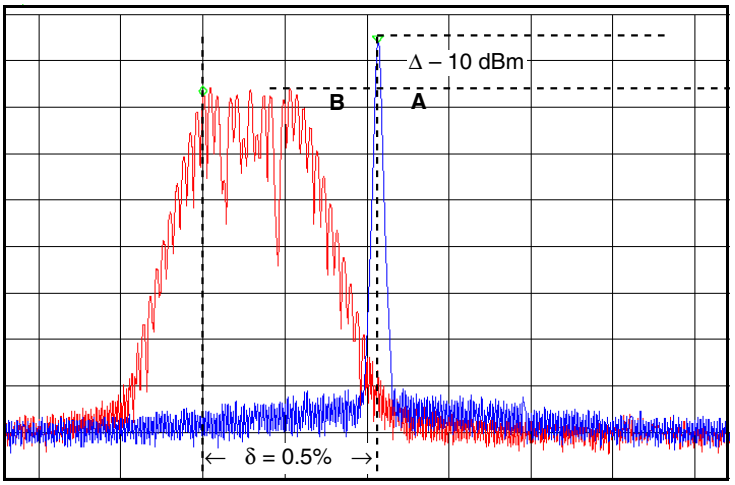


Figure 5B. 200MHz Clock Output In Frequency Domain
(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

Schematic Example

Figure 5 shows an example of ICS842S104E application schematic. In this example, the device is operated at V_{DD} = 3.3V and V_{DDO} = 1.8V. Both input options are shown. The device can either be driven using a quartz crystal or a 3.3V LVCMOS signal. The C1 and C2 = 18pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. The HSTL output driver termination examples are shown in this schematic. The decoupling capacitor should be located as close as possible to the power pin.

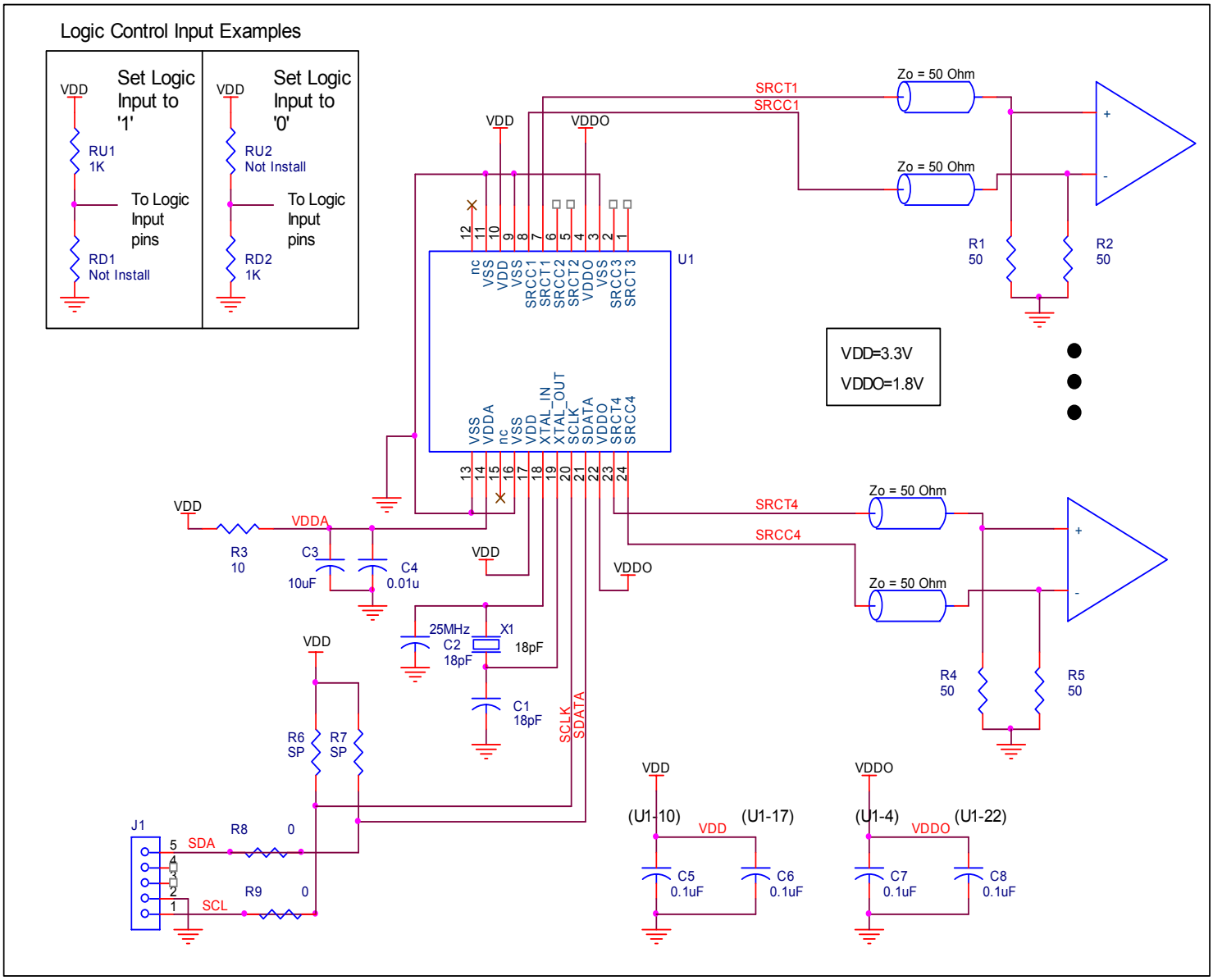


Figure 5. ICS842S104E Schematic Example

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

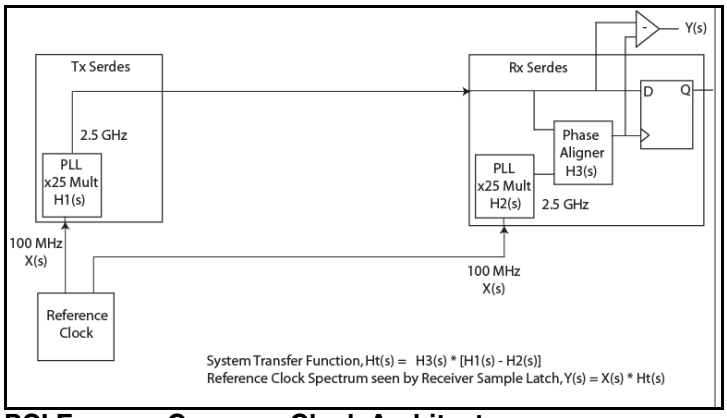
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

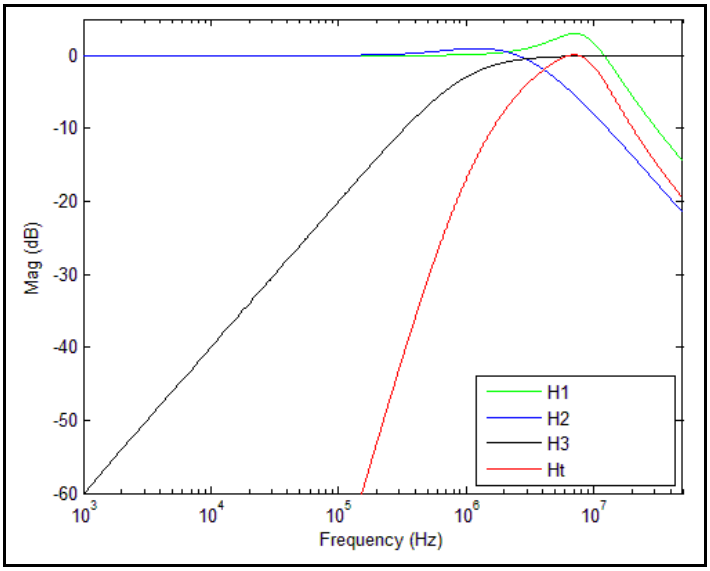
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].

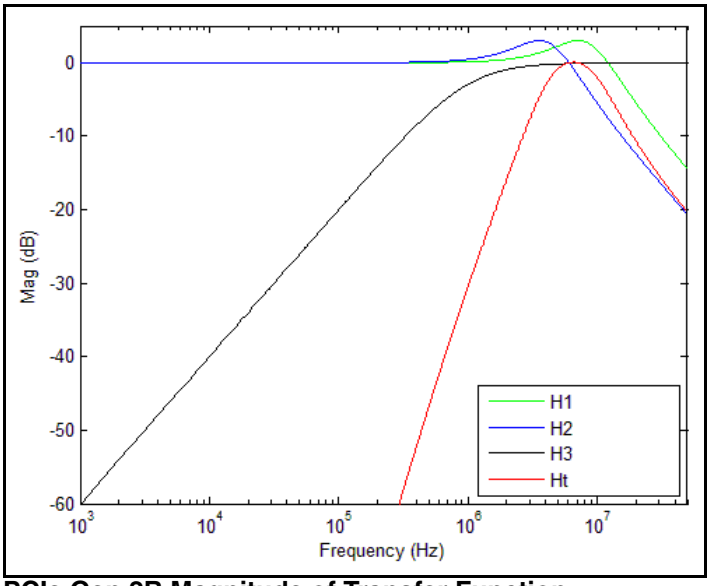


PCI Express Common Clock Architecture

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS842S104E.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS842S104E is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- The maximum current at 70°C is as follows:
  I_{DD_MAX} = 101.7mA
  I_{DDA_MAX} = 22mA

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (101.7mA + 22mA) = **428.6mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 32mW = **128mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 428.6mW + 128mW = **556.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 77.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.557W * 77.5°C/W = 113.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.5°C/W	73.2°C/W	71.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the HSTL output pair.

HSTL output driver circuit and termination are shown in *Figure 6.*

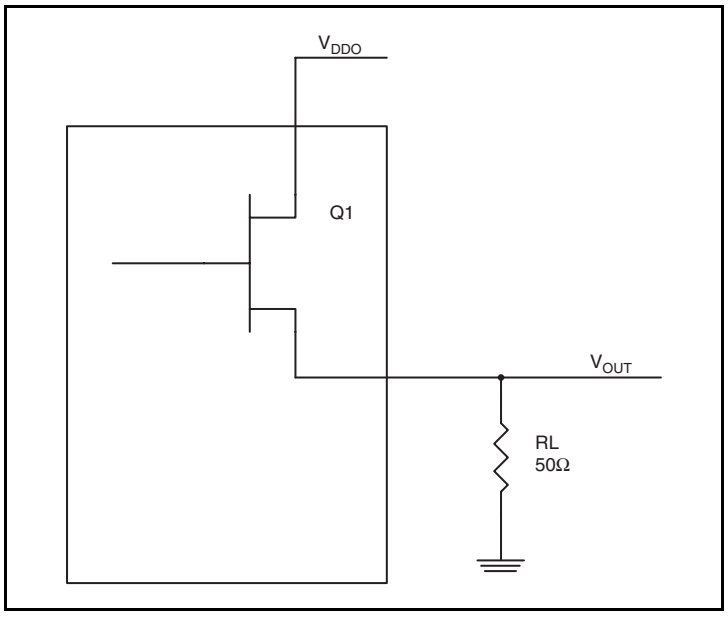


Figure 6. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX}/R_{L)} * (V_{DD\_MAX} - V_{OL\_MAX})$

Pd_H = (1.2V/50Ω) * (2.0V - 1.2V) = 19.2mW

Pd_L = (0.4V/50Ω) * (2.0V - 0.4V) = 12.8mW

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.5°C/W	73.2°C/W	71.0°C/W

Transistor Count

The transistor count for ICS842S104E is: 11,891

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

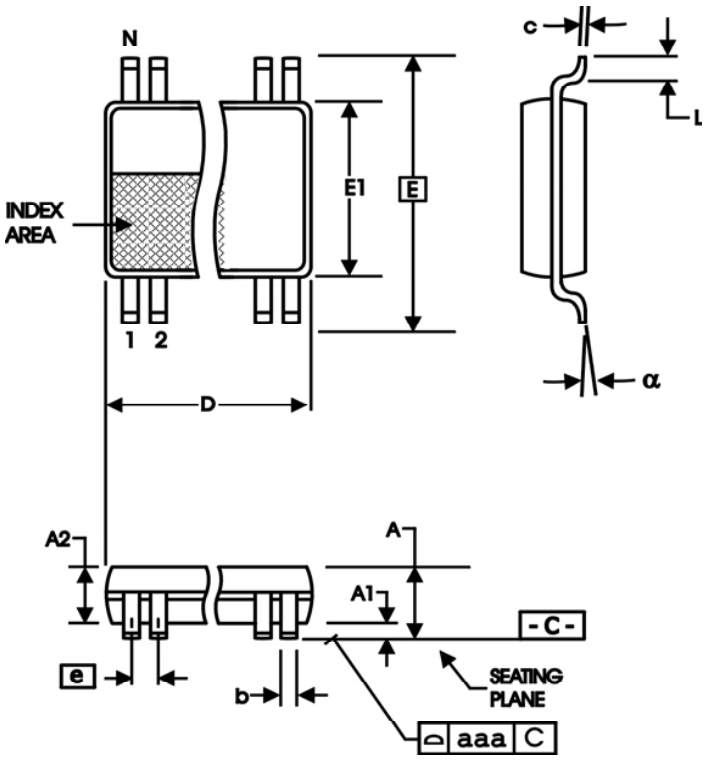


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
842S104EGLF	ICS842S104EGL	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
842S104EGLFT	ICS842S104EGL	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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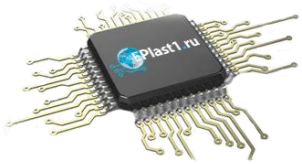

Как с нами связаться

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