Hot Swappable, Dual I^{2}C Isolators, 5 kV

Data Sheet

ADuM2250/ADuM2251

FEATURES

- **Bidirectional I^{2}C communication**
- **Open-drain interfaces**
- **Suitable for hot swap applications**
- **30 mA current sink capability**
- **1000 kHz operation**
- **3.0 V to 5.5 V supply/logic levels**
- **16-lead SOIC wide body package version (RW-16)**
- **16-lead SOIC wide body enhanced creepage version (RI-16-1)**
- **High temperature operation: 105°C**
- **Safety and regulatory approvals**
  - **UL recognition: 5000 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A (RI-16-1 package)**
    - **IEC 60601-1: 250 V rms (reinforced)**
    - **IEC 60950-1: 400 V rms (reinforced)**
  - **VDE certificate of conformity**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 849 V peak**

APPLICATIONS

- **Isolated I^{2}C, SMBus, or PMBus interfaces**
- **Multilevel I^{2}C interfaces**
- **Power supplies**
- **Networking**
- **Power-over-Ethernet**

GENERAL DESCRIPTION

The ADuM2250/ADuM2251[1] are hot swappable digital isolators with nonlatching, bidirectional communication channels that are compatible with I^{2}C interfaces. This eliminates the need for splitting I^{2}C signals into separate transmit and receive signals for use with standalone optocouplers.

The ADuM2250 provides two bidirectional channels, supporting a complete isolated I^{2}C interface. The ADuM2251 provides one bidirectional channel and one unidirectional channel for those applications where a bidirectional clock is not required.

The ADuM2250/ADuM2251 contain hot swap circuitry to prevent data glitches when an unpowered card is inserted onto an active bus.

These isolators are based on *i*Coupler® chip scale transformer technology from Analog Devices, Inc. *i*Coupler is a magnetic isolation technology with performance, size, power consumption, and functional advantages compared to optocouplers. The ADuM2250/ADuM2251 integrate *i*Coupler channels with semiconductor circuitry to enable a complete, isolated I^{2}C interface in a small form factor package.

FUNCTIONAL BLOCK DIAGRAMS

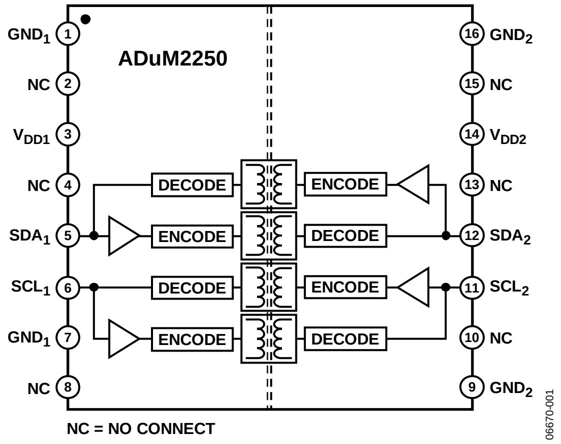

Figure 1. ADuM2250 Functional Block Diagram

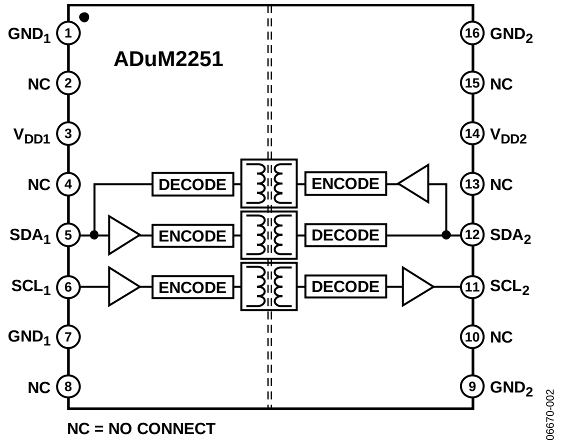

Figure 2. ADuM2251 Functional Block Diagram

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[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329; other patents pending.

Rev. B

Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

DC Specifications

All voltages are relative to their respective grounds. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25°C$, $V_{DD1} = 5$ V, and $V_{DD2} = 5$ V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM2250						
Input Supply Current, Side 1, 5 V	I_{DD1}		2.8	5.0	mA	$V_{DD1} = 5$ V
Input Supply Current, Side 2, 5 V	I_{DD2}		2.7	5.0	mA	$V_{DD2} = 5$ V
Input Supply Current, Side 1, 3.3 V	I_{DD1}		1.9	3.0	mA	$V_{DD1} = 3.3$ V
Input Supply Current, Side 2, 3.3 V	I_{DD2}		1.7	3.0	mA	$V_{DD2} = 3.3$ V
ADuM2251						
Input Supply Current, Side 1, 5 V	I_{DD1}		2.8	6.0	mA	$V_{DD1} = 5$ V
Input Supply Current, Side 2, 5 V	I_{DD2}		2.5	4.7	mA	$V_{DD2} = 5$ V
Input Supply Current, Side 1, 3.3 V	I_{DD1}		1.8	3.0	mA	$V_{DD1} = 3.3$ V
Input Supply Current, Side 2, 3.3 V	I_{DD2}		1.6	2.8	mA	$V_{DD2} = 3.3$ V
LEAKAGE CURRENTS	I_{ISDA1}, I_{ISDA2}, I_{ISCL1}, I_{ISCL2}		0.01	10	µA	$V_{SDA1} = V_{DD1}$, $V_{SDA2} = V_{DD2}$, $V_{SCL1} = V_{DD1}$, $V_{SCL2} = V_{DD2}$
SIDE 1 LOGIC LEVELS						
Logic Input Threshold[1]	V_{SDA1IL}, V_{SCL1IL}	500		700	mV	
Logic Low Output Voltage	V_{SDA1OL}, V_{SCL1OL}	600		900	mV	$I_{SDA1} = I_{SCL1} = 3.0$ mA
		600		850	mV	$I_{SDA1} = I_{SCL1} = 0.5$ mA
Input/Output Logic Low Level Difference[2]	ΔV_{SDA1}, ΔV_{SCL1}	50			mV	
SIDE 2 LOGIC LEVELS						
Logic Low Input Voltage	V_{SDA2IL}, V_{SCL2IL}			$0.3 \times V_{DD2}$	V	
Logic High Input Voltage	V_{SDA2IH}, V_{SCL2IH}	$0.7 \times V_{DD2}$			V	
Logic Low Output Voltage	V_{SDA2OL}, V_{SCL2OL}			400	mV	$I_{SDA2} = I_{SCL2} = 30$ mA

[1] $V_{IL} < 0.5$ V, $V_{IH} > 0.7$ V.

[2] $\Delta V_{S1} = V_{S1OL} - V_{S1IL}$. This is the minimum difference between the output logic low level and the input logic low threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.

AC Specifications

All voltages are relative to their respective grounds. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25°C$, $V_{DD1} = 5$ V, and $V_{DD2} = 5$ V, unless otherwise noted. See Figure 5 for a timing test diagram.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM FREQUENCY		1000			kHz	
OUTPUT FALL TIME						
5 V Operation						$4.5\text{ V} \le V_{DD1}, V_{DD2} \le 5.5\text{ V}$, $C_{L1} = 40$ pF, $R_1 = 1.6$ kΩ, $C_{L2} = 400$ pF, $R_2 = 180$ Ω
Side 1 Output (0.9 V_{DD1} to 0.9 V)	t_{f1}	13	26	120	ns	
Side 2 Output (0.9 V_{DD2} to 0.1 V_{DD2})	t_{f2}	32	52	120	ns	
3 V Operation						$3.0\text{ V} \le V_{DD1}, V_{DD2} \le 3.6\text{ V}$, $C_{L1} = 40$ pF, $R_1 = 1.0$ kΩ, $C_{L2} = 400$ pF, $R_2 = 120$ Ω
Side 1 Output (0.9 V_{DD1} to 0.9 V)	t_{f1}	13	32	120	ns	
Side 2 Output (0.9 V_{DD2} to 0.1 V_{DD2})	t_{f2}	32	61	120	ns	
PROPAGATION DELAY						
5 V Operation						$4.5\text{ V} \le V_{DD1}, V_{DD2} \le 5.5\text{ V}$, $C_{L1} = C_{L2} = 0$ pF, $R_1 = 1.6$ kΩ, $R_2 = 180$ Ω
Side 1 to Side 2, Rising Edge[1]	t_{PLH12}		95	130	ns	
Side 1 to Side 2, Falling Edge[2]	t_{PHL12}		162	275	ns	
Side 2 to Side 1, Rising Edge[3]	t_{PLH21}		31	70	ns	
Side 2 to Side 1, Falling Edge[4]	t_{PHL21}		85	155	ns	
3 V Operation						$3.0\text{ V} \le V_{DD1}, V_{DD2} \le 3.6\text{ V}$, $C_{L1} = C_{L2} = 0$ pF, $R_1 = 1.0$ kΩ, $R_2 = 120$ Ω
Side 1 to Side 2, Rising Edge[1]	t_{PLH12}		82	125	ns	
Side 1 to Side 2, Falling Edge[2]	t_{PHL12}		196	340	ns	
Side 2 to Side 1, Rising Edge[3]	t_{PLH21}		32	75	ns	
Side 2 to Side 1, Falling Edge[4]	t_{PHL21}		110	210	ns	
PULSE WIDTH DISTORTION						
5 V Operation						$4.5\text{ V} \le V_{DD1}, V_{DD2} \le 5.5\text{ V}$, $C_{L1} = C_{L2} = 0$ pF, $R_1 = 1.6$ kΩ, $R_2 = 180$ Ω
Side 1 to Side 2, $\lvert t_{PLH12} - t_{PHL12}\rvert$	PWD_{12}		67	145	ns	
Side 2 to Side 1, $\lvert t_{PLH21} - t_{PHL21}\rvert$	PWD_{21}		54	85	ns	
3 V Operation						$3.0\text{ V} \le V_{DD1}, V_{DD2} \le 3.6\text{ V}$, $C_{L1} = C_{L2} = 0$ pF, $R_1 = 1.0$ kΩ, $R_2 = 120$ Ω
Side 1 to Side 2, $\lvert t_{PLH12} - t_{PHL12}\rvert$	PWD_{12}		114	215	ns	
Side 2 to Side 1, $\lvert t_{PLH21} - t_{PHL21}\rvert$	PWD_{21}		77	135	ns	
COMMON-MODE TRANSIENT IMMUNITY[5]	$\lvert CM_H\rvert$, $\lvert CM_L\rvert$	25	35		kV/µs	

[1] t_{PLH12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.7 V_{DD2}.

[2] t_{PHL12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.4 V.

[3] t_{PLH21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.7 V_{DD1}.

[4] t_{PHL21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.9 V.

[5] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8$ V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	$θ_{JA}$		45		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

REGULATORY INFORMATION

The ADuM2250/ADuM2251 are approved by the organizations listed in Table 4.

Table 4.

UL	CSA	VDE
Recognized under UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 5000 V rms isolation voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (849 V peak) maximum working voltage RW-16 package: Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage Reinforced insulation per IEC 60601-1, 125 V rms (176 V peak) maximum working voltage RI-16-1 package: Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Reinforced insulation per IEC 60601-1, 250 V rms (353 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM2250/ADuM2251 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 10 μA).

[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM2250/ADuM2251 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout
Minimum External Tracking (Creepage)	L(I02)			Measured from input terminals to output terminals, shortest distance path along body
RW-16 Package		7.7 min	mm	
RI-16-1 Package		8.3 min	mm	
Minimum Internal Distance (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for an 849 V peak working voltage.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 450 V rms			I to II	
For Rated Mains Voltage ≤ 600 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1592	V peak
Input-to-Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		1358	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	V_{TR}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Supply Current	$I_{DD1} + I_{DD2}$	I_S	555	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

Thermal Derating Curve

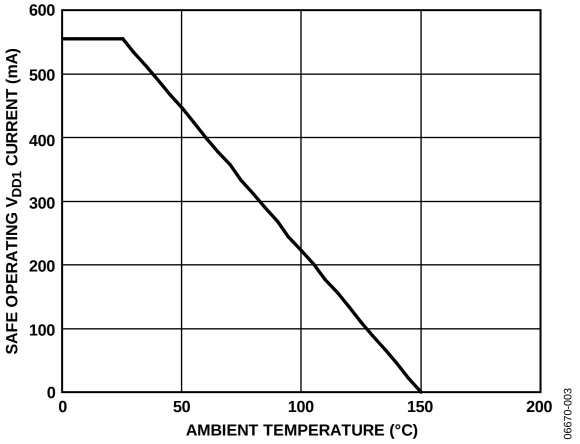


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Input/Output Signal Voltage	V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2}		5.5	V
Capacitive Load				
Side 1	C_{L1}		40	pF
Side 2	C_{L2}		400	pF
Static Output Loading				
Side 1	I_{SDA1}, I_{SCL1}	0.5	3	mA
Side 2	I_{SDA2}, I_{SCL2}	0.5	30	mA

[1] All voltages are relative to their respective grounds.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input/Output Voltage	
Side 1 (V_{SDA1}, V_{SCL1})[1]	−0.5 V to V_{DD1} + 0.5 V
Side 2 (V_{SDA2}, V_{SCL2})[1]	−0.5 V to V_{DD2} + 0.5 V
Average Output Current per Pin[2]	
Side 1 (I_{O1})	±18 mA
Side 2 (I_{O2})	±100 mA
Common-Mode Transients[3]	−100 kV/μs to +100 kV/μs

[1] All voltages are relative to their respective grounds.

[2] See Figure 3 for maximum rated current values for various temperatures.

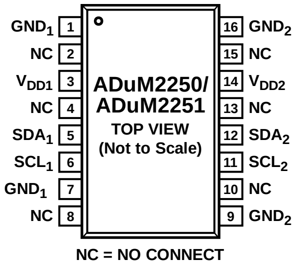
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PIN 1 AND PIN 7 ARE INTERNALLY CONNECTED TO EACH OTHER, AND IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.
2. PIN 9 AND PIN 16 ARE INTERNALLY CONNECTED TO EACH OTHER, AND IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.

06670-004

Figure 4. Pin Configuration

Table 9. ADuM2250 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 1 and Pin 7 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
2, 4, 8, 10, 13, 15	NC	No Connect.
3	V_{DD1}	Supply Voltage, 3.0 V to 5.5 V.
5	SDA_1	Data Input/Output, Side 1.
6	SCL_1	Clock Input/Output, Side 1.
9, 16	GND_2	Ground 2. Isolated ground reference for Isolator Side 2. Pin 9 and Pin 16 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
11	SCL_2	Clock Input/Output, Side 2.
12	SDA_2	Data Input/Output, Side 2.
14	V_{DD2}	Supply Voltage, 3.0 V to 5.5 V.

Table 10. ADuM2251 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 1 and Pin 7 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
2, 4, 8, 10, 13, 15	NC	No Connect.
3	V_{DD1}	Supply Voltage, 3.0 V to 5.5 V.
5	SDA_1	Data Input/Output, Side 1.
6	SCL_1	Clock Input, Side 1.
9, 16	GND_2	Ground 2. Isolated ground reference for Isolator Side 2. Pin 9 and Pin 16 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
11	SCL_2	Clock Output, Side 2.
12	SDA_2	Data Input/Output, Side 2.
14	V_{DD2}	Supply Voltage, 3.0 V to 5.5 V.

TEST CONDITIONS

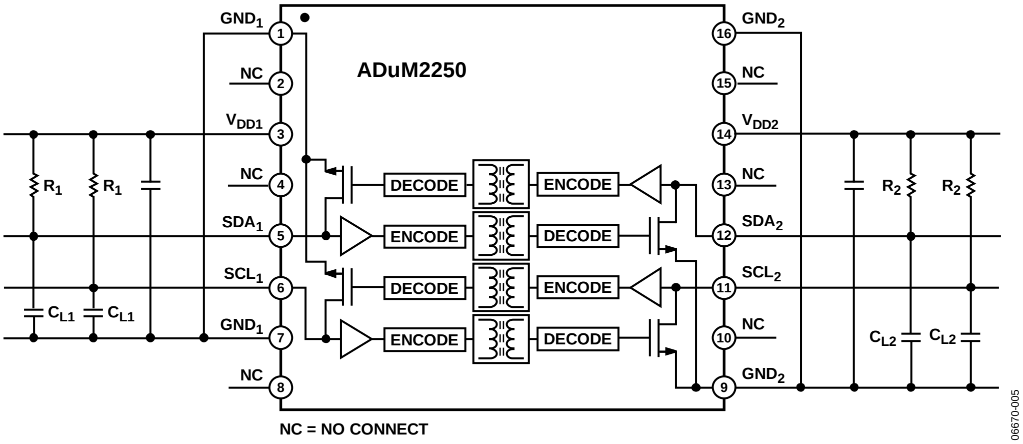


Figure 5. Timing Test Diagram

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The ADuM2250/ADuM2251 interface on each side to I^{2}C signals. Internally, the bidirectional I^{2}C signals are split into two unidirectional channels communicating in opposite directions via dedicated *i*Coupler isolation channels. One channel of each pair (the Side 1 input of each I/O pin in Figure 6) implements a special input buffer and output driver that can differentiate between externally generated inputs and its own output signals. It transfers only externally generated input signals to the corresponding Side 2 data or clock pin.

Both the Side 1 and Side 2 I^{2}C pins are designed to interface to an I^{2}C bus operating in the 3.0 V to 5.5 V range. A logic low on either side causes the corresponding I/O pin across the coupler to be pulled low enough to comply with the logic low threshold requirements of other I^{2}C devices on the bus. Bus contention and latch-up are avoided by guaranteeing that the input low threshold at SDA$_1$ or SCL$_1$ is at least 50 mV less than the output low signal at the same pin. This prevents an output logic low at Side 1 from being transmitted back to Side 2 and pulling down the I^{2}C bus by latching the state.

Because the Side 2 logic levels/thresholds and drive capabilities comply fully with standard I^{2}C values, multiple ADuM2250/ADuM2251 devices connected to a bus by their Side 2 pins can communicate with each other and with other I^{2}C-compatible devices, as shown in Figure 7. Note the distinction between I^{2}C compatibility and I^{2}C compliance. I^{2}C compatibility refers to situations in which the logic levels or drive capability of a component do not necessarily meet the requirements of the I^{2}C specification but still allow the component to communicate with an I^{2}C-compliant device. I^{2}C compliance refers to situations in which the logic levels and drive capability of a component fully meet the requirements of the I^{2}C specification.

Because the Side 1 pin has a modified output level/input threshold, Side 1 of the ADuM2250/ADuM2251 can communicate only with devices that are fully compliant with the I^{2}C standard. In other words, Side 2 of the ADuM2250/ADuM2251 is I^{2}C-compliant, whereas Side 1 is only I^{2}C-compatible.

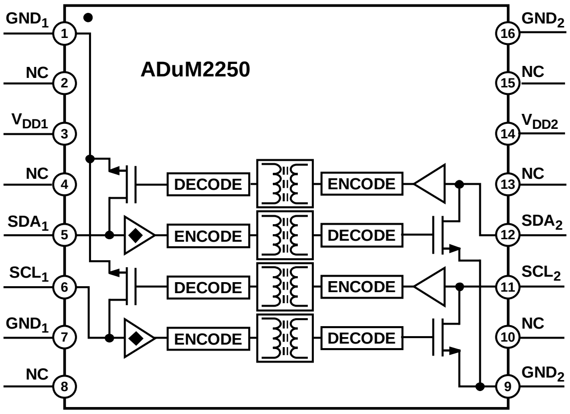
The Side 1 I/O pins must not be connected to other I^{2}C buffers that implement a similar scheme of dual I/O threshold detection. This latch-up prevention scheme is implemented in several popular I^{2}C level shifting and bus extension products currently available from Analog Devices and other manufacturers. Care should be taken to review the data sheet of potential I^{2}C bus buffering products to ensure that only one buffer on a bus segment implements a dual threshold scheme.

A bus segment is a portion of the I^{2}C bus that is isolated from other portions of the bus by galvanic isolation, bus extenders, or level shifting buffers. Table 11 shows how multiple ADuM2250/ADuM2251 components can coexist on a bus as long as two Side 1 buffers are not connected to the same bus segment.

Table 11. ADuM2250/ADuM2251 Buffer Compatibility

	Side 1	Side 2
Side 1	No	Yes
Side 2	Yes	Yes

The output logic low levels are independent of the V_{DD1} and V_{DD2} voltages. The input logic low threshold at Side 1 is also independent of V_{DD1}. However, the input logic low threshold at Side 2 is designed to be at 0.3 V_{DD2}, consistent with I^{2}C requirements. The Side 1 and Side 2 I/O pins have open-collector outputs whose high levels are set via pull-up resistors to their respective supply voltages.



◆ SYMBOL INDICATES A DUAL THRESHOLD INPUT BUFFER.

NC = NO CONNECT

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Figure 6. ADuM2250 Block Diagram

Figure 7 shows a typical application circuit, including the pull-up resistors required for both Side 1 and Side 2 buses. Bypass capacitors with values from 0.01 μF to 0.1 μF are required between V_{DD1} and GND$_1$ and between V_{DD2} and GND$_2$. The 200 Ω resistor shown in Figure 7 is required for latch-up immunity if the ambient temperature can be between 105°C and 125°C.

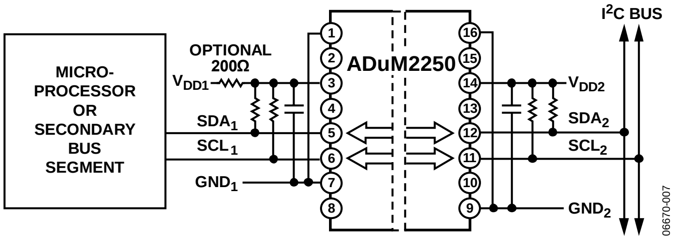


Figure 7. Typical Isolated I^{2}C Interface Using the ADuM2250

STARTUP

Both the V_{DD1} and V_{DD2} supplies have an undervoltage lockout feature that prevents the signal channels from operating unless certain criteria are met. This feature prevents the possibility of input logic low signals pulling down the I^2C bus inadvertently during power-up/power-down.

For the signal channels to be enabled, the following criteria must be met:

- Both supplies must be at least 2.5 V.
- At least 40 µs must elapse after both supplies exceed the internal start-up threshold of 2.0 V.

Until both criteria are met for both supplies, the ADuM2250/ADuM2251 outputs are pulled high, thereby ensuring a startup that avoids any disturbances on the bus. Figure 8 and Figure 9 illustrate the supply conditions for fast and slow input supply slew rates.

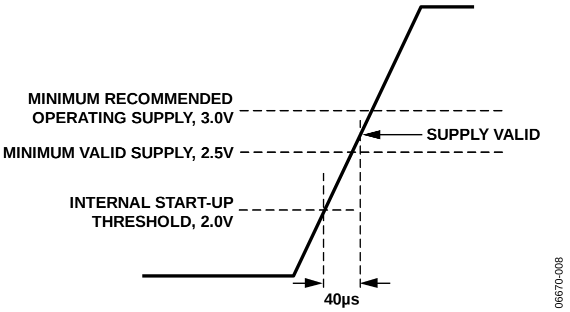


Figure 8. Start-Up Condition, Supply Slew Rate > 12.5 V/ms

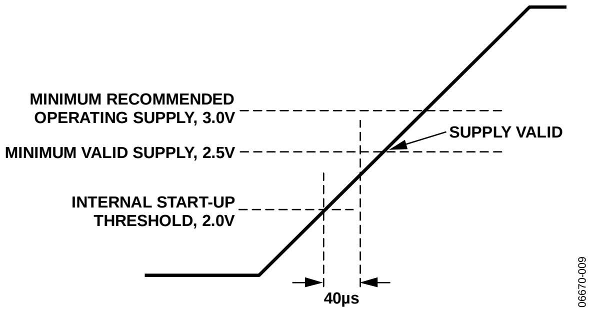


Figure 9. Start-Up Condition, Supply Slew Rate < 12.5 V/ms

MAGNETIC FIELD IMMUNITY

The ADuM2250/ADuM2251 are extremely immune to external magnetic fields. The limitation on the magnetic field immunity of the ADuM2250/ADuM2251 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM2250/ADuM2251 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the n^{th} turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM2250/ADuM2251 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 10.

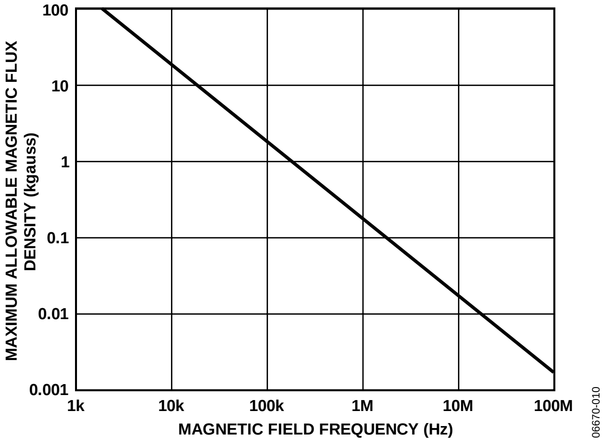


Figure 10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM2250/ADuM2251 transformers. Figure 11 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 11, the ADuM2250/ ADuM2251 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current must be placed 5 mm away from the ADuM2250/ADuM2251 to affect the operation of the component.

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

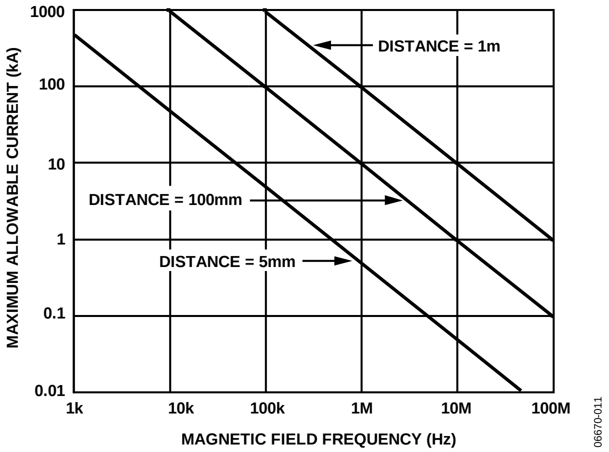
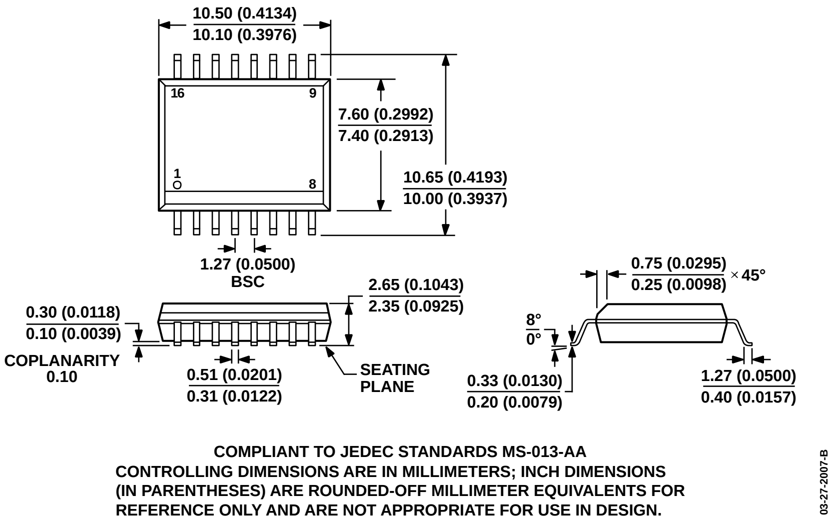


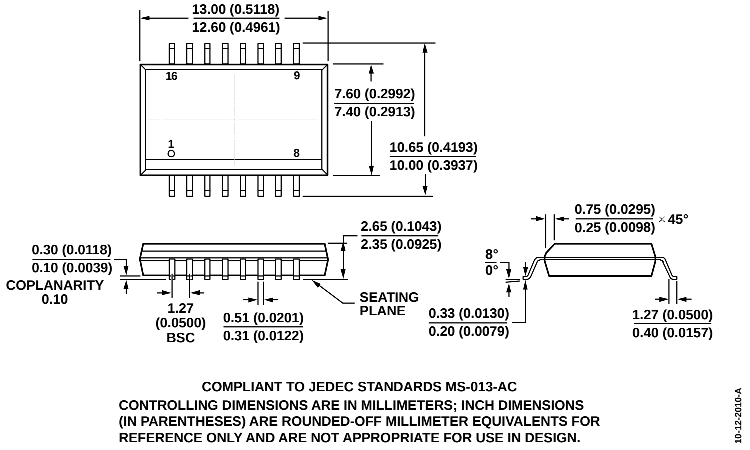
Figure 11. Maximum Allowable Current for Various Current-to-ADuM2250/ADuM2251 Spacings

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 12. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters (inches)



COMPLIANT TO JEDEC STANDARDS MS-013-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 13. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-16-1)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADuM2250ARWZ	2	2	1	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM2250ARWZ-RL	2	2	1	−40°C to +105°C	16-Lead SOIC_W, 13” Tape and Reel	RW-16
ADuM2250ARIZ	2	2	1	−40°C to +105°C	16-Lead SOIC_IC	RI-16-1
ADuM2250ARIZ-RL	2	2	1	−40°C to +105°C	16-Lead SOIC_IC, 13” Tape and Reel	RI-16-1
ADuM2251ARWZ	2	1	1	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM2251ARWZ-RL	2	1	1	−40°C to +105°C	16-Lead SOIC_W, 13” Tape and Reel	RW-16
ADuM2251ARIZ	2	1	1	−40°C to +105°C	16-Lead SOIC_IC	RI-16-1
ADuM2251ARIZ-RL	2	1	1	−40°C to +105°C	16-Lead SOIC_IC, 13” Tape and Reel	RI-16-1

[1] Z = RoHS Compliant Part.

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Экспресс доставка в любую точку России;
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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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