1 PRODUCT OVERVIEW

SAM8 PRODUCT FAMILY

Samsung's new SAM8 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM8 microcontrollers have an external interface that provides access to external memory and other peripheral devices.

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to one interrupt level at a time.

S3C8465/C8469 MICROCONTROLLER

The S3C8465/C8469 single-chip 8-bit microcontroller is designed for useful 10-bit resolution A/D converter, UART, SIO, ZCD extended PWM application field. Its powerful SAM87 CPU architecture includes. The internal register file is logically expanded to increase the on-chip register space.

The S3C8465/C8469 has 16/32K bytes of on-chip program ROM. A sophisticated bus interface enables access to external memory and other peripherals when you use the chip in ROM-less mode. Following Samsung's modular design approach, the following peripherals are integrated with the SAM87 core:

— Large number of programmable I/O ports (total 56 pins)
— One asynchronous UART module
— One synchronous SIO module
— Analog-to-digital converter with eight input channels and 10-bit resolution
— One 8-bit basic timer for watchdog function
— One 8-bit timer/counter with three operating modes (timer 0)
— One 8-bit timer for zero-cross detection circuit (timer 2)
— Two general-purpose 16-bit timer/counters with four operating modes (timer module 1)
— PWM block with one capture module, 16-bit timer/counter, PWM extension mode, and two PWM outputs
— One zero cross detection module

The S3C8465/C8469 is a versatile general-purpose microcontroller that is ideal for use in a wide range of electronics applications requiring complex timer/counter, PWM, capture, SIO, UART and ZCD functions. It is available in a 64-pin SDIP or 64-pin QFP package.

OTP

The S3P8469 is an OTP (One Time Programmable) version of the S3C8465/C8469 microcontroller. The S3P8469 microcontroller has an on-chip 32-Kbyte one-time-programmable EPROM instead of a masked ROM. The S3P8469 is comparable to the S3C8465/C8469, both in function and in pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 528-byte general purpose register area
- 16/32K-byte internal program memory
- ROM-less operating mode

External Interface

- 64K-byte external data memory area
- 64K-byte external program memory area (ROM-less mode)

Instruction Set

- 79 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 500 ns at 12 MHz f_{OSC} (minimum)

Interrupts

- 21 interrupt sources and 21 vectors
- Eight interrupt levels
- Fast interrupt processing

General I/O

- Seven I/O ports (total 56 pins)
- Seven bit-programmable ports

PWM and Capture

- Two 14-bit PWM output
- One capture

Serial I/O

- One synchronous serial I/O module
- Selectable transmit and receive rates
- Selectable baud rate for Rx and Tx respectively

Timer/Counters

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter with three operating modes (timer 0)
- One 8-bit timer for the zero-cross detection circuit
- Two 16-bit general-purpose timer/counters with four operating modes (timer C and D)

UART

- One UART module
- Full duplex serial I/O interface with three UART modes

A/D Converter

- Eight analog input pins
- 10-bit conversion resolution
- 20 µs conversion time (10 MHz CPU clock)

Zero Cross Detection Circuit

- Zero cross detection circuit that generates a digital signal in synchronization with an AC signal input

Buzzer Frequency Output

- 200 Hz to 20 kHz signal can be generated

Oscillator Frequency

- 1 MHz to 12 MHz external crystal oscillator
- Maximum 12 MHz CPU clock

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 2.7 V to 5.5 V

Package Types

- 64-pin SDIP, 64-pin QFP

BLOCK DIAGRAM

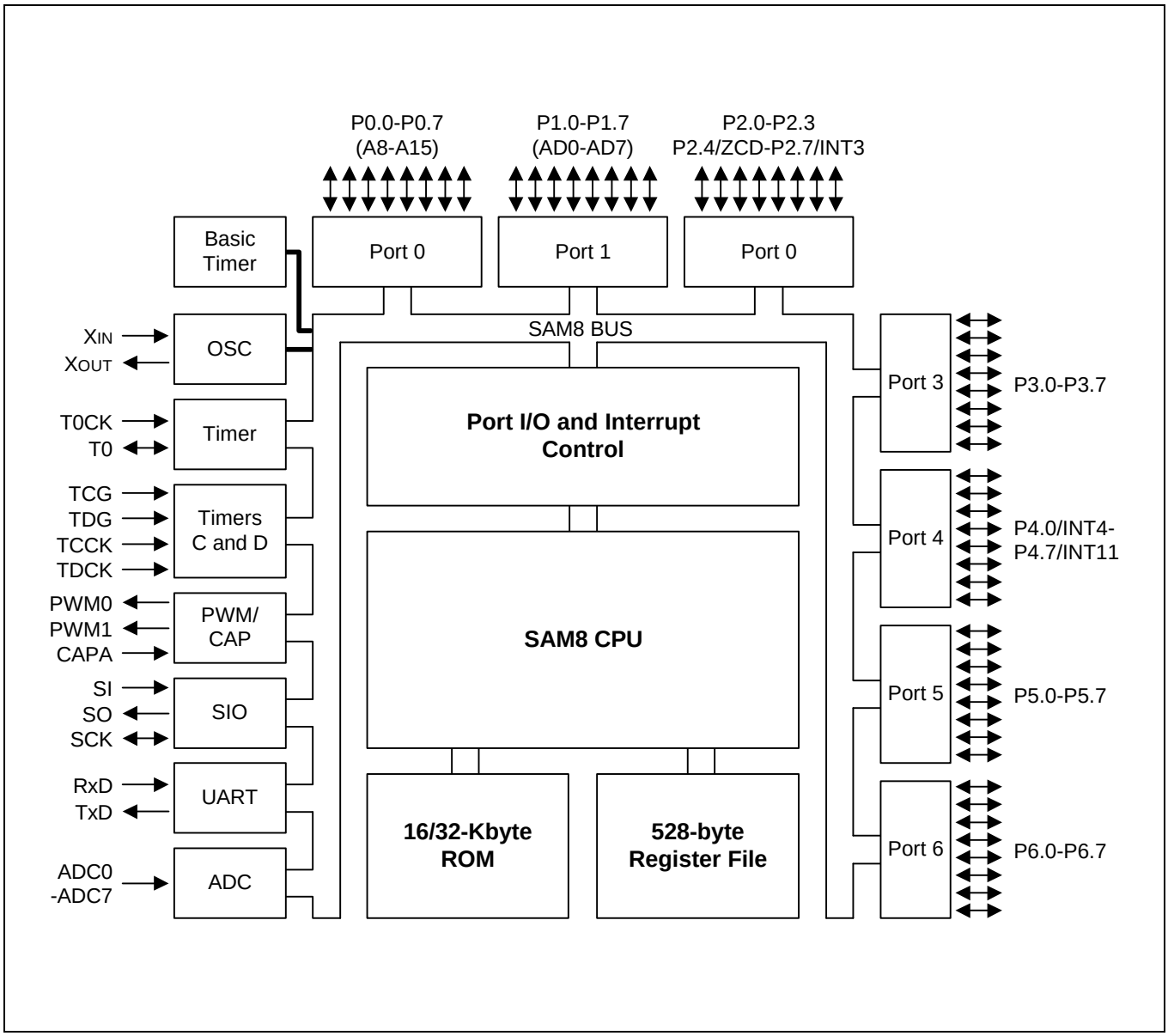


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

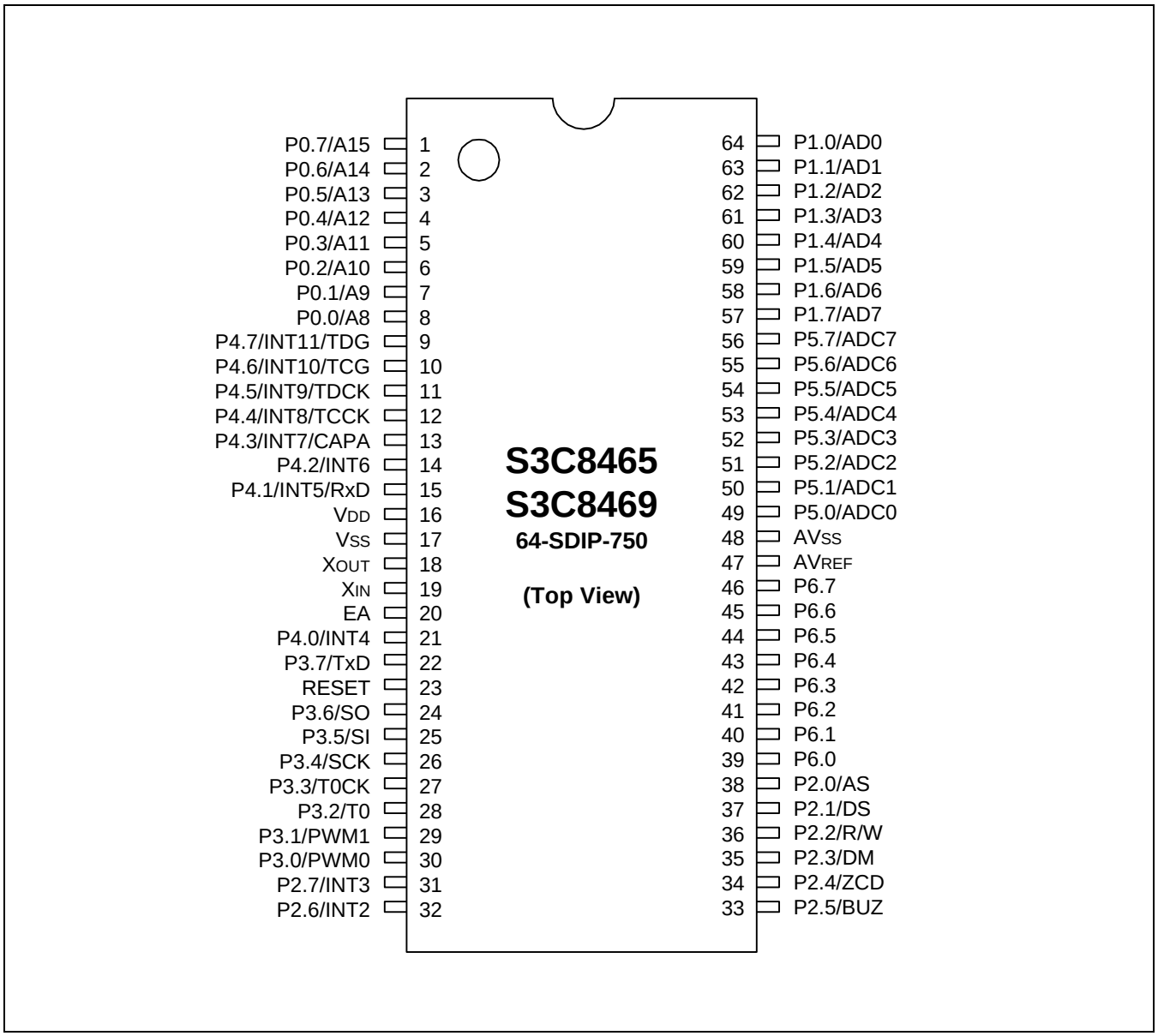


Figure 1-2. Pin Assignment Diagram (64-SDIP)

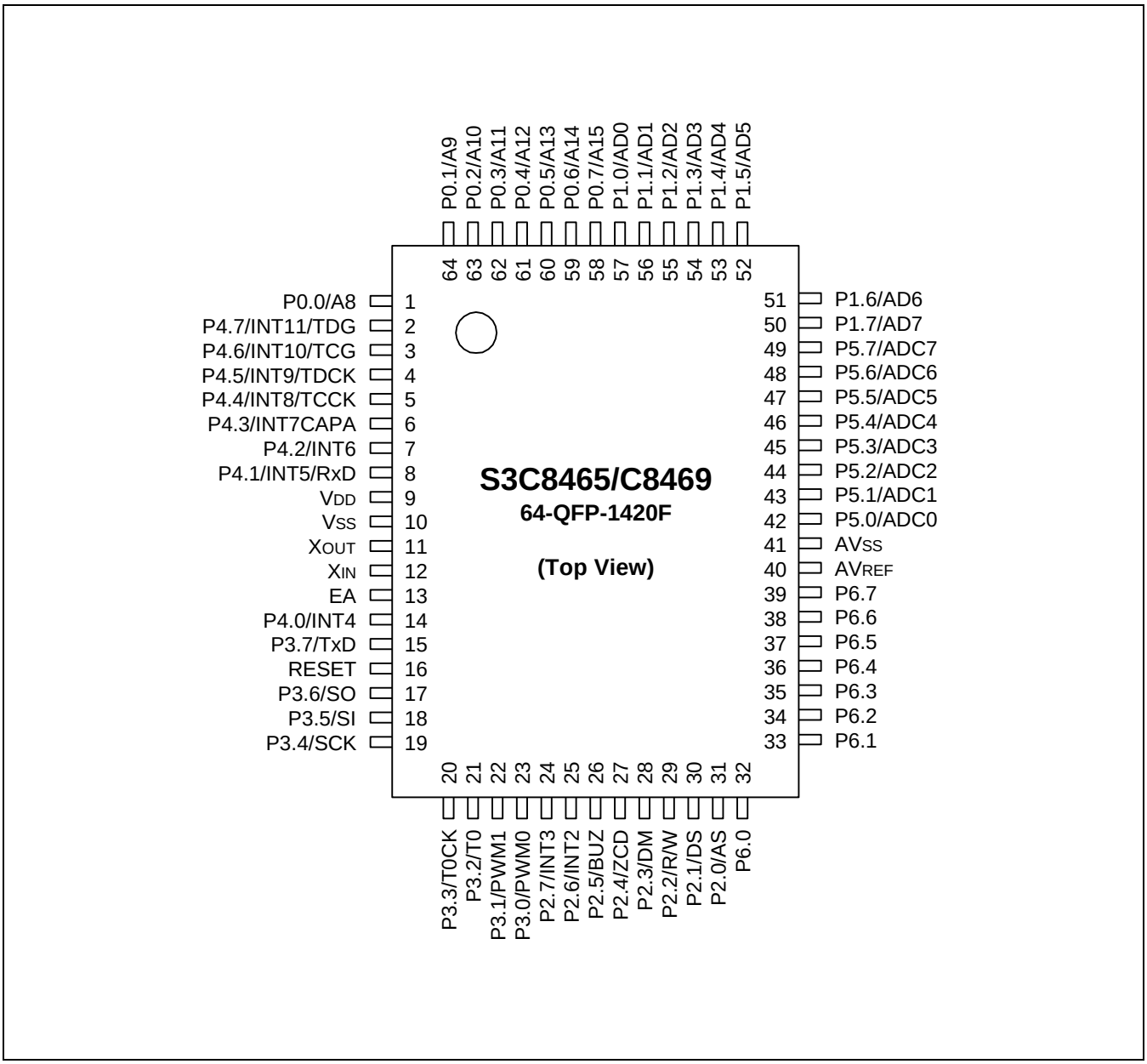


Figure 1-3. Pin Assignment Diagram (64-Pin QFP Package)

Table 1-1. S3C8465/C8469 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Number	Pin Number	Share Pins
P0.0–P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain, output. Pull-up resistors are assignable by software. Port 0 can also be configured as external interface address line A8–A15	1	8–1 (1, 64–58)	– A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0. Port 1 can also be configured as external interface address/data lines AD0–AD7	1	64–57 (57–50)	– AD0–AD7
P2.0–P2.3 P2.4–P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. P2.0–P2.3 can be configured for external bus control signals. P2.4–P2.7 are used for general I/O or for the ZCD, BUZ, INT2 and INT3	2 3	38–35 (31–28) 34–31 (27–24)	– AS, DS DM, R/W ZCD, BUZ INT2, INT3
P3.0–P3.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Each port 3 pin has an alternative function: P3.0: PWM0 (PWM0 module output) P3.1: PWM1 (PWM1 module ouptut) P3.2: T0 (T0 capture input or PWM output) P3.3: T0CK (timer 0 external clock input) P3.4: SCK (SIO module input) P3.5: SI (SIO module clock I/O) P3.6: SO (SIO module output) P3.7: TxD: SO1 (The T0 function for P3.2 is selected using the T0CON register.)	4	30–22 (23–15)	(See pin description)
P4.0–P4.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Port 4 pins are used external interrupts INT4–INT11 or for the following share functions: P4.1: RxD (UART module input) P4.3: CAPA (capture input) P4.4: TCCK (timer/counter C clock input) P4.5: TDCK (timer/counter D clock input) P4.6: TCG (timer C gate input) P4.7: TDG (timer D gate input)	5	21, 15–9 (14–2)	(See pin description)

Table 1-1. S3C8465/C8469 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Number	Pin Number	Share Pins
P5.0–P5.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, output. Pull-up resistors are assignable by software. Port 5 pins can also be used as A/D converter inputs.	6	49–56 (42–49)	ADC0–ADC7
P6.0–P6.7	I/O	Individual pins are software configurable as input or push-pull, open-drain, output. Pull-up resistors are assignable by software.	1	39–46 (32–39)	–
AD0–AD7	I/O	External interface address/data line	6	64–57 (57–50)	P1.0–P1.7
AS DS R/W DM	I/O	External bus control signals	2	38–35 (31–28)	P2.0–P2.3
ZCD	I/O	Zero cross detector input	2	34 (27)	P2.4
BUZ	I/O	200 Hz–20 kHz frequency output for buzzer sound	2	33 (26)	P2.5
PWM0 PWM1	I/O	PWM output	3	30, 29 (23, 22)	P3.0–P3.1
T0 (CAP)	I/O	T0 capture input or PWM output	3	28 (21)	P3.2
T0CK	I/O	External clock input for Timer 0	3	27 (20)	P3.3
SCK	I/O	SIO clock signal	3	26 (19)	P3.4
SI, SO	I/O	SIO data input/output	3	25, 24 (18, 17)	P3.5–P3.6
TxD	I/O	UART data output	3	22 (15)	P3.7
INT2–INT3	I/O	External interrupts: the triggering edge is selectable.	2	32, 31 (25, 24)	P2.6–P2.7
INT4	I/O	External interrupts: the triggering edge is selectable.	4	21 (14)	P4.0
RxD/INT5	I/O	UART data input or external interrupt: the triggering edge is selectable.	4	15 (8)	P4.1
INT6 CAPA/INT7	I/O	Capture module input or external interrupt: the triggering edge is selectable.	4	14,13 (7, 6)	P4.2–P4.3

Table 1-1. S3C8465/C8469 Pin Descriptions (Concluded)

Pin Name	Pin Type	Pin Description	Circuit Number	Pin Number	Share Pins
TCCK/INT8 TCDK/INT9	I/O	Timer/counter C and D clock input or external interrupts: the triggering edge is selectable.	4	12, 11 (5, 4)	P4.4–P4.5
TCG/INT10 TDG/INT11	I/O	Timer/counter C and D clock input or external interrupts: the triggering edge is selectable.	4	10, 9 (3, 2)	P4.6–P4.7
ADC0– ADC7	I/O	A/D converter inputs	5	49–56 (42–49)	P5.0–P5.7
X_{IN}, X_{OUT}	–	System clock input and output pins	–	19, 18 (12, 11)	–
RESET	I	System reset pin	7	23 (16)	–
EA	I	External access (EA) pin with three modes: 0 V: Normal operation (internal ROM) 5 V: ROM-less operation (external interface) 12.5 V: OTP read/write mode	–	20 (13)	–
AV_{REF}, AV_{SS}	–	A/D converter reference voltage input and ground	–	47, 48 (40, 41)	–
V_{DD} ,V_{SS}	–	Voltage input pin and ground	–	16, 17 (9, 10)	–

NOTE: Pin numbers shown in parentheses "( )" are for the 64-pin QFP package.

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the S3C8465/C8469

Circuit Number	Circuit Type	S3C8465/C8469 Assignments
1	I/O	Port 0,1 and port 6
2	I/O	Port 2 (P2.0–P2.3 only)
3	I/O	Port 2 (P2.4–P2.7 only)
4	I/O	Port 3
5	I/O	Port 4
6	I/O	Port 5
7	I	RESET

NOTE: Diagrams of circuit types 1–7 are presented below.

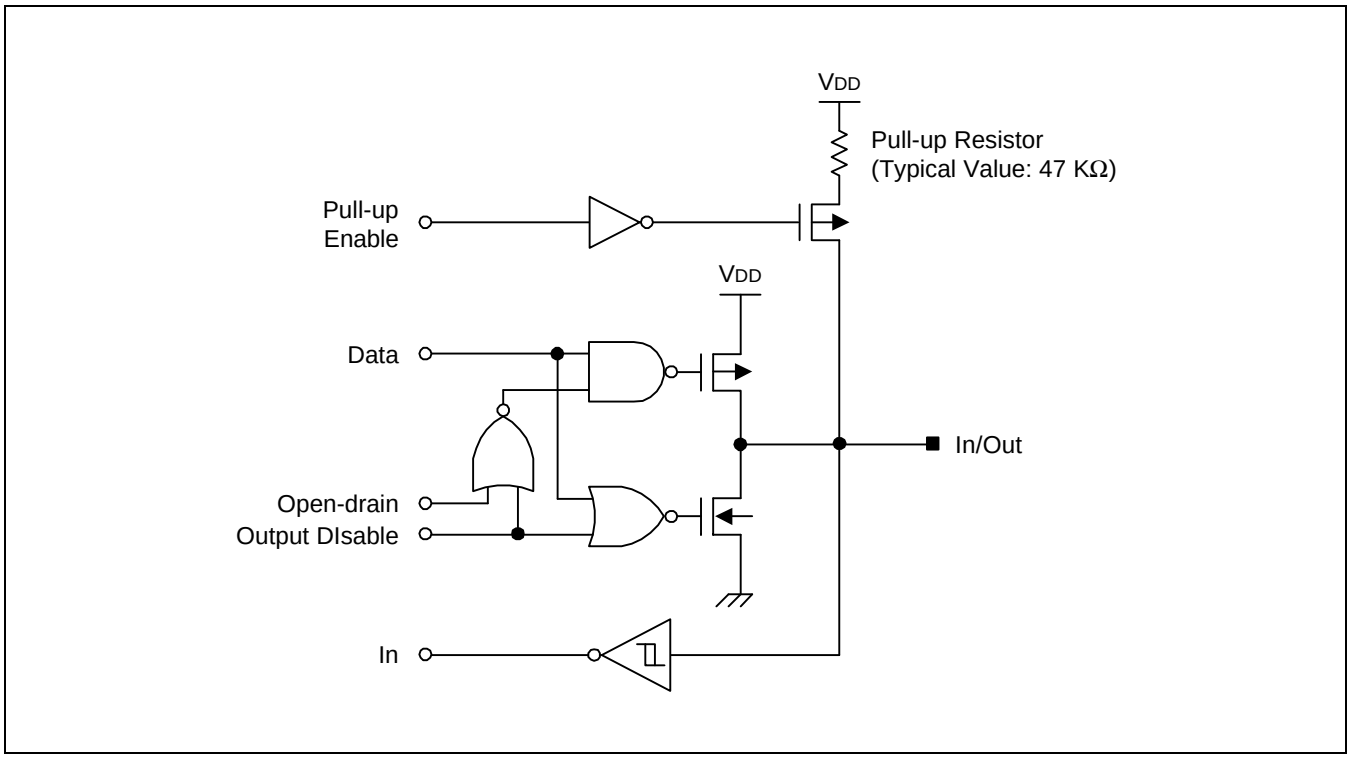


Figure 1-4. Pin Circuit Type 1 (Port 0,1 and Port 6)

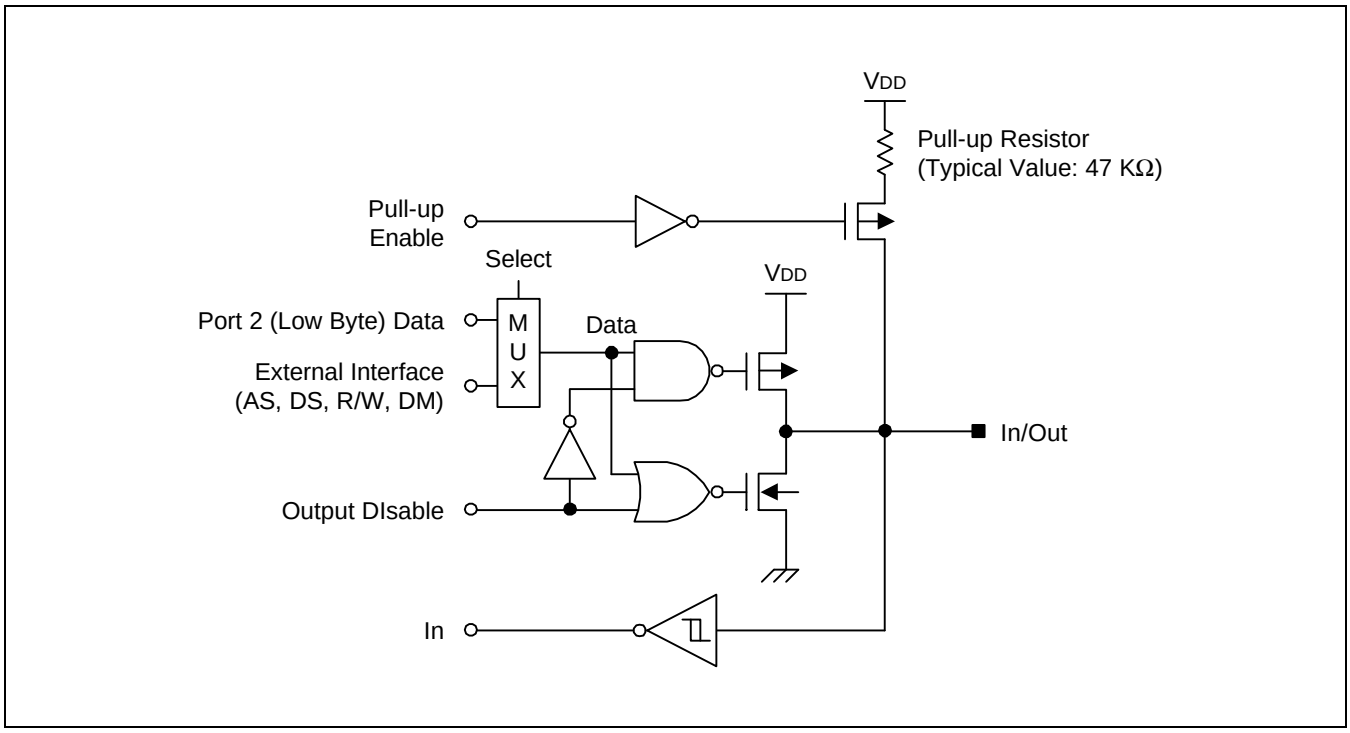


Figure 1-5. Pin Circuit Type 2 (Port 2, P2.0–P2.3 only)

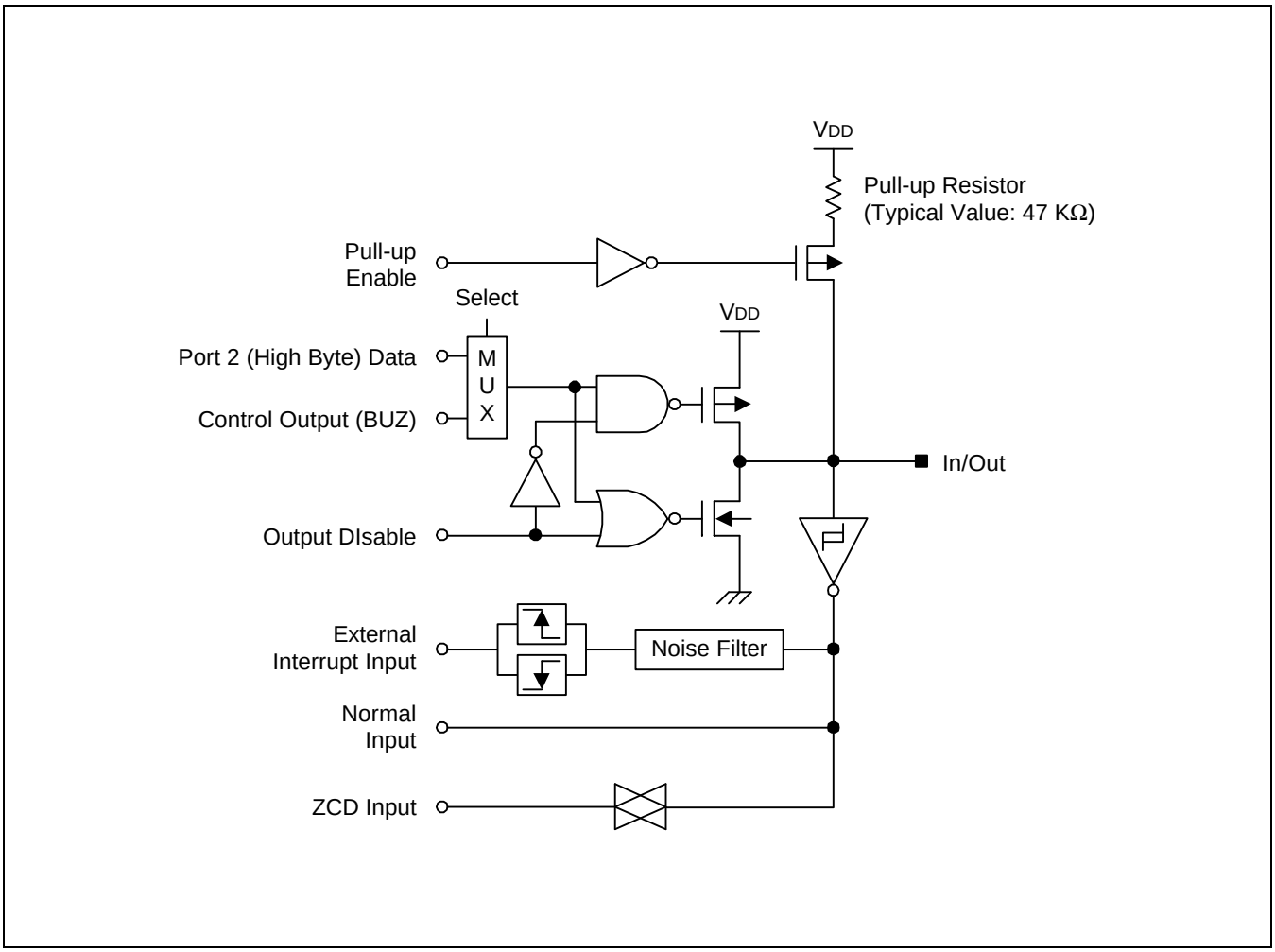


Figure 1-6. Pin Circuit Type 3 (Port 2, P2.4–P2.7 only)

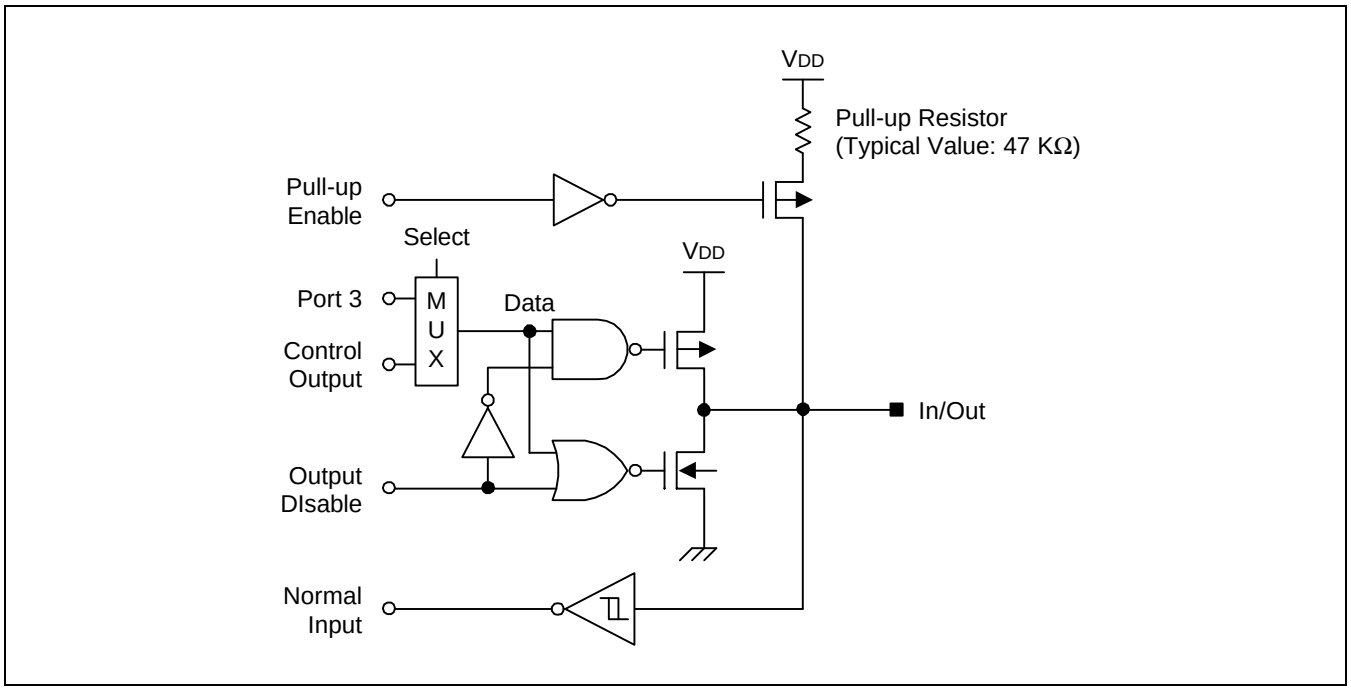


Figure 1-7. Pin Circuit Type 4 (Port 3)

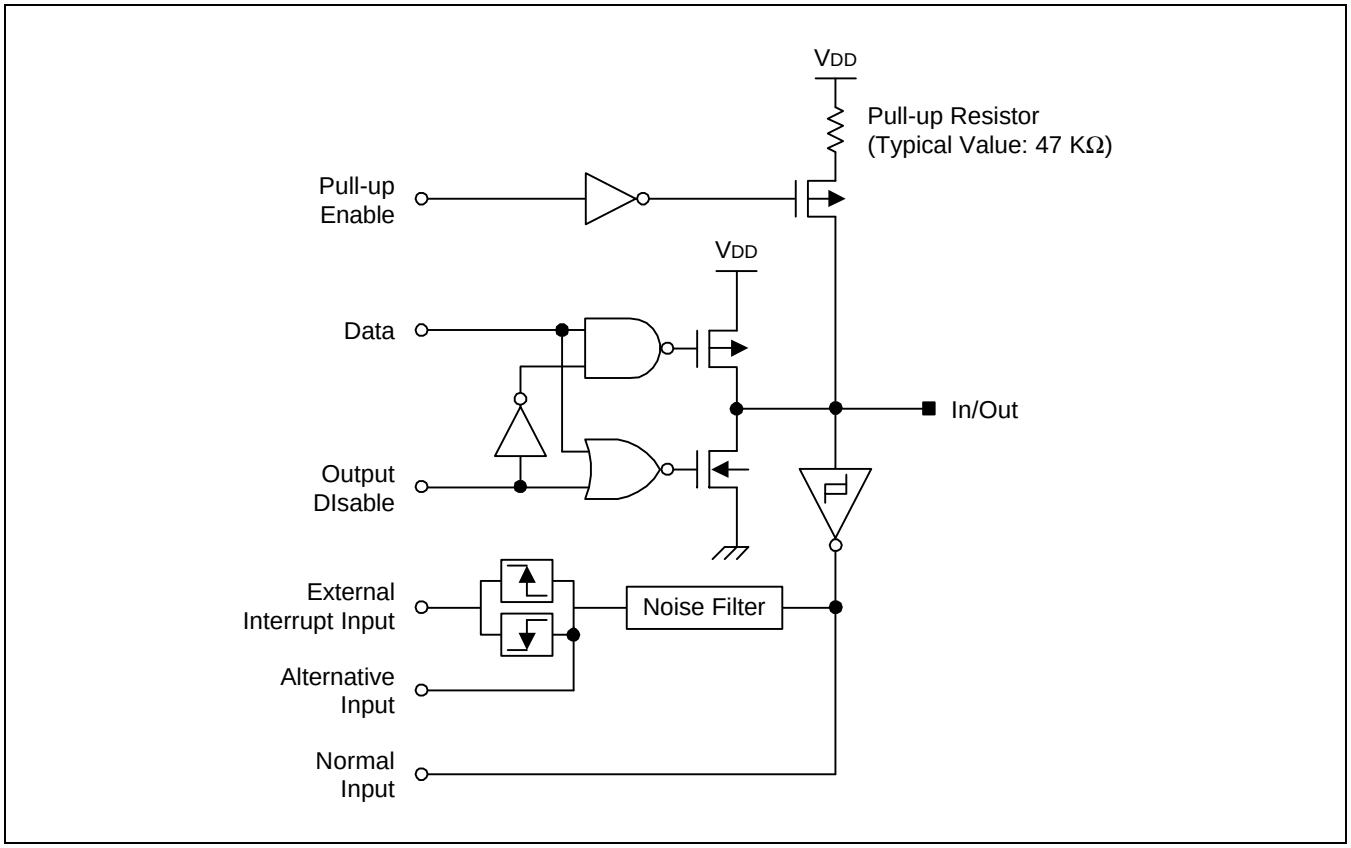


Figure 1-8. Pin Circuit Type 5 (Port 4)

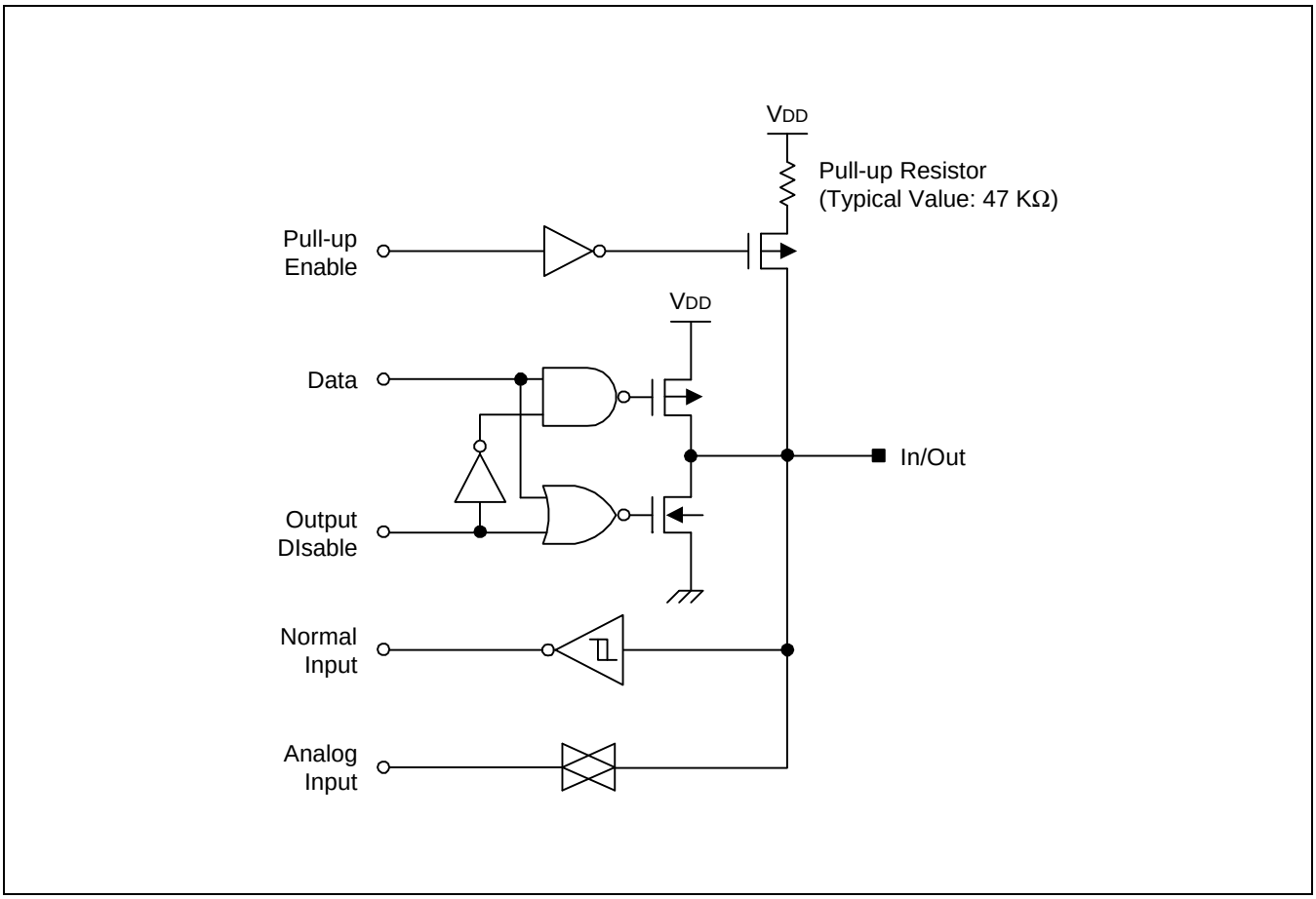


Figure 1-9. Pin Circuit Type 6 (Port 5)

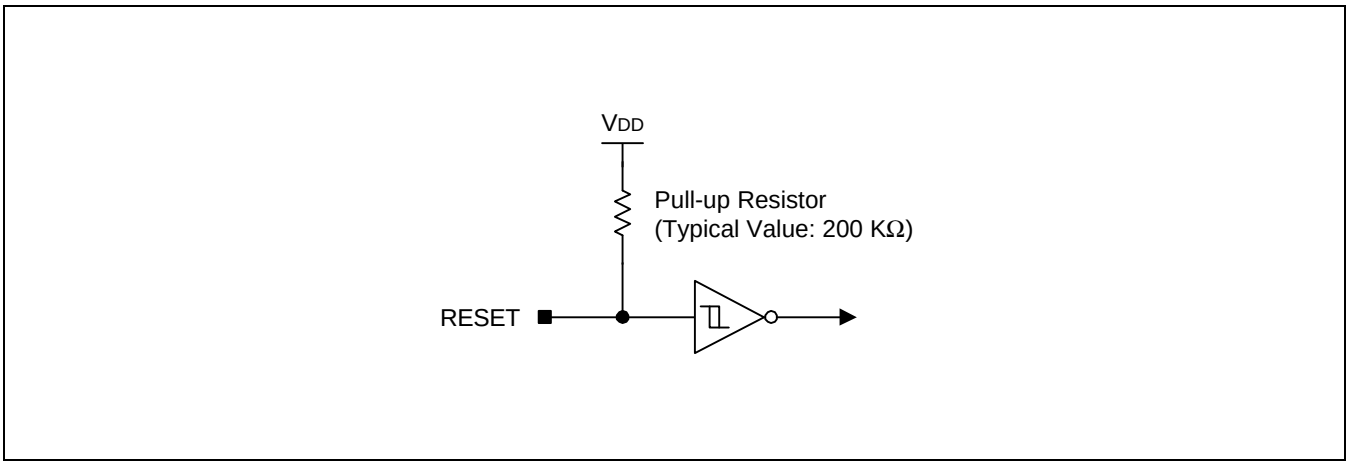


Figure 1-10. Pin Circuit Type 7 (RESET)

19 ELECTRICAL DATA

OVERVIEW

In this chapter, S3C8465/C8469 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— Input/output capacitance
— D.C. electrical characteristics
— A.C. electrical characteristics
— Oscillation characteristics
— Oscillation stabilization time
— Data retention supply voltage in stop mode
— Serial I/O timing characteristics
— UART timing characteristics in mode 0
— A/D converter electrical characteristics
— Zero crossing detector
— External memory timing characteristics

Table 19-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All input ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	All output ports	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 2–4, and 6	+ 100	
		Total pin current for ports 1 and 5	+ 200	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	°C

Table 19-2. Input/Output Capacitance

(T_A = – 40°C to 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1 MHz; unmeasured pins are tied to V_{SS}	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 19-3. D.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	V_{DD} = 2.7 V to 5.5 V All Port and RESET	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	V_{DD} = 4.5 V to 5.5 V X_{IN} and X_{OUT}	V_{DD} – 1.0			
Input Low Voltage	V_{IL1}	V_{DD} = 2.7 V to 5.5 V All Ports and RESET	–	–	0.2 V_{DD}	V
	V_{IL2}	V_{DD} = 4.5 V to 5.5 V X_{IN} and X_{OUT}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA All Ports	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 1,5, and 6	–	0.4	2.0	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 4 mA Ports 0, 2, 3, and 4				
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}	–	–	1	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except and I_{LIL2} and RESET	–	–	– 1	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT}			– 20	
Output High Leakage Current	I_{LOH1}	V_{OUT} = V_{DD} All output pins	–	–	2	µA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 2	µA

Table 19-3. D.C. Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull-up Resistor	R_{P1}	V_{DD} = 5 V; V_{IN} = 0 V	30	47	70	kΩ
		V_{DD} = 3 V; Ports 0–6	30	–	350	
	R_{P2}	V_{DD} = 5 V; V_{IN} = 0 V	100	200	400	
		V_{DD} = 3 V; RESET only	200	400	800	
Supply Current (note)	I_{DD1}	V_{DD} = 4.5 V to 5.5 V RUN mode 12 MHz CPU clock	–	16	30	mA
		V_{DD} = 2.7 V to 3.3 V 8 MHz CPU clock		5.5	12	
	I_{DD2}	V_{DD} = 4.5 V to 5.5 V Idle mode 12 MHz CPU clock		3	6	
		V_{DD} = 2.7 V to 3.3 V 8 MHz CPU clock		1	2.5	
	I_{DD3}	V_{DD} = 4.5 V to 5.5 V Stop mode		1	5	µA
		V_{DD} = 2.7 V to 3.3 V Stop mode				

NOTE: Supply current does not include current drawn through internal pull-up resistors, ZCD, ADC and external output current loads.

Table 19-4. A.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	Ports 2, 3, and 4	–	270	–	ns
RESET Input Low Width	t_{RSL}	Input	–	1500	–	ns

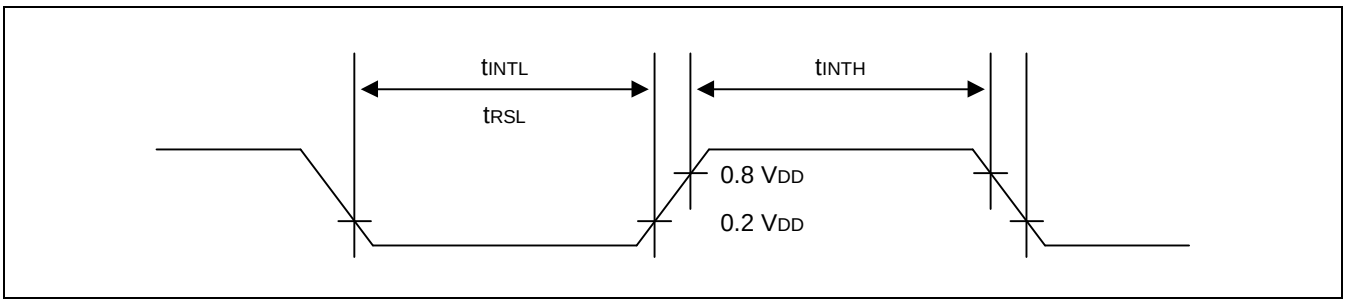
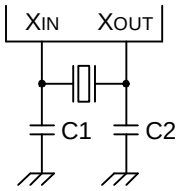
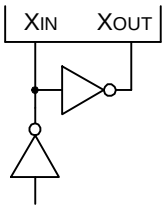


Figure 19-1. Input Timing Measurement Points

Table 19-5. Oscillation Characteristics

(T_A = – 40°C + 85°C)

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main Crystal or Ceramic		V_{DD} = 4.5 V to 5.5 V	1	–	12	MHz
		V_{DD} = 2.7 V to 4.5 V	1	–	8	
External Clock (Main System)		V_{DD} = 4.5 V to 5.5 V	1	–	12	MHz
		V_{DD} = 2.7 V to 4.5 V	1	–	8	

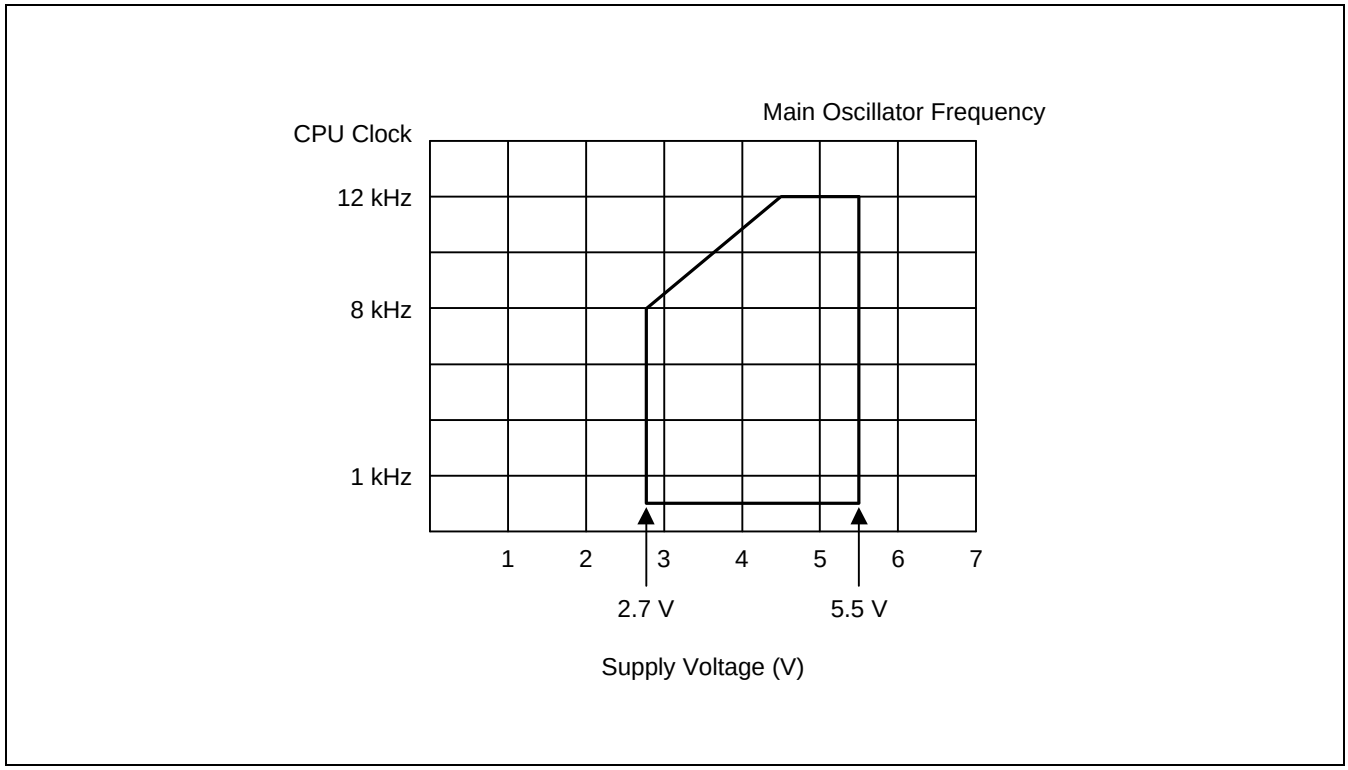


Figure 19-2. Operating Voltage Range

Table 19-6. Oscillation Stabilization Time

(T_A = – 40°C + 85°C, V_{DD} = 2.7 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main Crystal	f_{OSC} > 400 kHz;	–	–	20	ms
Main Ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	ms
External Clock (Main System)	X_{IN} input High and Low width (t_{XH}, t_{XL})	25	–	500	ns
Oscillator Stabilization Wait Time	t_{WAIT} when released by a reset (1)	–	$2^{16}/f_{OSC}$	–	ms
	t_{WAIT} when released by an interrupt (2)	–	–	–	ms

NOTES:

1. f_{OSC} is the oscillator frequency.
2. The duration of the oscillator stabilization wait time, t_{WAIT}, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

Table 19-7. Data Retention Supply Voltage in Stop Mode

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	2	–	5.5	V
Data Retention Supply Current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	5	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

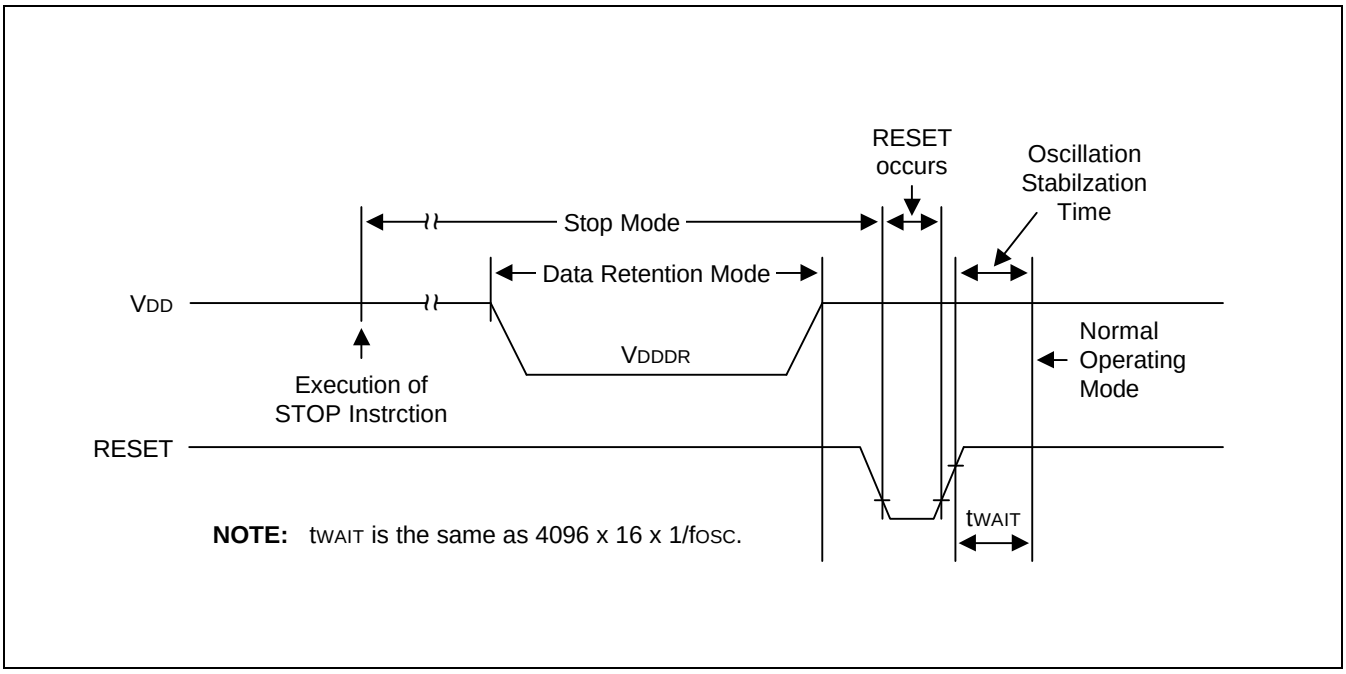


Figure 19-3. Stop Mode Release Timing When Initiated by a Reset

Table 19-8. Serial I/O Timing Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK Cycle Time	t_{CKY}	External SCK source	1000	–	–	ns
		Internal SCK source	1000			
SCK High, Low Width	t_{KH}, t_{KL}	External SCK source	500	–	–	
		Internal SCK source	t_{KCY}/2 – 50			
SI Setup Time to SCK Low	t_{SIK}	External SCK source	250	–	–	
		Internal SCK source	250			
SI Hold Time to SCK High	t_{KSI}	External SCK source	400	–	–	
		Internal SCK source	400			
Output Delay for SCK to SO	t_{KSO}	External SCK source	–	–	300	
		Internal SCK source			250	

NOTE: "SCK" means serial I/O clock frequency, "SI" means serial data input, and "SO" means serial data output.

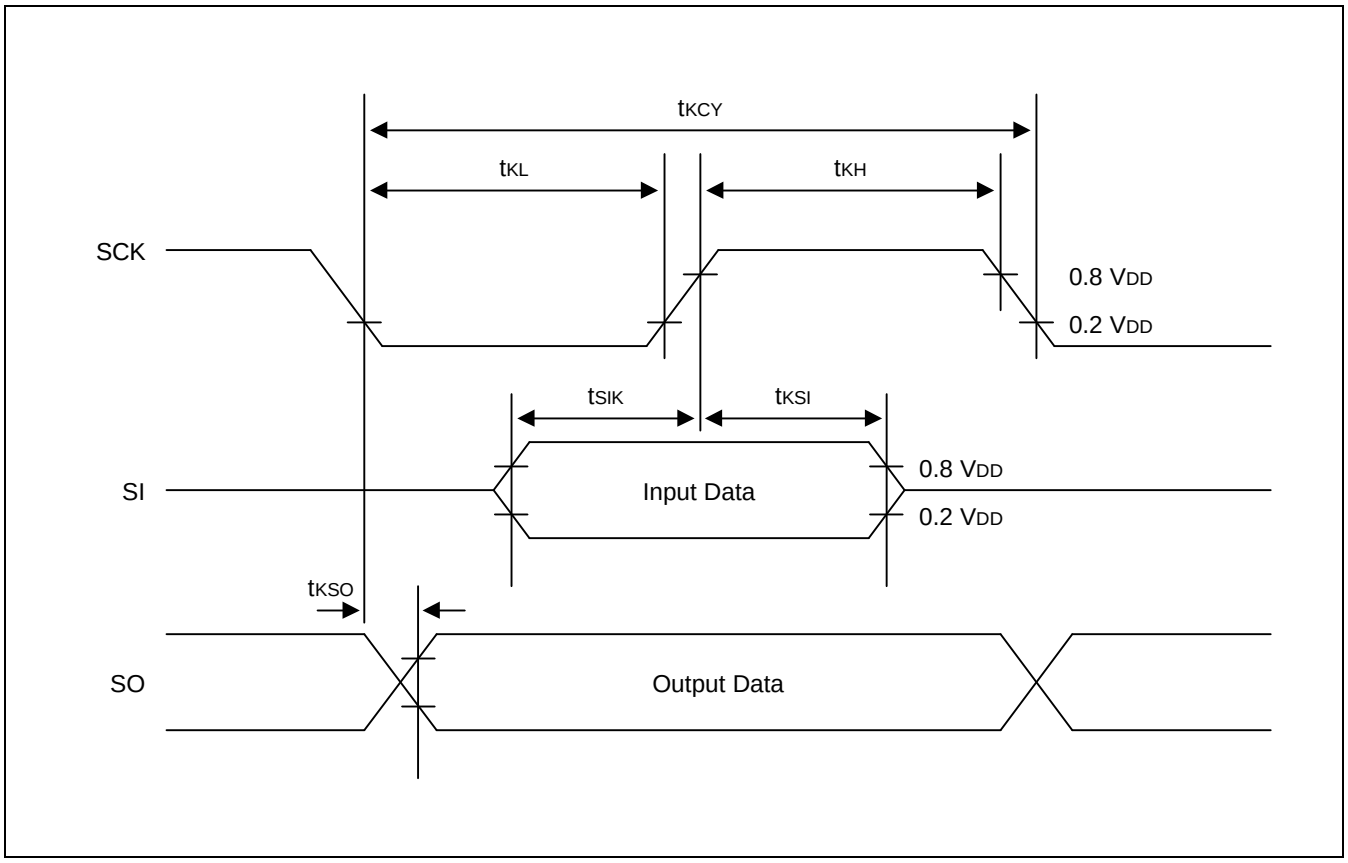


Figure 19-4. Serial Data Transfer Timing

Table 19-9. UART Timing Characteristics in Mode 0 (10 MHz)

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V, Load capacitance = 80 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Serial port clock cycle time	t_{SCK}	500	$t_{CPU} \times 6$	700	ns
Output data setup to clock rising edge	t_{S1}	300	$t_{CPU} \times 5$	–	
Clock rising edge to input data valid	t_{S2}	–	–	300	
Output data hold after clock rising edge	t_{H1}	$t_{CPU} – 50$	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	200	$t_{CPU} \times 3$	400	

NOTES:
1. All timings are in nanoseconds (ns) and assume a 10-MHz CPU clock frequency.
2. The unit t_{CPU} means one CPU clock period.

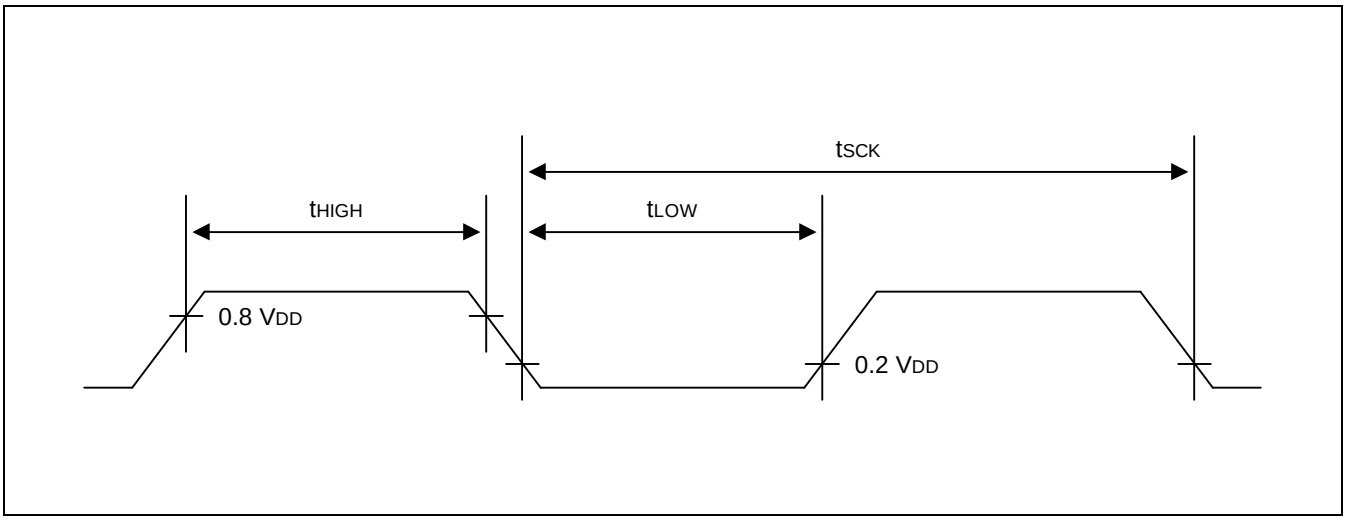
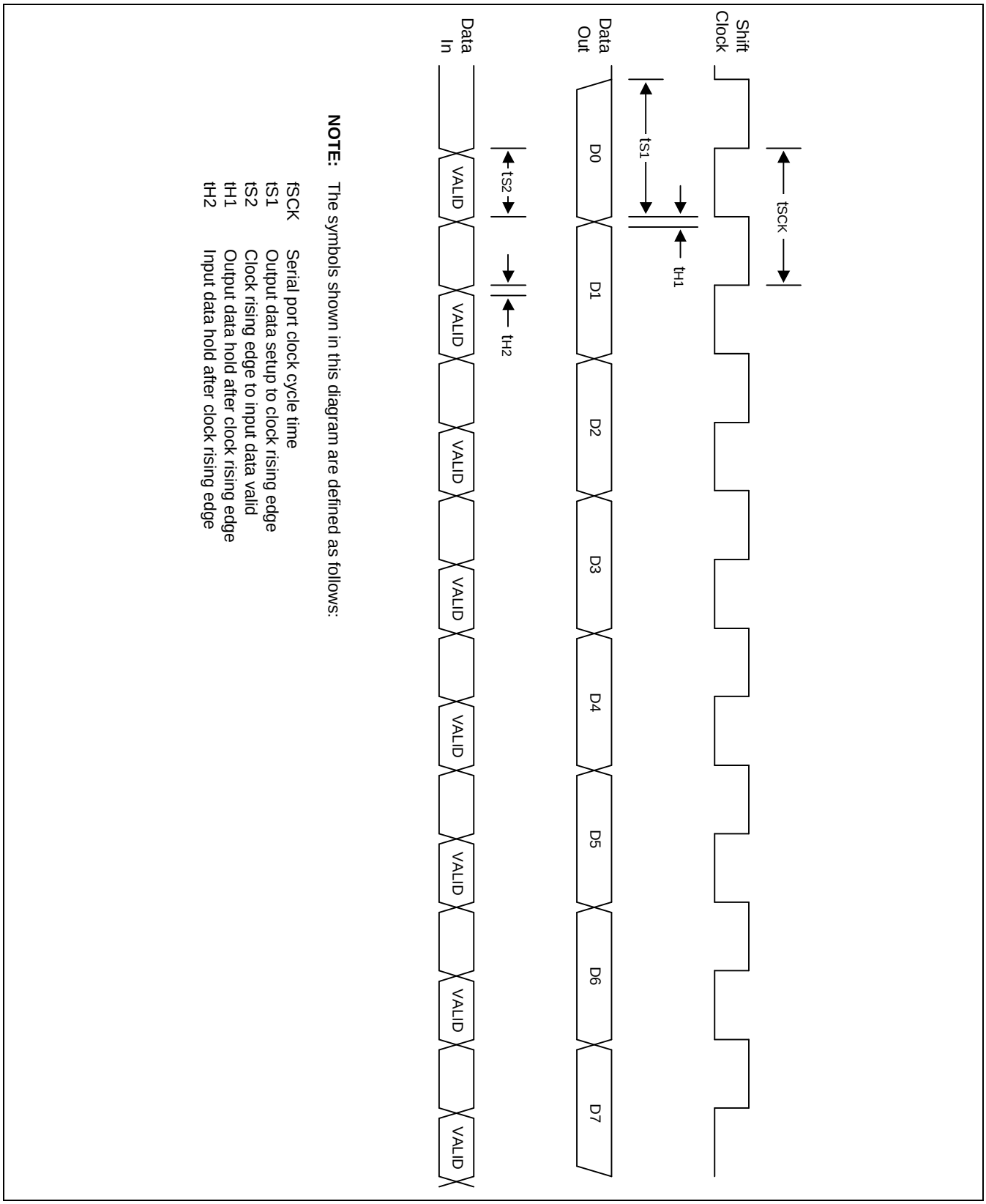


Figure 19-5. Waveform for UART Timing Characteristics



NOTE: The symbols shown in this diagram are defined as follows:

fSCK	Serial port clock cycle time
tS1	Output data setup to clock rising edge
tS2	Clock rising edge to input data valid
tH1	Output data hold after clock rising edge
tH2	Input data hold after clock rising edge

Figure 19-6. A.C. Timing Waveform for the UART Module

Table 19-10. A/D Converter Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution			–	10	–	bit
Total accuracy		V_{DD} = 5.12 V	–	–	± 3	LSB
Integral linearity error	ILE	CPU clock = 10 MHz AV_{REF} = 5.12 V		–	± 2	
Differential linearity error	DLE	AV_{SS} = 0 V		–	± 1	
Offset error of top	EOT			± 1	± 3	
Offset error of bottom	EOB			± 0.5	± 2	
Conversion time (1)	t_{CON}	10-bit conversion 50 x 4/f_{OSC} (3), f_{OSC} = 10 MHz	20	–	–	µs
Analog input voltage	V_{IAN}	–	AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	2	–	–	MΩ
Analog reference voltage	AV_{REF}	–	2.5	–	V_{DD}	V
Analog ground	AV_{SS}	–	V_{SS}	–	V_{SS} + 0.3	V
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 5 V conversion time = 20 µs	–	–	10	µA
Analog block current (2)	I_{ADC}	AV_{REF} = V_{DD} = 5 V conversion time = 20 µs		1	3	mA
		AV_{REF} = V_{DD} = 3 V conversion time = 20 µs		0.5	1.5	mA
		AV_{REF} = V_{DD} = 5 V when power down mode		100	500	nA

NOTES:

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is operating current during A/D conversion.
3. f_{OSC} is the main oscillator clock.

Table 19-11. Zero Crossing Detector

(T_A = – 40°C to + 85°C, V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero-crossing detection input voltage	V_{ZC}	AC connection c = 0.1 µF	1.0	–	3.0	Vp-p
Zero-crossing detection accuracy	V_{AZC}	f_{ZC} = 60 Hz (sine wave) V_{DD} = 5 V f_{OSC} = 10 MHz	–	–	± 150	mV
Zero-crossing detection input frequency	f_{ZC}	–	40	–	200	Hz

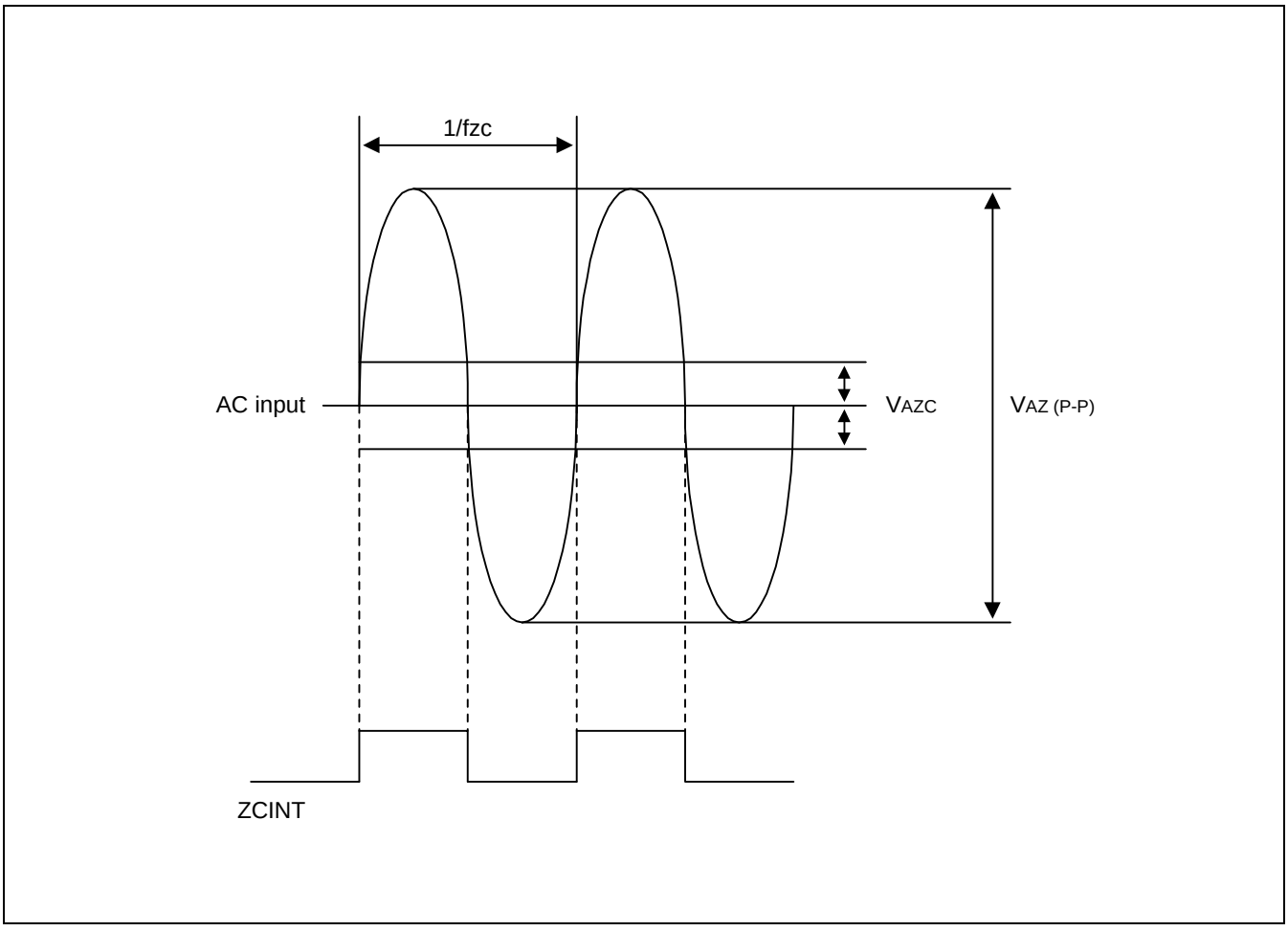


Figure 19-7. Zero Crossing Waveform Diagram

Table 19-12. External Memory Timing Characteristics (8 MHz)

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Number	Symbol	Parameter	Normal Timing (ns)	
			Min	Max
1	t_{dA} (AS)	Address valid to AS ↑ delay	10	–
2	t_{dAS} (A)	AS ↑ to address float delay	35	–
3	t_{dAS} (DR)	AS ↑ to read data required valid	–	140
4	t_{wAS}	AS Low width	43.75 (35)	–
5	t_{dA} (DS)	Address float to DS ↓	0	–
6a	t_{wDS} (read)	DS (read) Low width	156.25 (125)	–
6b	t_{wDS} (write)	DS (write) Low width	81.25 (65)	–
7	t_{dDS} (DR)	DS ↓ to read data required valid	–	80
8	t_{hDS} (DR)	Read data to DS ↑ hold time	0	–
9	t_{dDS} (A)	DS ↑ to address active delay	20	–
10	t_{dDS} (AS)	DS ↑ to AS ↓ delay	30	–
11	t_{dDO} (DS)	Write data valid to DS (write) ↓ delay	10	–
12	t_{dRW} (AS)	R/W valid to AS ↑ delay	20	–
13	t_{dDS} (DW)	DS ↑ to write data not valid delay	20	–

NOTES:
1. All times are in nanoseconds (ns) and assume an 8-MHz input frequency.
2. Wait states add 100 ns to the time of numbers 3, 6a, 6b, and 7.
3. The values for t_{wAS} and t_{wDS} that are shown in parentheses "( )" assume a 10-MHz input clock.

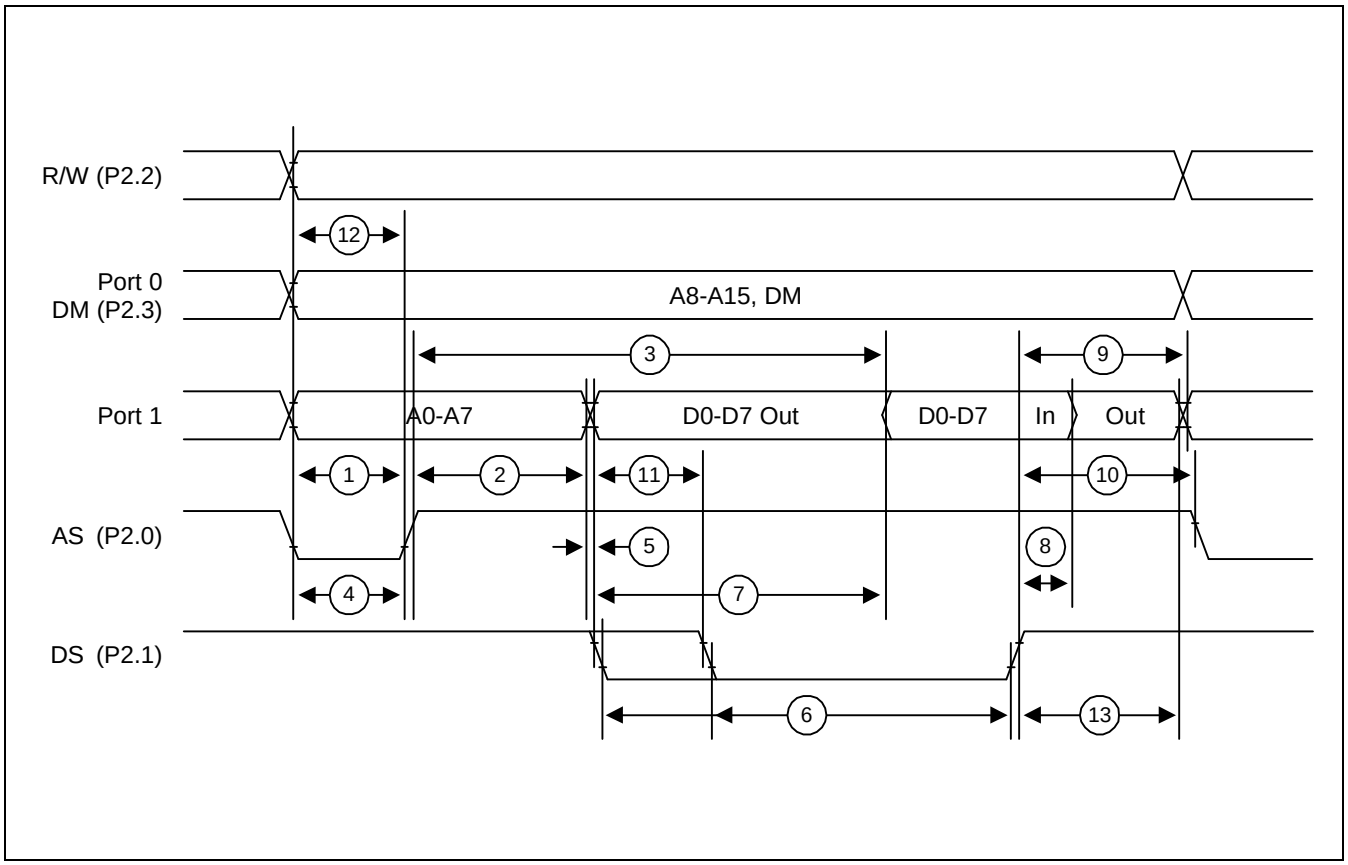


Figure 19-8. External Memory Read and Write Timing

(See Table 19-10 for a description of each timing point.)

20 MECHANICAL DATA

OVERVIEW

The S3C8465/C8469/P8469 microcontrollers are available in a 64-SDIP-750, 64-QFP-1420F package.

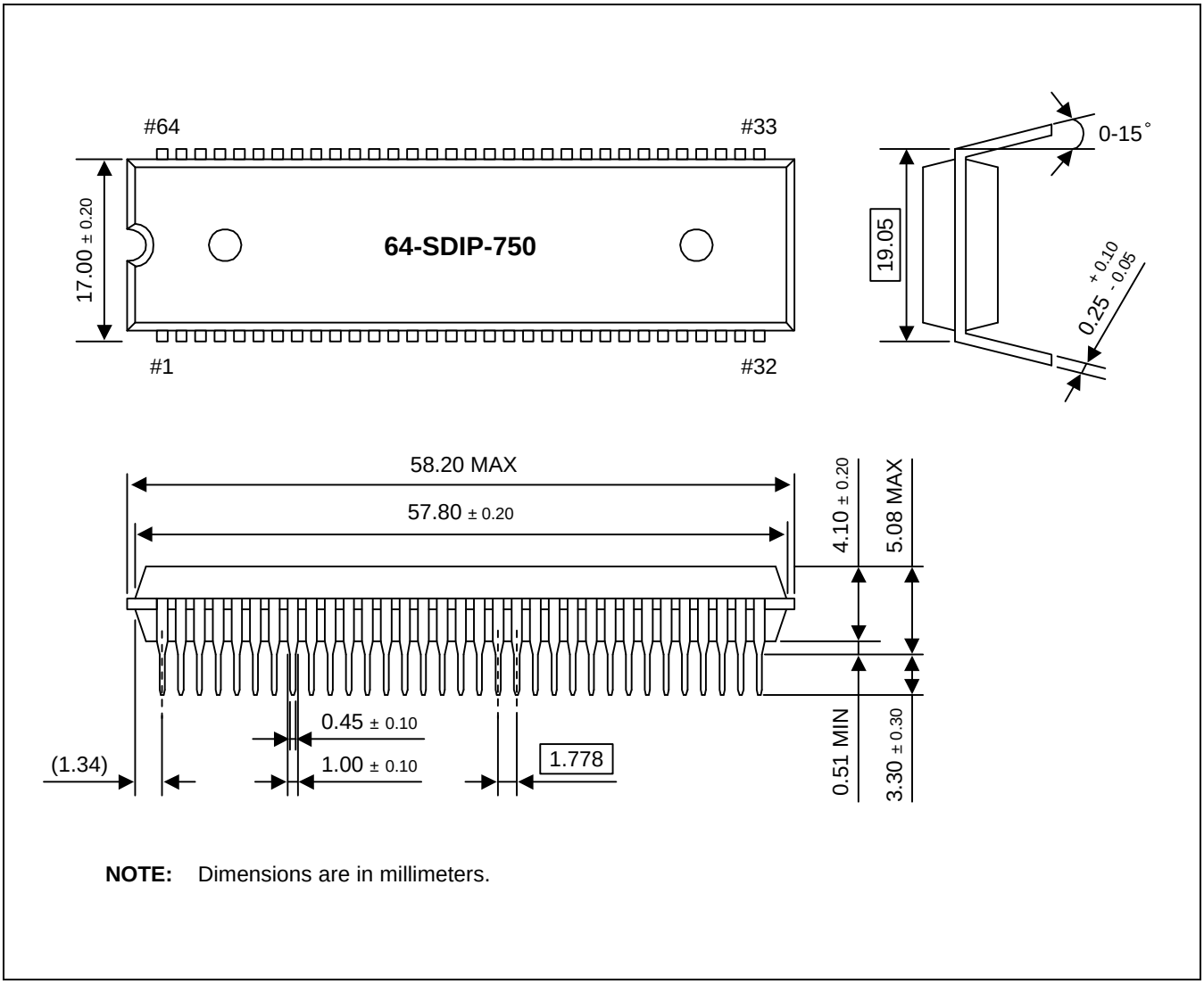
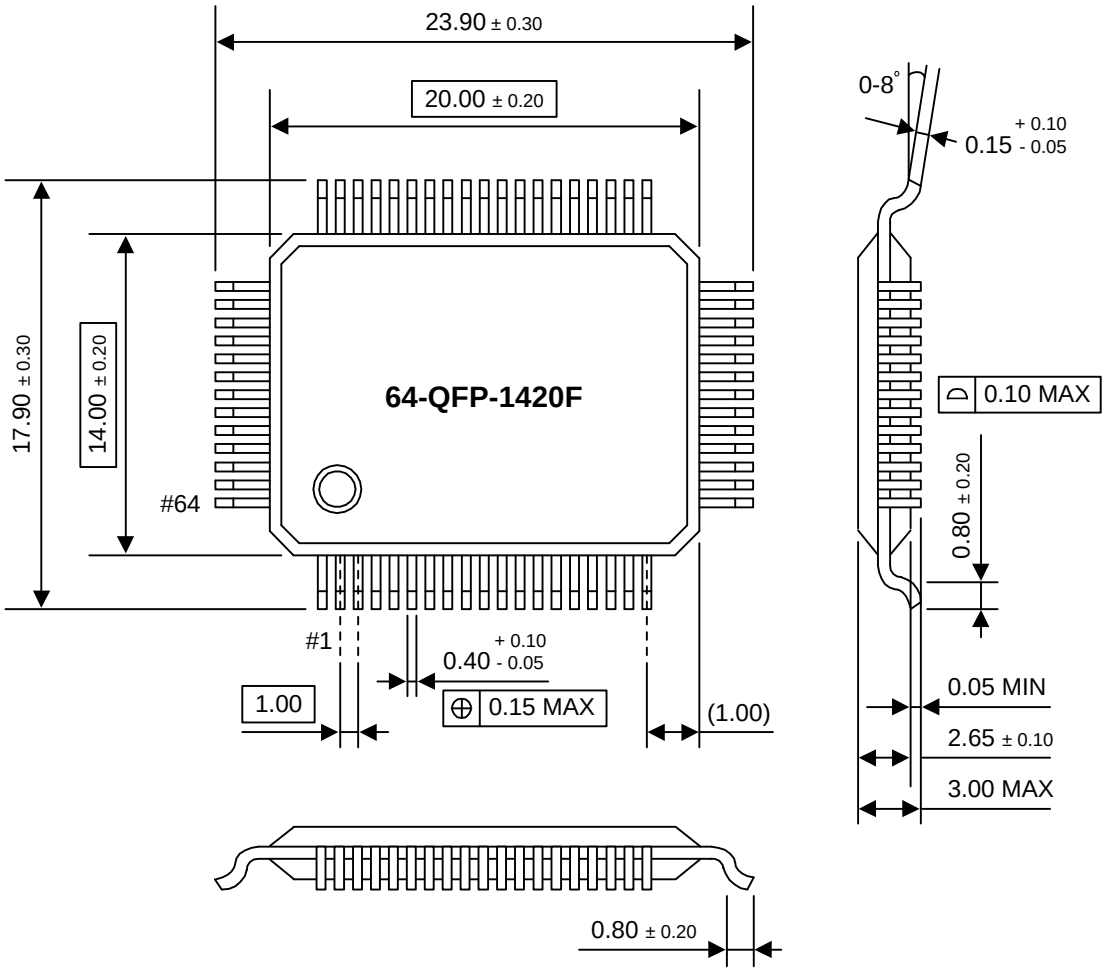


Figure 20-1. 64-SDIP-750 Package Dimensions



NOTE: Dimensions are in millimeters.

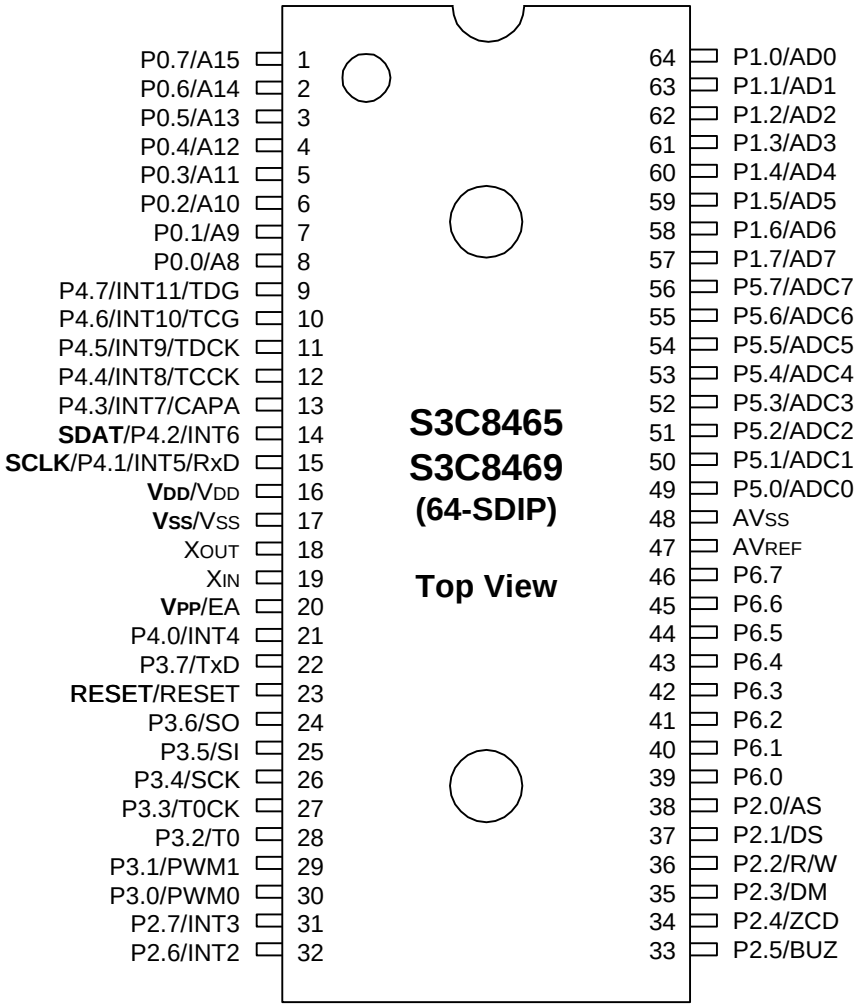
Figure 20-2. 64-QFP-1420F Package Dimensions

21 S3P8469 OTP

OVERVIEW

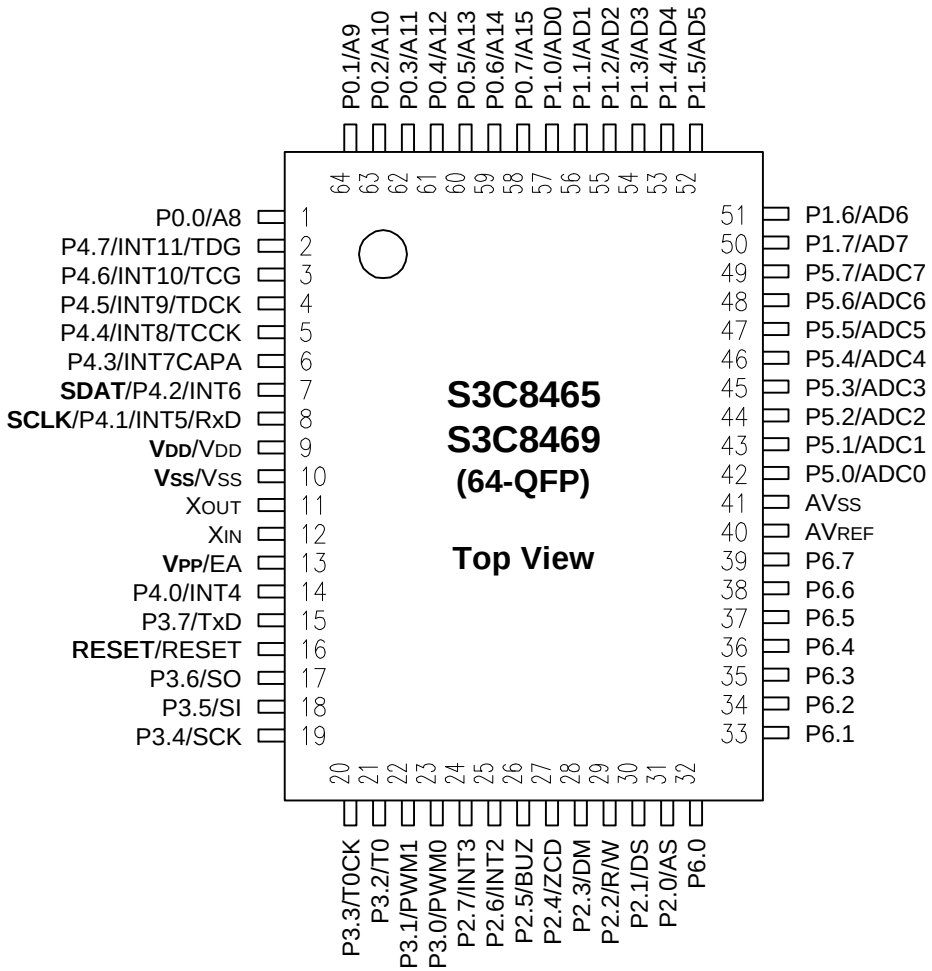
The S3P8469 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8465/C8469 microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The S3P8469 is fully compatible with the S3C8465/C8469, both in function in D.C. electrical characteristics and in pin configuration. Because of its simple programming requirements, the S3P8469 is ideal as an evaluation chip for the S3C8465/C8469.



NOTE: The bolds indicate an OTP pin name.

Figure 21-1. S3P8469 Pin Assignments (64-SDIP Package)



NOTE: The bolds indicate an OTP pin name.

Figure 21-2. S3P8469 Pin Assignments (64-QFP Package)

Table 21-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P4.2	SDAT	14(7)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P4.1	SCLK	15(8)	I	Serial clock pin. Input only pin.
EA	V_{PP}	20(13)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is aplied, OTP is in reading mode. (Option)
RESET	RESET	23(16)	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	16(9)/17(10)	–	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: ( ) means 64 QFP package.

Table 21-2. Comparison of S3P8469 and S3C8465/C8469 Features

Characteristic	S3P8469	S3C8465/C8469
Program Memory	32K-byte EPROM	16/32K-byte mask ROM
Operating Voltage (V_{DD})	2.7 V to 5.5 V	2.7 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (EA) = 12.5 V	
Pin Configuration	64 SDIP/64 QFP	64 SDIP/64 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (EA) pin of the S3P8469, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 21-3 below.

Table 21-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (EA)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

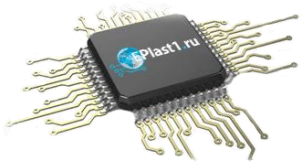
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.