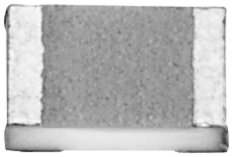
High Precision Wraparound - High Temperature (230 °C) Thin Film Chip Resistors



FEATURES

- Operating temperature range: - 55 °C; + 215 °C
- Storage temperature: - 55 °C; + 230 °C
- Gold terminations (< 1 µm thick)
- 4 sizes available (0603, 0805, 1206, 2010) - other sizes upon request
- Temperature coefficient down to 25 ppm (- 55 °C; + 215 °C)
- Tolerance down to 0.05 %
- Load life stability: 0.5 % max after 1000 h at 215 °C (ambient) at Pn
- SMD wraparound
- Compliant to RoHS directive 2002/95/EC

Pb-free

RoHS COMPLIANT

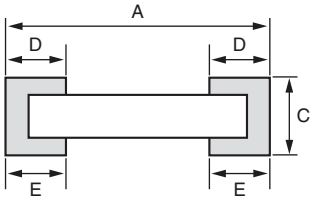
GREEN (5-2008)**

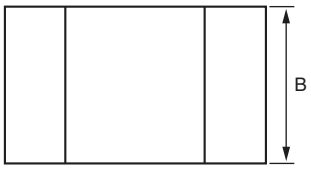
INTRODUCTION

For applications such as down hole applications, the need for parts able to withstand very severe conditions (temperature as high as 215 °C powered or up to 230 °C un-powered) has leaded Vishay Sfernice to push out the limit of the thin film technology.

Designers might read the application note: Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (P, PRA etc...) (High Temperature Application) www.vishay.com/doc?53047 in conjunction with this datasheet to help them to properly design their PCBs and get the best performances of the PHT. Vishay Sfernice R&D engineers will be willing to support any customer design considerations.

DIMENSIONS in millimeters (inches)

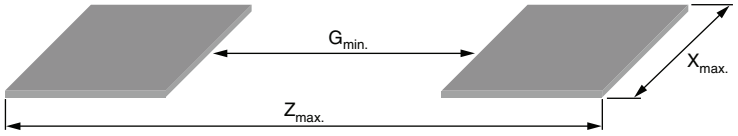




CASE SIZE	A	B	C	D/E	
	MAX. TOL. + 0.152 (+ 0.006) MIN. TOL. - 0.152 (- 0.006)	MAX. TOL. + 0.127 (+ 0.005) MIN. TOL. - 0.127 (- 0.005)			
	NOMINAL	NOMINAL		NOMINAL	TOLERANCE
0603	1.52 (0.060)	0.85 (0.033)	0.5 (0.02) ± 0.127 (0.005)	0.38 (0.015)	0.13 (0.005)
0805	1.91 (0.075)	1.27 (0.050)			
1206	3.06 (0.120)	1.60 (0.063)		0.40 (0.016)	
2010	5.08 (0.200)	2.54 (0.100)		0.48 (0.019)	

** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

SUGGESTED LAND PATTERN (to IPC-7351A)



CHIP SIZE	DIMENSIONS (in millimeter)		
	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0603	2.37	0.35	0.98
0805	2.76	0.74	1.40
1206	3.91	1.85	1.73
2010	5.93	3.71	2.67

STANDARD ELECTRICAL SPECIFICATIONS		
TEST	**SPECIFICATIONS**	**CONDITIONS**
Series	0603, 0805, 1206, 2010	
Ohmic Range (1)	10R to 7M6 (depending on series)	
Temperature Coefficient (2)	25 ppm/°C, 50 ppm/°C, 100 ppm/°C	- 55 °C; + 215 °C
Tolerance	0.05 %, 0.1 %, 0.5 %, 1 %	
Power Rating (Pn) (3)	12.5 mW to 100 mW	215 °C
Operating Temperature Range	- 55 °C; + 215 °C	
Limiting Voltage (3)	75 V to 300 V	
Load Life Stability	0.50 %	1000 h/215 °C (ambient) at Pn
Storage Temperature Range	- 55 °C; + 230 °C	
Shelf Life Stability	0.7 % typ. (1 % max.)	8000 h/230 °C

Notes
(1) Please refer to table 3 for TCR versus ohmic values
(2) See table 2
(3) See table 1

Caution:

Performances obtained with following mounting conditions:
PCB: Polyimide
Solder paste: PbSnAg (93.5/5/1.5)

TABLE 1		
SIZE	POWER RATING (1)	LIMITING VOLTAGE
0603	12.5 mW	75 V
0805	20 mW	150 V
1206	33 mW	200 V
2010	100 mW	300 V

Note

(1) For power handling improvement, please refer to application note 53047: Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (High Temperature Applications) www.vishay.com/doc?/53047 and consult Vishay Sfernice

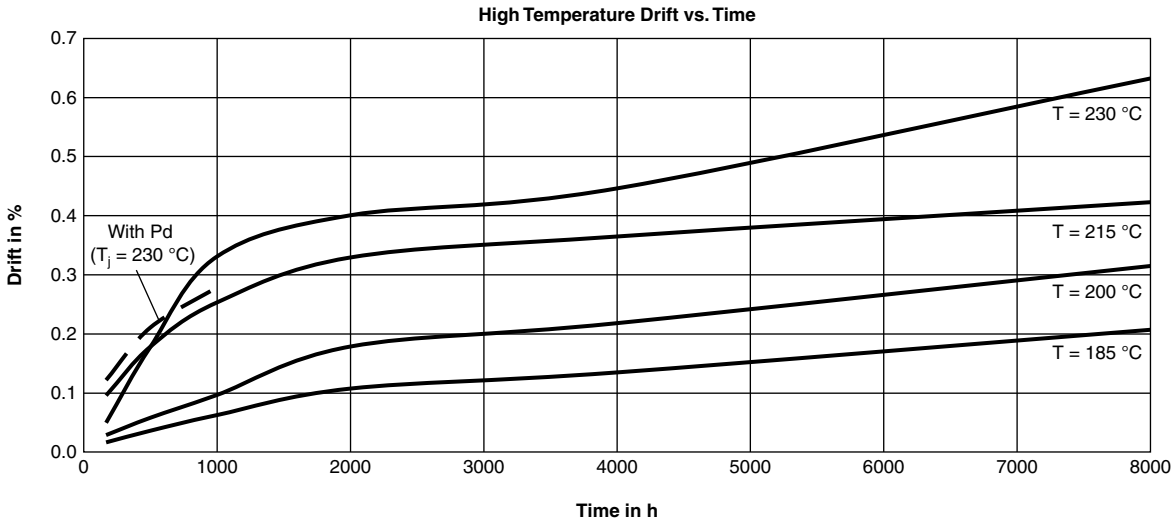
TABLE 2 - TEMPERATURE COEFFICIENT		
Y	10 ppm/°C	- 55 °C; + 155 °C
	25 ppm/°C	- 55 °C; + 215 °C
E	25 ppm/°C	- 55 °C; + 155 °C
	50 ppm/°C	- 55 °C; + 215 °C
H	50 ppm/°C	- 55 °C; + 155 °C
	100 ppm/°C	- 55 °C; + 215 °C

TABLE 3				
SERIES	OHMIC RANGE (2)			
	CT: Y		CT: E/H	
	Min.	Max.	Min.	Max.
0603	39 Ω	320K	10 Ω	320K
0805	39 Ω	511K	10 Ω	725K
1206	39 Ω	1M8	10 Ω	2M7
2010	39 Ω	5M	10 Ω	7M6

Note

(2) Best tolerance possible:
0.5 %: 10 Ω to < 20 Ω
0.1 %: 20 Ω to < 39 Ω
0.05 %: 39 Ω to max. value

PHT STABILITY CURVE



Note

- Stability will be dependent on resistivity of resistor. Above curves are worst case.

MECHANICAL SPECIFICATIONS	
Substrate	Alumina
Resistive Element	Nichrome (NiCr)
Passivation	Silicon nitride (Si_3N_4)
Protection	Epoxy + Silicone
Terminations	Gold (< 1 µm) over nickel barrier

Note

- For other terminations, please consult

POPULAR OPTIONS

It is recommended to consult Vishay Sfernice for availability first.

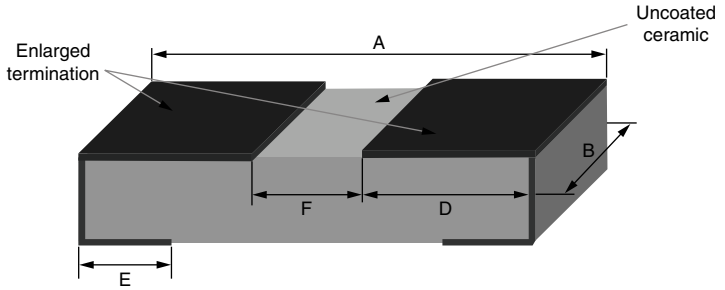
Option: Enlarged terminations:

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heatsink (see application note: 53048 Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film) www.vishay.com/doc?53048.

Option to order: 0063 (applies to size 1206/2010).

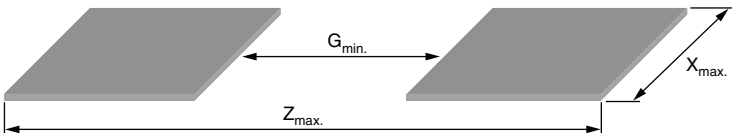
DIMENSIONS (Option 0063) in millimeters

Bottom view for mounting



CASE SIZE	A	B	E	D	F		
	MAX. TOL. + 0.152 MIN. TOL. - 0.152	MAX. TOL. + 0.127 MIN. TOL. - 0.127	MAX. TOL. + 0.13 MIN. TOL. - 0.13	MAX. TOL. + 0.13 MIN. TOL. - 0.13			
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06	1.60	0.40	1.215	0.63	0.50	0.76
2010	5.08	2.54	0.48	2.25			

SUGGESTED LAND PATTERN (Option 0063)



CHIP SIZE	DIMENSIONS (in millimeter)		
	$Z_{max.}$	$G_{min.}$	$X_{max.}$
1206	3.91	0.50	1.73
2010	5.93		2.67

PACKAGING

ESD packaging available: waffle-pack, and plastic tape and reel (low conductivity). Paper tape available upon request (ESD only).

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" × 2"	TAPE AND REEL		
			MIN.	MAX.	
0603	100	100	100	4000	8 mm
0805					
1206		140			
2010		60		2000	8 mm (1)

Note
(1) 12 mm on request

PACKAGING RULES

Waffle Pack
Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.
To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code

Tape and Reel
Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.
When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code

GLOBAL PART NUMBER INFORMATION

Global Part Numbering: PHT1206Y1001BGT063

P	H	T	1	2	0	6	Y	1	0	0	1	B	G	T	0	6	3

GLOBAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION
PHT	**0603** **0805** **1206** **2010**	**Y** **E** **H**	The first three digits are significant figures and the last digit specifies the number of zeros to follow, R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ	**W** = 0.05 % **B** = 0.1 % **D** = 0.5 % **F** = 1 %	**G** = Gold **N** = Tin/silver (2)	**T** = Tape and reel **Blank** = Waffle pack	Leave blank if no option

Note
(2) For usage at temperatures up to 200 °C maximum N (tin/silver termination are available upon request)

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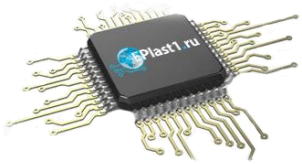
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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