

## D/A Converter Series for Electronic Adjustments

# Standard 8bit 8ch Type D/A Converters



BH2226FV, BH2226F

No.09052EBT05

## ●Description

The BH2226FV, BH2226F is an 8bit R-2R-type D/A converter with 8 channels. The D/A converter output and serial / parallel conversion function can be switched with one command, and a built-in RESET function ensures that the output voltage at all channels is Low during power up. A broad power supply voltage range (2.7V-5.5V) is available, providing design flexibility.

## ●Features

- 1) Integrated expansion port function
- 2) Built-in RESET function
- 3) High speed output response characteristics
- 4) 3-line-type serial interface
- 5) Broad power supply voltage range: 2.7V-5.5V

## ●Applications

DVCs, DSCs, DVDs, CD-Rs, CD-RWs

## ●Line up matrix

| Parameter                        | BH2226FV   | BH2226F    |
|----------------------------------|------------|------------|
| Power source voltage range       | 2.7~5.5V   | 2.7~5.5V   |
| Number of channels               | 8ch        | 8ch        |
| Current consumption              | 1.3 mA     | 1.3 mA     |
| Differential non linearity error | ±1.0LSB    | ±1.0LSB    |
| Integral non linearity error     | ±1.5LSB    | ±1.5LSB    |
| Output current performance       | ±1.0mA     | ±1.0mA     |
| Settling time                    | 100μs      | 100μs      |
| Data transfer frequency          | 10MHz      | 10MHz      |
| Input format                     | CMOS       | CMOS       |
| Data latch method                | CSB method | CSB method |
| Package                          | SSOP-B16   | SOP16      |

## ● Absolute Maximum Ratings

(Ta=25°C)

| Parameter                 | Symbol | Limits            | Unit | Remarks  |
|---------------------------|--------|-------------------|------|----------|
| Power source voltage      | VCC    | -0.3~7.0          | V    | -        |
| Terminal voltage          | VIN    | -0.3~VCC          | V    | -        |
| Storage temperature range | TSTG   | -55~125           | °C   | -        |
| Power dissipation         | PD     | 450 <sup>*1</sup> | mW   | BH2226FV |
|                           |        | 500 <sup>*2</sup> | mW   | BH2226F  |

\*1 Derated at 4.5mW/°C at Ta&gt;25°C

\*2 Derated at 5.0mW/°C at Ta&gt;25°C

\*3 Please note that this product is not robust against radiation.

## ● Recommended Operating Conditions

(Ta=25°C)

| Parameter                      | Symbol | Limits |      |      | Unit | Remarks |
|--------------------------------|--------|--------|------|------|------|---------|
|                                |        | MIN.   | TYP. | MAX. |      |         |
| VCC power source voltage       | VCC    | 2.7    | -    | 5.5  | V    | -       |
| Terminal input voltage range   | VIN    | 0      | -    | VCC  | V    | -       |
| Analog output current          | IO     | -1.0   | -    | 1.0  | mA   | -       |
| Operating temperature range    | TOPR   | -20    | -    | 85   | °C   | -       |
| Serial clock frequency         | FCLK   | -      | 1.0  | 10.0 | MHz  | -       |
| D/A output limit load capacity | CL     | -      | -    | 0.1  | μF   | -       |

## ● Electrical Characteristics

(Unless otherwise specified, VCC=3.0V, RL=OPEN, CL=0pF, Ta=25°C)

| Parameter                          | Symbol | Limits  |      |      | Unit | Conditions              |
|------------------------------------|--------|---------|------|------|------|-------------------------|
|                                    |        | MIN.    | TYP. | MAX. |      |                         |
| <Current consumption>              |        |         |      |      |      |                         |
| VCC system                         | ICC    | -       | 1.1  | 2.5  | mA   | CLK=1MHz, 80H setting   |
|                                    | ICCPD  | -       | 5    | 20   | μA   | At power down setting   |
| <Logic interface>                  |        |         |      |      |      |                         |
| L input voltage                    | VIL    | GND     | -    | 0.6  | V    | VCC=5V                  |
| H input voltage                    | VIH    | 2.4     | -    | VCC  | V    | VCC=5V                  |
| Input current                      | IIN    | -10     | -    | 10   | μA   |                         |
| L output voltage                   | VOL    | -       | -    | 0.4  | V    | IOH=2.5mA               |
| H output voltage                   | VOH    | VCC-0.4 | -    | -    | V    | IOL=0.4mA               |
| <Buffer amplifier>                 |        |         |      |      |      |                         |
| Output zero scale voltage          | ZS1    | GND     | -    | 0.1  | V    | 00H setting, at no load |
|                                    | ZS3    | GND     | -    | 0.3  | V    | 00H setting, IOH=1.0mA  |
| Output full scale voltage          | FS1    | VCC-0.1 | -    | VCC  | V    | FFH setting, at no load |
|                                    | FS3    | VCC-0.3 | -    | VCC  | V    | FFH setting, IOL=1.0mA  |
| <D/A converter precision>          |        |         |      |      |      |                         |
| Differential non linearity error   | DNL    | -1.0    | -    | 1.0  | LSB  | Input code 02H~FDH      |
| Integral non linearity error       | INL    | -1.5    | -    | 1.5  | LSB  | Input code 02H~FDH      |
| VCC power source voltage rise time | trVCC  | 100     | -    | -    | μs   | VCC=0→2.7V              |
| Power on reset release voltage     | VPOR   | -       | 1.9  | -    | V    |                         |

## ● Timing Chart

(Unless otherwise specified, VCC=3.0V, RL=OPEN, CL=0pF, Ta=25°C)

| Parameter                  | Symbol | Limits |      |      | Unit | Conditions       |
|----------------------------|--------|--------|------|------|------|------------------|
|                            |        | MIN.   | TYP. | MAX. |      |                  |
| CLK L level time           | tCLKL  | 50     | -    | -    | ns   |                  |
| CLK H level time           | tCLKH  | 50     | -    | -    | ns   |                  |
| DI setup time              | tsDI   | 20     | -    | -    | ns   |                  |
| DI hold time               | thDI   | 40     | -    | -    | ns   |                  |
| Parallel input setup time  | tsPI   | 20     | -    | -    | ns   |                  |
| Parallel input hold time   | thPI   | 40     | -    | -    | ns   |                  |
| CSB setup time             | tsCSB  | 50     | -    | -    | ns   |                  |
| CSB hold time              | thCSB  | 50     | -    | -    | ns   |                  |
| CSB H level time           | tCSBH  | 50     | -    | -    | ns   |                  |
| D/A output settling time   | tOUT   | -      | -    | 100  | μs   | CL=50pF, RL=10kΩ |
| Parallel output delay time | tpOUT  | -      | -    | 600  | ns   | CL=50pF, RL=10kΩ |
| Serial output delay time   | tsOUT  | -      | -    | 350  | ns   | CL=50pF, RL=10kΩ |

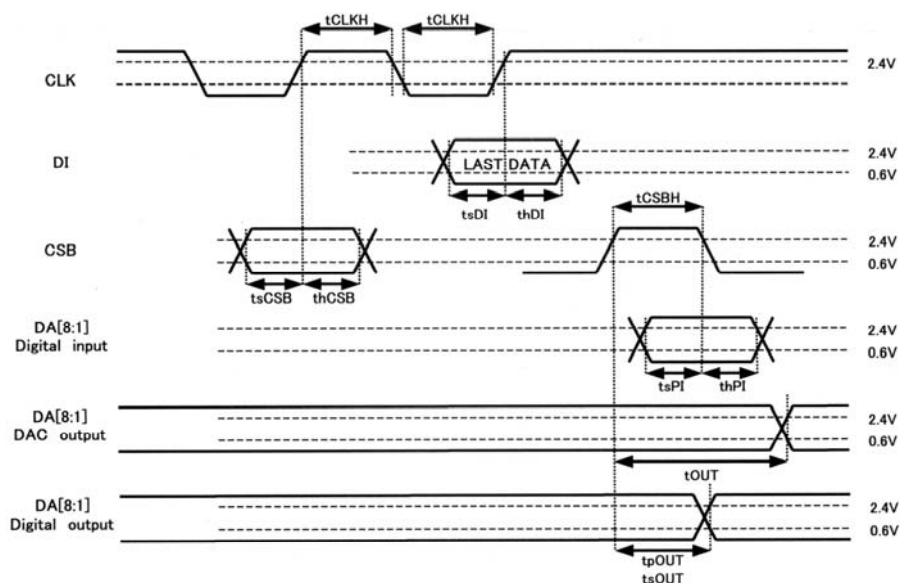


Fig.1

●Terminal Description / Block Diagrams

(BH2226FV,BH2226F)

| No. | Terminal name | Function  |
|-----|---------------|---|
| 1   | DA1           | Analog output terminal /<br>I/O input output terminal |
| 2   | DA2           |   |
| 3   | DA3           |   |
| 4   | DA4           |   |
| 5   | DA5           |   |
| 6   | DA6           |   |
| 7   | DA7           |   |
| 8   | DA8           |   |
| 9   | VCC           | Power source terminal                                 |
| 10  | RESETB        | Reset terminal  |
| 11  | TEST          | Test terminal (normal connected to GND)               |
| 12  | CSB           | Chip select signal input terminal                     |
| 13  | CLK           | Serial clock input terminal                           |
| 14  | DI            | Serial data input terminal                            |
| 15  | SO            | Serial data output terminal                           |
| 16  | GND           | Ground terminal                                       |

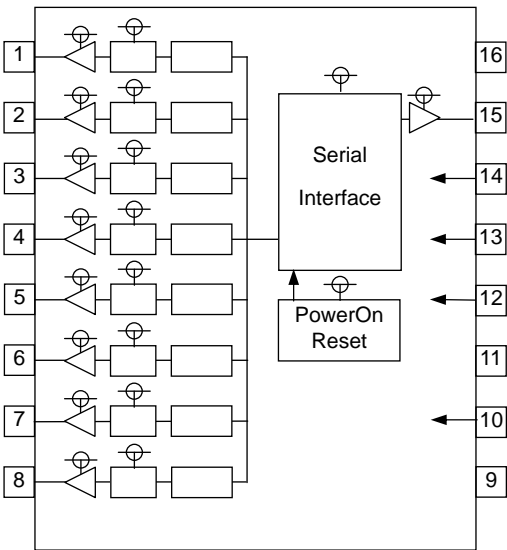


Fig.2

●Input-Output equivalence circuits

| Terminal   | Equivalence Circuit | Terminal                           | Equivalence Circuit |
|--|---------------------|------------------------------------|---------------------|
| DA1<br>DA2<br>DA3<br>DA4<br>DA5<br>DA6<br>DA7<br>DA8 |                     | DI<br>CLK<br>CSB<br>TEST<br>RESETB |                     |
|  |                     | SO                                 |                     |

Fig.3 Input-Output equivalence circuits

## ●Operation Description

### • Command Transmission

The Control command consists of 3 lines of 12bit serial input data (MSB first).

DI data is read at the rising edge of the CLK, and becomes valid in the CSB Low area (before the CSB rise for 12bit data).

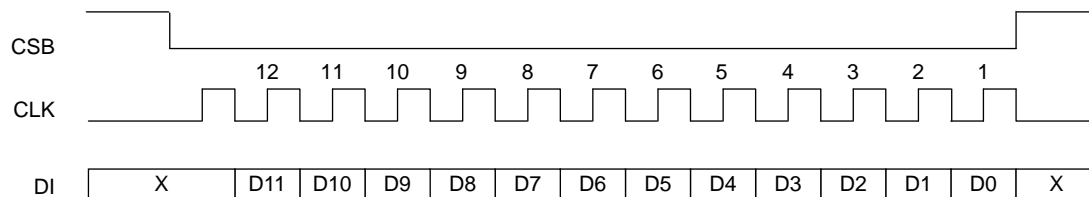


Fig.4

### Data Settings

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | Setting                              |
|----|----|----|----|----|----|----|----|--------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | At D/A setting : GND                 |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | At D/A setting : (VCC-GND)/256x1     |
| 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | At D/A setting : (VCC-GND)/256 x 2   |
| 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | At D/A setting : (VCC-GND)/256 x 3   |
| 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | At D/A setting : (VCC-GND)/256 x 4   |
| ~  |    |    |    |    |    |    |    | ~                                    |
| 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | At D/A setting : (VCC-GND)/256 x 254 |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | At D/A setting : (VCC-GND)/256 x 255 |

(Note) Default D[7:0]=00h

### Channel Settings

| D8 | D9 | D10 | D11 | Setting                      |
|----|----|-----|-----|------------------------------|
| 0  | 0  | 0   | 0   | Power down setting (default) |
| 0  | 0  | 0   | 1   | DA1                          |
| 0  | 0  | 1   | 0   | DA2                          |
| 0  | 0  | 1   | 1   | DA3                          |
| 0  | 1  | 0   | 0   | DA4                          |
| 0  | 1  | 0   | 1   | DA5                          |
| 0  | 1  | 1   | 0   | DA6                          |
| 0  | 1  | 1   | 1   | DA7                          |
| 1  | 0  | 0   | 0   | DA8                          |
| 1  | 0  | 0   | 1   | Power down release           |
| 1  | 0  | 1   | 0   | Inconsequential              |
| 1  | 0  | 1   | 1   | Inconsequential              |
| 1  | 1  | 0   | 0   | I/O D/A select               |
| 1  | 1  | 0   | 1   | I/O serial⇒Parallel          |
| 1  | 1  | 1   | 0   | I/O parallel⇒Serial          |
| 1  | 1  | 1   | 1   | I/O status setting           |

Input / Output D/A Selection settings : Each channel can be set for either I/O port or D/A converter output.

0: I/O mode (When I/O mode is selected, set the status as well.)

1: D/A mode (Set the I/O status to output mode.)

| D0  | D1  | D2  | D3  | D4  | D5  | D6  | D7  | Description                                      |
|-----|-----|-----|-----|-----|-----|-----|-----|--|
| DA1 | DA2 | DA3 | DA4 | DA5 | DA6 | DA7 | DA8 | Corresponding terminals for I/O or D/A selection |

I/O Status Setting : Set the status of the I/O input output terminal by D0 ~ D7.

0: input mode (High-Z status)

1: output mode

| D0  | D1  | D2  | D3  | D4  | D5  | D6  | D7  | Description                                |
|-----|-----|-----|-----|-----|-----|-----|-----|--|
| DA1 | DA2 | DA3 | DA4 | DA5 | DA6 | DA7 | DA8 | Corresponding terminals for status setting |

- Command Transmission Procedures

Carry out the following after power on and just after external reset:

- (1) Power Down Release (2) I/O D/A Select (3) I/O Status Set

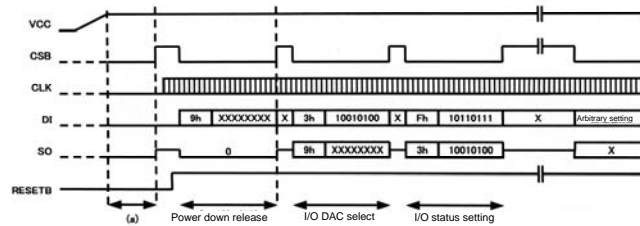


Fig.5

Note: When power is started, the power on reset is activated and the internal register initialized. However, as shown in the figure above, in area (a), if CSB cannot be made High and noise is introduced in the control line an error may occur when setting during the rising CSB signal.

In such a case, set the external RESETB terminal to Low and reset when CSB = High.

- Parallel - Serial Conversion

Parallel data {DA[8:1]} is taken in at the first CSB falling edge after setting the parallel serial command.

The data is then outputted in synch with the falling edge of the CLK in the next CSB = Low area, and output from 4CLK. However, please note that the SCLK falling edge that occurs from CSB fall to the first SCLK rising edge is not counted.

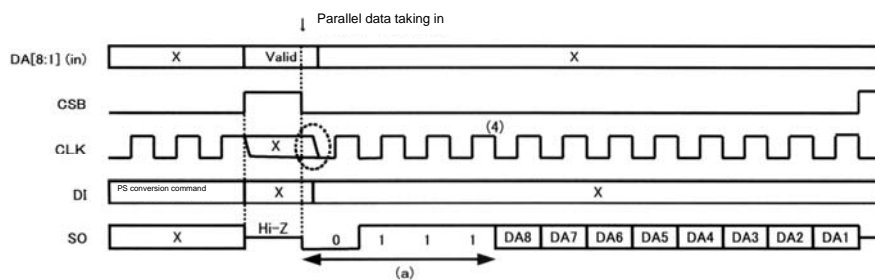


Fig.6

- Serial - Parallel Conversion

DI serial data is taken in at the rising edge of the CLK.

The data is then output from the DA[8:1] terminal just after the CSB rising edge.

During that time the SO terminal output becomes undetermined (just previous address setting + data output).

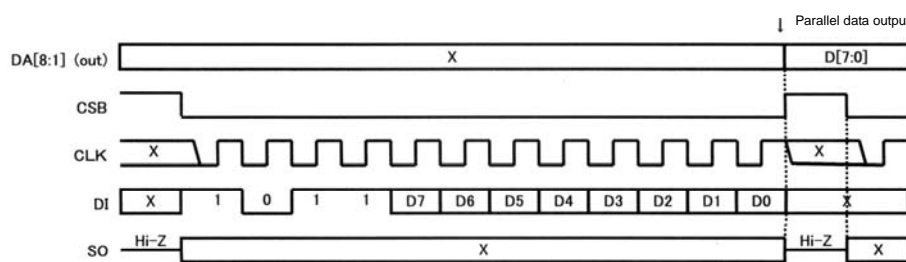


Fig.7

- D/A Converter Output Setting (Fig. 7)

DI serial data is taken in at the rising edge of the clock.

The D/A converter output is output from the DA[8:1] terminal just after the rising edge of the CSB.

During that time, the SO terminal output becomes undetermined (just previous address setting + data output).

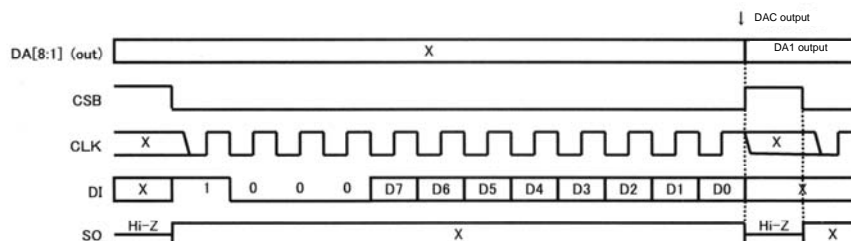


Fig.8

## ● Electrical Characteristics Curves

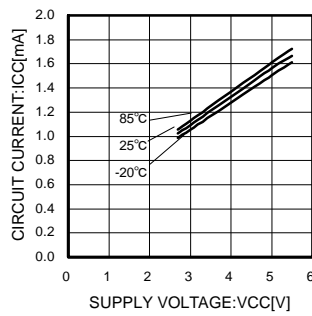


Fig.9 Action current consumption

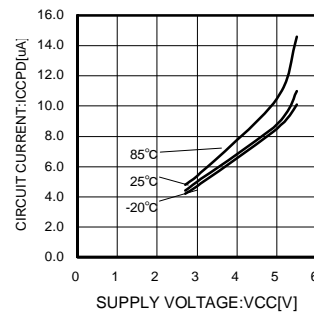


Fig.10 Consumption current at power down

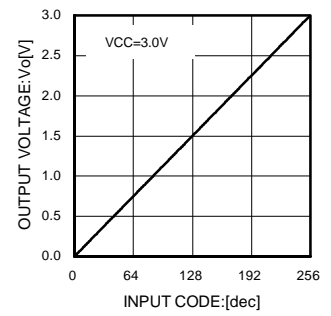


Fig.11 Output voltage characteristic

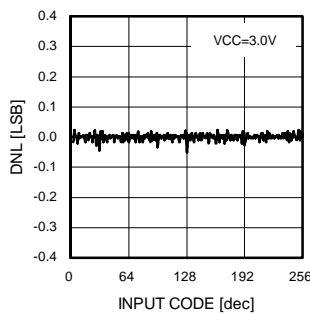


Fig.12 Differential non linearity error

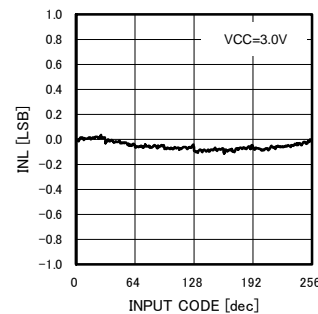


Fig.13 Integral non linearity error

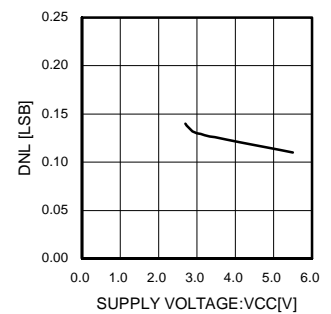


Fig.14 Power source voltage vs. differential non linearity error

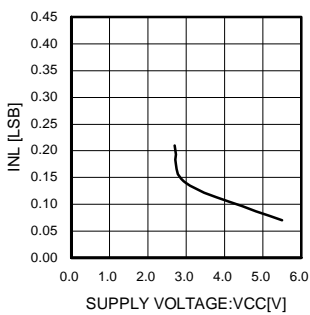


Fig.15 Power source voltage vs. integral non linearity error

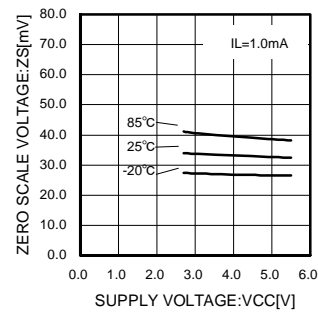


Fig.16 Output zero scale voltage

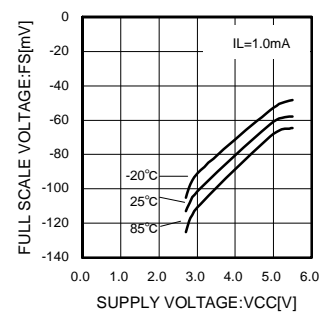


Fig.17 Output full scale voltage

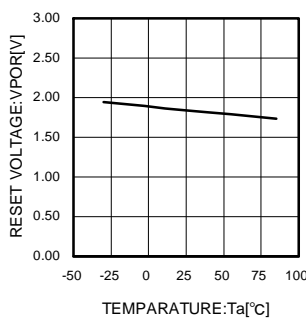


Fig.18 Reset release voltage

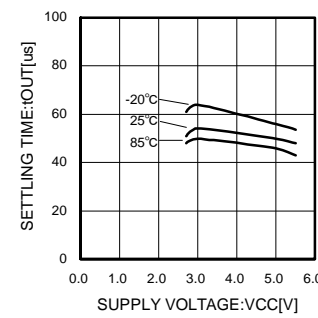


Fig.19 Settling time

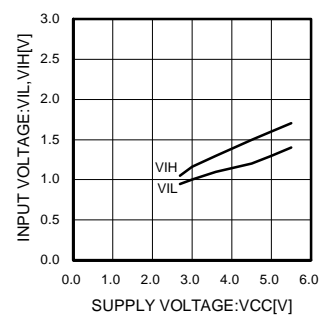


Fig.20 Input voltage

## ● Operation Notes

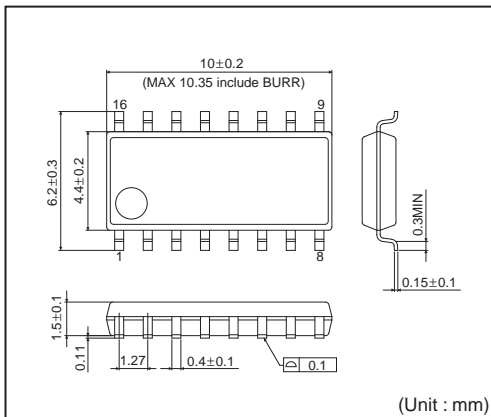
- (1) Numbers and data in entries are representative design values and are not guaranteed values of the items.
- (2) Although we are confident in recommending the sample application circuits, carefully check their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.
- (3) Absolute Maximum Ratings  
Operating or testing the device over the maximum specifications may damage the part itself as well as peripheral components. Therefore, please ensure that the specifications are not exceeded.
- (4) GND potential  
Ensure that the GND terminal is at the lowest potential under all operating conditions.
- (5) Thermal design  
Use a thermal design that allows for a sufficient margin regarding power dissipation (Pd) under actual operating conditions.
- (6) Terminal shorts and mis-mounting  
Incorrect orientation or misalignment of the IC when mounting to the PCB may damage part. Short-circuits caused by the introduction of foreign matter between the output terminals or across the output and power supply or GND may also result in destruction.
- (7) Operation in a strong magnetic field  
Operation in a strong electromagnetic field may cause malfunction.
- (8) Reset Function  
The power on reset circuit, which initializes internal settings, may malfunction during abrupt power ons. Therefore, set the time constant so as to satisfy the power source rise time.
- (9) After power on and after the external reset is in power down status, DA1 ~ DA8 will be in input mode (all terminals at High-Z).
- (10) In the case of condition changes in the DA1 ~ DA8 terminals (i.e. changes from D/A mode to serial-parallel mode, from serial-parallel mode to parallel-serial mode, excluding D/A data and I/O data updates), change both analog and digital settings of High-Z.
- (11) Connect the RESETB terminal to VCC and set it to High, making sure that it becomes Low only at reset.
- (12) Initialization of the serial interface shift register is carried out only by power on reset, or external reset, and is not reset by CSB = High. Therefore, when a specified clock number (12CLK) is not attained during command setting, interrupting processing, transfer regular data once again.
- (13) The power down function restricts the consumption current in the internal analog circuit. Set it by command. At power down, for channels set to D/A mode, "I/O D/A selection" is changed from "D/A mode" to "I/O mode". Therefore, when the "I/O status setting" of the channel is in input mode, the terminal is in High-Z status and the input becomes unstable and unnecessary current flows. Set the I/O status setting of channel to be in output mode, or set the terminal using resistance.
- (14) When shifting from PIO use status to D/A use status, a wait time in order to ensure D/A output stability is necessary. Therefore wait for a maximum of 1ms after the "I/O D/A select" command is input.  
If wait time is problematic, set the D/A setting code to 80hex and change it to the specified code setting.



### ● Ordering part number

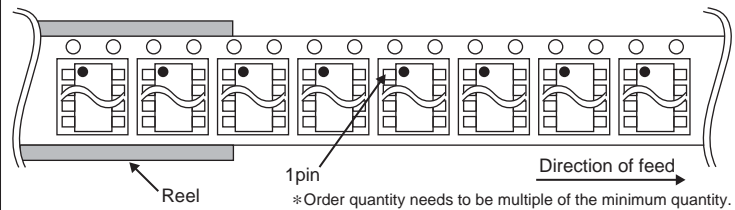
|          |          |                                     |   |
|----------|----------|-------------------------------------|---|
| B H      | 2 2 2 6  | F V                                 | - E 2   |
| Part No. | Part No. | Package<br>FV: SSOP-B16<br>F: SOP16 | Packaging and forming specification<br>E2: Embossed tape and reel<br>(SSOP-B16/SOP16) |

### SOP16

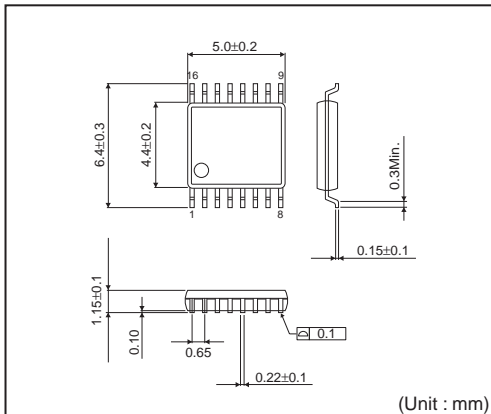


#### <Tape and Reel information>

|                   |   |
|-------------------|---|
| Tape              | Embossed carrier tape   |
| Quantity          | 2500pcs   |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |

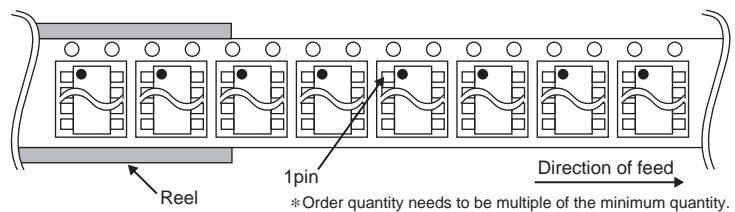


### SSOP-B16



#### <Tape and Reel information>

|                   |   |
|-------------------|---|
| Tape              | Embossed carrier tape   |
| Quantity          | 2500pcs   |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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