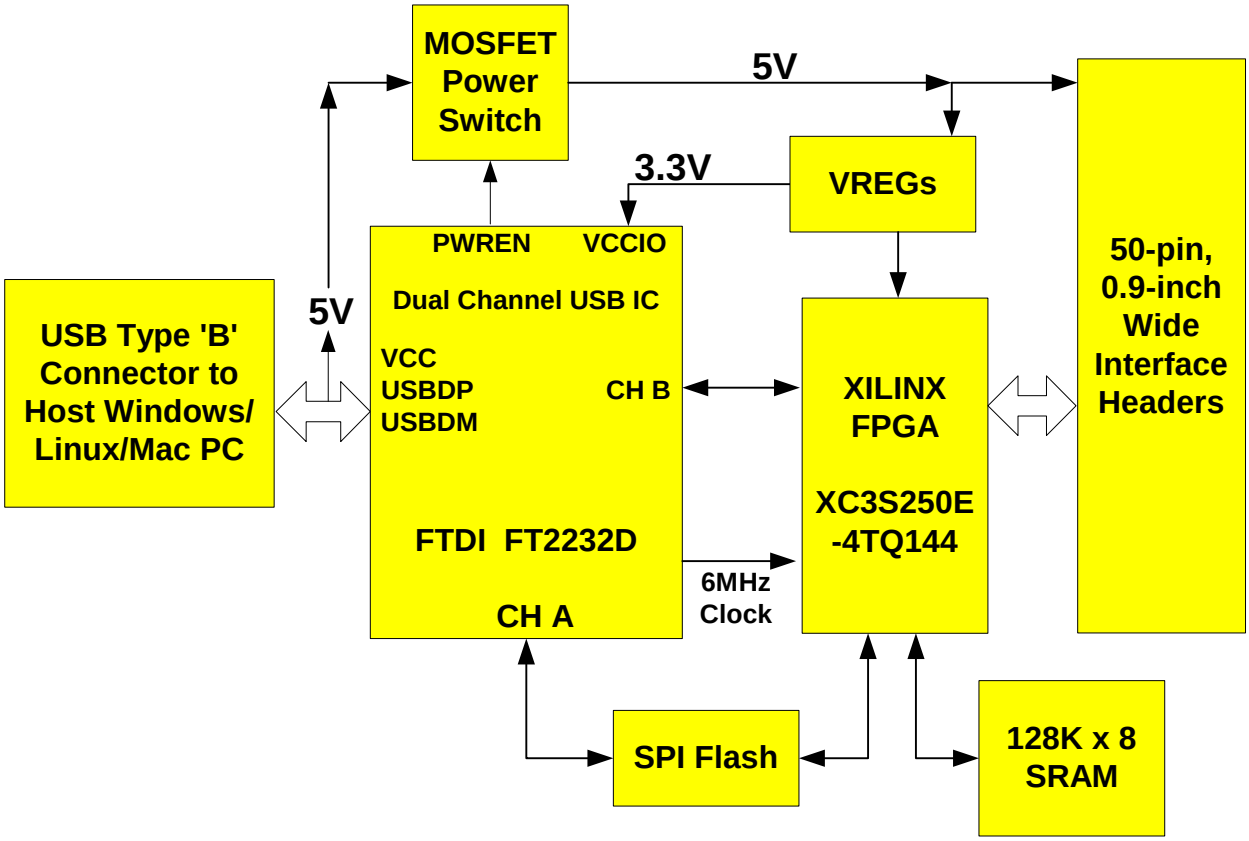
DLP-FPGA

LEAD-FREE

USB - FPGA MODULE



APPLICATIONS:

- Rapid Prototyping
- Educational Tool
- Industrial/Process Control

FEATURES:

- Training Manual/Tutorial Available
- Built-In Configuration Loader—Writes Bit File Directly to SPI Flash via Full-Speed USB Interface
- 40 I/O Channels: 27 Input/Output; 13 Input Only
- Xilinx XC3S250E-4TQ144 FPGA
- On-Board 128K x 8, 70nS SRAM
- USB Port Powered
- USB 1.1 and 2.0 Compatible Interface
- Small Footprint: 2.8 x 1.-Inch PCB
- Standard 50-Pin, 0.9-Inch DIP Interface

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1.0 INTRODUCTION

The DLP-FPGA Module is a low-cost, compact prototyping module that can be used for rapid proof of concept or for educational environments. The module is based on the Xilinx Spartan 3E and Future Technology Devices International's FT2232D Dual-Channel USB IC. Used by itself or with the optional 200-page training manual, the DLP-FPGA provides both the beginner as well as the experienced engineer with a rapid path to developing FPGA-based designs. When combined with the free WebPACK™ Tools from Xilinx, this module is more than sufficient for creating anything from basic logical functions to a highly complex system controller.

As a bonus feature, one channel of the dual-channel USB interface is used to load user bit files directly to the SPI Flash—no external programmer is required. This represents a savings of as much as $200 in that no additional programming cable is required for configuring the FPGA. All that is needed to load bit files to the DLP-FPGA is a Windows software utility (free with purchase), a Windows PC and a USB cable. The module can also be programmed from within the Xilinx ISE tool environment using a Xilinx programming cable (purchased separately).

The DLP-FPGA is fully compatible with the free ISE™ WebPACK™ tools from Xilinx. ISE WebPACK offers the ideal development environment for FPGA designs with HDL synthesis and simulation, implementation, device fitting and JTAG programming.

The DLP-FPGA has on-board voltage regulators that generate all required power supply voltages from a single 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply.

Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025 square inch post DIP header. Other on-board features include a 128K x 8 static RAM IC for user projects, and both JTAG and SPI Flash interface ports for connection to Xilinx programming tools.

2.0 TRAINING MANUAL

A 200+ page training manual for the DLP-FPGA is also available. While this manual is designed to provide entry-level instruction for those new to designing with FPGAs, it is recommended for developers who have some experience with FPGA products and associated development tools. An ISE™ WebPACK™ Software installation DVD is included with the manual.

The manual is comprised of 5 Chapters and 4 Labs as outlined below:

Chapter 1: Installing the Xilinx ISE WebPACK tools and Understanding the Design Flow

Chapter 2: Lab 1: Implementing a Simple AND Gate: Create a New Project, Implement the Design, View the Synthesized Design, View the Placed and Routed Design

Chapter 3: Lab 2: Heartbeat: Understanding the Digital Clock Manager (DCM), Methods of Starting ISE Project Navigator, VHDL Module Structure, Utilizing Hierarchy, Adding the DCM Component, Adding the Heartbeat Component, Connecting the Components, Synthesizing the Design Using XST, Simulating the Design Using the ISE Simulator, Adding the User Constraint File, Implementing the Design, Download the Design to the FPGA

Chapter 4: Lab 3: Memory Test: Block Diagram, DCM Design, SRAM State Machine, Bi-Directional Buffers, Test Failed Indicator, User Constraint File, Synthesize the Memory Test Design, Simulate the Memory Test Design, Implementing the Design, Download the Design to the FPGA

Chapter 5: Lab 4: USB Loopback: Initial Design, USB State Machine Module, Language Template, Bi-Directional Buffers, Synthesize, Simulate, Pin Constraints, Implement, Download the Design to the FPGA

(The completed design files for each lab are available for download from the DLP Design website upon purchase of the DLP-FPGA and Lab Manual.)

3.0 FPGA SPECIFICATIONS

The FPGA device used on the DLP-FPGA is the Xilinx Spartan 3E: XC3S250E-4TQ144.

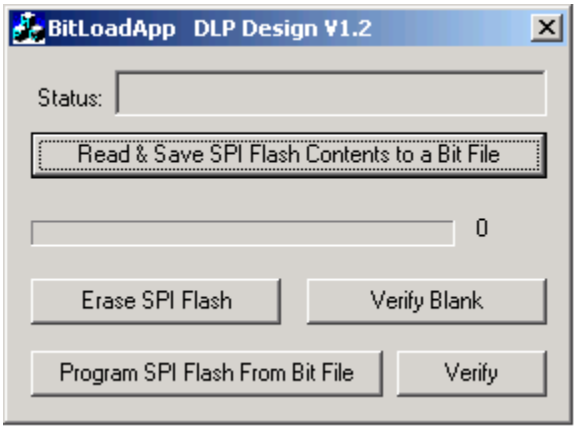
- Part Number: XC3S250E
- System Gates: 250K
- Equivalent Logic Cells: 5,508

- CLB Array
    - Rows: 34
    - Columns: 26
    - Total CLB's: 612
    - Total Slices: 2,448

- Distributed RAM Bits: 38K
- Block RAM Bits: 216K
- Dedicated Multipliers: 12
- DCM's: 4

4.0 BITLOADAPP SOFTWARE

Windows software is provided for use with the DLP-FPGA that will load an FPGA configuration (.bit) file directly to the SPI Flash device via the USB interface. This app (shown below) will allow the user to erase the flash, verify the erasure and then program and verify the flash:



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5.0 JTAG INTERFACE

The easiest way to load an FPGA configuration (bit file) to the FPGA is to run the BitLoadApp software, then select and program a file from the local hard drive directly to the SPI flash. Once written to the SPI flash, the configuration will load to the FPGA and execute. Alternatively, a traditional JTAG header location is provided on the DLP-FPGA giving the user access to the pins on the FPGA required by the development tools. (Refer to the schematic at the end of this datasheet for details.)

6.0 EEPROM SETUP / MPROG

The DLP-FPGA has a dual-channel USB interface to the host PC. Channel A is used exclusively to load an FPGA configuration (bit file) to the SPI flash. This configuration data is automatically transferred to the FPGA when power is applied to the module. Channel B is used for communication between the FPGA and host PC at run time. A 93C56B EEPROM connected to the USB interface IC is used to store the setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), Serial Number, Description String, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

As mentioned above, Channel A is used exclusively for loading the FPGA's configuration to the SPI flash, and Channel B is used for communication between the host PC and the DLP-FPGA. As such, the D2XX drivers and FIFO mode must be selected in the EEPROM for Channel A. Channel B must use the FIFO mode, but can use either the VCP or D2XX drivers. The VCP drivers make the DLP-FPGA appear as an RS232 port to the host app. The D2XX drivers provide faster throughput, but require working with a .lib or .dll library in the host app.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at **www.dlpdesign.com**.

7.0 TEST BIT FILE

A test file is provided as a download from the DLP Design website that provides rudimentary access to the I/O features of the DLP-FPGA.

The following features are provided:

- Ping
- Read the High/Low State of the Input-Only Pins
- Drive I/O Pins High/Low or Read their High/Low State
- Simple Loopback on Channel B
- Simple Read/Write of Each Address in the SRAM

This bit file is available from the DLP-FPGA's download page.

8.0 USB DRIVERS

USB drivers for the following operating systems are available for download from the DLP Design website at **http://www.dlpdesign.com**:

Windows XP x64	**Mac OSX**
Windows Server 2003	**Mac OS9**
Windows 2000	**Mac OS8**
Windows 98, ME	**Linux**

Notes:

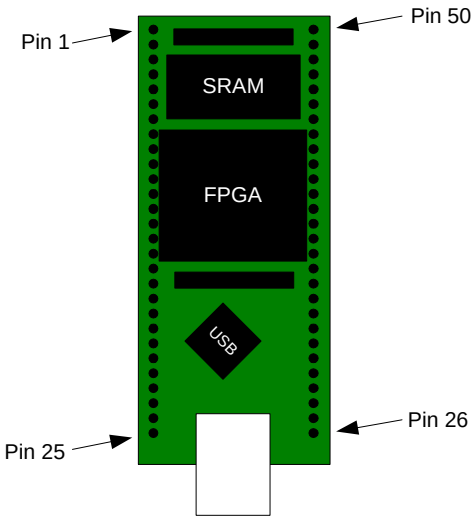
1. The bit file load utility only runs on the Windows platforms.

2. The bit file load utility requires the use of USB channel A, and channel A is dedicated to this function.

3. If you are using the dual-mode drivers from FTDI (CDM2.02.04) and wish to use the Virtual COM Port (VCP) drivers for Channel B communications, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the Channel B entry under USB Controllers that appears when the DLP-FPGA is connected, select Properties, select the Advanced tab, check the option for "Load VCP" and click OK. Once you unplug and then replug the DLP-FPGA, a COM port should appear in Device Manager under Ports (COM & LPT).

9.0 USING THE DLP-FPGA

Select a power source via Header Pins 23 and 24, and connect the DLP-FPGA to the PC to initiate the loading of USB drivers. The easiest way to do this is to connect Pins 23 and 24 to each other. This will result in operational power being taken from the host PC. Once the drivers are loaded, the DLP-FPGA is ready for use.



Top View (Interface Headers on bottom of PCB)

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TABLE 1

NN (dec)*	NN (hex)*	Name	FPGA Pin	JP2 Pin
0	0	user_io(0)	U5 Pin 58	JP2 Pin 2
1	1	user_io(1)	U5 Pin 59	JP2 Pin 4
2	2	user_io(2)	U5 Pin 93	JP2 Pin 5
3	3	user_io(3)	U5 Pin 94	JP2 Pin 6
4	4	user_io(4)	U5 Pin 96	JP2 Pin 7
5	5	user_io(5)	U5 Pin 97	JP2 Pin 8
6	6	user_io(6)	U5 Pin 103	JP2 Pin 9
7	7	user_io(7)	U5 Pin 104	JP2 Pin 10
8	8	user_io(8)	U5 Pin 105	JP2 Pin 12
9	9	user_io(9)	U5 Pin 106	JP2 Pin 13
10	A	user_io(10)	U5 Pin 112	JP2 Pin 14
11	B	user_io(11)	U5 Pin 113	JP2 Pin 15
12	C	user_io(12)	U5 Pin 116	JP2 Pin 16
13	D	user_io(13)	U5 Pin 117	JP2 Pin 17
14	E	user_in(14) [INPUT ONLY!]	U5 Pin 119	JP2 Pin 18
15	F	user_in(15) [INPUT ONLY!]	U5 Pin 120	JP2 Pin 19
16	10	user_io(16)	U5 Pin 122	JP2 Pin 20
17	11	user_io(17)	U5 Pin 123	JP2 Pin 21
18	12	user_io(18)	U5 Pin 124	JP2 Pin 22
19	13	user_io(19)	U5 Pin 125	JP2 Pin 27
20	14	user_io(20)	U5 Pin 126	JP2 Pin 29
21	15	user_io(21)	U5 Pin 130	JP2 Pin 30
22	16	user_io(22)	U5 Pin 131	JP2 Pin 31
23	17	user_io(23)	U5 Pin 132	JP2 Pin 32
24	18	user_io(24)	U5 Pin 134	JP2 Pin 33
25	19	user_io(25)	U5 Pin 135	JP2 Pin 34
26	1A	user_io(26)	U5 Pin 139	JP2 Pin 35
27	1B	user_io(27)	U5 Pin 140	JP2 Pin 36
28	1C	user_io(28)	U5 Pin 142	JP2 Pin 37
30	1E	user_in(0)	U5 Pin 10	JP2 Pin 49
31	1F	user_in(1)	U5 Pin 12	JP2 Pin 48
32	20	user_in(2)	U5 Pin 29	JP2 Pin 47
33	21	user_in(3)	U5 Pin 31	JP2 Pin 46
34	22	user_in(4)	U5 Pin 36	JP2 Pin 45
35	23	user_in(5)	U5 Pin 38	JP2 Pin 44
36	24	user_in(6)	U5 Pin 41	JP2 Pin 43
37	25	user_in(7)	U5 Pin 47	JP2 Pin 42
38	26	user_in(8)	U5 Pin 48	JP2 Pin 41
39	27	user_in(9)	U5 Pin 66	JP2 Pin 39
40	28	user_in(10)	U5 Pin 69	JP2 Pin 38
Read: 29, >40	Read:1D, >29	Returns Read Pin Error E4	n/a	n/a
Write: 14, 15, >30	Write: E, F, >1E	Returns Write Pin Error E2 for Pin Clear (low), or E3 for Pin Set (high)	n/a	n/a
		Ground		1,11,25,26,40,50
		FPGA_RESET	128	3
		5VIN – Module power source		23
		PORTVCC – Power from Host PC		24
		VCCSW – 5V power after host enumerates the USB port		28

*Note: This is the I/O number for use with the Test Bit File described in Section 7.

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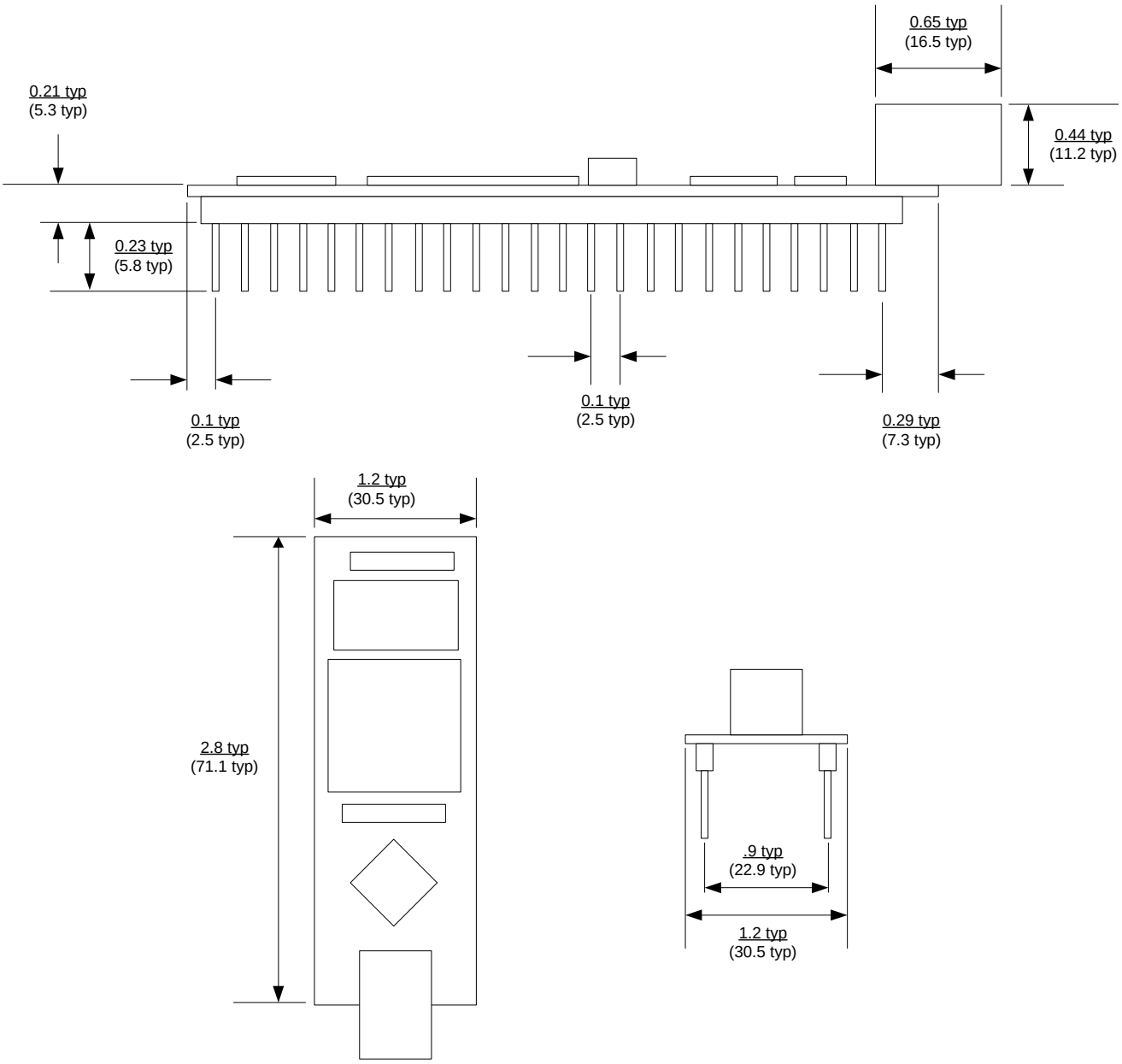
10.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



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12.0 CONTACT INFORMATION

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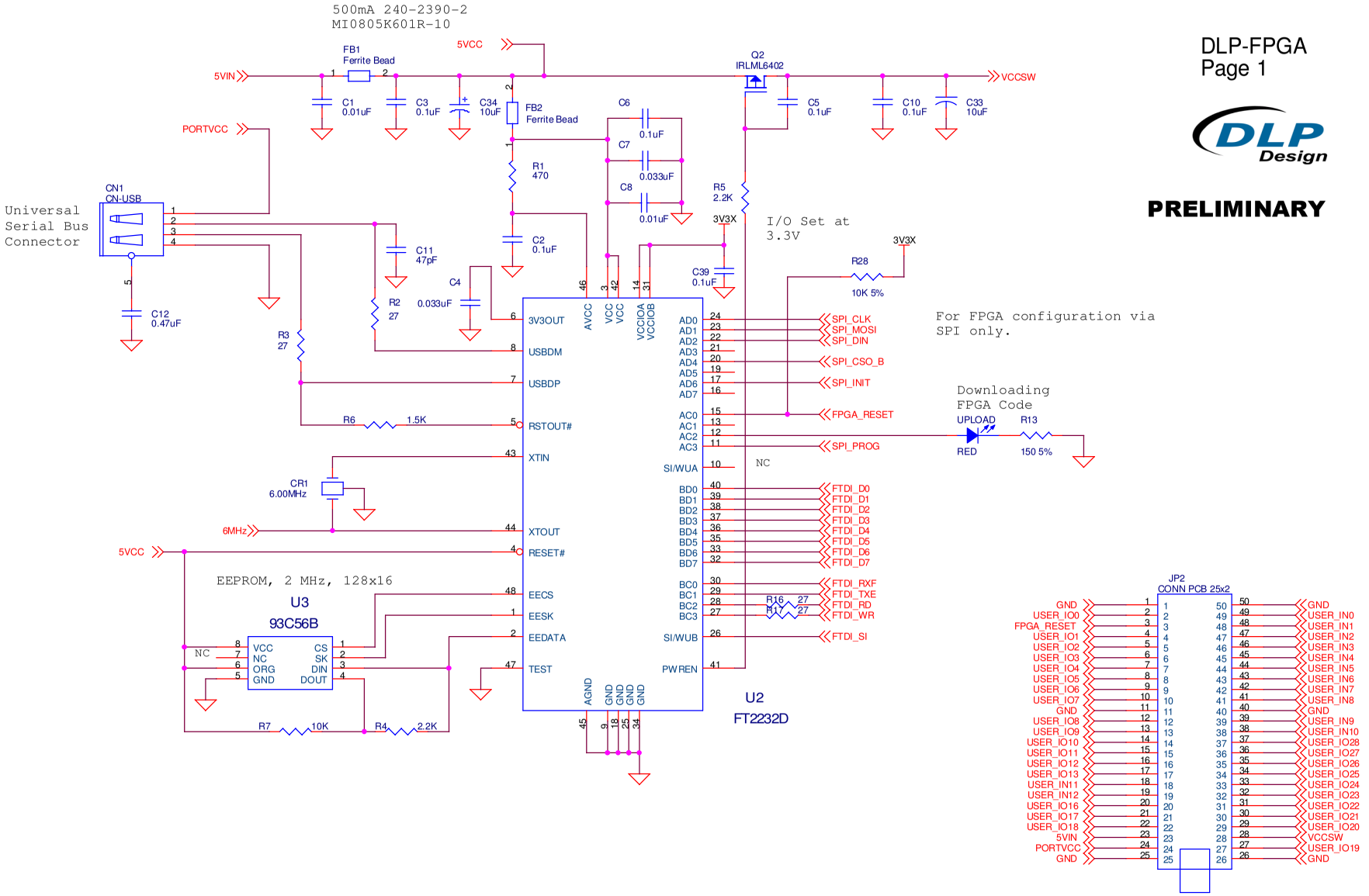
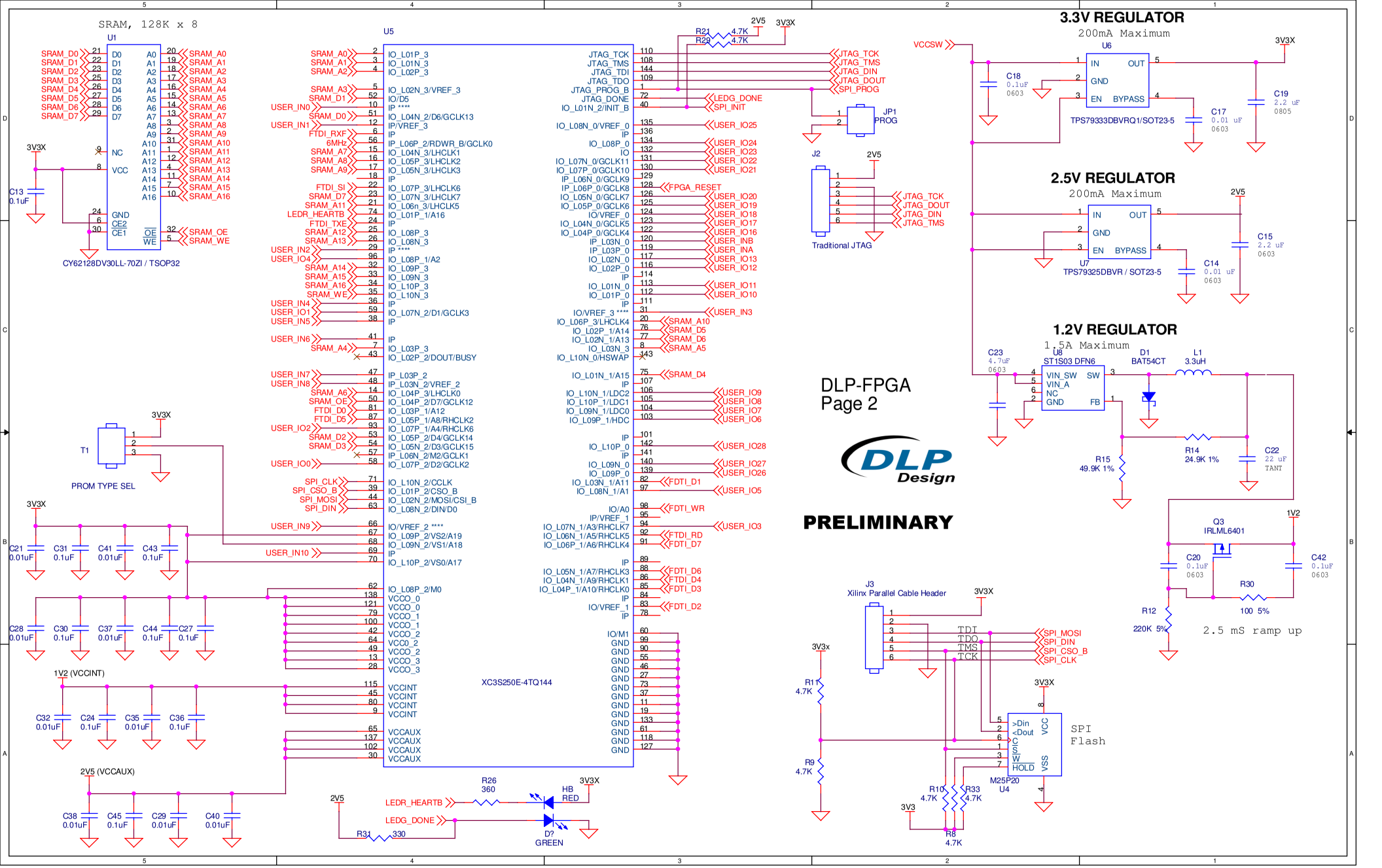

500mA 240-2390-2
MI0805K601R-10
DLP-FPGA
Page 1
DLP Design
PRELIMINARY
5VIN
5VCC
VCCSW
PORTVCC
FB1
Ferrite Bead
FB2
Ferrite Bead
Q2
IRLML6402
C1 0.01uF
C3 0.1uF
C34 10uF
C5 0.1uF
C10 0.1uF
C33 10uF
C6 0.1uF
C7 0.033uF
C8 0.01uF
R1 470
R5 2.2K
3V3X
I/O Set at 3.3V
CN1
CN-USB
Universal Serial Bus Connector
C11 47pF
C12 0.47uF
C2 0.1uF
C4 0.033uF
C39 0.1uF
R28 10K 5%
R2 27
R3 27
R6 1.5K
CR1 6.00MHz
6MHz
For FPGA configuration via SPI only.
Downloading FPGA Code
UPLOAD
R13 150 5%
RED
NC
3V3OUT
USBDM
USBDP
RSTOUT#
XTIN
XTOUT
RESET#
EECS
EESK
EEDATA
TEST
AVCC
VCC
VCCIOA
VCCIOB
AGND
GND
SI/WUA
SI/WUB
PWREN
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AC0
AC1
AC2
AC3
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BC0
BC1
BC2
BC3
SPI_CLK
SPI_MOSI
SPI_DIN
SPI_CSO_B
SPI_INIT
FPGA_RESET
SPI_PROG
FTDI_D0
FTDI_D1
FTDI_D2
FTDI_D3
FTDI_D4
FTDI_D5
FTDI_D6
FTDI_D7
FTDI_RXF
FTDI_TXE
FTDI_RD
FTDI_WR
FTDI_SI
R16 27
R17 27
U2
FT2232D
EEPROM, 2 MHz, 128x16
U3
93C56B
VCC
NC
ORG
GND
CS
SK
DIN
DOUT
R7 10K
R4 2.2K
JP2
CONN PCB 25x2
GND
USER_IO0
FPGA_RESET
USER_IO1
USER_IO2
USER_IO3
USER_IO4
USER_IO5
USER_IO6
USER_IO7
GND
USER_IO8
USER_IO9
USER_IO10
USER_IO11
USER_IO12
USER_IO13
USER_IN11
USER_IN12
USER_IO16
USER_IO17
USER_IO18
5VIN
PORTVCC
GND
GND
USER_IN0
USER_IN1
USER_IN2
USER_IN3
USER_IN4
USER_IN5
USER_IN6
USER_IN7
USER_IN8
GND
USER_IN9
USER_IN10
USER_IO28
USER_IO27
USER_IO26
USER_IO25
USER_IO24
USER_IO23
USER_IO22
USER_IO21
USER_IO20
VCCSW
USER_IO19
GND


SRAM, 128K x 8
U1
CY62128DV30LL-70ZI / TSOP32
U5
XC3S250E-4TQ144
3.3V REGULATOR
200mA Maximum
U6
TPS79333DBVRQ1/SOT23-5
2.5V REGULATOR
200mA Maximum
U7
TPS79325DBVR / SOT23-5
1.2V REGULATOR
1.5A Maximum
U8
ST1S03 DFN6
DLP-FPGA
Page 2
PRELIMINARY
DLP Design
Traditional JTAG
PROM TYPE SEL
J3
Xilinx Parallel Cable Header
SPI Flash
M25P20
U4
2.5 mS ramp up

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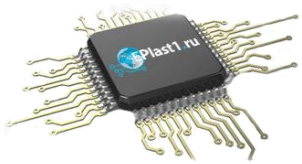

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