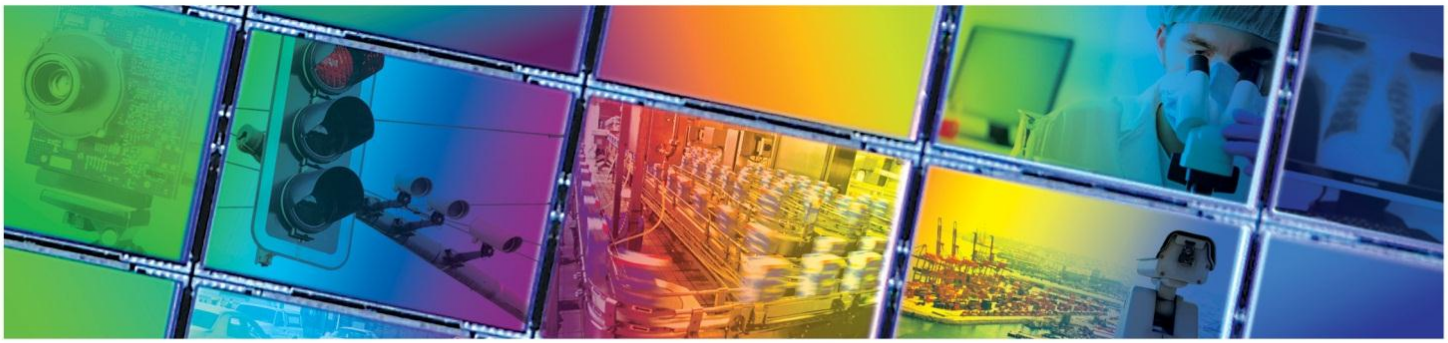
ON Semiconductor®

KAI-04050 IMAGE SENSOR

2336 (H) X 1752 (V) INTERLINE CCD IMAGE SENSOR



JULY 21, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 5.0 PS-0009

TABLE OF CONTENTS

Summary Specification **5**
Description 5
Features 5
Applications 5
Ordering Information **6**
Standard Devices 6
Not Recommended for New Designs 7
Device Description **8**
Architecture 8
Dark Reference Pixels 9
Dummy Pixels 9
Active Buffer Pixels 9
Image Acquisition 9
ESD Protection 9
Bayer Color Filter Pattern 10
TRUESENSE Sparse Color Filter Pattern 10
Physical Description 11
Pin Description and Device Orientation 11
Imaging Performance **13**
Typical Operation Conditions 13
Specifications 13
All Configurations 13
KAI-04050-ABA, KAI-04050-QBA, and KAI-04050-PBA[7] Configurations 14
KAI-04050-FBA and KAI-04050-QBA Gen2 Color Configurations with MAR Glass 14
KAI-04050-FBA Gen2 Color Configuration with Clear Glass 14
KAI-04050-CBA and KAI-04050-PBA Gen1 Color Configurations with MAR Glass 14
KAI-04050-CBA Gen1 Color Configuration with Clear Glass 14
Typical Performance Curves **16**
Quantum Efficiency 16
Monochrome, all configurations 16
Color (Bayer RGB) with Microlens and MAR Cover Glass (Gen2 and Gen1 CFA) 17
Color (Bayer RGB) with Microlens and Clear Cover Glass (Gen2 and Gen1 CFA) 17
Color (TRUESENSE Sparse CFA) with Microlens (Gen2 and Gen1 CFA) 18
Angular Quantum Efficiency 19
Monochrome with Microlens 19
Dark Current versus Temperature 19
Power – Estimated 20
Frame Rates 20
Defect Definitions **21**
Operation Conditions for Defect Testing at 40 °C 21
Defect Definitions for Testing at 40 °C 21
Operation Conditions for Defect Testing at 27 °C 22
Defect Definitions for Testing at 27 °C 22
Defect Map 22
Test Definitions **23**
Test Regions of Interest 23
Overclocking 23
Tests 24

Dark Field Global Non-Uniformity ... 24
Global Non-Uniformity ... 24
Global Peak to Peak Non-Uniformity ... 24
Center Non-Uniformity ... 25
Dark Field Defect Test ... 25
Bright Field Defect Test ... 25
Test Sub Regions of Interest ... 26
Operation ... 27
Absolute Maximum Ratings ... 27
Absolute Maximum Voltage Ratings Between Pins and Ground ... 27
Power-Up and Power-Down Sequence ... 28
DC Bias Operating Conditions ... 29
AC Operating Conditions ... 30
Clock Levels ... 30
Device Identification ... 31
Recommended Circuit ... 31
Timing ... 32
Requirements and Characteristics ... 32
Timing Diagrams ... 33
Photodiode Transfer Timing ... 34
Line and Pixel Timing ... 34
Pixel Timing Detail ... 35
Frame/Electronic Shutter Timing ... 35
VCCD Clock Edge Alignment ... 35
Line and Pixel Timing – Vertical Binning by 2 ... 36
Storage and Handling ... 37
Storage Conditions ... 37
ESD ... 37
Cover Glass Care and Cleanliness ... 37
Environmental Exposure ... 37
Soldering Recommendations ... 37
Mechanical Information ... 38
Completed Assembly ... 38
MAR Cover Glass ... 39
Clear Cover Glass ... 40
Cover Glass Transmission ... 41
Shipping Configuration ... 42
Cover Glass Protective Tape ... 42
Tray Packing ... 43
Tray Configuration ... 43
Brick Configuration ... 44
Brick in Vacuum Sealed Bag ... 44
Shipping Container ... 45
Parts List ... 46
Quality Assurance and Reliability ... 47
Quality and Reliability ... 47
Replacement ... 47
Liability of the Supplier ... 47
Liability of the Customer ... 47
Test Data Retention ... 47

Mechanical 47
Life Support Applications Policy 47
Revision Changes 48
MTD/PS-1172 48
PS-0009 48

TABLE OF FIGURES

Figure 1: Block Diagram 8
Figure 2: Bayer Color Filter Pattern 10
Figure 3: TRUESENSE Sparse Color Filter Pattern 10
Figure 4: Package Pin Designations - Top View 11
Figure 5: Monochrome Configurations - Quantum Efficiency 16
Figure 6: MAR Glass Color (Bayer) with Microlens Quantum Efficiency 17
Figure 7: Clear Glass Color (Bayer) with Microlens Quantum Efficiency 17
Figure 8: Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency 18
Figure 9: Monochrome with Microlens Angular Quantum Efficiency 19
Figure 10: Dark Current versus Temperature 19
Figure 11: Power 20
Figure 12: Frame Rates 20
Figure 13: Regions of Interest 23
Figure 14: Test Sub Regions of Interest 26
Figure 15: Power-Up and Power-Down Sequence 28
Figure 16: Output Amplifier 29
Figure 17: Device Identification Recommended Circuit 31
Figure 18: Photodiode Transfer Timing 34
Figure 19: Line and Pixel Timing 34
Figure 20: Pixel Timing Detail 35
Figure 21: Frame/Electronic Shutter Timing 35
Figure 22: VCCD Clock Edge Alignment 35
Figure 23: Line and Pixel Timing - Vertical Binning by 2 36
Figure 24: Completed Assembly 38
Figure 25: MAR Cover Glass 39
Figure 26: Clear Cover Glass 40
Figure 27: Cover Glass Transmission 41
Figure 28: Cover Glass Protective Tape 42
Figure 29: Tray Pin-Up View 43
Figure 30: Tray Pin-Down View 43
Figure 31: Brick 44
Figure 32: Brick ID Label 44
Figure 33: Sealed Brick 44
Figure 34: Bick Loaded in Shipping Container 45
Figure 35: Open Shipping Container with Part List 45
Figure 36: Sealed Shipping Container 45
Figure 37: Brick Label 45
Figure 38: Parts List 46

Summary Specification

KAI-04050 Image Sensor

DESCRIPTION

The KAI-04050 Image Sensor is a 4-megapixel CCD in a 1" optical format. Based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, the sensor features broad dynamic range, excellent imaging performance, and a flexible readout architecture that enables use of 1, 2, or 4 outputs. The sensor supports full resolution readout up to 32 frames per second, while a Region of Interest (ROI) mode enables partial readout of the sensor at even higher frame rates. A vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

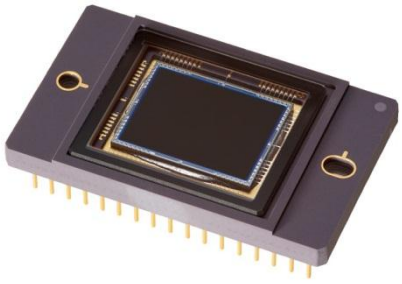
The sensor shares common pin-out and electrical configurations with other devices based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, allowing a single camera design to support multiple members of this sensor family.

FEATURES

- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome configurations
- Progressive scan readout
- Flexible readout architecture
- High frame rate
- High sensitivity
- Low noise architecture
- Excellent smear performance
- Package pin reserved for device identification

APPLICATIONS

- Industrial Imaging
- Medical Imaging
- Security



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	2404 (H) x 1800 (V)
Number of Effective Pixels	2360 (H) x 1776 (V)
Number of Active Pixels	2336 (H) x 1752 (V)
Pixel Size	5.5 µm (H) x 5.5 µm (V)
Active Image Size	12.85 mm (H) x 9.64 mm (V) 16.06 mm (diag) 1" optical format
Aspect Ratio	4:3
Number of Outputs	1, 2, or 4
Charge Capacity	20,000 electrons
Output Sensitivity	34 µV/e^-
Quantum Efficiency Pan (-ABA, -QBA, -PBA) R, G, B (-FBA, -QBA) R, G, B (-CBA, -PBA)	 44% 31%, 37%, 38% 29%, 37%, 39%
Read Noise (f= 40MHz)	12 electrons rms
Dark Current Photodiode VCCD	 7 electrons/s 100 electrons/s
Dark Current Doubling Temp Photodiode VCCD	 7 °C 9 °C
Dynamic Range	64 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 300 X
Smear	-100 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rates Quad Output Dual Output Single Output	 32 fps 16 fps 8 fps
Package	68 pin PGA
Cover Glass	AR Coated, 2 Sides or Clear Glass

All parameters are specified at T = 40 ° C unless otherwise noted

Ordering Information

STANDARD DEVICES

See full datasheet for ordering information associated with devices no longer recommended for new designs.

Catalog Number	Product Name	Description	Marking Code
4H2085	KAI-04050-AAA-JP-BA	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade	KAI-04050-AAA Serial Number
4H2086	KAI-04050-AAA-JP-AE	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Grade	
4H2087	KAI-04050-ABA-JD-BA	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04050-ABA Serial Number
4H2088	KAI-04050-ABA-JD-AE	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2089	KAI-04050-ABA-JP-BA	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade	
4H2090	KAI-04050-ABA-JP-AE	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Grade	
4H2345	KAI-04050-FBA-JD-BA	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04050-FBA Serial Number
4H2346	KAI-04050-FBA-JD-AE	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2349	KAI-04050-FBA-JB-B2	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2	KAI-04050-FBA Serial Number Vab=xx.x
4H2350	KAI-04050-FBA-JB-AE	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Engineering Grade	
4H2351	KAI-04050-FBA-JB-B2-T	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2, Packed in Trays	
4H2347	KAI-04050-QBA-JD-BA	Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04050-QBA Serial Number
4H2348	KAI-04050-QBA-JD-AE	Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

NOT RECOMMENDED FOR NEW DESIGNS

Catalog Number	Product Name	Description	Marking Code
4H2091 (1)	KAI-04050-CBA-JD-BA	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04050-CBA Serial Number
4H2092 (1)	KAI-04050-CBA-JD-AE	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2244 (1)	KAI-04050-CBA-JB-B2	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2	KAI-04050-CBA Serial Number Vab=xx.x
4H2245 (1)	KAI-04050-CBA-JB-AE	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Engineering Grade	
4H2293 (1)	KAI-04050-CBA-JB-B2-T	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2, Packed in Trays	
4H2182 (1)	KAI-04050-PBA-JD-BA	Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04050-PBA Serial Number
4H2183 (1)	KAI-04050-PBA-JD-AE	Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	

Notes:
1. Not recommended for new designs.

Device Description

ARCHITECTURE

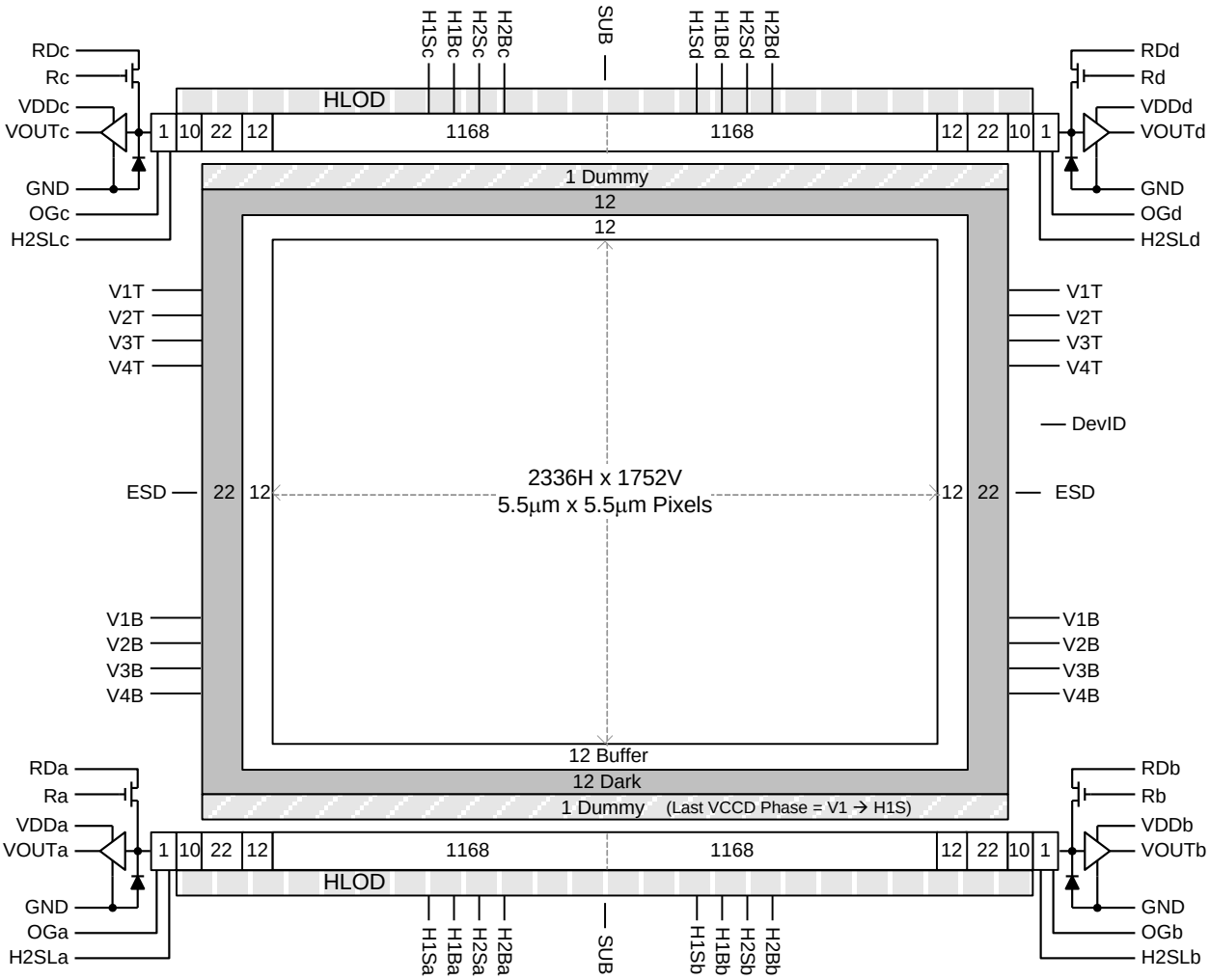


Figure 1: Block Diagram

Dark Reference Pixels

There are 12 dark reference rows at the top and 12 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level. Use the 22 dark columns on the left or right side of the image sensor as a dark reference.

Under normal circumstances use only the center 20 columns of the 22 column dark reference due to potential light leakage.

Dummy Pixels

Within each horizontal shift register there are 11 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.

Active Buffer Pixels

12 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

BAYER COLOR FILTER PATTERN

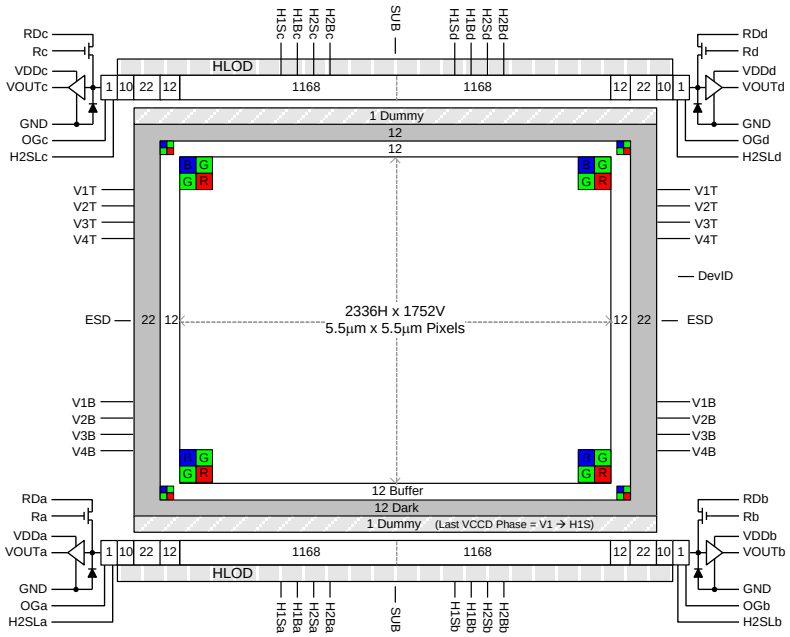


Figure 2: Bayer Color Filter Pattern

TRUESENSE SPARSE COLOR FILTER PATTERN

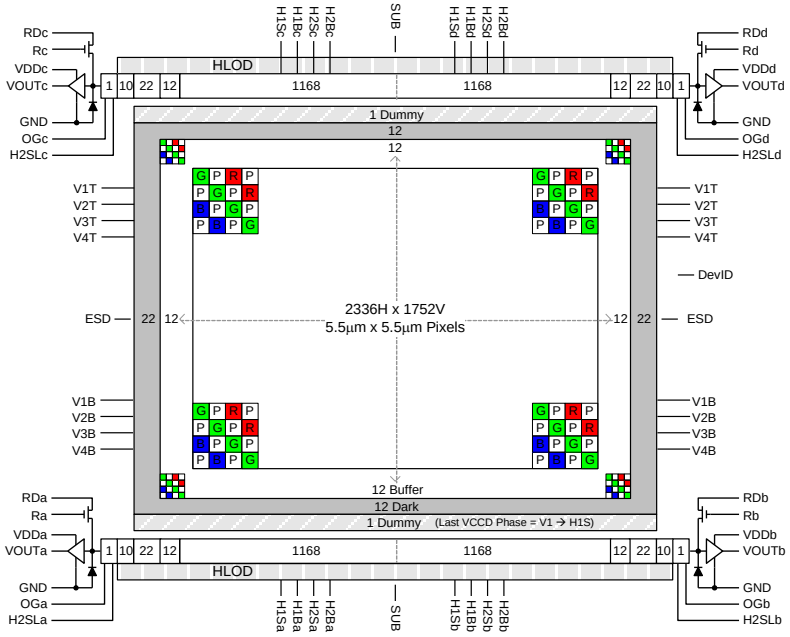


Figure 3: TRUESENSE Sparse Color Filter Pattern

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

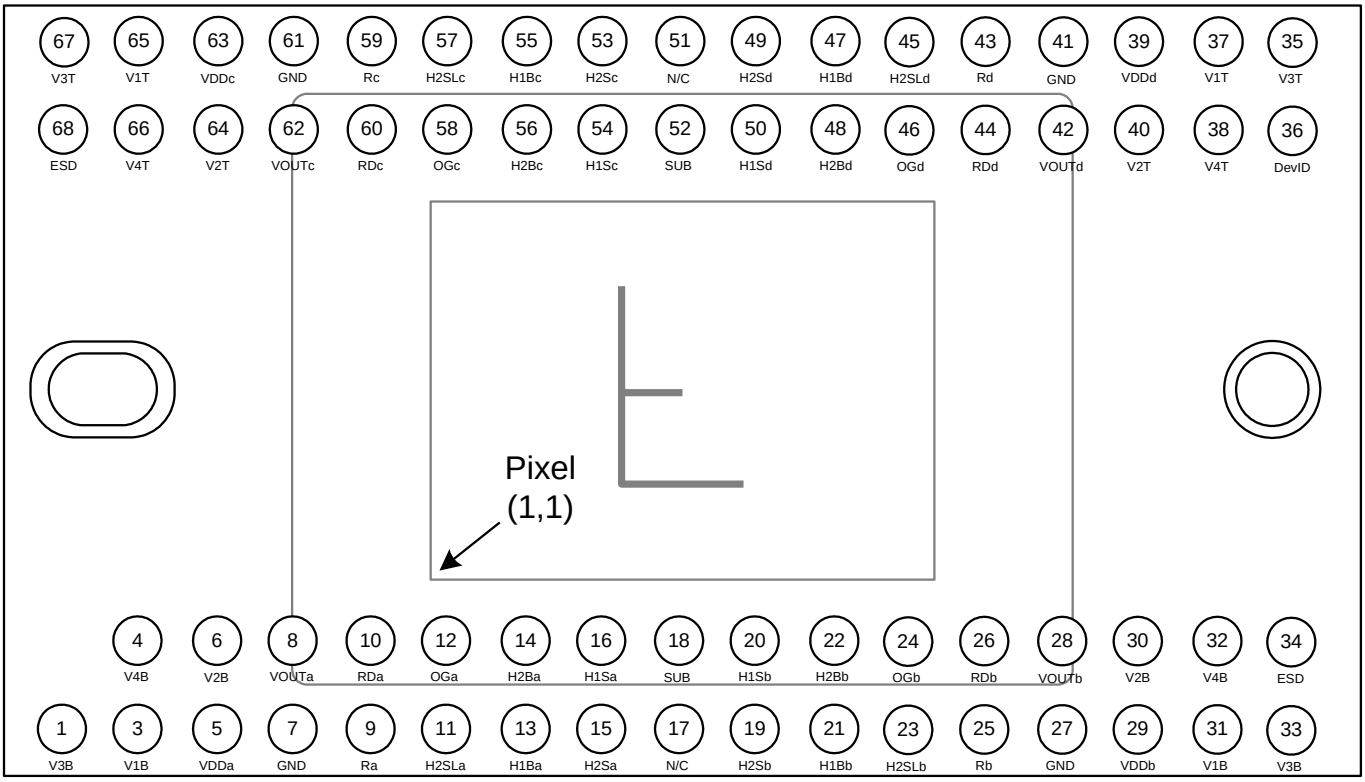


Figure 4: Package Pin Designations - Top View

Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Quadrant a
10	RDa	Reset Drain, Quadrant a
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	N/C	No Connect
18	SUB	Substrate
19	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
20	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
21	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
22	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b
23	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b
24	OGb	Output Gate, Quadrant b
25	Rb	Reset Gate, Quadrant b
26	RDb	Reset Drain, Quadrant b
27	GND	Ground
28	VOUTb	Video Output, Quadrant b
29	VDDb	Output Amplifier Supply, Quadrant b
30	V2B	Vertical CCD Clock, Phase 2, Bottom
31	V1B	Vertical CCD Clock, Phase 1, Bottom
32	V4B	Vertical CCD Clock, Phase 4, Bottom
33	V3B	Vertical CCD Clock, Phase 3, Bottom
34	ESD	ESD Protection Disable

Pin	Name	Description
68	ESD	ESD Protection Disable
67	V3T	Vertical CCD Clock, Phase 3, Top
66	V4T	Vertical CCD Clock, Phase 4, Top
65	V1T	Vertical CCD Clock, Phase 1, Top
64	V2T	Vertical CCD Clock, Phase 2, Top
63	VDDc	Output Amplifier Supply, Quadrant c
62	VOUTc	Video Output, Quadrant c
61	GND	Ground
60	RDc	Reset Drain, Quadrant c
59	Rc	Reset Gate, Quadrant c
58	OGc	Output Gate, Quadrant c
57	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
56	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
55	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
54	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
53	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
52	SUB	Substrate
51	N/C	No Connect
50	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
49	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
48	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
47	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
46	OGd	Output Gate, Quadrant b
45	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
44	RDd	Reset Drain, Quadrant d
43	Rd	Reset Gate, Quadrant d
42	VOUTd	Video Output, Quadrant d
41	GND	Ground
40	V2T	Vertical CCD Clock, Phase 2, Top
39	VDDd	Output Amplifier Supply, Quadrant d
38	V4T	Vertical CCD Clock, Phase 4, Top
37	V1T	Vertical CCD Clock, Phase 1, Top
36	DevID	Device Identification
35	V3T	Vertical CCD Clock, Phase 3, Top

Notes:

1. Liked named pins are internally connected and should have a common drive signal.
2. N/C pins (17, 51) should be left floating.

Imaging Performance

TYPICAL OPERATION CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

Notes:
1. For monochrome sensor, only green LED used.

SPECIFICATIONS

All Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Dark Field Global Non-Uniformity	DSNU	-	-	2.0	mVpp	Die	27, 40	
Bright Field Global Non-Uniformity		-	2.0	5.0	%rms	Die	27, 40	1
Bright Field Global Peak to Peak Non-Uniformity	PRNU	-	5.0	15.0	%pp	Die	27, 40	1
Bright Field Center Non-Uniformity		-	1.0	2.0	%rms	Die	27, 40	1
Maximum Photoresponse Nonlinearity	NL	-	2	-	%	Design		2
Maximum Gain Difference Between Outputs	ΔG	-	10	-	%	Design		2
Maximum Signal Error due to Nonlinearity Differences	ΔNL	-	1	-	%	Design		2
Horizontal CCD Charge Capacity	HNe	-	55	-	ke^-	Design		
Vertical CCD Charge Capacity	VNe	-	40	-	ke^-	Design		
Photodiode Charge Capacity	PNe	-	20	-	ke^-	Die	27, 40	3
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	-		Die		
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	-		Die		
Photodiode Dark Current	Ipd	-	7	70	e/p/s	Die	40	
Vertical CCD Dark Current	Ivd	-	100	300	e/p/s	Die	40	
Image Lag	Lag	-	-	10	e^-	Design		
Antiblooming Factor	Xab	300	-	-		Design		
Vertical Smear	Smr	-	-100	-	dB	Design		
Read Noise	n_{e-T}	-	12	-	e^-rms	Design		4
Dynamic Range	DR	-	64	-	dB	Design		4, 5
Output Amplifier DC Offset	V_{odc}	-	9.4	-	V	Die	27, 40	
Output Amplifier Bandwidth	f_{-3db}	-	250	-	MHz	Die		6
Output Amplifier Impedance	R_{OUT}	-	127	-	Ohms	Die	27, 40	
Output Amplifier Sensitivity	ΔV/ΔN	-	34	-	μV/e-	Design		

KAI-04050-ABA, KAI-04050-QBA, and KAI-04050-PBA[7] Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	QE_{max}	-	46	-	%	Design		
Peak Quantum Efficiency Wavelength	λQE	-	500	-	nm	Design		

KAI-04050-FBA and KAI-04050-QBA Gen2 Color Configurations with MAR Glass

Description		Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	Blue Green Red	QE_{max}	-	38 37 31	-	%	Design		
Peak Quantum Efficiency Wavelength	Blue Green Red	λQE	-	460 530 605	-	nm	Design		

KAI-04050-FBA Gen2 Color Configuration with Clear Glass

Description		Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	Blue Green Red	QE_{max}	-	35 34 29	-	%	Design		
Peak Quantum Efficiency Wavelength	Blue Green Red	λQE	-	460 530 605	-	nm	Design		

KAI-04050-CBA and KAI-04050-PBA Gen1 Color Configurations with MAR Glass

Description		Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	Blue Green Red	QE_{max}	-	39 37 29	-	%	Design		7
Peak Quantum Efficiency Wavelength	Blue Green Red	λQE	-	470 540 620	-	nm	Design		7

KAI-04050-CBA Gen1 Color Configuration with Clear Glass

Description		Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	Blue Green Red	QE_{max}	-	36 34 27	-	%	Design		7
Peak Quantum Efficiency Wavelength	Blue Green Red	λQE	-	470 540 620	-	nm	Design		7

Notes:

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 680 mV.
4. At 40 MHz
5. Uses 20LOG(PNe/ n_{e-T})
6. Assumes 5pF load
7. This color filter set configuration (Gen1) is not recommended for new designs.

Typical Performance Curves

QUANTUM EFFICIENCY

Monochrome, all configurations

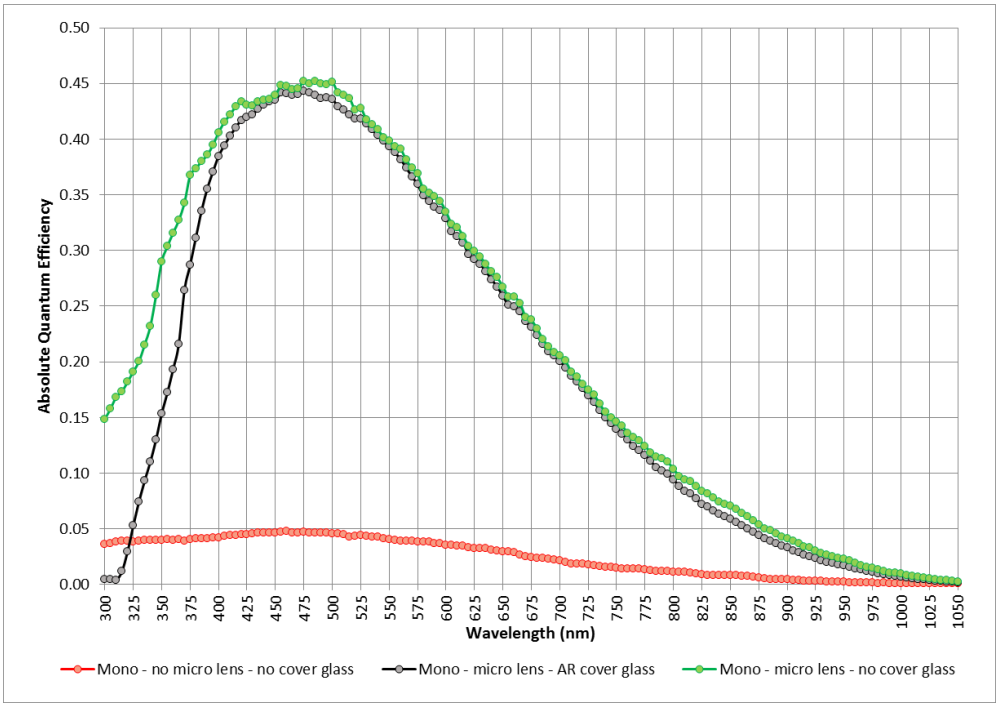


Figure 5: Monochrome Configurations - Quantum Efficiency

Color (Bayer RGB) with Microlens and MAR Cover Glass (Gen2 and Gen1 CFA)

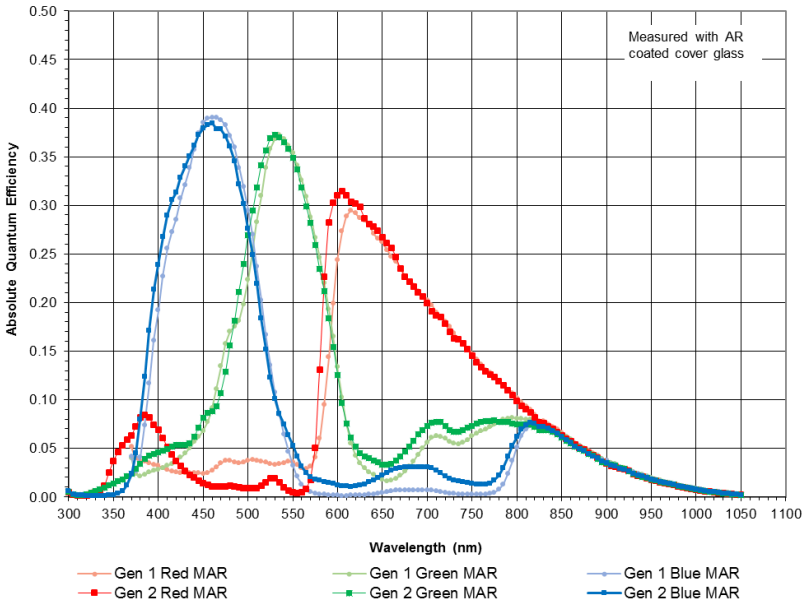


Figure 6: MAR Glass Color (Bayer) with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens and Clear Cover Glass (Gen2 and Gen1 CFA)

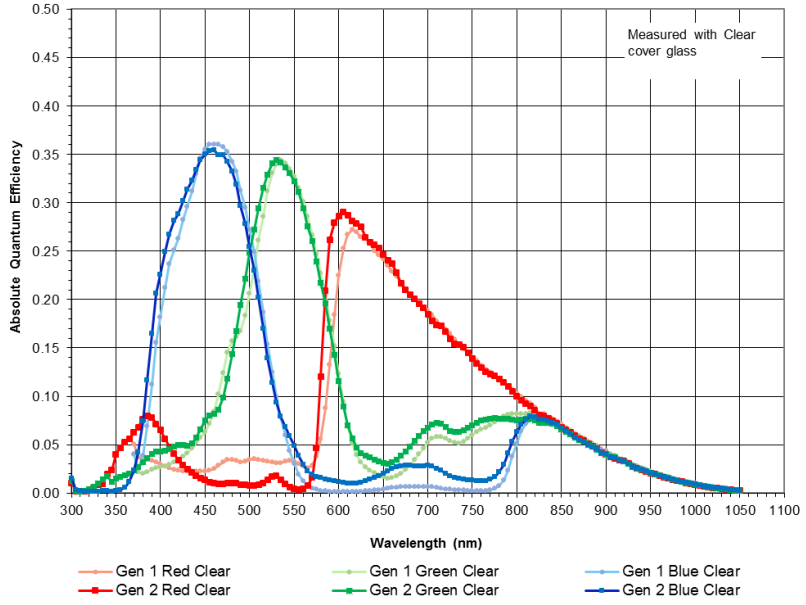


Figure 7: Clear Glass Color (Bayer) with Microlens Quantum Efficiency

Color (TRUESENSE Sparse CFA) with Microlens (Gen2 and Gen1 CFA)

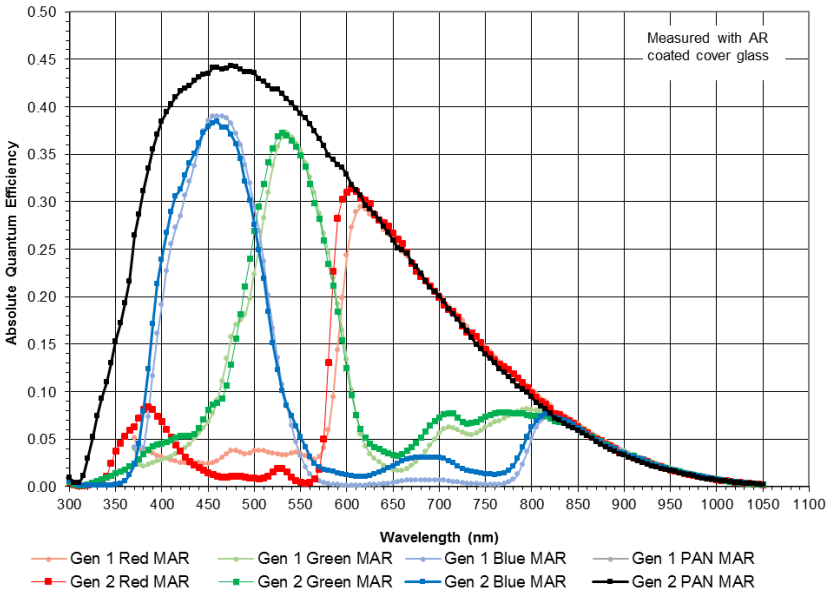


Figure 8: Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency

ANGULAR QUANTUM EFFICIENCY

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

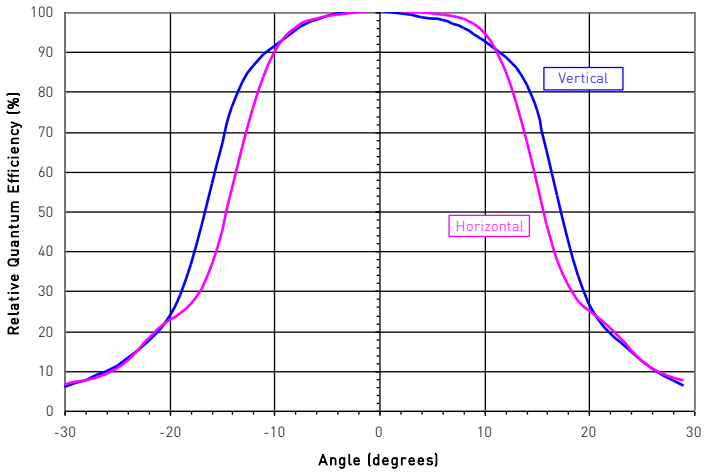


Figure 9: Monochrome with Microlens Angular Quantum Efficiency

DARK CURRENT VERSUS TEMPERATURE

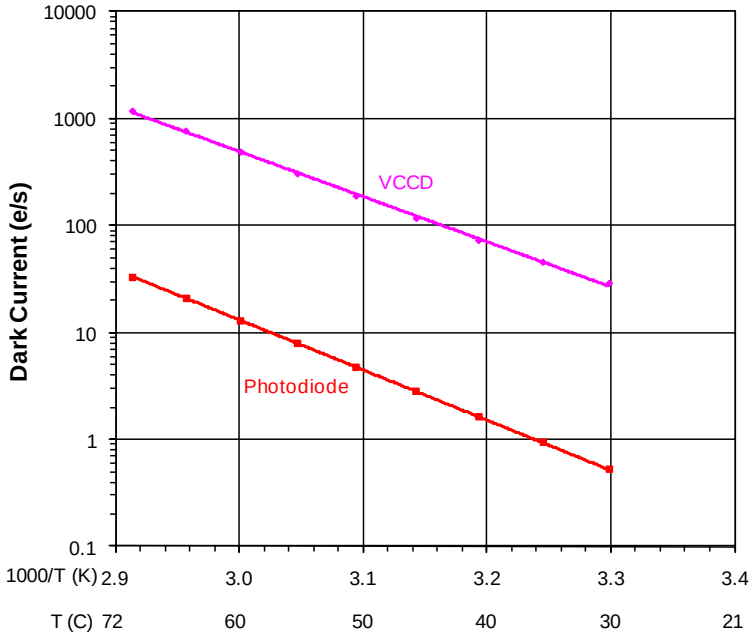


Figure 10: Dark Current versus Temperature

POWER – ESTIMATED

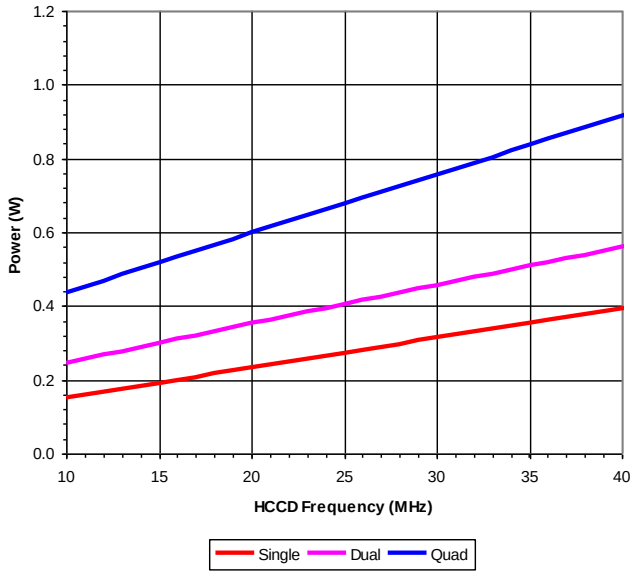


Figure 11: Power

FRAME RATES

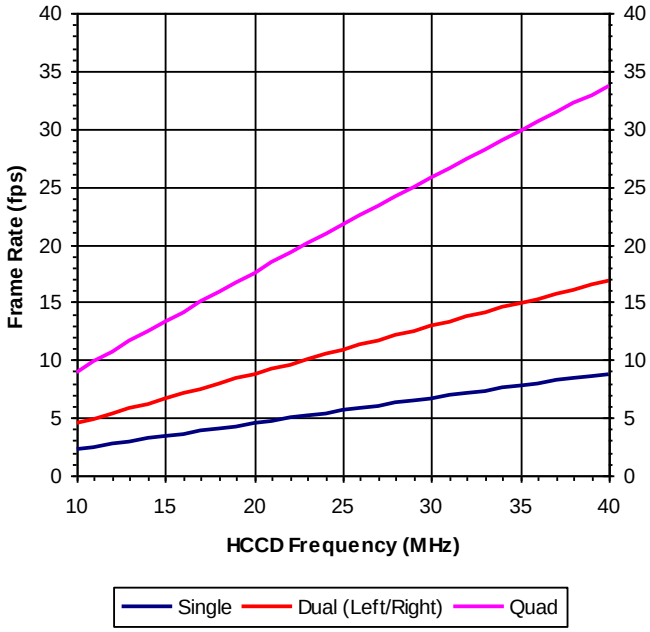


Figure 12: Frame Rates

Defect Definitions

Operation Conditions for Defect Testing at 40 °C

Description	Condition	Notes
Operational Mode	Two outputs, using VOUTa and VOUTc, continuous readout	
HCCD Clock Frequency	10 MHz	
Pixels Per Line	2560	1
Lines Per Frame	992	2
Line Time	259.8 µsec	
Frame Time	256.8 msec	
Photodiode Integration Time	Mode A: PD_Tint = Frame Time = 256.8 msec, no electronic shutter used	
	Mode B: PD_Tint = 33 msec, electronic shutter used	
VCCD Integration Time	233.0 msec	3
Temperature	40 °C	
Light Source	Continuous red, green and blue LED illumination	4
Operation	Nominal operating voltages and timing	

Notes:
1. Horizontal overclocking used
2. Vertical overclocking used
3. VCCD Integration Time = 900 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

Defect Definitions for Testing at 40 °C

Description	Definition	Standard Grade	Grade 2	Notes
Major dark field defective bright pixel	PD_Tint = Mode A → Defect ≥ 88 mV or PD_Tint = Mode B → Defect ≥ 12 mV	40	40	1
Major bright field defective dark pixel	Defect ≥ 12%			
Minor dark field defective bright pixel	PD_Tint = Mode A → Defect ≥ 44 mV or PD_Tint = Mode B → Defect ≥ 6 mV	400	400	
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.	8	n/a	2
Cluster Defect (Grade 2)	A group of 2 to 10 contiguous major defective pixels	n/a	10	2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	0	2

Notes:
1. For the color device (KAI-04050-FBA, KAI-04050-CBA, KAI-04050-QBA, or KAI-04050-PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Operation Conditions for Defect Testing at 27 °C

Description	Condition	Notes
Operational Mode	Two outputs, using VOUTa and VOUTc, continuous readout	
HCCD Clock Frequency	20 MHz	
Pixels Per Line	2560	1
Lines Per Frame	992	2
Line Time	131.5 µsec	
Frame Time	130.4 msec	
Photodiode Integration Time (PD_Tint)	Mode A: PD_Tint = Frame Time = 130.4msec, no electronic shutter used	
	Mode B: PD_Tint = 33 msec, electronic shutter used	
VCCD Integration Time	118.2 msec	3
Temperature	27 °C	
Light Source	Continuous red, green and blue LED illumination	4
Operation	Nominal operating voltages and timing	

Notes
1. Horizontal overclocking used
2. Vertical overclocking used
3. VCCD Integration Time = 900 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

Defect Definitions for Testing at 27 °C

Description	Definition	Standard Grade	Grade 2	Notes
Major dark field defective bright pixel	PD_Tint = Mode A → Defect ≥ 14 mV or PD_Tint = Mode B → Defect ≥ 4 mV	40	40	1
Major bright field defective dark pixel	Defect ≥ 12%			
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.	8	n/a	2
Cluster Defect (Grade 2)	A group of 2 to 10 contiguous major defective pixels	n/a	10	2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	0	2

Notes:
1. For the color device (KAI-04050-FBA, KAI-04050-CBA, KAI-04050-QBA, or KAI-04050-PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 13: Regions of Interest for the location of pixel 1, 1.

Test Definitions

Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (2360, 1776)

Active Area ROI: Pixel (13, 13) to Pixel (2348, 1764)

Center ROI: Pixel (1131, 839) to Pixel (1230, 938)

Only the Active Area ROI pixels are used for performance and defect tests.

Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 13 for a pictorial representation of the regions of interest.

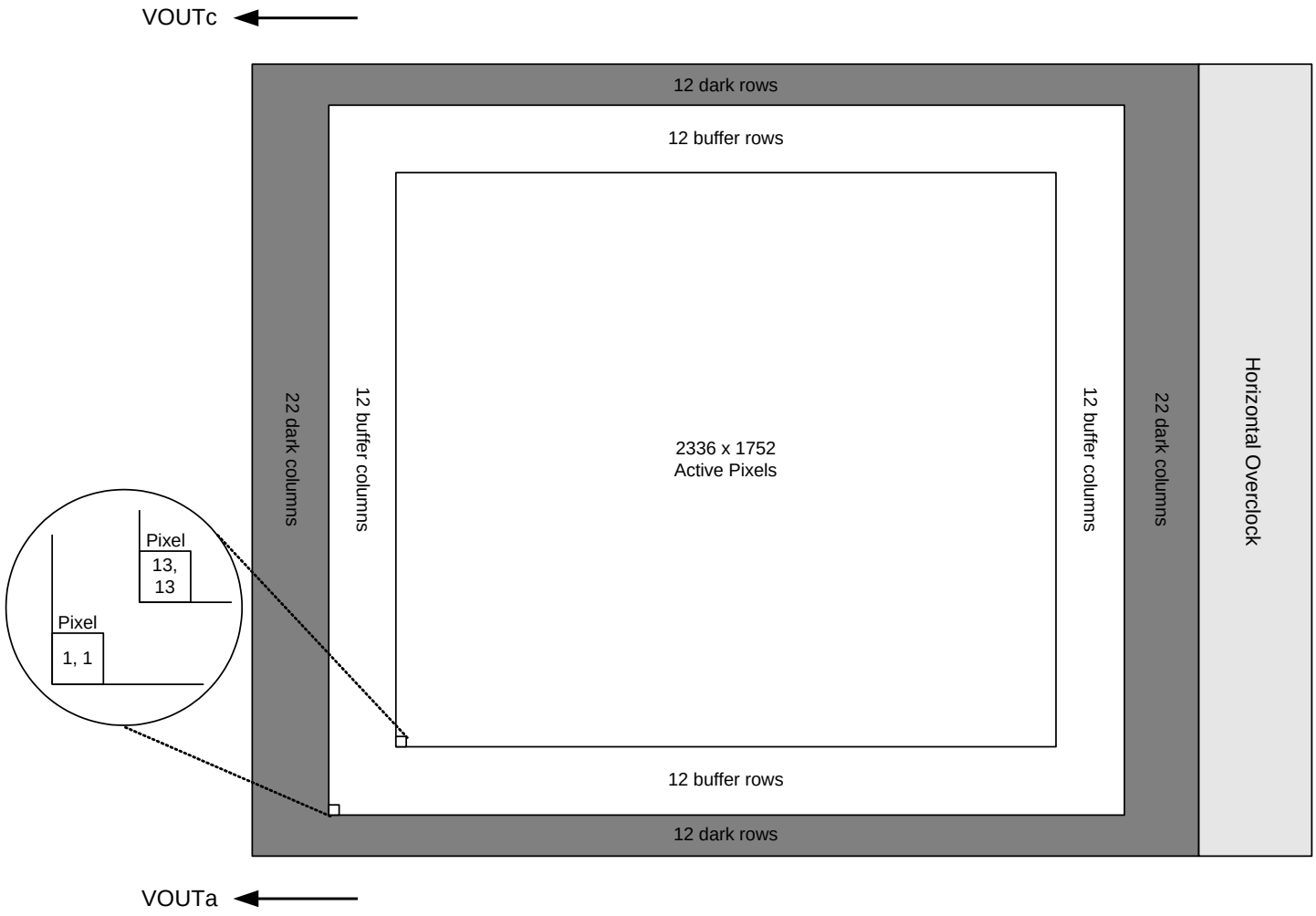


Figure 13: Regions of Interest

TESTS

Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 146 by 146 pixels in size. See Figure 14: Test Sub Regions of Interest. The average signal level of each of the 192 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overclock average in counts) * mV per count

Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Global non-uniformity is defined as

$$\text{Global Non-Uniformity} = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$ Units: %rms

Active Area Signal = Active Area Average – Dark Column Average

Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The sensor is partitioned into 192 sub regions of interest, each of which is 146 by 146 pixels in size. See Figure 14: Test Sub Regions of Interest. The average signal level of each of the 192 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overclock average in counts) * mV per count

Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = 100 * \frac{\text{Maximum Signal} - \text{Minimum Signal}}{\text{Active Area Signal}}$$

Units: %pp

Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms. Center ROI Signal = Center ROI Average – Dark Column Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 146 by 146 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the "Defect Definitions" section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 476 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 192 sub regions of interest, each of which is 146 by 146 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 476 mV
- Dark defect threshold: 476 mV * 12 % = 57 mV
- Bright defect threshold: 476 mV * 12 % = 57 mV
- Region of interest #1 selected. This region of interest is pixels 13, 13 to pixels 158, 158.
    - Median of this region of interest is found to be 470 mV.
    - Any pixel in this region of interest that is >= (470 + 57 mV) 527 mV in intensity will be marked defective.
    - Any pixel in this region of interest that is <= (470 - 57 mV) 413 mV in intensity will be marked defective.
- All remaining 192 sub regions of interest are analyzed for defective pixels in the same manner.

Test Sub Regions of Interest

Pixel (2348, 1764)

177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192
161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Pixel (13,13)

VOUTa ←

Figure 14: Test Sub Regions of Interest

Operation

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{OP}	-50	+70	°C	1
Humidity	RH	+5	+90	%	2
Output Bias Current	Iout	-	60	mA	3
Off-chip Load	C_L	-	10	pF	

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25 °C. Excessive humidity will degrade MTTF.
3. Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Absolute Maximum Voltage Ratings Between Pins and Ground

Description	Minimum	Maximum	Units	Notes
VDDα, VOUTα	-0.4	17.5	V	1
RDα	-0.4	15.5	V	1
V1B, V1T	ESD – 0.4	ESD + 24.0	V	
V2B, V2T, V3B, V3T, V4B, V4T	ESD – 0.4	ESD + 14.0	V	
H1Sα, H1Bα, H2Sα, H2Bα, H2SLα, Rα, OGα	ESD – 0.4	ESD + 14.0	V	1
ESD	-10.0	0.0	V	
SUB	-0.4	40.0	V	2

Notes:
1. α denotes a, b, c or d
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

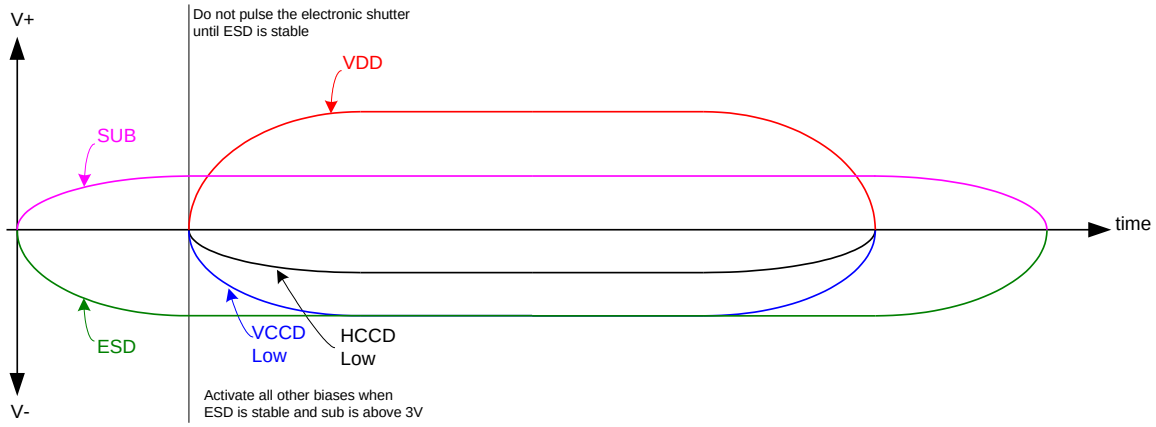
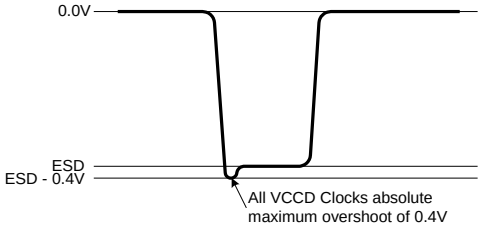


Figure 15: Power-Up and Power-Down Sequence

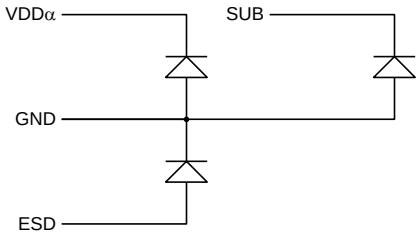
Notes:

1. Activate all other biases when ESD is stable and SUB is above 3V
2. Do not pulse the electronic shutter until ESD is stable
3. VDD cannot be +15V when SUB is 0V
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4V below the ESD voltage.



Example of external diode protection for SUB, VDD and ESD. α denotes a, b, c or d



DC Bias Operating Conditions

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Reset Drain	RDα	RD	+11.8	+12.0	+12.2	V	10 µA	1
Output Gate	OGα	OG	-2.2	-2.0	-1.8	V	10 µA	1
Output Amplifier Supply	VDDα	VDD	+14.5	+15.0	+15.5	V	11.0 mA	1, 2
Ground	GND	GND	0.0	0.0	0.0	V	-1.0 mA	
Substrate	SUB	VSUB	+5.0	VAB	VDD	V	50 µA	3, 8
ESD Protection Disable	ESD	ESD	-9.5	-9.0	Vx_L	V	50 µA	6, 7, 9
Output Bias Current	VOUTα	Iout	-3.0	-7.0	-10.0	mA	——	1, 4, 5

Notes:
1. α denotes a, b, c or d
2. The maximum DC current is for one output. Idd = Iout + Iss. See Figure 16.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power-Up and Power-Down Sequence section.
7. ESD maximum value must be less than or equal to V1_L+0.4V and V2_L+0.4V
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*
9. Where Vx_L is the level set for V1_L, V2_L, V3_L, or V4_L in the application.

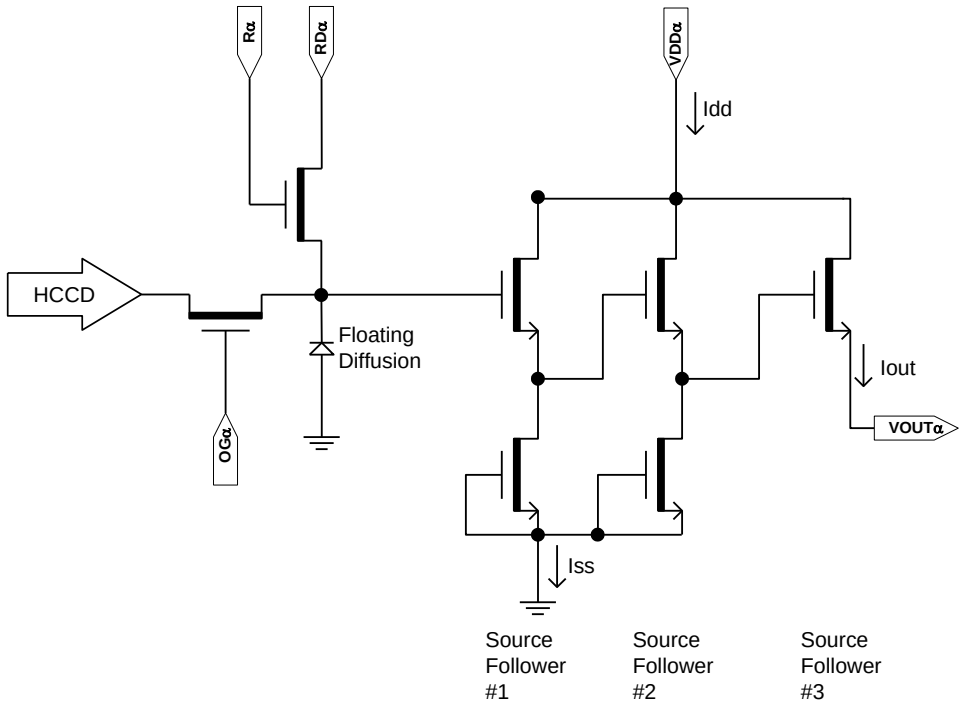


Figure 16: Output Amplifier

AC Operating Conditions

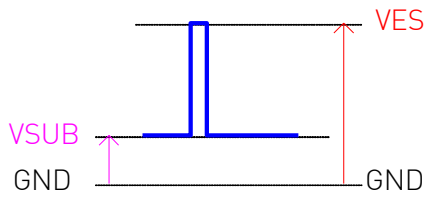
Clock Levels

Description	Pins[1]	Symbol	Level	Minimum	Nominal	Maximum	Units	Capacitance[2]
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	-8.2	-8.0	-7.8	V	21 nF (6)
		V1_M	Mid	-0.2	+0.0	+0.2		
		V1_H	High	+11.5	+12.0	+12.5		
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	-8.2	-8.0	-7.8	V	21 nF (6)
		V2_H	High	-0.2	+0.0	+0.2		
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	-8.2	-8.0	-7.8	V	21 nF (6)
		V3_H	High	-0.2	+0.0	+0.2		
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	-8.2	-8.0	-7.8	V	21 nF (6)
		V4_H	High	-0.2	+0.0	+0.2		
Horizontal CCD Clock, Phase 1 Storage	H1Sα	H1S_L	Low	-5.2 (7)	-4.0	-3.8	V	200 pF (6)
		H1S_A	Amplitude	+3.8	+4.0	+5.2 (7)		
Horizontal CCD Clock, Phase 1 Barrier	H1Bα	H1B_L	Low	-5.2 (7)	-4.0	-3.8	V	130 pF (6)
		H1B_A	Amplitude	+3.8	+4.0	+5.2 (7)		
Horizontal CCD Clock, Phase 2 Storage	H2Sα	H2S_L	Low	-5.2 (7)	-4.0	-3.8	V	200 pF (6)
		H2S_A	Amplitude	+3.8	+4.0	+5.2 (7)		
Horizontal CCD Clock, Phase 2 Barrier	H2Bα	H2B_L	Low	-5.2 (7)	-4.0	-3.8	V	130 pF (6)
		H2B_A	Amplitude	+3.8	+4.0	+5.2 (7)		
Horizontal CCD Clock, Last Phase[3]	H2SLα	H2SL_L	Low	-5.2	-5.0	-4.8	V	20 pF (6)
		H2SL_A	Amplitude	+4.8	+5.0	+5.2		
Reset Gate	Rα	R_L[4]	Low	-3.5	-2.0	-1.5	V	16 pF (6)
		R_H	High	+2.5	+3.0	+4.0		
Electronic Shutter[5]	SUB	VES	High	+29.0	+30.0	+40.0	V	1400 pF (6)

Notes:

1. α denotes a, b, c or d
2. Capacitance is total for all like named pins
3. Use separate clock driver for improved speed performance.
4. Reset low should be set to –3 volts for signal levels greater than 40,000 electrons.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*
6. Capacitance values are estimated
7. If the minimum horizontal clock low level is used (–5.2V), then the maximum horizontal clock amplitude should be used (5.2V amplitude) to create a –5.2V to 0.0V clock. If a 5 volt clock driver is used, the horizontal low level should be set to –5.0V and the high level should be a set to 0.0V

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.



DEVICE IDENTIFICATION

The device identification pin (DevID) may be used to determine which Truesense Imaging 5.5 micron pixel interline CCD sensor is being used.

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Device Identification	DevID	DevID	20,000	25,000	30,000	Ohms	50 µA	1, 2, 3

Notes:
1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. Values specified are for 40 °C.

Recommended Circuit

Note that V1 must be a different value than V2.

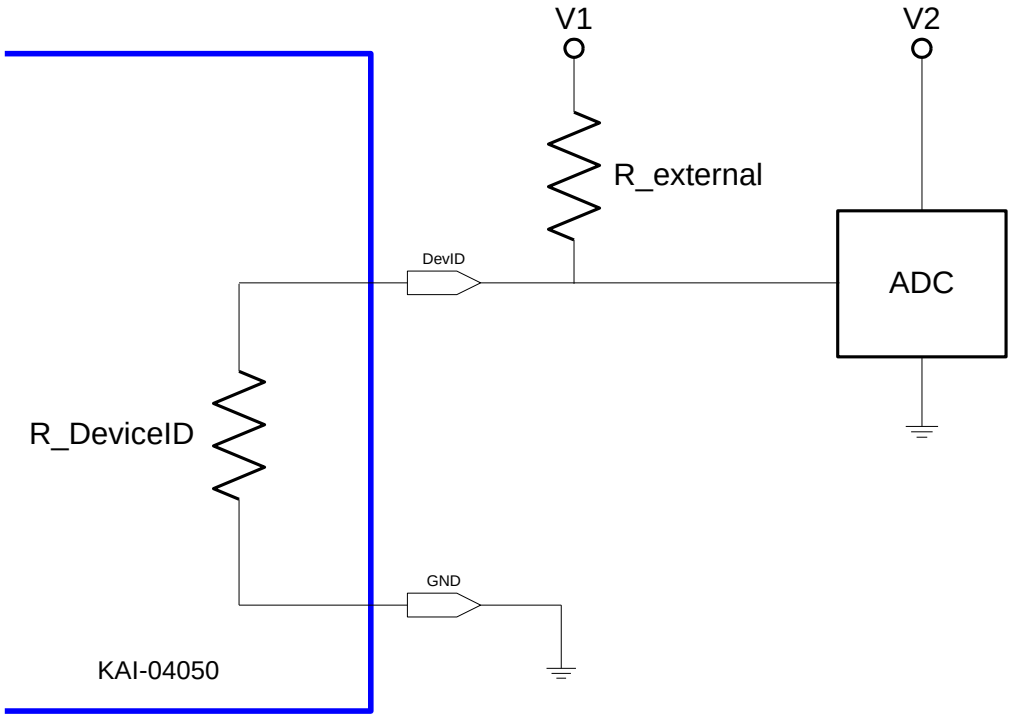


Figure 17: Device Identification Recommended Circuit

Timing

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Photodiode Transfer	t_{pd}	1.0	-	-	µs	
VCCD Leading Pedestal	t_{3p}	4.0	-	-	µs	
VCCD Trailing Pedestal	t_{3d}	4.0	-	-	µs	
VCCD Transfer Delay	t_{d}	1.0	-	-	µs	
VCCD Transfer	t_{v}	1.6	-	-	µs	
VCCD Clock Cross-over	v_{VCR}	75		100	%	
VCCD Rise, Fall Times	t_{VR}, t_{VF}	5	-	10	%	2, 3
HCCD Delay	t_{hs}	0.2	-	-	µs	
HCCD Transfer	t_{e}	25.0	-	-	ns	
Shutter Transfer	t_{sub}	1.0	-	-	µs	
Shutter Delay	t_{hd}	1.0	-	-	µs	
Reset Pulse	t_{r}	2.5	-	-	ns	
Reset – Video Delay	t_{rv}	-	2.2	-	ns	
H2SL – Video Delay	t_{hv}	-	3.1	-	ns	
Line Time	t_{line}	32.9	-	-	µs	Dual HCCD Readout
		63.0	-	-		Single HCCD Readout
Frame Time	t_{frame}	29.7	-	-	ms	Quad HCCD Readout
		59.3	-	-		Dual HCCD Readout
		113.4	-	-		Single HCCD Readout

Notes:
1. Refer to timing diagrams as shown in Figure 18, Figure 19, Figure 20, Figure 21 and Figure 22
2. Refer to Figure 22: VCCD Clock Edge Alignment
3. Relative to the pulse width

TIMING DIAGRAMS

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1-P7) as shown in the table below. The patterns are defined in Figure 18 and Figure 19. Contact Truesense Imaging Application Engineering for other readout modes.

Device Pin	Quad Readout	Dual Readout VOUTa, VOUTb	Dual Readout VOUTa, VOUTc	Single Readout VOUTa
V1T	P1T	P1B	P1T	P1B
V2T	P2T	P4B	P2T	P4B
V3T	P3T	P3B	P3T	P3B
V4T	P4T	P2B	P4T	P2B
V1B	P1B			
V2B	P2B			
V3B	P3B			
V4B	P4B			
H1Sa	P5			
H1Ba				
H2Sa[2]	P6			
H2Ba				
Ra	P7			
H1Sb	P5		P5	
H1Bb			P6	
H2Sb[2]	P6		P6	
H2Bb			P5	
Rb	P7		P7[1] or Off[3]	P7[1] or Off[3]
H1Sc	P5	P5[1] or Off[3]	P5	P5[1] or Off[3]
H1Bc				
H2Sc[2]	P6	P6[1] or Off[3]	P6	P6[1] or Off[3]
H2Bc				
Rc	P7	P7[1] or Off[3]	P7	P7[1] or Off[3]
H1Sd	P5	P5[1] or Off[3]	P5	P5[1] or Off[3]
H1Bd			P6	
H2Sd[2]	P6	P6[1] or Off[3]	P6	P6[1] or Off[3]
H2Bd			P5	
Rd	P7	P7[1] or Off[3]	P7[1] or Off[3]	P7[1] or Off[3]
# Lines/Frame (Minimum)	900	1800	900	1800
# Pixels/Line (Minimum)	1213		2426	

Notes:

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx For optimal speed performance, use a separate clock driver.
3. Off = +5V. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The "Last Line" is dependent on readout mode – either 632 or 1264 minimum counts required. It is important to note that, in general, the rising edge of a vertical clock (patterns P1-P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3rd level) state to the mid-state when P4 transitions from the low state to the high state.

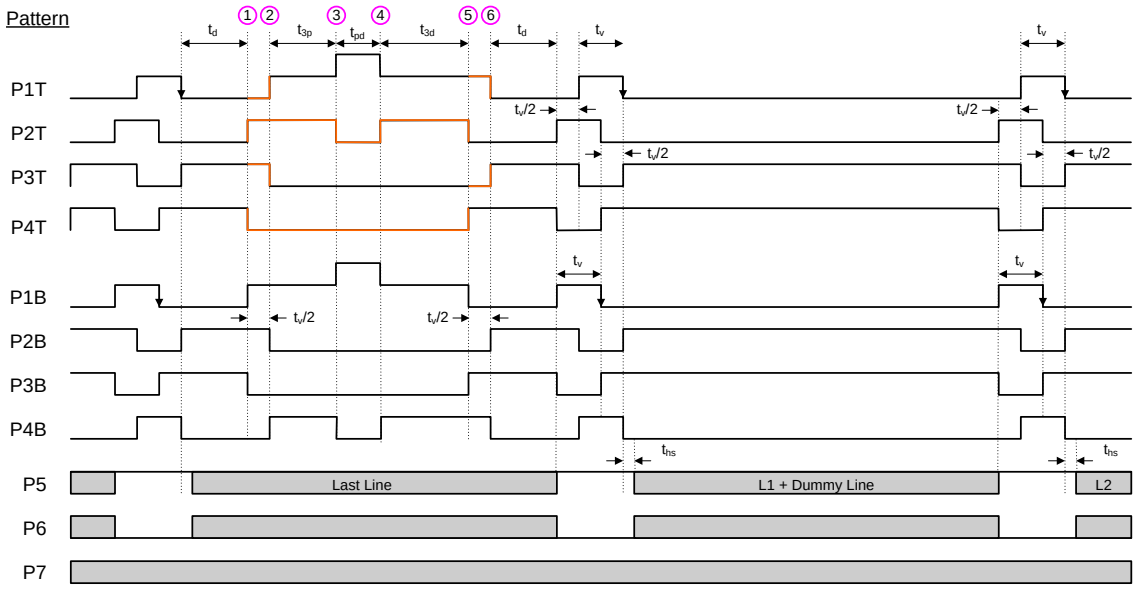


Figure 18: Photodiode Transfer Timing

Line and Pixel Timing

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as P6 pattern). The number of pixels in a row is dependent on readout mode – either 1213 or 2426 minimum counts required.

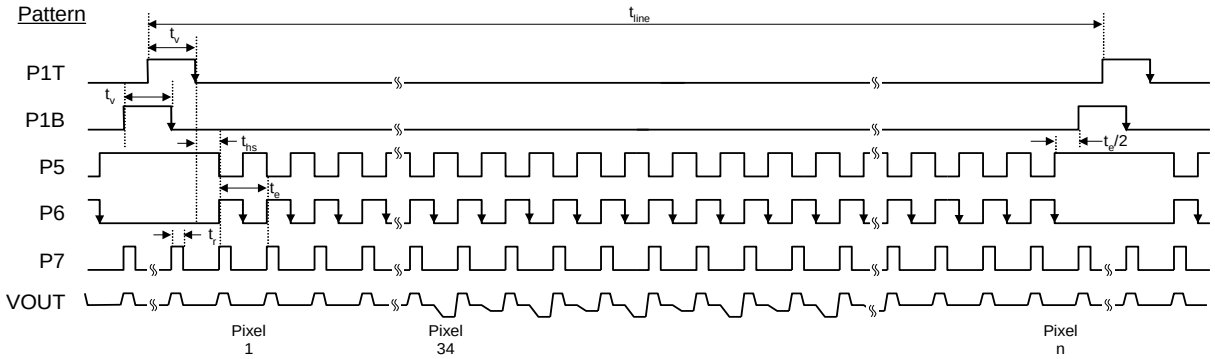


Figure 19: Line and Pixel Timing

Pixel Timing Detail

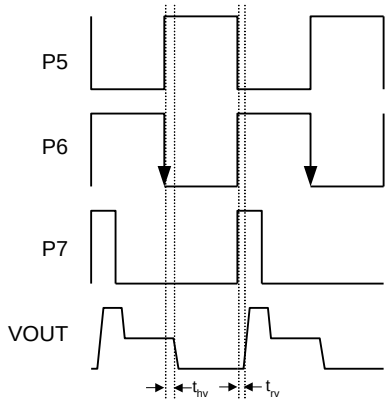


Figure 20: Pixel Timing Detail

Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below. The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

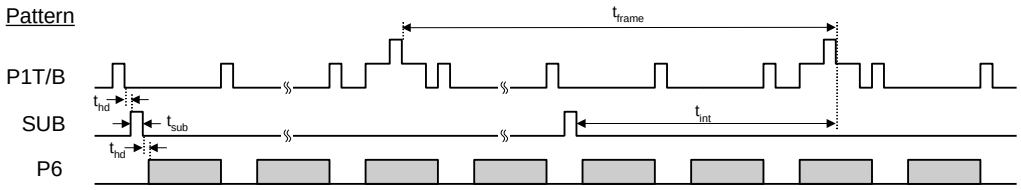


Figure 21: Frame/Electronic Shutter Timing

VCCD Clock Edge Alignment

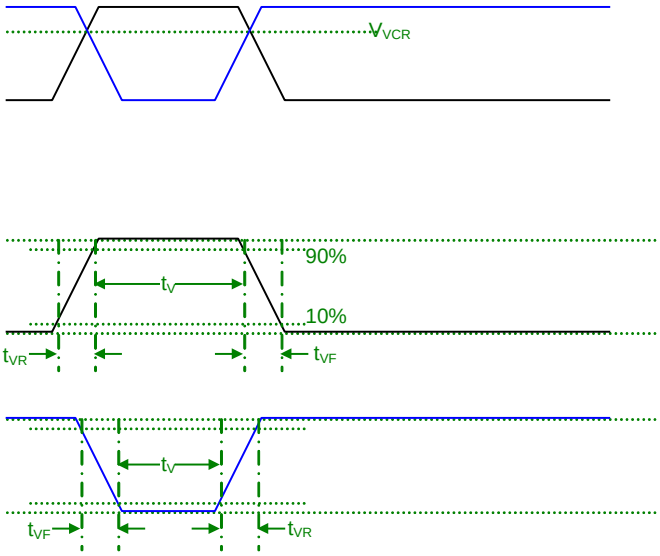


Figure 22: VCCD Clock Edge Alignment

Line and Pixel Timing – Vertical Binning by 2

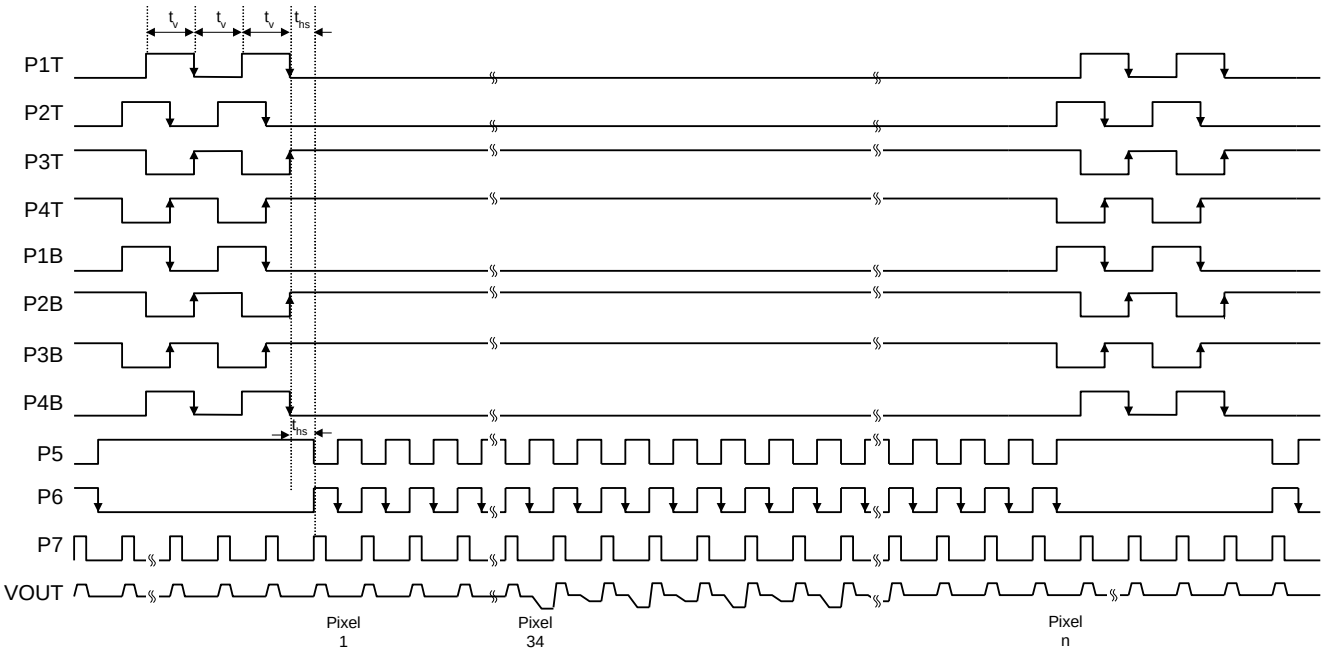


Figure 23: Line and Pixel Timing - Vertical Binning by 2

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	+80	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

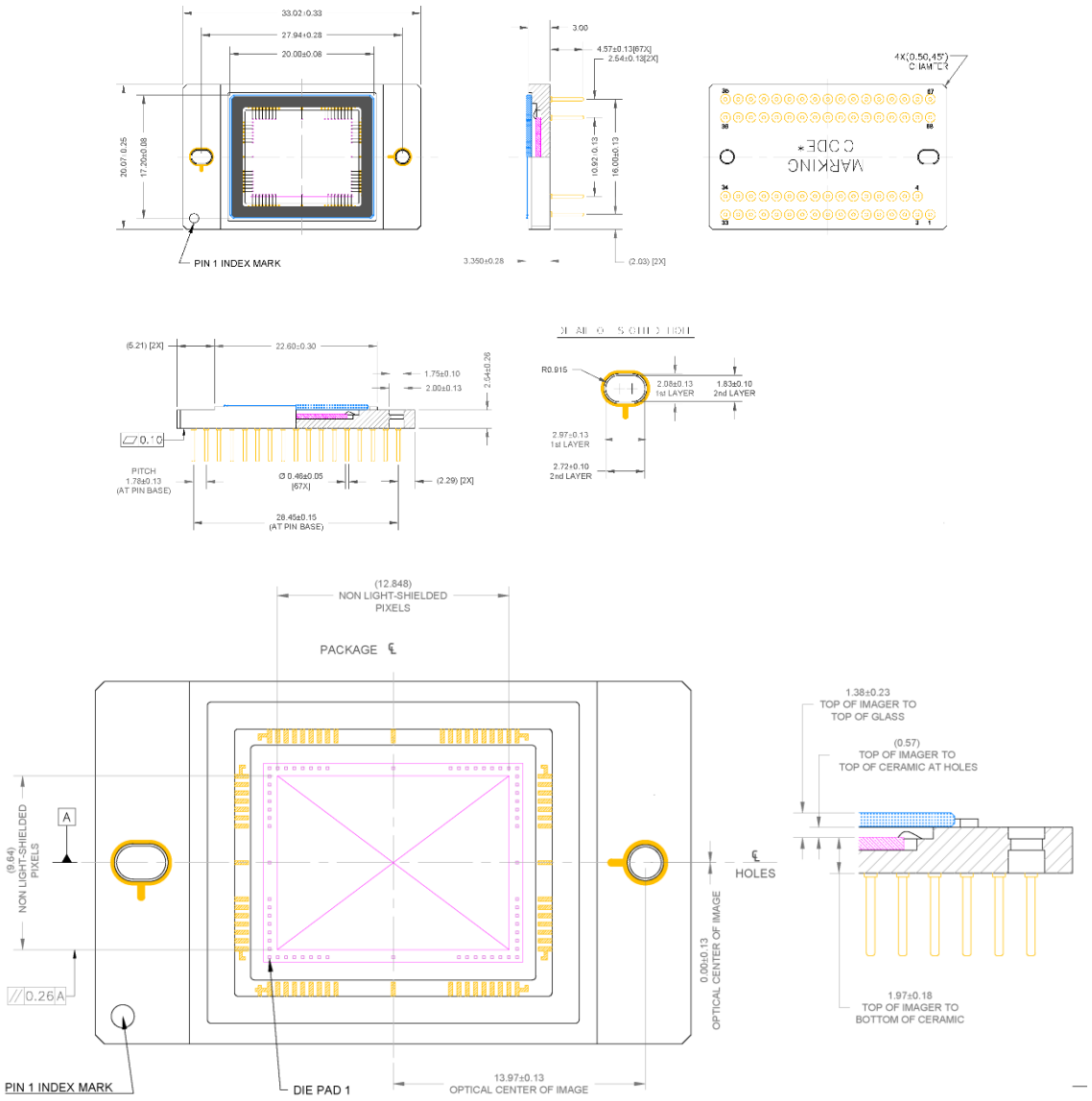


Figure 24: Completed Assembly

Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through guide holes.
3. The center of the active image is nominally at the center of the package.
4. Die rotation < 0.5 degrees
5. Cover glass placement is within recess cavity wall
6. Internal traces may be exposed on sides of package. Do not allow metal to contact sides of ceramic package.
7. Recommended mounting screws: 1.6 X 0.35 mm (ISO Standard); 0 – 80 (Unified Fine Thread Standard)
8. Units: millimeters

MAR Cover Glass

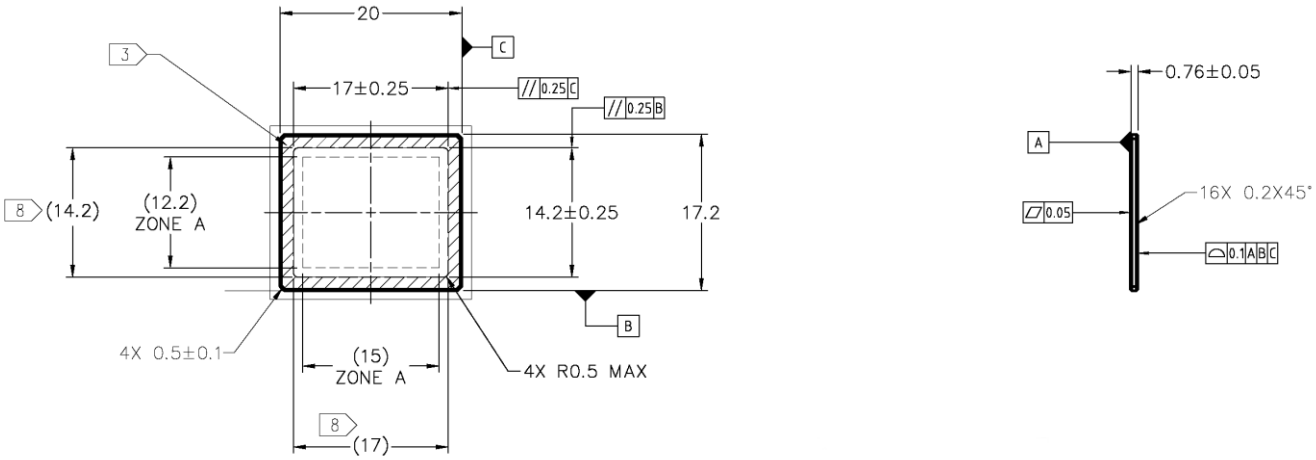


Figure 25: MAR Cover Glass

Notes:

1. Dust/Scratch count – 12 micron maximum
2. Units: MM

Clear Cover Glass

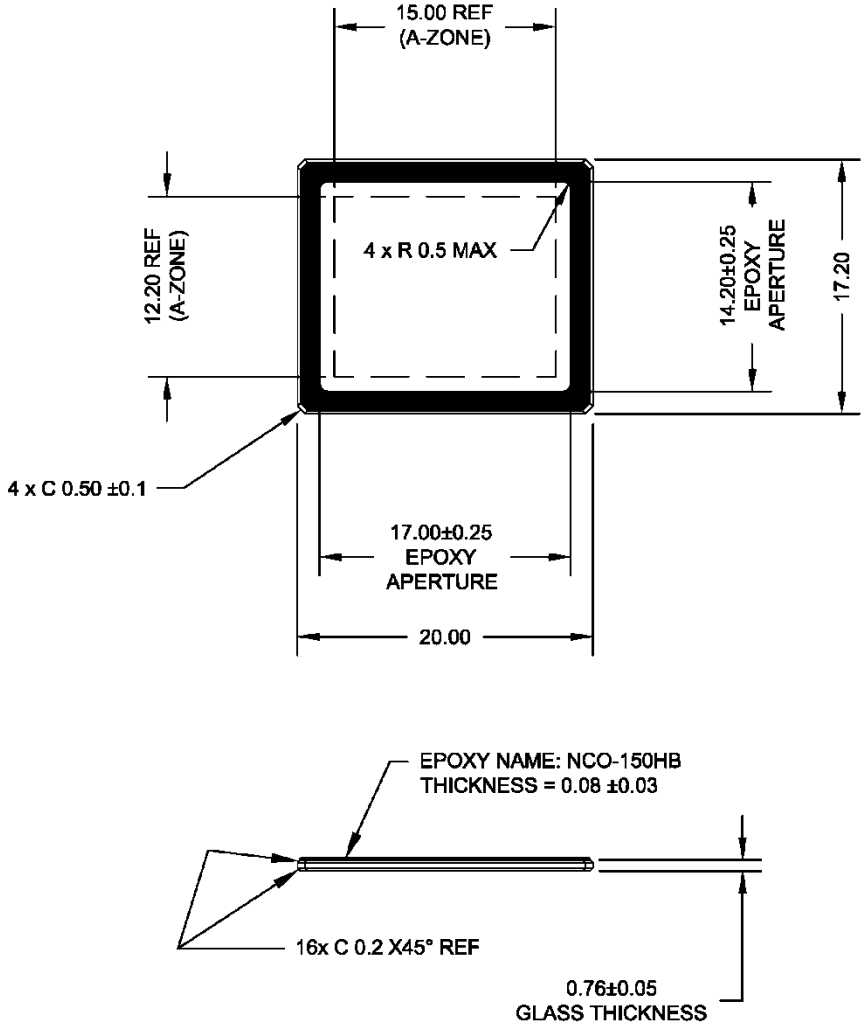


Figure 26: Clear Cover Glass

Notes:

1. Dust/Scratch count – 12 micron maximum
2. Units: MM

COVER GLASS TRANSMISSION

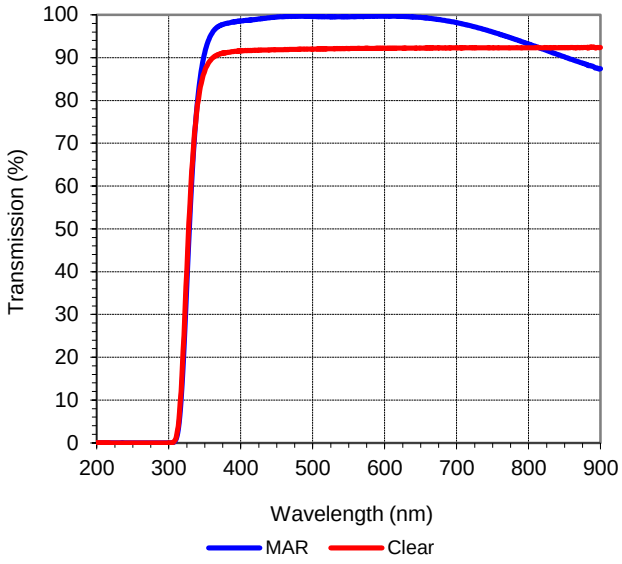


Figure 27: Cover Glass Transmission

Shipping Configuration

Cover Glass Protective Tape

Cover glass protective tape, as shown in Figure 28, is utilized to help ensure the cleanliness of the cover glass during transportation and camera manufacturing. This protective tape is not intended to be optically correct, and should be removed prior to any image testing. The protective tape should be removed in an ionized air stream to prevent static build-up and the attraction of particles. The following part numbers will have the protective tape applied:

Catalog Number	Product Name	Description
4H2244	KAI-04050-CBA-JB-B2	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2
4H2245	KAI-04050-CBA-JB-AE	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Engineering Grade
4H2293	KAI-04050-CBA-JB-B2-T	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2, Packed in Trays

Criteria	Description
Placement	Per the drawing. The lid tape shall not overhang the edge of the package or mounting holes. The lid tape always overhangs the top surface of the glass (chamfers not included).
Tab Location	The tape tab is located near pin 68.
Scratches	The tape application equipment will make slight scratches on the lid tape. This is allowed.

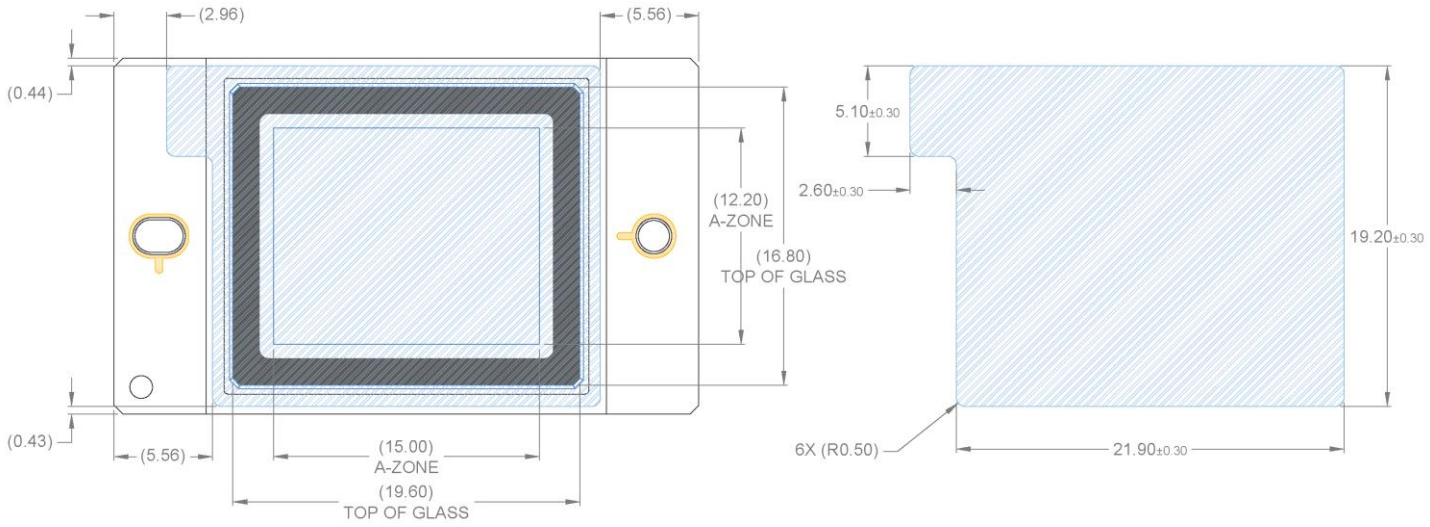


Figure 28: Cover Glass Protective Tape

TRAY PACKING

The following part numbers are packed in bricks of 6 trays, each tray containing 32 image sensors, for a total of 192 image sensors per brick. The minimum order and multiple quantities for this configuration are 192 image sensors.

Catalog Number	Product Name	Description
4H2293	KAI-04050-CBA-JB-B2-T	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2, Packed in Trays

Tray Configuration

Pin Up View

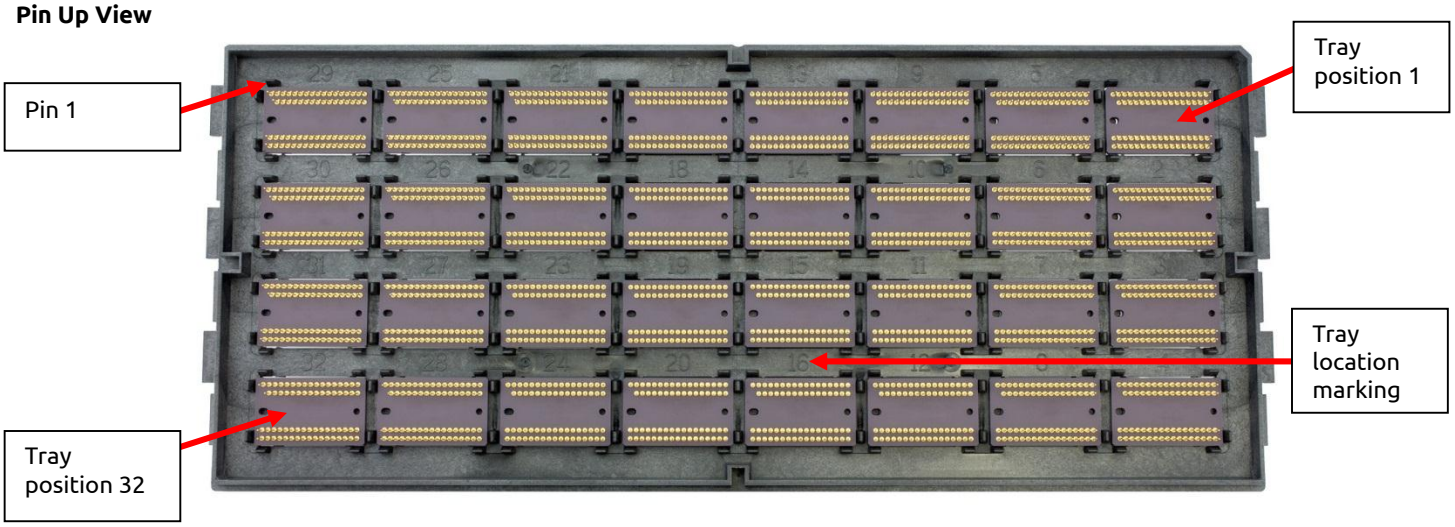


Figure 29: Tray Pin-Up View

Pin Down View

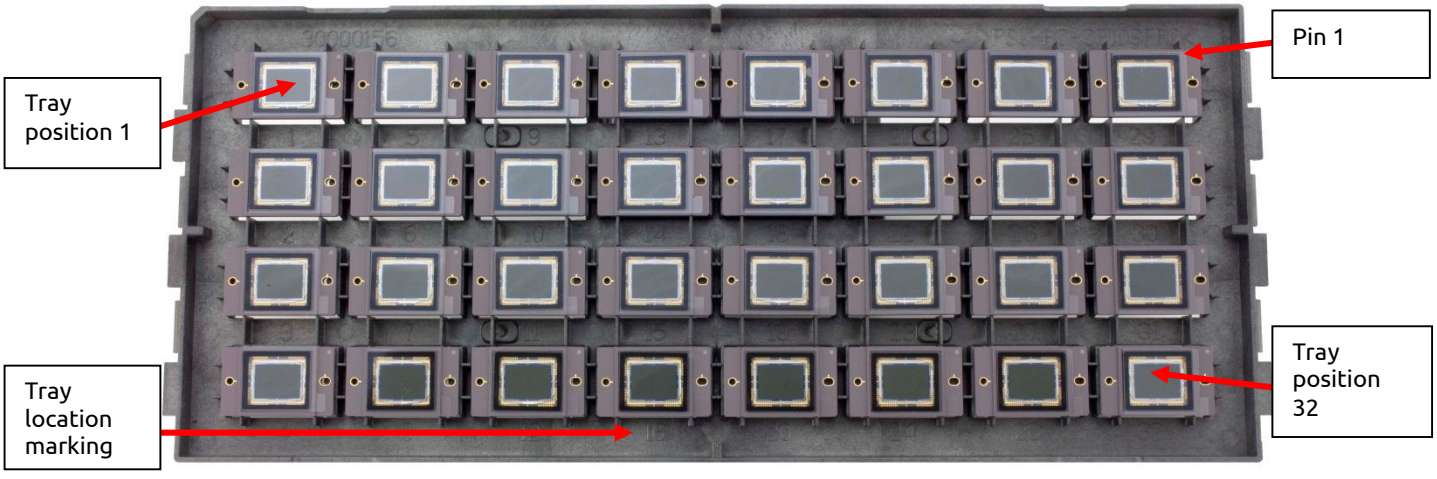


Figure 30: Tray Pin-Down View

Brick Configuration

Bricks consist of 6 full trays and 1 empty tray. Each tray contains 32 image sensors. There are a total of 192 image sensors in the brick. The ID label is applied to the top of the brick. Tray 1 is at the bottom of the brick and the empty tray is at the top of the brick.

Figure 31: Brick

The brick ID is encoded in the bar code.

Figure 32: Brick ID Label

Brick in Vacuum Sealed Bag

Figure 33: Sealed Brick

Shipping Container

Brick Loaded in Shipping Container

Figure 34: Bick Loaded in Shipping Container

Open Shipping Container with Parts List

The parts list (see Figure 38) details information for each sensor in the brick. The parts list includes the serial number, tray and location, and VAB value for each sensor.

Figure 35: Open Shipping Container with Part List

Sealed Shipping Container

The Brick Label (see Figure 37) is applied to both ends of the shipping container.

Figure 36: Sealed Shipping Container

Brick Label

Figure 37: Brick Label

Parts List

The parts list details information for each sensor in the brick. The parts list includes the serial number, tray and location, and VAB value for each sensor. Additionally, the VAB value and serial number are encoded in the bar code

Figure 38: Parts List

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-1172

Revision Number	Description of Changes
1.0	• Initial formal release
2.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections • Absolute Maximum Voltage Ratings Between Pins and Ground • DC Bias Operating Conditions • AC Operating Conditions • Storage and Handling
3.0	• Changed the nominal Vertical CCD Charge Capacity from 45 ke$^-$ to 40 ke$^-$ • Changed the nominal Vertical CCD Dark Current from 140 e/s to 100 e/s • Changed the maximum Vertical CCD Dark Current from 400 e/s to 300 e/s • Updated Dark Current versus Temperature graph
4.0	• Added TRUESENSE Sparse Color Filter information
5.0	• Updated reference documentation statement on Ordering Page

PS-0009

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections • Updated Ordering Information Table with Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings) part numbers • Updated Color (Bayer CFA) with Microlens Quantum Efficiency figure • Updated Defect Definitions tables with Grade 2 information • Added Clear Glass drawing • Updated Cover Glass Transmission figure
2.0	• Updated AC Clock Level Table to clarify that 5V amplitude horizontal clocks may be used • Updated AC Clock Level Table to note that capacitance values are estimated
3.0	• Configuration change for catalog numbers: 4H2085, 4H2086, 4H2089, and 4H2090. New configuration or these catalog numbers replaces the taped on MAR glass with a taped on clear glass. A product name and description change applies to each of these catalog numbers. • Update V_{VCR} from the previous level of 50% min to a new specification of 75% min. • Added new specification for vertical rise time, t_{vr}, and vertical fall time, t_{vf}, to be specified at 5% min and a value of 10% max of the pulse width. • The timing diagram in the *Frame Timing* section is modified. • Updated the Vx_L level from the current values of -9.0V +/- 0.5V to a new requirement of -8.0V +/- 0.2V. • Updated the VESD level from the current values of -9.0V +/- 0.5V to a new requirement of Vx_L max (-8.2V) to -9.5V min. • Updated the monochrome QE curve with new measured value. Restate the monochrome QEmax typical performance value from the current 50% value to a new value of 46%. • Updated the RGB QE curves with new measured values. Restate the RGB QEmax typical performance values from the current 31%, 42%, and 43% values to new values of 29%, 37%, 39%, respectively. • Reduced the RD maximum allowed value from 17.5V to 15.5V.
4.0	• Marking Code change for catalog numbers 4H2244 and 4H2245: the marking code now includes the VAB value. • Added part number 4H2293 KAI-04050-CBA-JB-B2-T Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (no coatings), Grade 2, Packed in Trays to the Ordering Information table • Added section for parts that ship with cover glass protective tape • Added Shipping Configuration section for parts sold in trays • Updated PGA Completed Assembly Drawing
4.1	• Updated branding
5.0	• Added ordering information, descriptions, and QE curves for Gen2 CFA configuration. • Updated the Mono QE curve and values

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

© 2014, Semiconductor Components Industries, LLC.

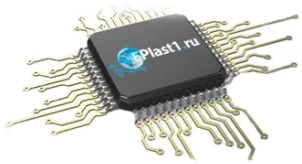
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.