MAX16838B

Integrated, 2-Channel, High-Brightness LED Driver with High-Voltage Boost and SEPIC Controller

General Description

The MAX16838B is a dual-channel LED driver that integrates both the DC-DC switching boost regulator and two 150mA current sinks. A current-mode switching DC-DC controller provides the necessary voltage to both strings of HB LEDs. The device accepts a wide 4.75V to 40V input voltage range and directly withstands automotive load-dump events. For a 5V ±10% input voltage, connect V_{IN} to V_{CC}. The wide input range allows powering HB LEDs for small-to-medium-sized LCD displays in automotive and display backlight applications.

An internal current-mode switching DC-DC controller supports the boost or SEPIC topologies and operates in an adjustable frequency range between 200kHz and 2MHz. The current-mode control provides fast response and simplifies loop compensation. The device also features an adaptive output-voltage adjustment scheme that minimizes the power dissipation in the LED current-sink paths. The MAX16838B can be combined with the MAX15054 to achieve a buck-boost LED driver with two integrated current sinks.

The channel current is adjustable from 20mA to 150mA using an external resistor. The external resistor sets both channel currents to the same value. The device allows connecting both strings in parallel to achieve a maximum current of 300mA in a single channel. The MAX16838B also features pulsed dimming control with minimum pulse widths as low as 500ns on both channels through a logic input (DIM).

The device includes output overvoltage protection, open-LED/shorted-LED detection, and overtemperature protection. The device is available in 20-pin TSSOP (4.4mm) and TQFN (4mm x 4mm) packages and operates over the -40ºC to +125ºC automotive temperature range.

Applications

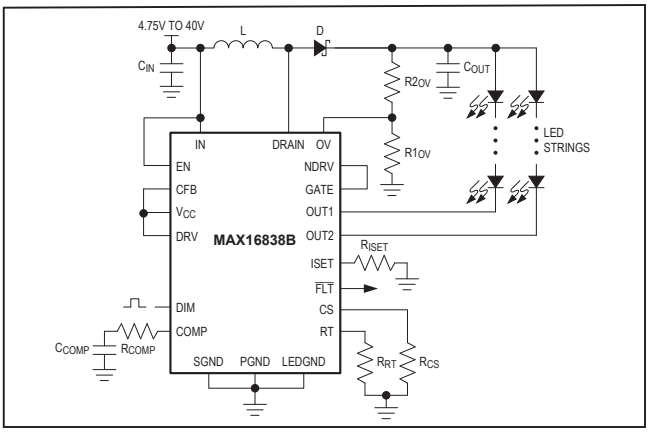
- Automotive Display Backlights
- LCD Display Backlights
- Automotive Lighting Applications

Benefits and Features

- High Integration Provides for a Compact Solution
  - Integrates 2-Channel, 20mA to 150mA Linear LED Current Sinks
  - Internal Slope Compensation and Switching MOSFET
- Flexible IC Fits Many Applications
  - Boost or SEPIC Converter Topologies
  - Wide 4.75V to 40V or 5V ±10% Input Operating Range
  - 200kHz to 2MHz Resistor-Programmable Switching Frequency with External Synchronization
- Wide Contrast Ratio Ideal for High Quality TFT and Head-Up Displays
  - PWM Dimming Ratio of 10,000:1 at 200Hz
- Robust with Respect to Temperature and Fault Conditions
  - Current Foldback Reference Input
  - LED Open/Short Detection and Protection
  - Output Overvoltage and Overtemperature Protection
  - Thermally Enhanced 20-Pin TSSOP (4.4mm) and TQFN (4mm x 4mm) Packages

Typical Operating Circuit* and *Ordering Information* appear at end of data sheet.

Simplified Schematic



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Absolute Maximum Ratings

IN, OUT_, DRAIN to SGND .....-0.3V to +45V
EN to SGND .....-0.3V to (V_{IN} + 0.3V)
PGND to SGND.....-0.3V to +0.3V
LEDGND to SGND.....-0.3V to +0.3V
DRV to PGND .....-0.3V to the lower of (V_{IN} + 0.3V) and +6V
GATE to PGND .....-0.3V to +6V
NDRV to PGND.....-0.3V to (V_{DRV} + 0.3V)
V_{CC}, $\overline{FLT}$, DIM, CS, OV, CFB, to SGND.....-0.3V to +6V
RT, COMP, ISET to SGND .....-0.3V to (V_{CC} + 0.3V)
DRAIN and CS Continuous Current.....±2.5A
OUT_ Continuous Current.....175mA
V_{DRV} Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70ºC)
20-Pin TQFN (derate 25.6mW/ºC above +70ºC) 2051mW
20-Pin TSSOP (derate 26.5mW/ºC above +70ºC)....2122mW
Operating Temperature Range.....-40ºC to +125°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65ºC to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Juction-to-Ambient Thermal Resistance (θ_{JA}) .....+39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....+6°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....+37.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....+2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, DRAIN, COMP, OUT_, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = T_J = -40ºC to +125°C, unless otherwise noted. Typical values are at T_A = 25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Internal LDO on	4.75		40	V
Input Voltage Range	V_{IN}	V_{IN} = V_{CC}	4.55		5.5	V
Quiescent Supply Current	I_Q	V_{DIM} = 5V		3.1	5	mA
Standby Supply Current	I_{SH}	V_{EN} = SGND (Note 3)		15.5	40	µA
Undervoltage Lockout	$UVLO_{IN}$	V_{IN} rising, V_{DIM} = 5V	4	4.3	4.55	V
Undervoltage Lockout Hysteresis				177		mV
DRV REGULATOR						
Output Voltage	V_{DRV}	5.75V < V_{IN} < 10V, 0.1mA < I_{LOAD} < 30mA 6.5V < V_{IN} < 40V, 0.1mA < I_{LOAD} < 3mA	4.75	5	5.25	V
Dropout Voltage	V_{DO} (V_{IN} - V_{DRV})	V_{IN} = 4.75V, I_{OUT} = 30mA		0.11	0.5	V
Short-Circuit Current Limit		DRV shorted to GND		97		mA
V_{CC} Undervoltage Lockout Threshold	$UVLO_{VCC}$	V_{CC} rising	3.4	4.0	4.4	V
V_{CC} (UVLO) Hysteresis				123		mV

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, DRAIN, COMP, OUT_, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = T_J = -40ºC to +125°C, unless otherwise noted. Typical values are at T_A = 25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RT OSCILLATOR						
Switching Frequency Range	f_{SW}		200		2000	kHz
Duty Cycle	D_{MAX}	f_{SW} = 200kHz to 600kHz	90	94	98	%
		f_{SW} = 600kHz to 2MHz	86	90	94	%
Oscillator Frequency Accuracy		f_{SW} = 200kHz to 2MHz	-7.5		+7.5	%
Logic-Level Before SYNC Capacitor			4			V
Synchronization Pulse Width				100		ns
SYNC Frequency Range	f_{SYNC}		1.1 x f_{SW}		1.5 x f_{SW}	Hz
PWM COMPARATOR						
Leading-Edge Blanking				66		ns
Propagation Delay to NDRV		Including leading-edge blanking time		100		ns
SLOPE COMPENSATION						
Slope Compensation Peak Voltage per Cycle		Voltage ramp added to CS		0.12		V
CS LIMIT COMPARATOR						
CS Threshold Voltage	V_{CS_MAX}	V_{COMP} = 3V	285	300	315	mV
CS Limit Comparator Propagation Delay to NDRV		10mV overdrive (including leading-edge blanking time)		100		ns
CS Input Current	I_{CS}	0 ≤ V_{CS} ≤ 0.35V	-1.3		+0.5	µA
ERROR AMPLIFIER						
OUT_ Regulation Voltage		V_{DIM} = 5V	0.9	1	1.1	V
Transconductance	Gm		340	600	880	µS
No-Load Gain	A	(Note 4)		50		dB
COMP Sink Current	I_{SINK}	V_{DIM} = $V_{OUT\_}$ = 5V, V_{COMP} = 3V		400	800	µA
COMP Source Current	I_{SOURCE}	V_{DIM} = 5V, $V_{OUT\_}$ = V_{COMP} = 0V		400	800	µA
MOSFET DRIVER						
NDRV On-Resistance		I_{SINK} = 100mA, V_{IN} > 5.5V		1.5	4	Ω
		I_{SOURCE} = 100mA, V_{IN} > 5.5V		1.5	4	Ω
POWER MOSFET						
Power Switch On-Resistance		I_{SWITCH} = 0.5A, V_{GS} = 5V		0.15	0.35	Ω
Switch Leakage Current		V_{DRAIN} = 40V, V_{GATE} = 0V		0.003	1.2	µA
Switch Gate Charge		V_{DRAIN} = 40V, V_{GS} = 4.5V		3.1		nC

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, DRAIN, COMP, OUT_, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = T_J = -40ºC to +125°C, unless otherwise noted. Typical values are at T_A = 25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LED CURRENT SINKS							
OUT_ Current Range	$I_{OUT\_}$	V_{DIM} = 5V, $V_{OUT\_}$ = 1.0V		20		150	mA
LED Strings Current Matching		$I_{OUT\_}$ = 100mA, R_{ISET} = 15kΩ				±2	%
Output Current Accuracy		$I_{OUT\_}$ = 100mA, R_{ISET} = 15kΩ	T_A = +25ºC	97	100	103	mA
			T_A = -40ºC to +125ºC	95	100	105	mA
		$I_{OUT\_}$ = 20mA, R_{ISET} = 75kΩ	T_A = -40ºC to +125ºC	18.7	20	21.3	mA
OUT_ Leakage Current		V_{DIM} = 0V, $V_{OUT\_}$ = 40V			1	300	nA
Current Foldback Threshold Voltage					1.23		V
CFB Input Bias Current		0 ≤ V_{CFB} ≤ 1.3V		-0.3		+0.3	µA
ENABLE COMPARATOR (EN)							
Enable Threshold	V_{ENHI}	V_{EN} rising		1.1	1.24	1.34	V
Enable Threshold Hysteresis	V_{EN_HYS}				71		mV
Enable Input Current		V_{EN} = 40V		-500	+50	+700	nA
DIM LOGIC							
DIM Input Logic-High	V_{IH}			2.1			V
DIM Input Logic-Low	V_{IL}					0.8	V
Hysteresis	V_{DIM_HYS}				110		mV
DIM Input Current	I_{DIM}	V_{DIM} = 5V or 0		-600		+100	nA
DIM to LED Turn-On Time		V_{DIM} rising edge to 90% of set current		50	290	1000	ns
DIM to LED Turn-Off Time		V_{DIM} falling edge to 10% of set current			50		ns
$I_{OUT\_}$ Rise Time	t_R	Rise time measured from 10% to 90%			120	600	ns
$I_{OUT\_}$ Fall Time	t_F	Fall time measured from 90% to 10%			50	500	ns
LED FAULT DETECTION							
LED Shorted Fault Indicator Threshold				3.1		5.5	V
		T_A = +125ºC		3.55	4.2	4.85	
LED String Shorted Shutoff Threshold				6		9.5	V
		T_A = +125ºC		6.8	7.7	8.6	
Shorted LED Detection FLAG Delay					6		µs

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, DRAIN, COMP, OUT_, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = T_J = -40ºC to +125°C, unless otherwise noted. Typical values are at T_A = 25°C.) (Note 2)

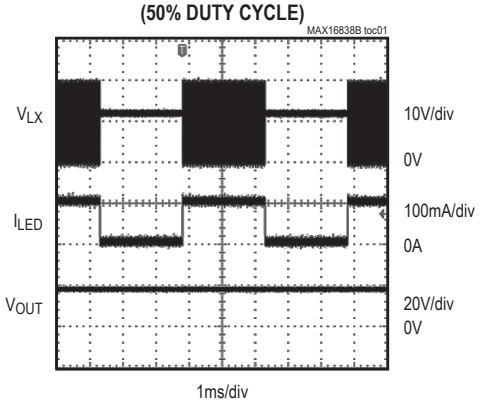
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FLT}$ LOGIC						
Output-Voltage Low	V_{OL}	V_{IN} = 4.75V and I_{SINK} = 5mA			0.4	V
Output Leakage Current		$V_{\overline{FLT}}$ = 5.5V	-1		+1	µA
OVERVOLTAGE PROTECTION						
OV Trip Threshold		V_{OV} rising	1.19	1.23	1.265	V
OV Hysteresis				70		mV
OV Input Bias Current		0 ≤ V_{OV} ≤ 1.3V	-100		+100	nA
THERMAL SHUTDOWN						
Thermal Shutdown				165		ºC
Thermal Shutdown Hysteresis				15		ºC

Note 2: All devices are 100% tested at T_A = +125ºC. Limits over temperature are guaranteed by design, not production tested.
Note 3: The shutdown current does not include currents in the OV and CFB resistive dividers.
Note 4: Gain = $\Delta V_{COMP}/\Delta V_{CS}$, 0.05V < V_{CS} < 0.15V.

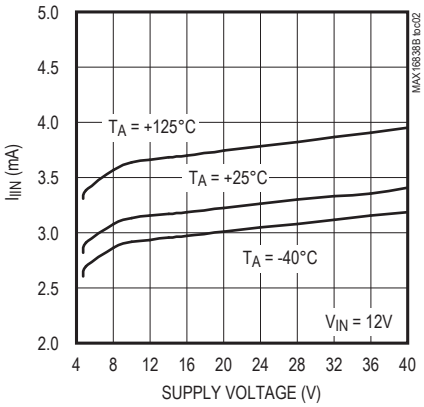
Typical Operating Characteristics

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, V_{DRAIN} = V_{COMP} = $V_{OUT\_}$, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = +25°C, unless otherwise noted.)

SWITCHING WAVEFORM AT 200Hz (50% DUTY CYCLE)



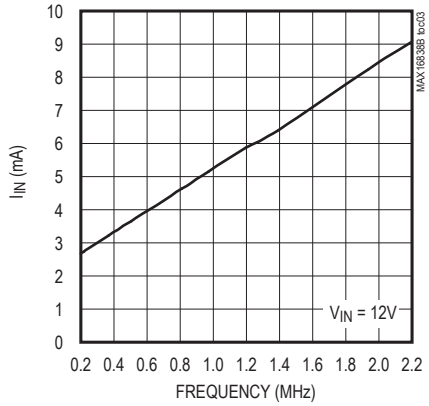
I_{IN} vs. SUPPLY VOLTAGE



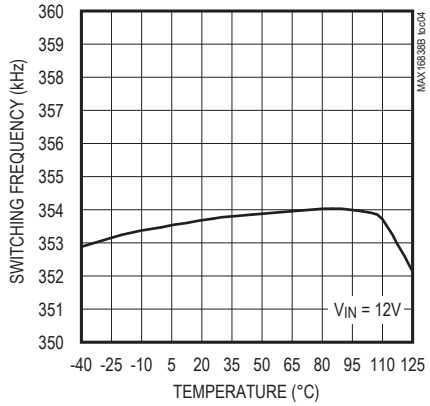
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, V_{DRAIN} = V_{COMP} = $V_{OUT\_}$, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = +25°C, unless otherwise noted.)

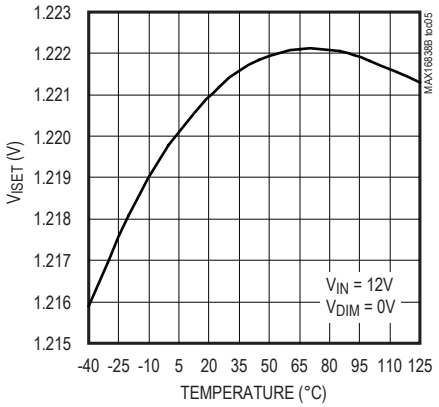
I_{IN} vs. FREQUENCY



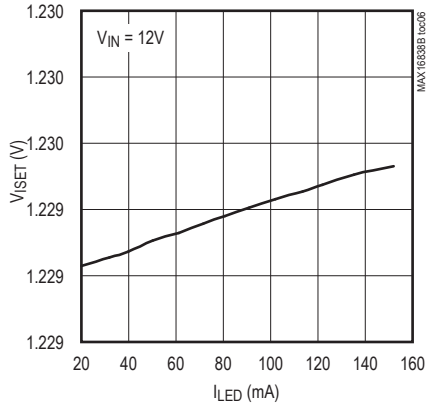
SWITCHING FREQUENCY vs. TEMPERATURE



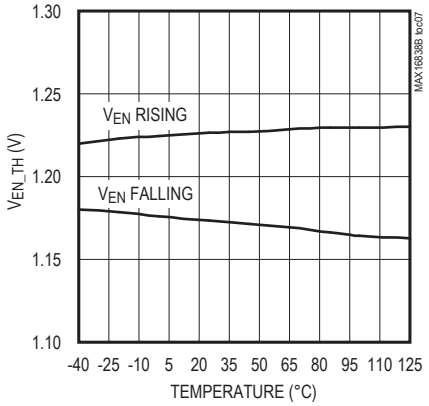
V_{ISET} vs. TEMPERATURE



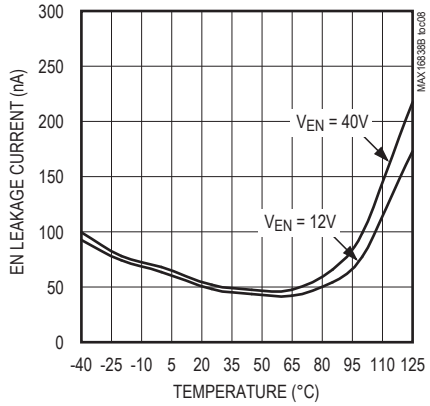
V_{ISET} vs. I_{LED}



V_{EN_TH} vs. TEMPERATURE



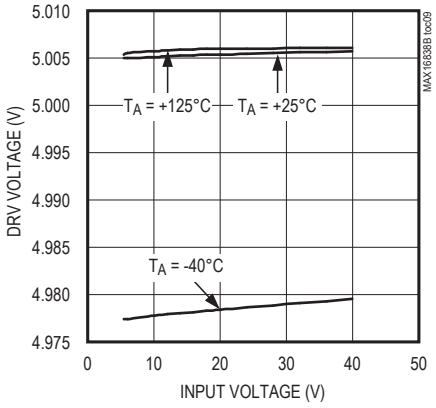
EN LEAKAGE CURRENT vs. TEMPERATURE



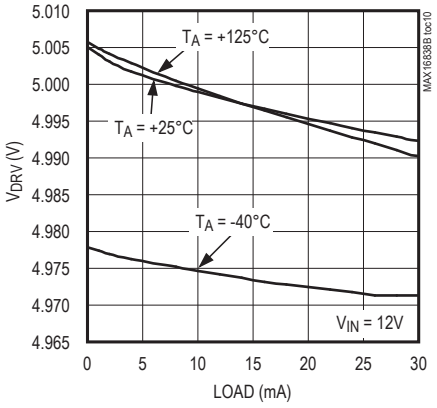
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, V_{DRAIN} = V_{COMP} = $V_{OUT\_}$, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = +25°C, unless otherwise noted.)

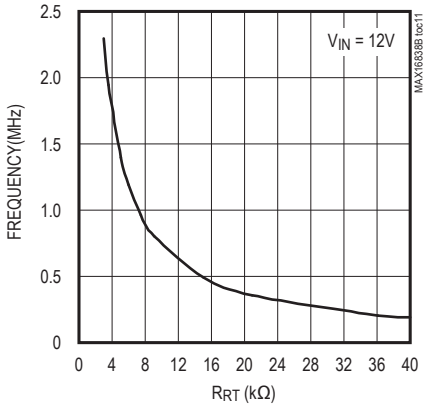
DRV LINE REGULATION



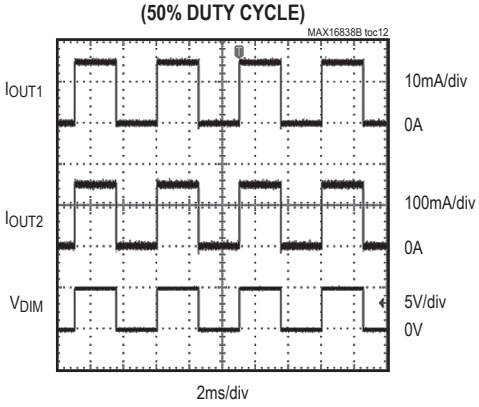
DRV LOAD REGULATION



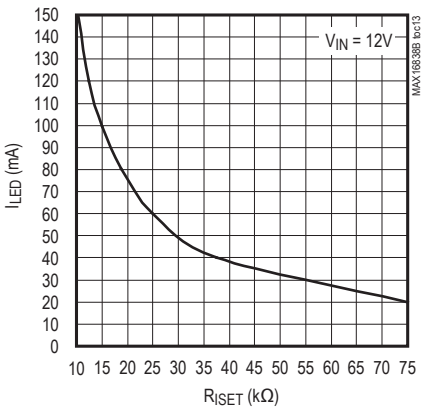
FREQUENCY vs. R_{RT}



LED SWITCHING WITH DIM AT 200Hz (50% DUTY CYCLE)



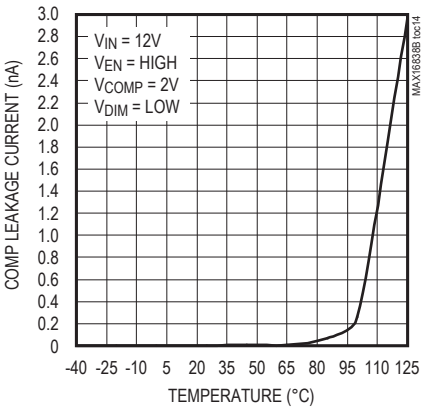
I_{LED} vs. R_{ISET}



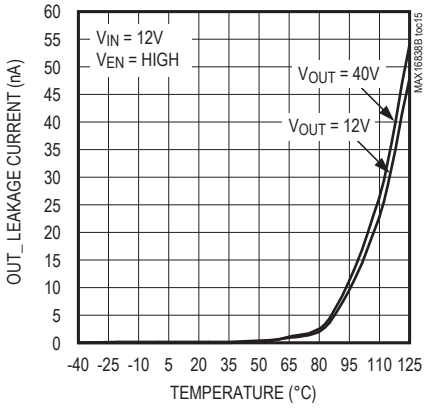
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.2kΩ, R_{ISET} = 15kΩ, C_{VCC} = 1µF, V_{CC} = V_{DRV} = V_{CFB}, V_{DRAIN} = V_{COMP} = $V_{OUT\_}$, $\overline{FLT}$ = unconnected, V_{OV} = V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, V_{GATE} = V_{NDRV}, T_A = +25°C, unless otherwise noted.)

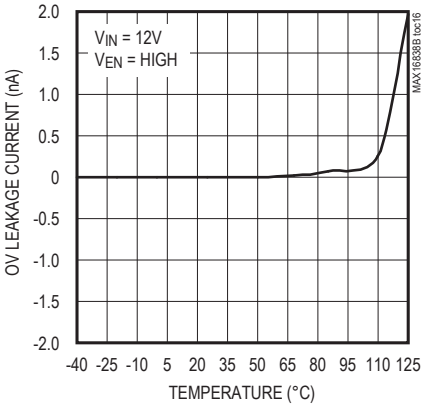
COMP LEAKAGE CURRENT vs. TEMPERATURE



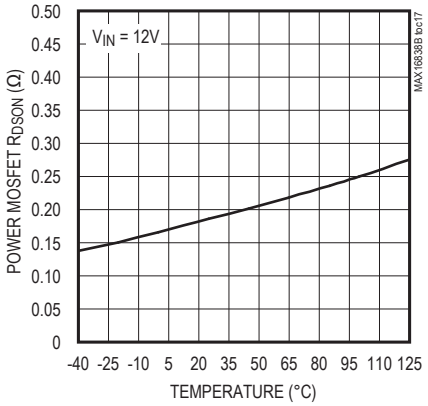
OUT_ LEAKAGE CURRENT vs. TEMPERATURE



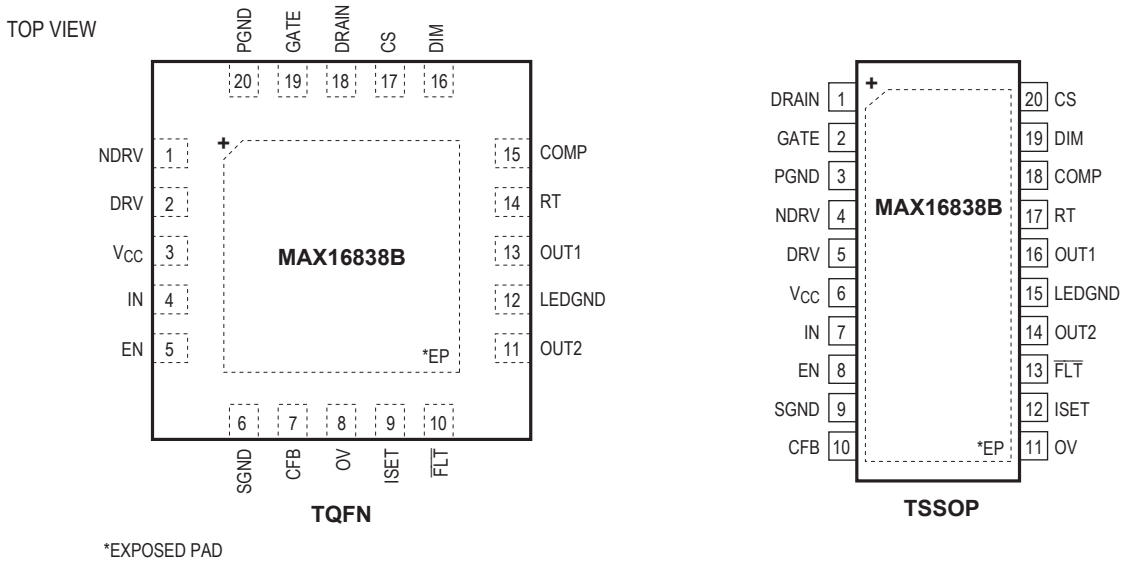
OV LEAKAGE CURRENT vs. TEMPERATURE



POWER MOSFET R_{DSON} vs. TEMPERATURE



Pin Configurations



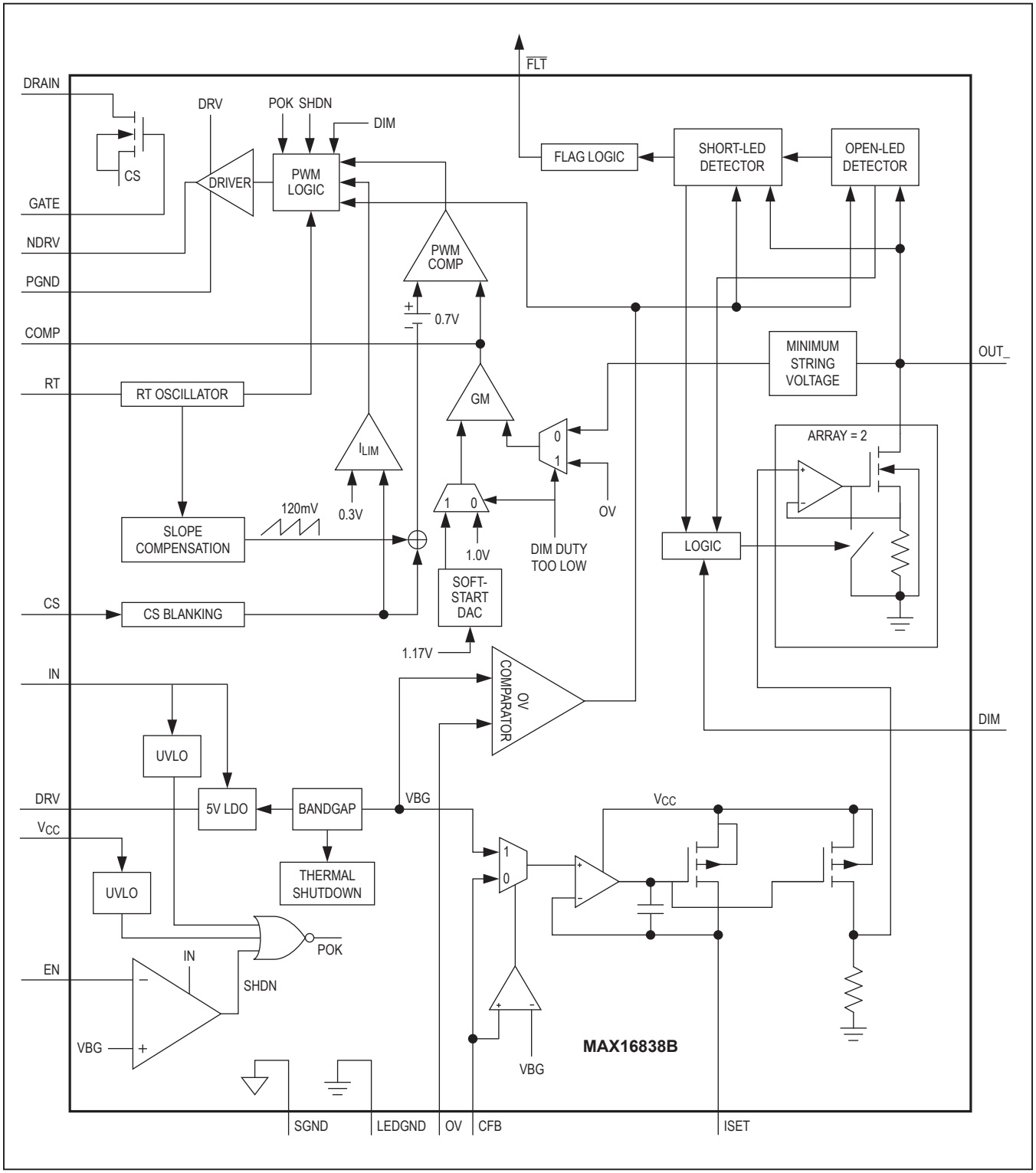
Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	4	NDRV	Gate Drive for Switching MOSFET. Connect NDRV to GATE directly or through a resistor to control the rise and fall times of the gate drive.
2	5	DRV	5V Regulator Output. MOSFET gate-driver supply input. Bypass DRV to PGND with a minimum of 1µF ceramic capacitor. Place the capacitor as close as possible to DRV and PGND.
3	6	V_{CC}	Internal Circuitry Supply Voltage. Bypass V_{CC} to SGND with a minimum of 0.1µF ceramic capacitor. Place the capacitor as close as possible to V_{CC} and SGND.
4	7	IN	Supply Input. Connect a 4.75V to 40V supply to IN. Bypass IN to PGND with a minimum of 1µF ceramic capacitor. For a 5V ±10% supply voltage, connect V_{IN} to V_{CC}.
5	8	EN	Enable/Undervoltage-Lockout (UVLO) Threshold Input. EN is a dual-function input. Connect EN to V_{IN} through a resistor-divider to program the UVLO threshold.
6	9	SGND	Signal Ground. SGND is the current return path connection for the low-noise analog signals. Connect SGND, LEDGND, and PGND at a single point.
7	10	CFB	Current Foldback Reference Input. Connect a resistor-divider between IN, CFB, and ground to set the current foldback threshold. When the voltage at CFB goes below 1.23V, the LED current starts reducing linearly. Connect to V_{CC} to disable the current foldback feature.
8	11	OV	Overvoltage Threshold Adjust Input. Connect a resistor-divider from the switching converter output to OV and SGND. The OV comparator reference is internally set to 1.23V.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
9	12	ISET	LED Current-Adjust Input. Connect a resistor (R_{ISET}) from ISET to SGND to set the current through each LED string (I_{LED}) according to the formula I_{LED} = 1512V/R_{ISET}.
10	13	$\overline{FLT}$	Open-Drain, Active-Low Flag Output. $\overline{FLT}$ asserts when there is an open/short-LED condition at the output or when there is a thermal shutdown event.
11	14	OUT2	LED String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 150mA.
12	15	LEDGND	LED Ground. LEDGND is the return path connection for the linear current sinks. Connect SGND, LEDGND, and PGND at a single point.
13	16	OUT1	LED String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT1. OUT1 sinks up to 150mA.
14	17	RT	Oscillator Timing Resistor Connection. Connect a timing resistor (R_{RT}) from RT to SGND to program the switching frequency. Apply an AC-coupled external clock at RT to synchronize the switching frequency with an external clock source.
15	18	COMP	Switching Converter Compensation Input. Connect an RC network from COMP to SGND (see the *Feedback Compensation* section).
16	19	DIM	Digital PWM Dimming Input
17	20	CS	Current-Sense Input. CS is the current-sense input for the switching regulator and is also connected to the source of the internal power MOSFET. Connect a sense resistor from CS to PGND to set the switching current limit.
18	1	DRAIN	Internal Switching MOSFET Drain Output
19	2	GATE	Internal Switching MOSFET Gate Input. Connect GATE to NDRV directly or through a resistor to control the rise and fall times of the gate drive. The switching MOSFET has a typical gate charge of 3.1nC.
20	3	PGND	Power Ground. PGND is the high-switching current return path connection. Connect SGND, LEDGND, and PGND at a single point.
—	—	EP	Exposed Pad. EP is internally connected to SGND. Connect EP to a large-area contiguous ground plane for effective power dissipation. Connect EP to SGND. Do not use as the only ground connection.

Simplified Functional Diagram



Detailed Description

The MAX16838B high-efficiency, HB LED driver integrates all the necessary features to implement a high performance backlight driver to power LEDs in small-to-medium-sized displays for automotive as well as general applications. The device provides load-dump voltage protection up to 40V in automotive applications. The device incorporates a DC-DC controller with peak current-mode control to implement a boost, coupled-inductor boost-buck, or SEPIC-type switched-mode power supply and a 2-channel LED driver with 20mA to 150mA constant-current-sink capability per channel. The MAX16838B can be combined with the MAX15054 to achieve boost-buck topology without a coupled inductor (see Figure 5).

The device features a constant-frequency peak current-mode control with internal slope compensation to control the duty cycle of the PWM controller. The DC-DC converter generates the required supply voltage for the LED strings from a wide input supply range. Connect LED strings from the DC-DC converter output to the 2-channel constant current sinks that control the current through the LED strings. A single resistor connected from ISET to ground sets the forward current through both LED strings.

The device features adaptive LED voltage control that adjusts the converter output voltage depending on the forward voltage of the LED strings. This feature minimizes the voltage drops across the constant-current sinks and reduces power dissipation in the device. The device provides a very wide PWM dimming range where a dimming pulse as narrow as 500ns is possible at a 200Hz dimming frequency.

A logic input (EN) shuts down the device when pulled low. The device includes an internal 5V LDO to power up the internal circuitry and drive the internal switching MOSFET.

The device includes output overvoltage protection that limits the converter output voltage to the programmed OV threshold in the event of an open-LED condition. The device also features an overtemperature protection that shuts down the controller if the die temperature exceeds +165°C. In addition, the MAX16838B has a shorted-LED string detection and an open-drain $\overline{FLT}$ signal to indicate open-LED, shorted-LED, and overtemperature conditions.

Features

Additional features of the MAX16838B include:

- Integrated, 2-Channel, 20mA to 150mA Linear LED Current Sinks
- Boost or SEPIC Power Topologies for Maximum Flexibility
- Adaptive Voltage Optimization to Minimize Power Dissipation in Linear Current Sinks
- 4.75V to 40V or 5V ±10% Input Operating Voltage Range
- 10,000:1 PWM Dimming at 200Hz
- Open-Drain Fault-Indicator Output
- LED Open/Short Detection and Protection
- Output Overvoltage and Overtemperature Protection
- Programmable LED Current Foldback at Lower Input Voltages
- 200kHz to 2MHz Resistor-Programmable Switching Frequency with External Synchronization
- Current-Mode Control Switching Stage with Internal Slope Compensation
- Enable Input
- Thermally Enhanced 20-Pin TSSOP (4.4mm) and TQFN (4mm x 4mm) Packages

Current-Mode DC-DC Controller

The device uses current-mode control to provide the required supply voltage for the LED strings. The internal MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensedfrom the voltage across the current-sense resistor (R_{CS}) connected from the source of the internal MOSFET to PGND. A PWM comparator compares the current-sense voltage plus the internal slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the internal MOSFET when the voltage at CS exceeds the error amplifier's output voltage. This process repeats every switching cycle to achieve peak current-mode control.

Error Amplifier

The internal error amplifier compares an internal feedback (FB) signal with an internal reference voltage (V_{REF}) and regulates its output to adjust the inductor current. An internal minimum string detector measures the minimum LED string cathode voltage with respect to SGND. During normal operation, this minimum $V_{OUT\_}$ voltage is regulated to 1V through feedback. The resulting DC-DC converter output voltage is 1V above the maximum required total LED voltage.

The converter stops switching when LED strings are turned off during PWM dimming. The error amplifier is disconnected from the COMP output to retain the compensation capacitor charge. This allows the converter to settle to a steady-state level immediately when the LED strings are turned on again. This unique feature provides fast dimming response without having to

use large output capacitors. If the PWM dimming on-pulse is less than five switching cycles, the feedback controls the voltage on OV such that the converter output voltage is regulated at 95% of the OV threshold. This mode ensures that narrow PWM dimming pulses are not affected by the response time of the converter. During this mode, the error amplifier remains continuously connected to the COMP output.

Adaptive LED Voltage Control

The device reduces power dissipation using an adaptive LED voltage-control scheme. The adaptive LED voltage control regulates the DC-DC converter output based on the operating voltage of the LED strings.

The voltage at each of the current-sink outputs (OUT_) is the difference between the DC-DC regulator output voltage (V_{LED}) and the total forward voltage of the LED string connected to the output (OUT_). The DC-DC converter then adjusts V_{LED} until the output channel with the lowest voltage at OUT_ is 1V relative to LEDGND. As a result, the device minimizes power dissipation in the current sinks and still maintains LED current regulation. For efficient adaptive control functionality, use an equal number of HB LEDs of the same forward-voltage rating in each string.

Current Limit

The device includes a fast current-limit comparator to terminate the on-cycle during an overload or a fault condition. The current-sense resistor (R_{CS}) connected between the source of the internal MOSFET and ground sets the current limit. The CS input has a 0.3V voltage trip level (V_{CS}). Use the following equation to calculate R_{CS}:

$$R_{CS} = (V_{CS})/I_{PEAK}$$

where I_{PEAK} is the peak current that flows through the MOSFET.

Undervoltage Lockout

The device features two undervoltage lockouts: $UVLO_{IN}$ and $UVLO_{VCC}$. The undervoltage-lockout threshold for V_{IN} is 4.3V (typ) and the undervoltage-lockout threshold for V_{CC} is 4V (typ).

Soft-Start

The device features a soft-start that activates during power-up. The soft-start ramps up the output of the converter in 64 steps in a period of 100ms (typ), unless both strings reach regulation point, in which case the soft-start would terminate to resume normal operation immediately. Once the soft-start is over, the internal soft-start circuitry is disabled and the normal operation begins.

Oscillator Frequency/External Synchronization

The device's oscillator frequency is programmable between 200kHz and 2MHz using one external resistor (R_{RT}) connected between RT and SGND. The PWM MOSFET driver output switching frequency is the same as the oscillator frequency. The oscillator frequency is determined using the following formula:

$$f_{SW} = (7.342 \times 10^9/R_{RT})(Hz)$$

where R_{RT} is in Ω.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the R_{RT} input. The capacitor used for the AC-coupling should satisfy the following relation:

$$C_{SYNC} \le \left(\frac{9.862}{R_{RT}} - 0.144 \times 10^{-3}\right)(\mu F)$$

where R_{RT} is in Ω.

The pulse width for the synchronization signal should satisfy the following relations:

$$\frac{t_{PW}}{t_{CLK}} V_S < 0.8$$

$$\left(0.8 - \frac{t_{PW}}{t_{CLK}} V_S\right) + V_S > 3.4$$

where t_{PW} is the synchronization source pulse width, t_{CLK} is the synchronization clock time period, and V_S is the synchronization pulse voltage level. See Figure 1.

5V LDO Regulator (DRV)

The internal LDO regulator converts the input voltage at IN to a 5V output voltage at DRV. The LDO regulator output supports up to 30mA current, enough to provide power to the internal control circuitry and the gate driver.

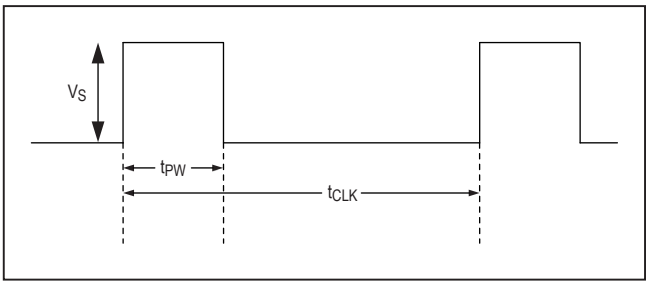


Figure 1. Synchronizing External Clock Signal

Connect a 4.7Ω resistor from V_{CC} to DRV to power the rest of the chip from the V_{CC} pin with the 5V internal regulator. Bypass DRV to PGND with a minimum of 1µF ceramic capacitor as close as possible to the device. For input voltage range of 4.5V to 5.5V, connect IN to V_{CC}.

LED Current Control (ISET)

The device features two identical constant-current sources used to drive multiple HB LED strings. The current through each of the channels is adjustable between 20mA and 150mA using an external resistor (R_{ISET}) connected between ISET and SGND. Select R_{ISET} using the following formula:

$$R_{ISET} = \frac{1512}{I_{OUT\_}}(\Omega)$$

where $I_{OUT\_}$ is the desired output current for both channels in amps.

For single-channel operation, connect channel 1 and channel 2 together. See Figure 2.

LED Dimming Control

The device features LED brightness control using an external PWM signal applied at DIM. The device accepts a minimum pulse width of 500ns. Therefore, a 10,000:1 dimming ratio is achieved when using a PWM frequency of 200Hz. Drive DIM high to enable both LED current sinks and drive DIM low to disable both LED current sinks.

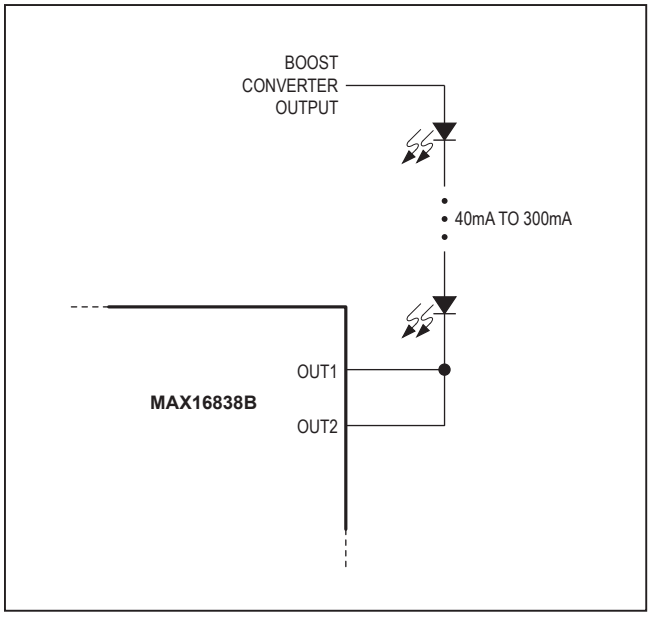


Figure 2. Configuration for Higher LED String Current

The duty cycle of the PWM signal applied to DIM also controls the DC-DC converter's output voltage. If the turn-on duration of the PWM signal is less than 20 oscillator clock cycles (DIM pulse width decreasing), then the boost converter regulates its output based on feedback from the OV input. During this mode, the converter output voltage is regulated to 95% of the OV threshold voltage. If the turn-on duration of the PWM signal is greater than or equal to 24 oscillator clock cycles (DIM pulse width increasing), then the converter regulates its output such that the minimum voltage at OUT_ is 1V.

Fault Protections

The device's fault protections include cycle-by-cycle current limiting, DC-DC converter output overvoltage protection, open-LED detection, short-LED detection, and overtemperature detection. An open-drain LED fault flag output ($\overline{FLT}$) goes low when an open-LED/short-LED or overtemperature condition is detected.

Open-LED Management and Overvoltage Protection

The device monitors the drains of the current sinks (OUT_) to detect any open string. If the voltage at any output falls below 300mV and the OV threshold is triggered (i.e., even with OUT_ at the OV voltage the string is not able to regulate above 300mV), then the device interprets that string to be open, asserts $\overline{FLT}$, and disconnects that string from the operation loop. The device features an adjustable overvoltage-threshold input (OV). Connect a resistor-divider from the switching converter output to OV and SGND to set the overvoltage-threshold level. Use the following formula to program the overvoltage threshold:

$$V_{OV} = 1.23V \times \left(1 + \frac{R2_{OV}}{R1_{OV}}\right)$$

Open-LED detection is disabled when PWM pulse width is less than 20 switching clock cycles (DIM pulse width decreasing).

Short-LED Detection

The device features two-level short-LED detection circuitry. If a level 1 short is detected on any one of the strings, $\overline{FLT}$ is asserted. A level 1 short is detected if the difference between the total forward LED voltages of the two strings exceeds 4.2V (typ). If a level 2 short is detected on any one of the strings, the particular LED string with the short is turned off after 6µs and $\overline{FLT}$ is asserted. A level 2 short is detected if the difference between the total forward LED voltages of the two strings exceeds 7.8V (typ). The strings are reevaluated on each DIM rising edge and $\overline{FLT}$ is deasserted if the short is removed. Short-LED detection is disabled when PWM pulse width

is less than 20 switching clock cycles (DIM pulse width decreasing).

Enable (EN)

EN is a logic input that completely shuts down the device when connected to logic-low, reducing the current consumption of the device to less than 15µA (typ). The logic threshold at EN is 1.24V (typ). The voltage at EN must exceed 1.24V before any operation can commence. There is a 71mV hysteresis on EN. The EN input also allows programming the supply input UVLO threshold using an external voltage-divider to sense the input voltage, as shown in Figure 3. Use the following equation to calculate the value of $R1_{EN}$ and $R2_{EN}$ in Figure 3:

$$R1_{EN} = \left(\frac{V_{ON}}{V_{UVLOIN}} - 1\right) \times R2_{EN}$$

where V_{UVLOIN} is the EN rising threshold (1.24V) and V_{ON} is the desired input startup voltage. Choose an $R2_{EN}$ between 10kΩ and 50kΩ. Connect EN to IN if not used.

Current Foldback

The device includes a current-foldback feature to limit the input current at low V_{IN}. Connect a resistor-divider between IN, CFB, and SGND to set the current-foldback threshold. When the voltage at CFB goes below 1.23V, then the LED current starts reducing proportionally to V_{CFB}.

This feature can also be used for analog dimming of the LEDs. Connect CFB to V_{CC} to disable this feature.

Applications Information

Boost-Circuit Design

First, determine the required input supply voltage range, the maximum voltage needed to drive the LED strings including the minimum 1V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}).

Calculate the maximum duty cycle (D_{MAX}) using the following equation:

$$D_{MAX} = (V_{LED} + V_D - V_{IN\_MIN})/(V_{LED} + V_D)$$

where V_D is the forward drop of the rectifier diode, V_{IN_MIN} is the minimum input supply voltage, and V_{LED} is the output voltage. Select the switching frequency (f_{SW}) depending on the space, noise, dynamic response, and efficiency constraints.

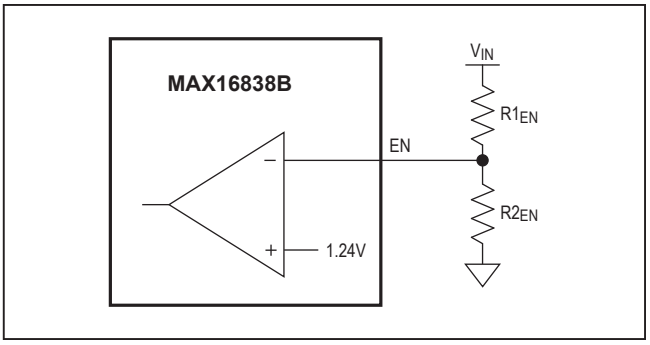


Figure 3. Setting the MAX16838B Undervoltage-Lockout Threshold

Inductor Selection in Boost Configuration

Select the maximum peak-to-peak ripple on the inductor current (IL_{P-P}). Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_{PEAK}):

$$IL_{AVG} = I_{LED}/(1 - D_{MAX})$$

Assuming IL_{P-P} is 40% of the average inductor current:

$$IL_{P-P} = IL_{AVG} \times 0.4$$

$$IL_{PEAK} = IL_{AVG} + IL_{P-P}/2$$

Calculate the minimum inductance value L_{MIN} with the inductor current ripple set to the maximum value:

$$L_{MIN} = V_{IN\_MIN} \times D_{MAX}/(f_{SW} \times IL_{P-P})$$

Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_{PEAK}. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current. The IL_{P-P} can be chosen to have a higher ripple than 40%. Adjust the minimum value of the inductance according to the chosen ripple. One fact that must be noted is that the slope compensation is fixed and has a 120mV peak per switching cycle. The dv/dt of the slope-compensation ramp is $120f_{SW}$V/µs, where f_{SW} is in kHz. After selecting the inductance it is necessary to verify that the slope compensation is adequate to prevent subharmonic oscillations. In the case of the boost, the following criteria must be satisfied:

$$120f_{SW} > R_{CS} (V_{LED} - 2V_{IN\_MIN})/2L$$

where L is the inductance value in µH, R_{CS} is the current-sense resistor value in Ω, V_{IN_MIN} is the minimum input voltage in V, V_{LED} is the output voltage, and f_{SW} is the switching frequency in kHz.

If the inductance value is chosen to keep the inductor in discontinuous-conduction mode, the equation above does not need to be satisfied.

Output Capacitor Selection in Boost Configuration

For the boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at higher duty cycles.

Calculate the output capacitor (C_{OUT}) using the following equation:

$$C_{OUT} > (D_{MAX} \times I_{LED})/(V_{LED\_P-P} \times f_{SW})$$

where V_{LED_P-P} is the peak-to-peak ripple in the LED supply voltage. Use a combination of low-ESR and high-capacitance ceramic capacitors for lower output ripple and noise.

Input Capacitor Selection in Boost Configuration

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor C_{IN} using the following equation:

$$C_{IN} = IL_{P-P}/(8 \times f_{SW} \times V_{IN\_P-P})$$

where V_{IN_P-P} is the peak-to-peak input ripple voltage. This equation assumes that input capacitors supply most of the input ripple current.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that calculated in the following equation:

$$I_D = IL_{AVG} (1 - D_{MAX}) (A)$$

Feedback Compensation

The voltage-feedback loop needs proper compensation for stable operation. This is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to SGND. R_{COMP} is chosen to set the high-frequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. For optimum performance, choose the components using the following equations:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED}}{5 \times FP1 \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

where

$$f_{ZRHP} = \frac{V_{LED}(1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

is the right-half plane zero for the boost regulator.

R_{CS} is the current-sense resistor in series with the source of the internal switching MOSFET. I_{LED} is the total LED current that is the sum of the LED currents in both the channels. V_{LED} is the output voltage of the boost regulator. D_{MAX} is the maximum duty cycle that occurs at minimum input voltage. GM_{COMP} is the transconductance of the error amplifier.

$$FP1 = \frac{I_{LED}}{2 \times \pi \times V_{LED} \times C_{OUT}}$$

is the output pole formed by the boost regulator.

Set the zero formed by R_{COMP} and C_{COMP} a decade below the crossover frequency. Using the value of R_{COMP} from above, the crossover frequency is at $f_{ZRHP}/5$:

$$C_{COMP} = \frac{50}{2\pi \times R_{COMP} \times f_{ZRHP}}$$

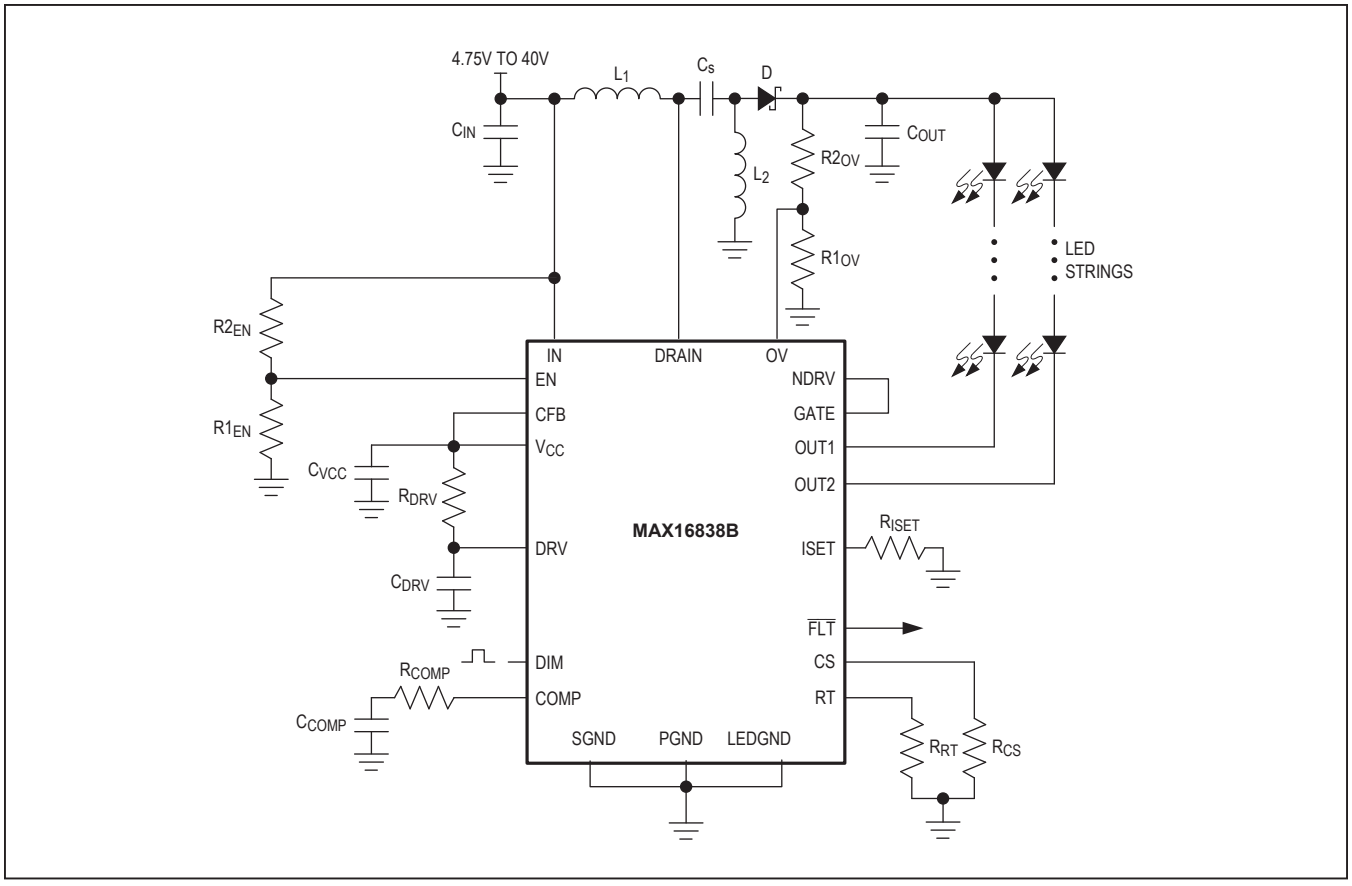


Figure 4. SEPIC Configuration

SEPIC Operation

Figure 4 shows a SEPIC application circuit using the MAX16838B. The SEPIC topology is necessary to keep the output voltage of the DC-DC converter regulated when the input voltage can rise above and drop below the output voltage.

Boost-Buck Configuration

Figure 5 shows a boost-buck configuration with the MAX16838B and MAX15054.

PCB Layout Considerations

LED driver circuits based on the MAX16838B device use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure proper operation. The switching-converter part of the circuit has nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit. Follow these guidelines to reduce noise as much as possible:

1) Connect the bypass capacitor on V_{CC} and DRV as close as possible to the device, and connect the capacitor ground to the analog ground plane using vias close to the capacitor terminal. Connect SGND of the device to the analog ground plane using a via close to SGND. Lay the analog ground plane on the inner layer, preferably next to the top layer. Use the analog ground plane to cover the entire area under critical signal components for the power converter.
2) Have a power-ground plane for the switching-converter power circuit under the power components (input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power-ground plane as close as possible to PGND. Connect all other ground connections to the power-ground plane using vias close to the terminals.

3) There are two loops in the power circuit that carry high-frequency switching currents. One loop is when the MOSFET is on—from the input filter capacitor positive terminal, through the inductor, the internal MOSFET, and the current-sense resistor, to the input capacitor negative terminal. The other loop is when the MOSFET is off—from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal. Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power-ground plane for the switching currents on the top-layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.

4) Connect the power-ground plane for the constant-current LED driver part of the circuit to LEDGND as close as possible to the device. Connect SGND to PGND at the same point.

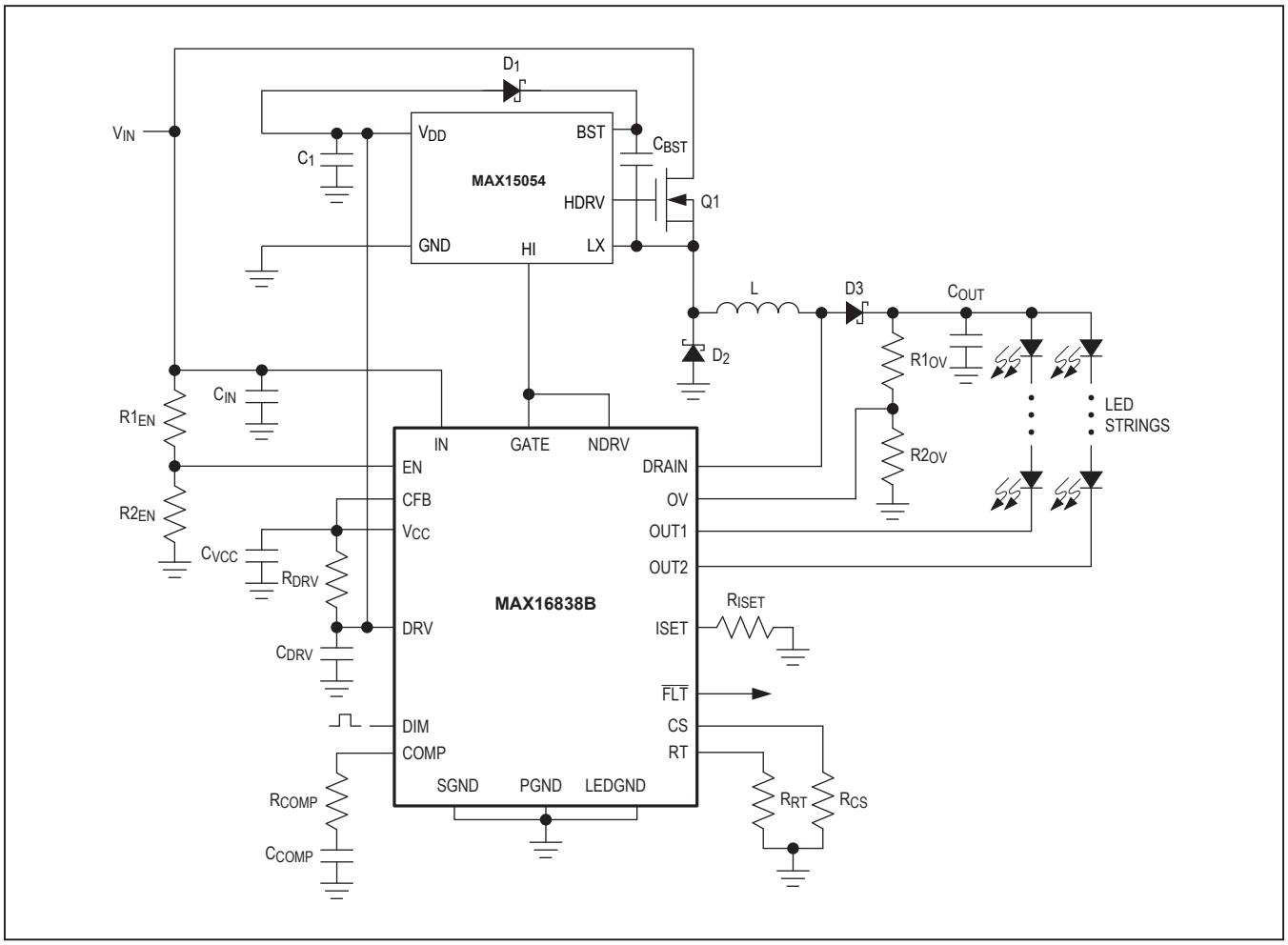
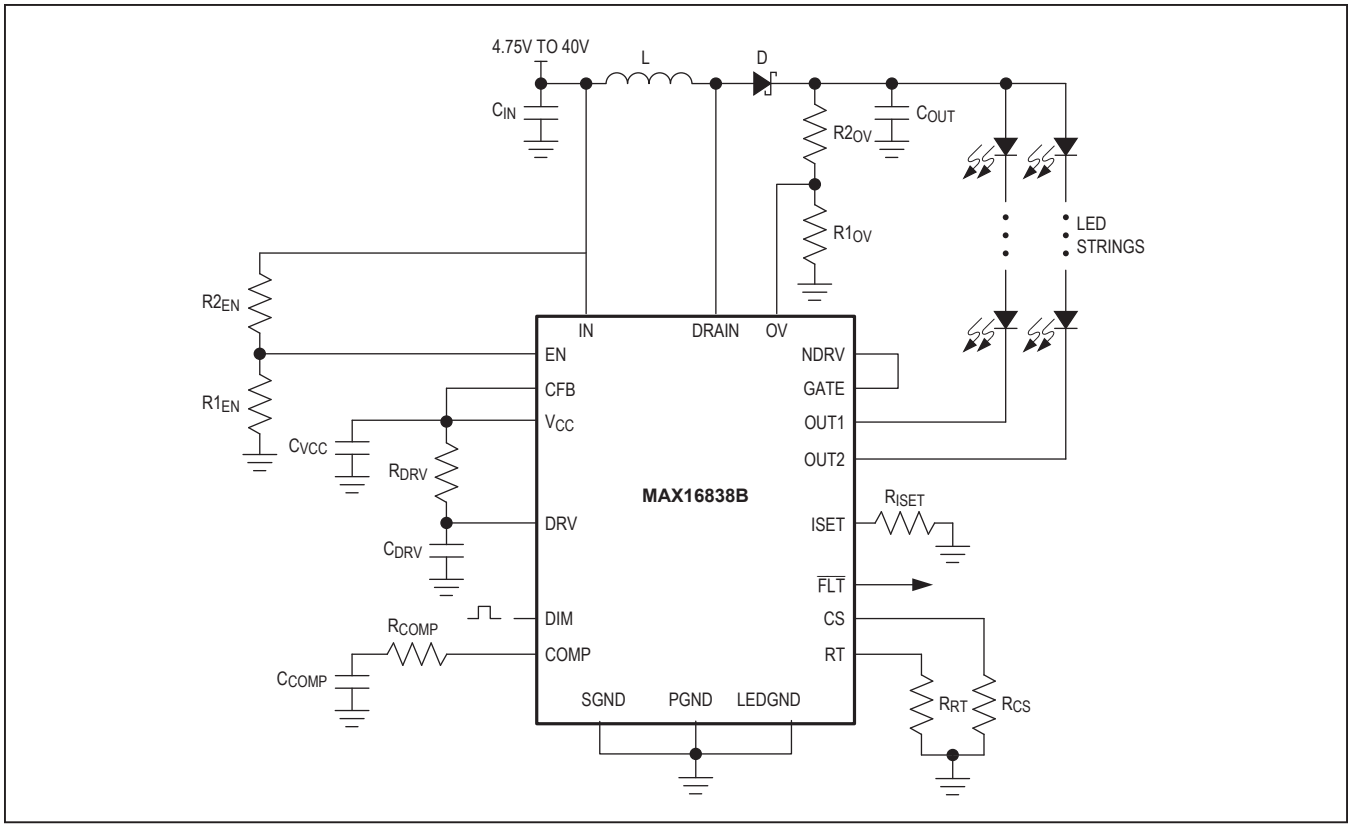


Figure 5. Boost-Buck Configuration

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16838BATP/V+*	-40ºC to +125ºC	20 TQFN-EP**
MAX16838BAUP/V+	-40ºC to +125ºC	20 TSSOP-EP**

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product*—contact factory for availability.
***EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS DMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2044+3	21-0139	90-0037
20 TSSOP-EP	U20E+1	21-0108	90-0114

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/14	Initial release	—
1	12/14	Widened spec for $\overline{FLT}$ output leakage current in *Electrical Characteristics* table	5

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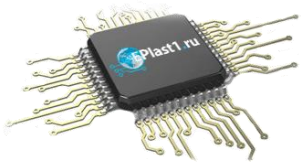
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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