# SMART SLAVE IC WITH INTEGRATED CURRENT AND TEMPERATURE SENSORS

| Device Type | Operating Current | Input Voltage |
|---|---|---|
| VT1697SB | 55A Per Phase | 8.5V to 14.0V |

The VT1697SB is a feature-rich smart slave IC designed to work with Maxim's seventh-generation masters to implement a high-density multiphase voltage regulator. Up to six smart slave ICs, plus a master IC, provide a compact synchronous buck converter that includes accurate individual phase-current and temperature reporting via SMBus/PMBus. This smart slave device includes protection circuits for overtemperature, VX short, all power supplies UVLO faults and main power supply OVLO fault. If a fault is detected, the slave IC will immediately shut down and send a fault signal to the master IC.

Monolithic integration and advanced packaging technologies allow practical per-phase, high switching frequencies with significantly lower losses than alternative implementations. Smart slave devices are designed to support phase-shedding and DCM modes for efficiency optimization over a wide range of load currents. High per-phase current-capability designs with low $C_{OUT}$ enable a design with fewer phases and a smaller footprint.

The VT1697SB is packaged in a QFN package with exposed top-side thermal pads. Top-side cooling allows improved heat transfer to ambient and reduces PC board and component temperatures.
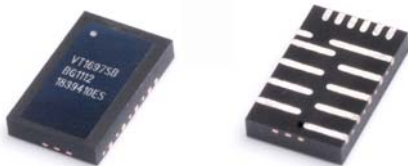
## FEATURES AND BENEFITS

- Increased Power Density with Fewer External Components
  - Monolithic Integration For Reduced Parasitics
  - 4-Phase Scalable Architecture Compatible with Coupled Inductors
  - 94% Peak Efficiency
  - Top-Side Cooling For Improved Heat Transfer To Ambient
- Accurate Telemetry and Monitoring Provides Real-Time Reporting of Critical Parameters
  - PMBus Compliant Interface via Master Controller for Telemetry and Power Management
  - Junction Temperature Monitoring & Reporting
  - Per-Phase Current Reporting
- Advanced Self-Protection Features Protects System and IC
  - Overcurrent Protection
  - Overtemperature Protection
  - Boost Voltage UVLO
  - VX Short Protection

## APPLICATIONS

- Communication and Networking Equipment
- Servers and Storage Equipment
- High-Current Voltage Regulators
  - Networking ASICs
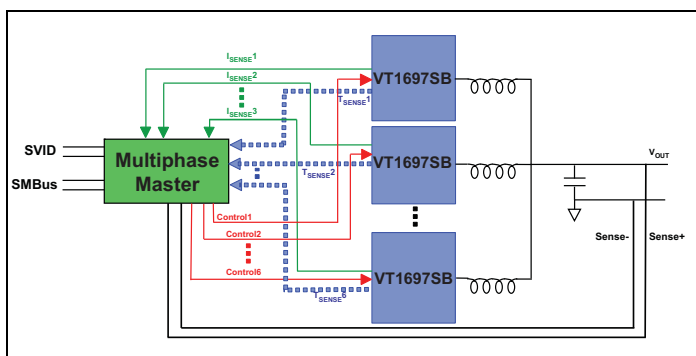  - FPGAs
  - Microprocessor Chipsets
  - Memory



**Figure 1:** Basic Application Circuit

# VT1697SB

## Ordering Information

| Part Number | Description | Package | Drawing Number | Shipping Method | Package Marking |
|---|---|---|---|---|---|
| **RoHS Compliant[3]** | | | | | |
| VT1697SBFQX | 55A smart slave Device | QFN-16 [Type G] | ES AP-2896 | 2.5ku Tape & Reel | VT1697SBF |

## ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage (12V)............................................-0.3V to 16V

Supply & Input Pin Voltages (1.8V) ...................-0.3V to 2.5V

Switching Node Voltage (VX) DC ........................-0.3V to 16V

Switching Node Voltage (VX) 25ns[2] .....................-10V to 23V

$V_{DDH}$ Pin - VX Pin Differential 25ns[4] ....................-10V to 23V

BST Pin (BST) DC...............................................-0.3V to 20V

BST Pin (BST) 25ns ...........................................-6.0V to 27V

BST Pin - VX Pin Differential ..........................................2.5V

Operating Junction Temperature ($T_J$) ...........................150°C

Storage Temperature Range  ..........................-65°C to 150°C

Peak Reflow Temperature..............................................260°C

## OPERATING RATINGS

$V_{DD}$, $V_{CC}$.......................................................... 1.71V to 1.98V

12V Supply ($V_{DDH}$) ........................................... 8.5V to 14.0V

Junction Temperature ($T_J$) ..............................-40°C to 125°C

Frequency (Fsw).......................................300kHz to 1.3MHz

## THERMAL RATINGS

VT1697SB $\Theta_{JC}$ Max .................................................0.42°C/W

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**Note 1:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** The 25ns rating is the allowable voltage that the VX node may exceed the -0.3V to 16V ratings in either positive or negative direction for up to 25ns per cycle.

**Note 3:** These products are completely Halogen-free and Pb-free, employing special materials sets: molding compounds/die attach materials and 100% matte tin plate including anneal. These products are RoHS compliant with an -e3 termination finish and are compatible with both SnPb and Pb-free soldering operations. These products are MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.

**Note 4:** The $V_{DDH}$ input pin voltage AC should not exceed 19V (25ns). This measurement is taken at the $V_{DDH}$ pin referenced to $V_{SS}$ pin immediately adjacent using a high frequency scope probe with $I_{LOAD}$ at $I_{MAX}$. A high-frequency input bypass capacitor must be located less than 60mils (1.524mm) from the $V_{DDH}$ pin and the Maxim device per our design guidelines.

# Electrical Characteristics

$V_{DD} = V_{CC} = 1.71V - 1.98V$, $V_{DDH} = 12V$. The ✶ symbol denotes specifications which apply over the following temperature range: $T_J = 0$ to 125°C, otherwise specifications are for $T_J = 25$°C. The # symbol denotes specifications which apply over the following temperature range: $T_J = -25$ to 125°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Voltages , Supply Current** | | | | | | |
| $V_{DD}$, $V_{CC}$ | Bias Supply Voltage | | 1.71 | | 1.98 | V |
| $V_{DDH}$ | Power Train Input Voltage | | 8.5 | 12.0 | 14.0 | V |
| $I_{CC} + I_{DD}$ | 1.8V Bias Supply Current | Shutdown (See Note 1) | | 0.5 | 2 | µA |
| | | Inactive, No Switching (See Note 2) | | 3.2 | 5.0 | mA |
| | | Load = 0A, $V_{OUT}$ = 1.8V, Fsw = 1.5MHz | | 43 | 61 | mA |
| | | Load = 0A, $V_{OUT}$ = 1.8V, Fsw = 300KHz | | 14 | 20 | mA |
| | | Load = 0A, $V_{OUT}$ = 1.8V, Fsw = 600KHz | | 29 | 41 | mA |
| $I_{DDH}$ | 12V Bias Supply Current | Shutdown (See Note 1) | | 1.3 | 10 | µA |
| | | Inactive, No Switching (See Note 2) | | 6.5 | 20 | µA |
| **$I_{RECON}$ Specification** | | | | | | |
| $A_I$ | Current gain ($I_L$ to $I_{SENSE}$) | -70A < $I_L$ < 70A | 95000 | 100000 | 105000 | A/A |
| **Temperature Sensor Specifications** | | | | | | |
| $T_{RANGE}$ | Temperature Sensor Dynamic Range | | 0 | | 150 | °C |
| $A_{TEMP}$ | Temperature Sensor Gain | | | 3.01 | | mV/°C |
| – | Temperature Sensor Voltage | $T_J = 0$°C | | 832 | | mV |
| **Protection Features** | | | | | | |
| $V_{DD\_UVLO}$ | $V_{DD}$ UVLO Threshold (Rising) | | 1.47 | 1.57 | 1.64 | V |
| | $V_{DD}$ UVLO Threshold (Falling) | | 1.41 | 1.5 | 1.58 | V |
| $V_{DDH\_OVLO}$ | $V_{DDH}$ OVLO Threshold (Rising) | | 15.48 | 16 | 16.41 | V |
| | $V_{DDH}$ OVLO Threshold (Falling) | | 14.95 | 15.5 | 15.81 | V |
| $V_{DDH\_UVLO}$ | $V_{DDH}$ UVLO Threshold (Rising) | | 4.05 | 4.27 | 4.40 | V |
| | $V_{DDH}$ UVLO Threshold (Falling) | | 3.90 | 4.09 | 4.25 | V |
| $V_{BST\_UVLO}$ | $V_{BST}$ UVLO Threshold (Rising) | Note 3 | 1.39 | 1.52 | 1.66 | V |
| | $V_{BST}$ UVLO Threshold (Falling) | Note 3 | 1.32 | 1.45 | 1.57 | V |
| OCP | Peak Positive OCP Clamp Level | | 59 | 67 | 80 | A |
| | Peak Positive OCP Clamp Delay | | | | 63 | ns |
| | Peak Positive OCP Shutdown Level | | 99 | 110 | 121 | A |
| | Peak Positive OCP Shutdown Delay | | | | 42 | ns |
| | Peak Negative OCP Clamp Level | | -79.1 | -71.9 | -64.7 | A |
| | Peak Negative OCP Delay | | | | 110 | ns |
| OTP | Overtemperature Shutdown | Rising Threshold | 140 | 150 | 165 | °C |
| **PWM Input** | | | | | | |
| $V_{IH}$ | Input Voltage, High State | | $V_{DD}$ - 0.20 | | | V |
| $V_{IL}$ | Input Voltage, Low State | | | | 0.20 | V |
| – | Tristate Control Threshold ($V_{IN}$ Rising) | | | 0.63 | | V |
| **TS_FAULTB Input** | | | | | | |
| $V_{IH}$ | TS_FAULTB Digital Threshold $V_{IH}$ | | 0.41 | | | V |
| $V_{IL}$ | TS_FAULTB Digital Threshold $V_{IL}$ | | | | 0.17 | V |

**Note 1:** $T_{SENSE}$, PWM and $I_{SENSE}$ pins of the slave are pulled LOW by the master. The slave is in this state before master OE is enabled.
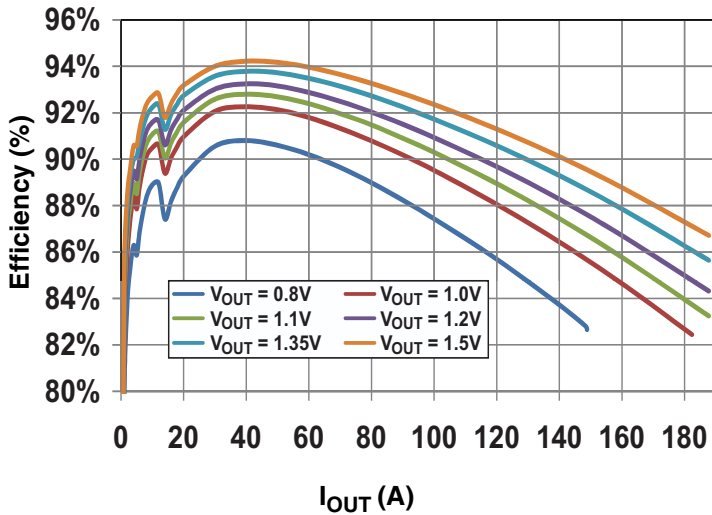**Note 2:** Inactive, no switching: PWM signal is tristated by the master. The slave is in this mode when the master sheds a phase (temporarily disabling this slave) to save power at lighter loads.
**Note 3:** $V_{BST\_UVLO}$ is measured with respect to VX and not from ground.
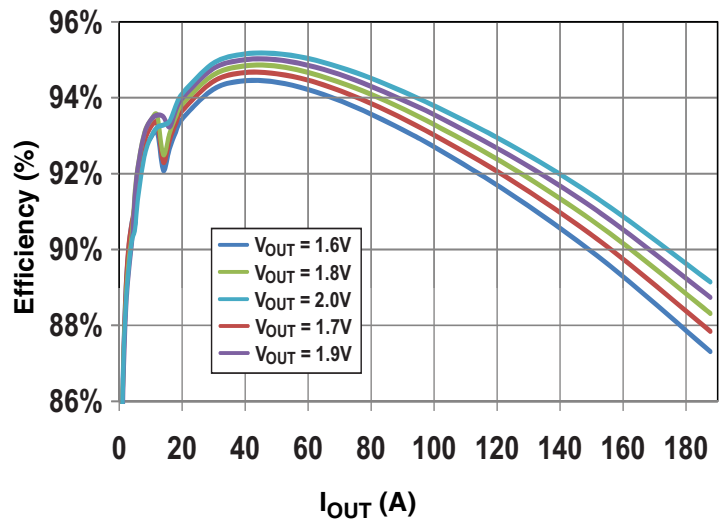
## Typical Operating Characteristics

Master: $T_A$ = 25°C; Fsw = 600kHz
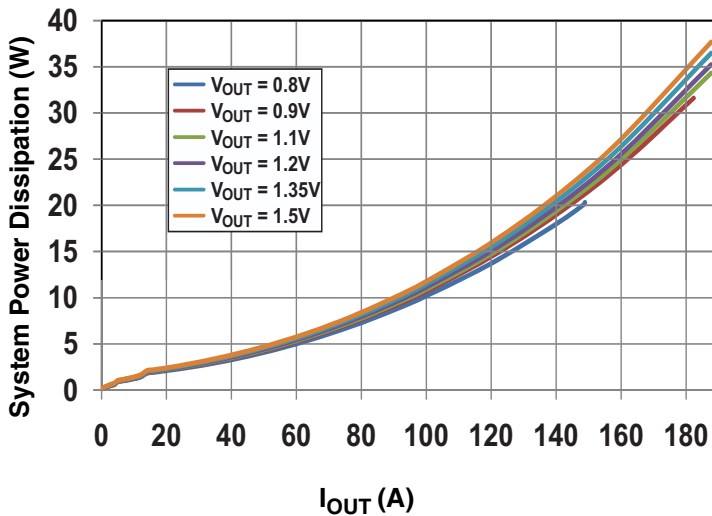
**Efficiency vs Load Current - 4 VT1697SB (VR12.0)**



Conditions: $V_{IN}$ = 12V
$V_{BIAS}$ = 1.8V
Inductor: CLB1108-4-50TR-R

**Efficiency vs Load Current - 4 VT1697SB (VR12.5)**
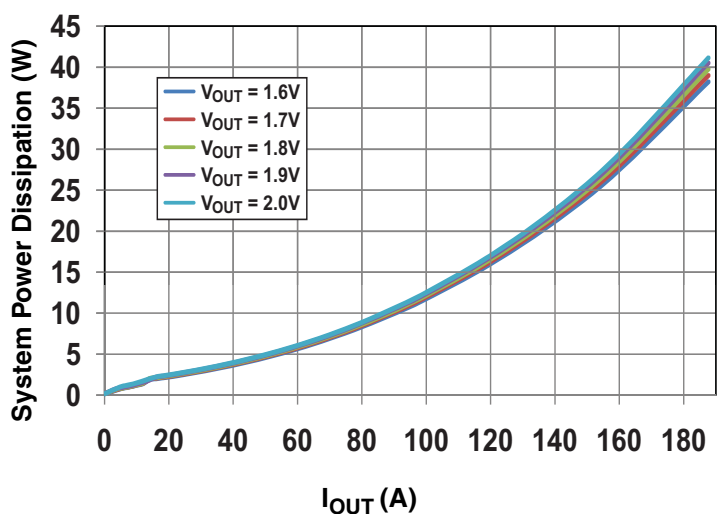


Conditions: $V_{IN}$ = 12V
$V_{BIAS}$ = 1.8V
Inductor: CLB1108-4-50TR-R

**System Power Dissipation - 4 VT1697SB (VR12.0)**



Conditions: $V_{IN}$ = 12V
$V_{BIAS}$ = 1.8V
Inductor: CLB1108-4-50TR-R

**System Power Dissipation - 4 VT1697SB (VR12.5)**



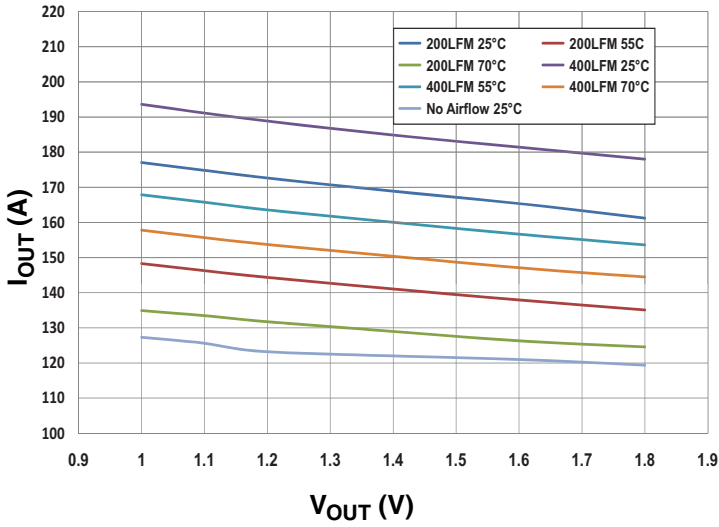Conditions: $V_{IN}$ = 12V
$V_{BIAS}$ = 1.8V
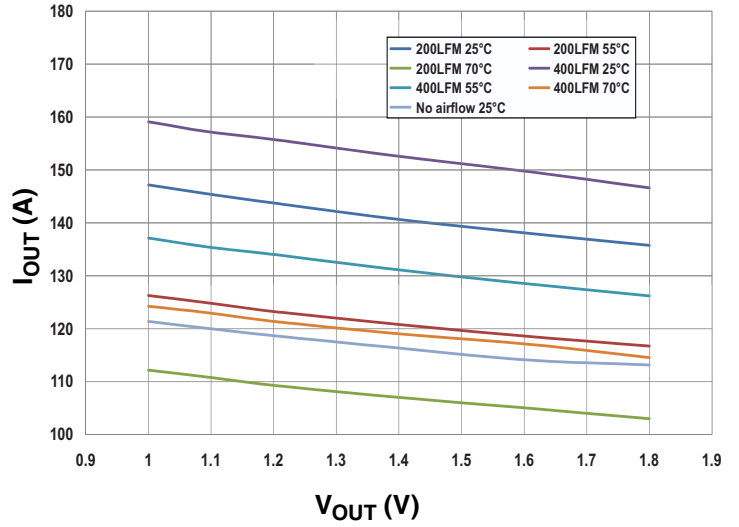Inductor: CLB1108-4-50TR-R

# Typical Operating Characteristics

Master: $T_A = 25°C$; Fsw = 600kHz

## VT1697SB 4-Phase Safe Operating Area (Heatsink)



Legend:
- 200LFM 25°C
- 200LFM 55C
- 200LFM 70°C
- 400LFM 25°C
- 400LFM 55°C
- 400LFM 70°C
- No Airflow 25°C

X-axis: $V_{OUT}$ (V), Y-axis: $I_{OUT}$ (A)

Conditions: $V_{IN}$ = 12V
$V_{BIAS}$ = 1.8V
Inductor: CL1108-4-50TR-R

## VT1697SB 4-Phase Safe Operating Area (No Heatsink)



Legend:
- 200LFM 25°C
- 200LFM 55C
- 200LFM 70°C
- 400LFM 25°C
- 400LFM 55°C
- 400LFM 70°C
- No airflow 25°C

X-axis: $V_{OUT}$ (V), Y-axis: $I_{OUT}$ (A)

Conditions: $V_{IN}$ = 12V
$V_{BIAS}$ = 1.8V
Inductor: CL1108-4-50TR-R
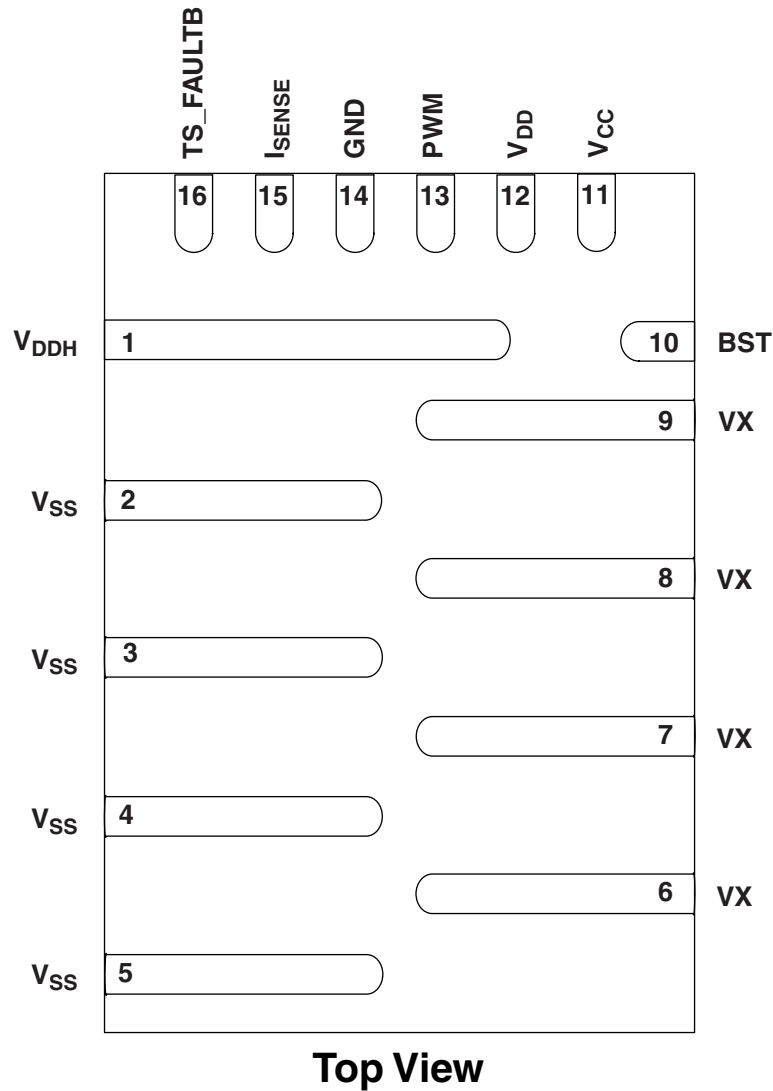
## Pinout and Block Diagrams



**Figure 2:** VT1697SB Pinout (QFN-16)

## PIN INFORMATION FOR VT1697SB SMART SLAVE DEVICE

$V_{DDH}$ (Pin 1): 12V input supply voltage node. This node connects to the 12V input power supply source. High-frequency decoupling capacitors must be placed in close proximity to the slave IC on the same side as the VT1697SB. See Table 2 for reference.

$V_{SS}$ (Pins 2-5): Power switch ground node. These nodes normally connect directly to the ground plane.

**VX** (Pins 6-9): Switching node. These nodes connect the switching node of the power devices to the output inductor.

**BST** (Pin 10): Bootstrap supply for high-side drivers.

$V_{CC}$ (Pin 11): 1.8V supply for low-side drivers.

$V_{DD}$ (Pin 12): 1.8V supply for control circuits.

**PWM** (Pin 13): PWM input node. Connect this node to the PWM output pin from the Master.

**GND** (Pin 14): Ground for control circuits.

$I_{SENSE}$ (Pin 15): Current sense output node. Connect this node to the current sense input of the Master through a simple passive filter.

**TS_FAULTB** (Pin 16): Temperature sense and fault output node. Connect this node to the temperature sense pin of the Master through a simple passive filter.
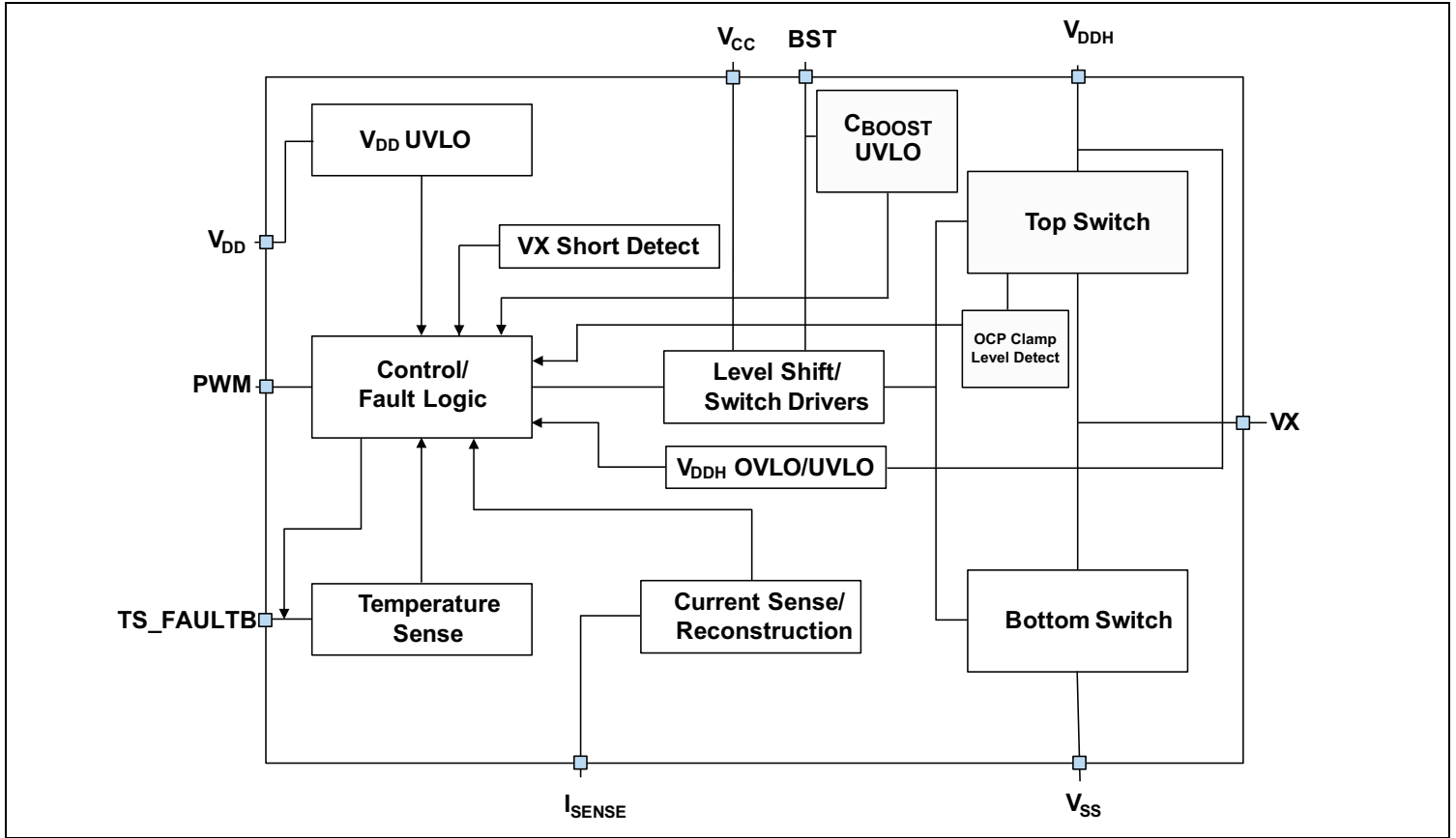
# Pinout and Block Diagrams



**Figure 3:** IC Block Diagram

# Theory of Operation

## VOLTAGE REGULATION

Maxim smart slave ICs provide the control logic, drivers, monitoring circuits and power semiconductors for a synchronous buck converter with fault protection, status monitoring and accurate lossless current sensing. Phases are controlled by the Master IC independently by separate phase control signals.

### Power Switch Control and Drivers

The smart slave ICs operate in conjunction with a Maxim Master IC. The Master controller will configure the voltage regulator based on its configuration resistors and the number of phases populated. The smart slave device's switching is controlled by the proprietary command signals on the phase control lines. The phase control signal has three defined states: high, low and a "tri-state". "Tri-state" is used for phase shedding and DCM modes. An external boost capacitor is required to supply the voltage for the high-side switch driver. VDD and VCC are brought out separately to allow separate decoupling to improve noise immunity on the VDD rail.

### Current Sense Output

The integrated lossless current sense (or "current reconstruction") produces a precise ratiometric current sense signal for both positive and negative currents which is sent to the master as an analog current signal. This current sense technology provides accurate current information over load and temperature that is not affected by tolerances of passive elements such as the output inductor, resistors and capacitors.

### Phase Configuration

The ability for the Master to dynamically disable and re-enable a phase is an integral part of the Maxim Master/Slave architecture. The Master sets the phase control signal to "tri-state" to disable a phase. The same state is used to control DCM operation. When using a coupled inductor, a proprietary mode (Coupled Inductor Mode) may be set by the master and communicated to the smart slave via the phase control signal to minimize losses due to coupled currents in inactive phases.

## PROTECTION CIRCUITS

### Overcurrent Protection

The smart slave ICs incorporate instantaneous overcurrent fault protection using the lossless current sense/reconstruction. This overcurrent protection is separate from the system overcurrent protection, and is intended to operate only in extreme fault conditions to protect the IC and other components. The system overcurrent protection set by the master should be set with sufficient margin below the individual Slave's threshold to ensure correct system operation.

For current sourcing operation, if the instantaneous current in the top switch (based on the current sense/reconstruction circuit) exceeds the overcurrent protection value shown in the Electrical Characteristics table, the slave will regulate the period of the top-side switch so as to keep its peak current at a safe level. The protection threshold has been set to ensure

that the IC's maximum allowable peak current is not exceeded when using the recommended inductors. The sourcing current limiting is not considered a hard fault condition for slave, and therefore TS_FAULTB will not be asserted. Since clamping is based on instantaneous reconstructed current, the ripple current must be considered when calculating the maximum average current per slave. The maximum average current before clamping can be calculated as shown in Equation 1. Note that the clamping is based on reconstructed current. Limits shown in the Electrical Characteristics table for Clamp Level reflect expected variations in application conditions and external component characteristics. Also note that the master (i.e., system) overcurrent protection should be set lower than the corresponding slaves' maximum operating current as stated above.

**Equation 1**

$$\text{Maximum Average DC Slave Current} = \text{OCP} - \frac{I_{RIPPLE}}{2}$$

where,

OCP = Peak OCP Clamp Level (A)
$I_{RIPPLE}$ = Peak-to-Peak Inductor Ripple Current (A)

For current sinking protection, if the negative overcurrent protection threshold is reached, the slave limits the current and TS_FAULTB is not asserted.

The VT1697SB implements an additional OCP shutdown level (beyond the clamp levels). If the current in the top switch exceeds the OCP shutdown level (shown in the Electrical Characteristics table), the IC is turned OFF and fault is reported by asserting FAULTB pin. The slave is then latched OFF until the power is cycled.

### $V_{DD}$ and $V_{BOOST}$ Undervoltage Lockout

The smart slave ICs include undervoltage lockout circuits: $V_{DD}$ and $V_{BOOST}$. For power sequencing guidelines and operation with separate bias rails for master and slaves, please refer to appropriate master data sheet. $V_{BOOST}$ UVLO is active at all times after the initial system start up. It is not active during the initial system power on state (before regulation is enabled) and is activated approximately 20µs after initial start up. If either of these UVLO circuits is tripped during operation, the smart slave will stop switching and a fault signal (TS_FAULTB pulled LOW) will be sent to the master.

# Theory of Operation

## V$_{IN}$ (V$_{DDH}$) Undervoltage and Overvoltage Lockout

The slaves include protection circuits that shut down the slave and assert TS_FAULTB if V$_{DDH}$ is above or below the correct operating range. If either of these circuits is tripped during operation, the slave will stop switching and a fault signal (TS_FAULTB pulled LOW) will be sent to the master.

## Temperature Sensing and Overtemperature Protection

Each smart slave IC incorporates an accurate die temperature sensor. The temperature sense signal is sent to the master as an analog signal via the temperature sense pin. The actual temperature of each smart slave device is then made available via the SMBus of the master. The smart slave IC also includes overtemperature protection. If the trip point is reached, the IC immediately shuts down and the fault is reported to the master via the TS_FAULTB pin.

## VX Short Protection

The smart slave ICs include a VX short detection to detect a local short circuit from the VX node to either V$_{DDH}$ or ground. If such a fault is detected, the slave shuts down and communicates a fault to the master via the TS_FAULTB pin.

## TS_FAULTB Signal

If a fault is detected, the smart slave sends a signal to the master by pulling the TS_FAULTB pin to ground. Under normal conditions, this pin is used to send an accurate analog representation of the slave temperature. If a fault is detected, this pin is asserted LOW to indicate that a fault condition was detected by a slave IC. Table 1 shows the faults that result in this signal being asserted. For a latching fault, the fault must be cleared and the V$_{DD}$ power cycled to re-enable the IC (for non-latching faults, see note below the Table 1.). Please refer to the applicable master IC data sheet for details about han-

**Table 1:** Fault Detection and Protection Circuits

| Fault | Description | Type | Fault Flag (TS_FAULTB) |
|---|---|---|---|
| Boost UVLO | Undervoltage Lockout on Boost Supply | Shutdown* | Asserted |
| V$_{DDH}$ UVLO | Undervoltage Lockout on V$_{DDH}$ | Shutdown* | Asserted |
| V$_{DDH}$ OVLO | Overvoltage Lockout Signal on V$_{DDH}$ | Shutdown* | Asserted |
| V$_{DD}$ UVLO | Undervoltage Lockout Signal on V$_{DD}$ | Shutdown* | Asserted |
| V$_X$ Short | VX Short-to-Ground or V$_{DDH}$ | Shutdown | Asserted |
| POCP (Sourcing) | Positive/Sourcing Overcurrent Protection | Cycle-by-Cycle Current Limit | Not Asserted |
| NOCP (Sinking) | Negative/Sinking Overcurrent Protection | Cycle-by-Cycle Current Limit | Not Asserted |
| OTP | Overtemperature Protection | Shutdown | Asserted |

\* VDDH_UVLO, VDDH_OVLO, VBST_UVLO and VDD_UVLO are non-latching faults. If a non-latching fault is detected by the slave, it will assert TS_FAULTB signal low and stop switching. The slave resumes switching and de-asserts TS_FAULTB around 37µs from when the fault condition is removed. Please refer to the master data sheet for master response to TS_FAULTB asserted LOW by the slave device.

# Theory of Operation

## DESIGN CONSIDERATIONS

### Phase Current Sharing and Steering Control

Maxim master/slave chipsets offer options for thermal balancing in applications where one or more phases have different thermal characteristics. The current sense and chipset regulation system offer the potential for current steering, where a percentage of current can be steered away from any phase, allowing that phase to operate at a different current than the other phases. This allows a precise scaling of current in any slave(s) to achieve proper thermal balance between phases. Refer to the applicable Maxim master IC datasheet for more information on how to program this feature.

### Thermal Path and Printed Circuit Board Design

The smart slave IC has an exposed pad on the top-side of the package that is designed as an additional thermal path. This pad is electrically connected to $A_{GND}/V_{SS}$, but is not intended for use as an electrical connection. Since there is normally sufficient airflow above the regulator, conducting heat from the top of the package results in a low junction-to-ambient thermal impedance, and hence lower junction temperature. This method provides additional thermal path to the heat flow from the die to the PCB to ambient and also reduces the temperature of the PCB. Thermal performance is presented for various thermal conditions and airflow rates in the SOA plots.

### Printed Circuit Board (PCB) Layout

PCB layout can significantly affect the performance of the regulator. Careful attention should be paid to the location of the input capacitors and the output inductor which should be placed close to the IC. The VX traces include large voltage swings (greater than 12V) with dv/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but also are shielded with a ground plane immediately beneath.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative. Please contact Maxim to obtain QFN layout guidelines for optimal design.

**Table 2:** Typical Boost, Filtering and Decoupling Capacitor Requirements

| Description | Value | Type | Package | Qty |
|---|---|---|---|---|
| $V_{DD}$ Capacitor | 0.1μF/6.3V | X7R/125°C | 0603 | 1 |
| $V_{CC}$ Capacitor | 1μF/6.3V | X7R/125°C | 0603 | 1 |
| Boost Capacitor | 0.22μF/6.3V | X7R/125°C | 0402 | 1 |
| $V_{DD}$ $R_{FILTER}$ | 10Ω | 1/16W 1% | 0402 | 1 |
| $V_{DDH}$ HF Capacitor[1] | 1μF/16V | X7R/125°C | 0603 | 2 |
| $V_{DDH}$ HF Capacitor[1] | 0.1μF/16V | X7R/125°C | 0402 | 2 |
| $V_{DDH}$ Bulk Capacitor[2] | 10μF/16V | X5R | 0805/1206 | 2 |

**Note 1:** All $V_{DDH}$ high-frequency capacitors must be placed in close proximity to the slave IC and on the same side of the PCB as the slave IC. Please refer to Maxim's layout guideline for component placement requirements and recommendations.
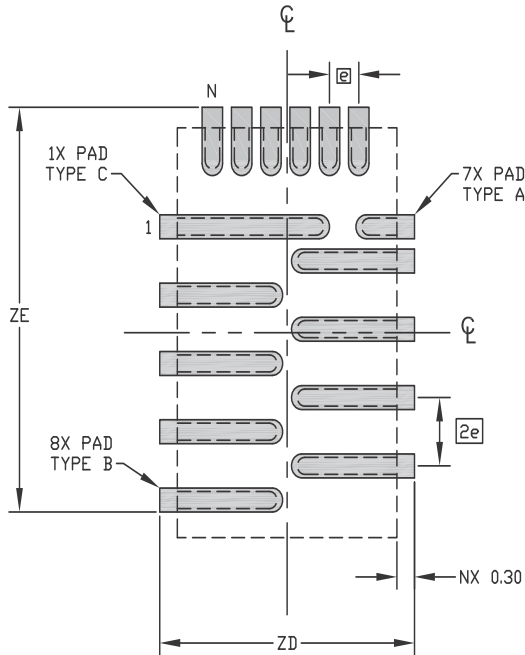
**Note 2:** For operation below 10.8V, two 22μF bulk capacitor are recommended instead of two 10μF capacitors.

**Note 3:** $V_{CC}$ should be directly connected to bias supply.

## Package Dimensions

| | Title: | Doc No. | Rev. |
|---|---|---|---|
| | **Package Outline - 16 Lead QFN [Type G]** | **ES AP-2896** | **0** |
| | | **Page 1 of 3** | |

TOP VIEW

2X
⌖ 0.10 C

−A−
−B−

D

0.44

PIN 1 ID

E

2X
⌖ 0.10 C

0.25

0.47    0.54

SIDE VIEW

A3

0.10 MAX

NX b  ⌖ 0.10 Ⓜ C A B  ⚠6

NX A1  ⌖ 0.08 C  ⚠5

A

∥ 0.10 C    −C−

SEATING PLANE

BOTTOM VIEW

℄

8X 1.70±0.10

NX R0.09 MIN

2e

1.95

℄

0.55

1

7X 0.60±0.10

N

e

0.28

2.50±0.10

| DIM | MILLIMETERS | | | INCHES | | |
|-----|------|------|------|-------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.90 | 0.95 | 1.00 | 0.035 | 0.037 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D | 3.75 BSC | | | 0.148 BSC | | |
| E | 6.00 BSC | | | 0.236 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| N | 16 PINS | | | 16 PINS | | |

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.
4. Dimensioning & tolerancing conform to ASME Y14.5−2009.
⚠5 Coplanarity applies to the terminals and all other bottom surface metallization.
⚠6 Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

# Package Dimensions

| | Title:<br><br>**Package Outline - 16 Lead QFN [Type G]** | Doc No.<br>**ES AP-2896** | Rev.<br>**0** |
|---|---|---|---|
| | | **Page 2 of 3** | |

RECOMMENDED LAND PATTERN
WITH PACKAGE OVERLAY



| DIM | MILLIMETERS MIN | MILLIMETERS NOM | MILLIMETERS MAX | INCHES MIN | INCHES NOM | INCHES MAX |
|---|---|---|---|---|---|---|
| e | | 0.50 BSC | | | 0.020 BSC | |
| N | | 16 PINS | | | 16 PINS | |
| ZD | | 4.35 REF | | | 0.171 REF | |
| ZE | | 5.93 REF | | | 0.233 REF | |

PAD DETAIL INFORMATION
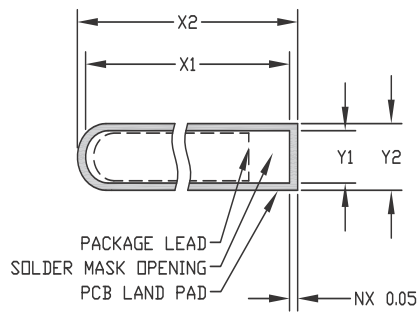


| DIM | MILLIMETERS TYPE A | MILLIMETERS TYPE B | MILLIMETERS TYPE C | INCHES TYPE A | INCHES TYPE B | INCHES TYPE C |
|---|---|---|---|---|---|---|
| Y1 | 0.28 | 0.28 | 0.28 | 0.011 | 0.011 | 0.011 |
| Y2 | 0.35 | 0.35 | 0.35 | 0.014 | 0.014 | 0.014 |
| X1 | 0.90 | 2.00 | 2.80 | 0.035 | 0.079 | 0.110 |
| X2 | 1.00 | 2.10 | 2.90 | 0.039 | 0.083 | 0.114 |

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.

## Revision History

### REVISION HISTORY

| Revision | Description | Date |
|---|---|---|
| 0 | Initial Data Sheet | N/A |
| 1 | Changed Status of VT1697SB to New Product.<br>Updated $I_{CC} + I_{DD}$, $V_{BST\_UVLO}$ and NOCP specifications in the Electrical Characteristics table.<br>Made a change in the "filter" (from $V_{DDH}$ to $V_{DD}$) in Table 2. | 1/14 |
| 2 | Updated to Maxim Template | 2/14 |
| 3 | Updated Electrical Characteristics Table and Overcurrent Protection section.<br>Updated Operating Current Rating to 55A.<br>Removed all VT1677SB references from data sheet. | 9/14 |
| 4 | Removed "Scalable 120A Multiphase Solution in < 835mm$^2$" in *Features and Benefits* section | 11/14 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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-  Поставка более 17-ти миллионов наименований электронных компонентов;
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**Как с нами связаться**

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