

MPC5602D



MPC5602D Microcontroller Data Sheet

- Single issue, 32-bit CPU core complex (e200z0h)
 - Compliant with the Power Architecture® embedded category
 - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 256 KB on-chip Code Flash supported with Flash controller and ECC
- 64 KB on-chip Data Flash with ECC
- Up to 16 KB on-chip SRAM with ECC
- Interrupt controller (INTC) with multiple interrupt vectors, including 20 external interrupt sources and 18 external interrupt/wakeup sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, Flash, or SRAM from multiple bus masters
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- Up to 33 channel 12-bit analog-to-digital converter (ADC)
- 2 serial peripheral interface (DSPI) modules
- 3 serial communication interface (LINFlex) modules
 - LINFlex 1 and 2: Master capable
 - LINFlex 0: Master capable and slave capable; connected to eDMA
- 1 enhanced full CAN (FlexCAN) module with configurable buffers
- Up to 79 configurable general purpose pins supporting input and output operations (package dependent)
- Real Time Counter (RTC) with clock source from 128 kHz or 16 MHz internal RC oscillator supporting autonomous wakeup with 1 ms resolution with max timeout of 2 seconds
- Up to 4 periodic interrupt timers (PIT) with 32-bit counter resolution
- 1 System Timer Module (STM)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class 1 standard
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table of Contents

| | | | | | |
|-------|--|----|--------|---|----|
| 1 | Introduction | 3 | 4.10 | Power consumption | 41 |
| 1.1 | Document overview | 3 | 4.11 | Flash memory electrical characteristics | 42 |
| 1.2 | Description | 3 | 4.11.1 | Program/Erase characteristics | 42 |
| 2 | Block diagram | 4 | 4.11.2 | Flash power supply DC characteristics | 44 |
| 3 | Package pinouts and signal descriptions | 7 | 4.11.3 | Start-up/Switch-off timings | 45 |
| 3.1 | Package pinouts | 7 | 4.12 | Electromagnetic compatibility (EMC) characteristics | 45 |
| 3.2 | Pad configuration during reset phases | 9 | 4.12.1 | Designing hardened software to avoid noise problems | 45 |
| 3.3 | Voltage supply pins | 9 | 4.12.2 | Electromagnetic interference (EMI) | 46 |
| 3.4 | Pad types | 10 | 4.12.3 | Absolute maximum ratings (electrical sensitivity) | 46 |
| 3.5 | System pins | 10 | 4.13 | Fast external crystal oscillator (4 to 16 MHz) electrical characteristics | 48 |
| 3.6 | Functional ports | 11 | 4.14 | FMPLL electrical characteristics | 51 |
| 4 | Electrical characteristics | 21 | 4.15 | Fast internal RC oscillator (16 MHz) electrical characteristics | 51 |
| 4.1 | Introduction | 21 | 4.16 | Slow internal RC oscillator (128 kHz) electrical characteristics | 52 |
| 4.2 | Parameter classification | 21 | 4.17 | ADC electrical characteristics | 54 |
| 4.3 | NVUSRO register | 21 | 4.17.1 | Introduction | 54 |
| 4.3.1 | NVUSRO[<code>PAD3V5V</code>] field description | 22 | 4.17.2 | Input impedance and ADC accuracy | 55 |
| 4.3.2 | NVUSRO[<code>OSCILLATOR_MARGIN</code>] field description | 22 | 4.17.3 | ADC electrical characteristics | 60 |
| 4.3.3 | NVUSRO[<code>WATCHDOG_EN</code>] field description | 22 | 4.18 | On-chip peripherals | 62 |
| 4.4 | Absolute maximum ratings | 22 | 4.18.1 | Current consumption | 62 |
| 4.5 | Recommended operating conditions | 23 | 4.18.2 | DSPI characteristics | 63 |
| 4.6 | Thermal characteristics | 26 | 4.18.3 | JTAG characteristics | 70 |
| 4.6.1 | Package thermal characteristics | 26 | 5 | Package characteristics | 70 |
| 4.6.2 | Power considerations | 26 | 5.1 | Package mechanical data | 70 |
| 4.7 | I/O pad electrical characteristics | 27 | 5.1.1 | 100 LQFP | 70 |
| 4.7.1 | I/O pad types | 27 | 5.1.2 | 64 LQFP | 74 |
| 4.7.2 | I/O input DC characteristics | 27 | 6 | Ordering information | 77 |
| 4.7.3 | I/O output DC characteristics | 28 | 7 | Document revision history | 78 |
| 4.7.4 | Output pin transition times | 31 | | | |
| 4.7.5 | I/O pad current specification | 31 | | | |
| 4.8 | RESET electrical characteristics | 35 | | | |
| 4.9 | Power management electrical characteristics | 37 | | | |
| 4.9.1 | Voltage regulator electrical characteristics | 37 | | | |
| 4.9.2 | Low voltage detector electrical characteristics | 40 | | | |

1 Introduction

1.1 Document overview

This document describes the device features and highlights the important electrical and physical characteristics.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations.

The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

Table 1. MPC5602D device comparison

| Feature | Device | | | |
|---------------------------------------|-----------------------|---------------|---------------|---------------|
| | MPC5601DxLH | MPC5601DxLL | MPC5602DxLH | MPC5602DxLL |
| CPU | e200z0h | | | |
| Execution speed | Static – up to 48 MHz | | | |
| Code flash memory | 128 KB | | 256 KB | |
| Data flash memory | 64 KB (4 x 16 KB) | | | |
| SRAM | 12 KB | | 16 KB | |
| eDMA | 16 ch | | | |
| ADC (12-bit) | 16 ch | 33 ch | 16 ch | 33 ch |
| CTU | 16 ch | | | |
| Total timer I/O ¹ eMIOS | 14 ch, 16-bit | 28 ch, 16-bit | 14 ch, 16-bit | 28 ch, 16-bit |
| • Type X ² | 2 ch | 5 ch | 2 ch | 5 ch |
| • Type Y ³ | — | 9 ch | — | 9 ch |
| • Type G ⁴ | 7 ch | 7 ch | 7 ch | 7 ch |
| • Type H ⁵ | 4 ch | 7 ch | 4 ch | 7 ch |
| SCI (LINFlex) | 3 | | | |
| SPI (DSPI) | 2 | | | |
| CAN (FlexCAN) | 1 | | | |
| GPIO ⁶ | 45 | 79 | 45 | 79 |

Table 1. MPC5602D device comparison (continued)

| Feature | Device | | | |
|---------|-------------|-------------|-------------|-------------|
| | MPC5601DxLH | MPC5601DxLL | MPC5602DxLH | MPC5602DxLL |
| Debug | JTAG | | | |
| Package | 64 LQFP | 100 LQFP | 64 LQFP | 100 LQFP |

¹ Refer to eMIOS chapter of device reference manual for information on the channel configuration and functions.

² Type X = MC + MCB + OPWMT + OPWMB + OPWFMB + SAIC + SAOC

³ Type Y = OPWMT + OPWMB + SAIC + SAOC

⁴ Type G = MCB + IPWM + IPM + DAOC + OPWMT + OPWMB + OPWFMB + OPWMCB + SAIC + SAOC

⁵ Type H = IPWM + IPM + DAOC + OPWMT + OPWMB + SAIC + SAOC

⁶ I/O count based on multiplexing with peripherals

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602D device series.



Figure 1. MPC5602D series block diagram

Table 2 summarizes the functions of all blocks present in the MPC5602D series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

Table 2. MPC5602D series block summary

| Block | Function |
|---|---|
| Analog-to-digital converter (ADC) | Multi-channel, 12-bit analog-to-digital converter |
| Boot assist module (BAM) | A block of read-only memory containing VLE code which is executed according to the boot mode of the device |
| Clock generation module (MC_CGM) | Provides logic and control required for the generation of system and peripheral clocks |
| Clock monitor unit (CMU) | Monitors clock source (internal and external) integrity |
| Cross triggering unit (CTU) | Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT |
| Crossbar switch (XBAR) | Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width. |
| Deserial serial peripheral interface (DSPI) | Provides a synchronous serial interface for communication with external devices |
| Enhanced direct memory access (eDMA) | Performs complex data transfers with minimal intervention from a host processor via "n" programmable channels. |
| Enhanced modular input output system (eMIOS) | Provides the functionality to generate or measure events |
| Error correction status module (ECSM) | Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes |
| Flash memory | Provides non-volatile storage for program code, constants and variables |
| FlexCAN (controller area network) | Supports the standard CAN communications protocol |
| Frequency-modulated phase-locked loop (FMPLL) | Generates high-speed system clocks and supports programmable frequency modulation |
| Internal multiplexer (IMUX) SIU subblock | Allows flexible mapping of peripheral interface on the different pins of the device |
| Interrupt controller (INTC) | Provides priority-based preemptive scheduling of interrupt requests |
| JTAG controller (JTAGC) | Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode |
| LINFlex controller | Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load |
| Mode entry module (MC_ME) | Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications |
| Non-maskable interrupt (NMI) | Handles external events that must produce an immediate response, such as power down detection |
| Periodic interrupt timer (PIT) | Produces periodic interrupts and triggers |
| Power control unit (MC_PCU) | Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU |

Table 2. MPC5602D series block summary (continued)

| Block | Function |
|---|--|
| Real-time counter (RTC) | Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications |
| Reset generation module (MC_RGM) | Centralizes reset sources and manages the device reset sequence of the device |
| Static random-access memory (SRAM) | Provides storage for program code, constants, and variables |
| System integration unit lite (SIUL) | Provides control over all the electrical pad controls and up to 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration |
| System status and configuration module (SSCM) | Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable |
| System timer module (STM) | Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks |
| Software watchdog timer (SWT) | Provides protection from runaway code |
| Wakeup unit (WKPU) | Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events. |

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to [Table 5](#).

Package pinouts and signal descriptions

Figure 2 shows the MPC5602D in the 100 LQFP package.

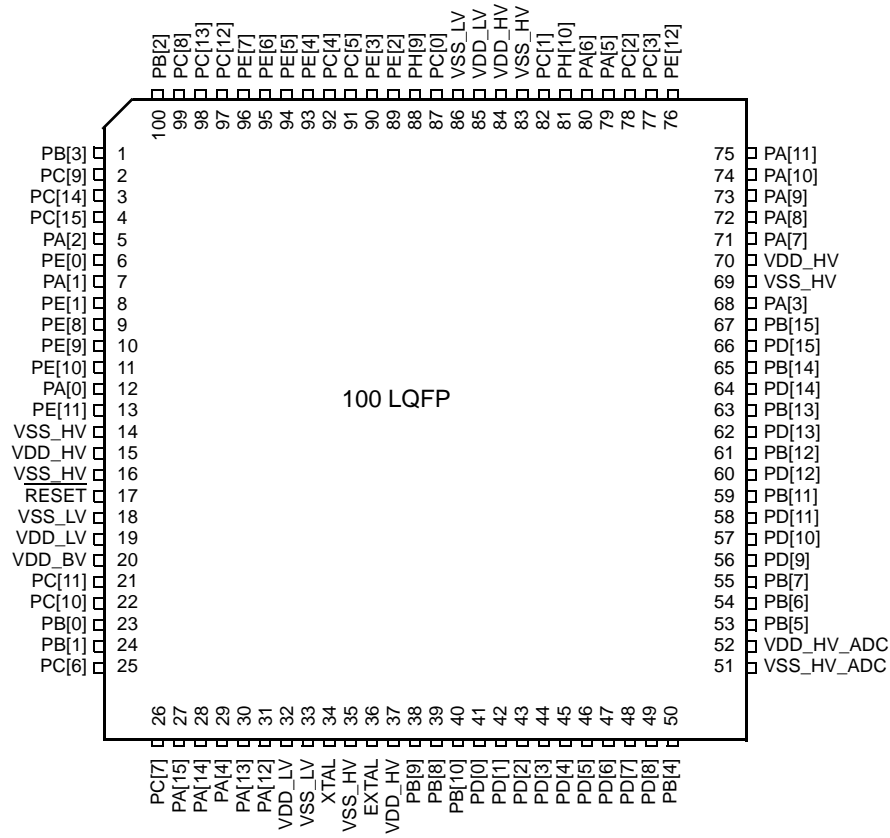


Figure 2. 100 LQFP pin configuration (top view)

Figure 3 shows the MPC5602D in the 64 LQFP package.



Figure 3. 64 LQFP pin configuration (top view)

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up while TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

Table 3. Voltage supply pin descriptions

| Port pin | Function | Pin number | |
|----------|--|------------------|------------------------|
| | | 64 LQFP | 100 LQFP |
| VDD_HV | Digital supply voltage | 7, 28, 34, 56 | 15, 37, 52, 70, 84 |
| VSS_HV | Digital ground | 6, 8, 26, 33, 55 | 14, 16, 35, 51, 69, 83 |
| VDD_LV | 1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V _{SS_LV} pin. ¹ | 11, 23, 57 | 19, 32, 85 |
| VSS_LV | 1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V _{DD_LV} pin. ¹ | 10, 24, 58 | 18, 33, 86 |
| VDD_BV | Internal regulator supply voltage | 12 | 20 |

¹ A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

- S = Slow¹
- M = Medium^{1 2}
- F = Fast^{1 2}
- I = Input only with analog feature¹
- J = Input/Output ('S' pad) with analog feature
- X = Oscillator

3.5 System pins

The system pins are listed in [Table 4](#).

Table 4. System pin descriptions

| Port pin | Function | I/O direction | Pad type | RESET configuration | Pin number | |
|----------|--|---------------|----------|---------------------------------------|------------|----------|
| | | | | | 64 LQFP | 100 LQFP |
| RESET | Bidirectional reset with Schmitt-Trigger characteristics and noise filter. | I/O | M | Input, weak pull-up only after PHASE2 | 9 | 17 |
| EXTAL | Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode. ¹ | I/O | X | Tristate | 27 | 36 |
| XTAL | Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode. ¹ | I | X | Tristate | 25 | 34 |

¹ Refer to the relevant section of the device datasheet.

1. See the I/O pad electrical characteristics in the device datasheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see the PCR[SRC] description in the device reference manual).

3.6 Functional ports

The functional port pins are listed in [Table 5](#).

Table 5. Functional port pin descriptions

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|---------------|--------|------------------------------------|--|---|----------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| Port A | | | | | | | | | |
| PA[0] | PCR[0] | AF0 AF1 AF2 AF3 — | GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19] ³ | SIUL eMIOS_0 CGL eMIOS_0 WKPU | I/O I/O O I/O I | M | Tristate | 5 | 12 |
| PA[1] | PCR[1] | AF0 AF1 AF2 AF3 — — | GPIO[1] E0UC[1] — — NMI ⁴ WKPU[2] ³ | SIUL eMIOS_0 — — WKPU WKPU | I/O I/O — — I I | S | Tristate | 4 | 7 |
| PA[2] | PCR[2] | AF0 AF1 AF2 AF3 — | GPIO[2] E0UC[2] — MA[2] WKPU[3] ³ | SIUL eMIOS_0 — ADC WKPU | I/O I/O — O I | S | Tristate | 3 | 5 |
| PA[3] | PCR[3] | AF0 AF1 AF2 AF3 — — | GPIO[3] E0UC[3] — CS4_0 EIRQ[0] ADC1_S[0] | SIUL eMIOS_0 — DSPI_0 SIUL ADC | I/O I/O — I/O I I | S | Tristate | 43 | 68 |
| PA[4] | PCR[4] | AF0 AF1 AF2 AF3 — | GPIO[4] E0UC[4] — CS0_1 WKPU[9] ³ | SIUL eMIOS_0 — DSPI_1 WKPU | I/O I/O — I/O I | S | Tristate | 20 | 29 |
| PA[5] | PCR[5] | AF0 AF1 AF2 AF3 | GPIO[5] E0UC[5] — — | SIUL eMIOS_0 — — | I/O I/O — — | M | Tristate | 51 | 79 |
| PA[6] | PCR[6] | AF0 AF1 AF2 AF3 — | GPIO[6] E0UC[6] — CS1_1 EIRQ[1] | SIUL eMIOS_0 — DSPI_1 SIUL | I/O I/O — I/O I | S | Tristate | 52 | 80 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|----------|---------|---|---|---|-------------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PA[7] | PCR[7] | AF0 AF1 AF2 AF3 — — | GPIO[7] E0UC[7] — — EIRQ[2] ADC1_S[1] | SIUL eMIOS_0 — — SIUL ADC | I/O I/O — — I I | S | Tristate | 44 | 71 |
| PA[8] | PCR[8] | AF0 AF1 AF2 AF3 — N/A ⁵ | GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] | SIUL eMIOS_0 eMIOS_0 — SIUL BAM | I/O I/O — — I I | S | Input, weak pull-up | 45 | 72 |
| PA[9] | PCR[9] | AF0 AF1 AF2 AF3 N/A ⁵ | GPIO[9] E0UC[9] — CS2_1 FAB | SIUL eMIOS_0 — DSPI_1 BAM | I/O I/O — I/O I | S | Pull-down | 46 | 73 |
| PA[10] | PCR[10] | AF0 AF1 AF2 AF3 — | GPIO[10] E0UC[10] — LIN2TX ADC1_S[2] | SIUL eMIOS_0 — LINFlex_2 ADC | I/O I/O — O I | S | Tristate | 47 | 74 |
| PA[11] | PCR[11] | AF0 AF1 AF2 AF3 — — — | GPIO[11] E0UC[11] — — EIRQ[16] ADC1_S[3] LIN2RX | SIUL eMIOS_0 — — SIUL ADC LINFlex_2 | I/O I/O — — I I I | S | Tristate | 48 | 75 |
| PA[12] | PCR[12] | AF0 AF1 AF2 AF3 — — | GPIO[12] — — — EIRQ[17] SIN_0 | SIUL — — — SIUL DSPI_0 | I/O — — — I I | S | Tristate | 22 | 31 |
| PA[13] | PCR[13] | AF0 AF1 AF2 AF3 | GPIO[13] SOUT_0 — CS3_1 | SIUL DSPI_0 — DSPI_1 | I/O O — I/O | M | Tristate | 21 | 30 |
| PA[14] | PCR[14] | AF0 AF1 AF2 AF3 — | GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4] | SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL | I/O I/O I/O I/O I | M | Tristate | 19 | 28 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|---------------|---------|------------------------------------|--|--|-------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PA[15] | PCR[15] | AF0 AF1 AF2 AF3 — | GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10] ³ | SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU | I/O I/O I/O I/O I | M | Tristate | 18 | 27 |
| Port B | | | | | | | | | |
| PB[0] | PCR[16] | AF0 AF1 AF2 AF3 | GPIO[16] CAN0TX — LIN2TX | SIUL FlexCAN_0 — LINFlex_2 | I/O O — O | M | Tristate | 14 | 23 |
| PB[1] | PCR[17] | AF0 AF1 AF2 AF3 — — | GPIO[17] — — LIN0RX WKPU[4] ³ CAN0RX | SIUL — — LINFlex_0 WKPU FlexCAN_0 | I/O — — I I I | S | Tristate | 15 | 24 |
| PB[2] | PCR[18] | AF0 AF1 AF2 AF3 | GPIO[18] LIN0TX — — | SIUL LINFlex_0 — — | I/O O — — | M | Tristate | 64 | 100 |
| PB[3] | PCR[19] | AF0 AF1 AF2 AF3 — — | GPIO[19] — — — WKPU[11] ³ LIN0RX | SIUL — — — WKPU LINFlex_0 | I/O — — — I I | S | Tristate | 1 | 1 |
| PB[4] | PCR[20] | AF0 AF1 AF2 AF3 — | GPIO[20] — — — ADC1_P[0] | SIUL — — — ADC | I — — — I | I | Tristate | 32 | 50 |
| PB[5] | PCR[21] | AF0 AF1 AF2 AF3 — | GPIO[21] — — — ADC1_P[1] | SIUL — — — ADC | I — — — I | I | Tristate | 35 | 53 |
| PB[6] | PCR[22] | AF0 AF1 AF2 AF3 — | GPIO[22] — — — ADC1_P[2] | SIUL — — — ADC | I — — — I | I | Tristate | 36 | 54 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|----------|---------|------------------------------------|---|---------------------------------------|------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PB[7] | PCR[23] | AF0 AF1 AF2 AF3 — | GPIO[23] — — — ADC1_P[3] | SIUL — — — ADC | I — — — I | I | Tristate | 37 | 55 |
| PB[8] | PCR[24] | AF0 AF1 AF2 AF3 — — | GPIO[24] — — — ADC1_S[4] WKPU[25] ³ | SIUL — — — ADC WKPU | I — — — I I | I | Tristate | 30 | 39 |
| PB[9] | PCR[25] | AF0 AF1 AF2 AF3 — — | GPIO[25] — — — ADC1_S[5] WKPU[26] ³ | SIUL — — — ADC WKPU | I — — — I I | I | Tristate | 29 | 38 |
| PB[10] | PCR[26] | AF0 AF1 AF2 AF3 — — | GPIO[26] — — — ADC1_S[6] WKPU[8] ³ | SIUL — — — ADC WKPU | I/O — — — I I | J | Tristate | 31 | 40 |
| PB[11] | PCR[27] | AF0 AF1 AF2 AF3 — | GPIO[27] E0UC[3] — CS0_0 ADC1_S[12] | SIUL eMIOS_0 — DSPI_0 ADC | I/O I/O — I/O I | J | Tristate | 38 | 59 |
| PB[12] | PCR[28] | AF0 AF1 AF2 AF3 — | GPIO[28] E0UC[4] — CS1_0 ADC1_X[0] | SIUL eMIOS_0 — DSPI_0 ADC | I/O I/O — O I | J | Tristate | 39 | 61 |
| PB[13] | PCR[29] | AF0 AF1 AF2 AF3 — | GPIO[29] E0UC[5] — CS2_0 ADC1_X[1] | SIUL eMIOS_0 — DSPI_0 ADC | I/O I/O — O I | J | Tristate | 40 | 63 |
| PB[14] | PCR[30] | AF0 AF1 AF2 AF3 — | GPIO[30] E0UC[6] — CS3_0 ADC1_X[2] | SIUL eMIOS_0 — DSPI_0 ADC | I/O I/O — O I | J | Tristate | 41 | 65 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|--------------------|---------|------------------------------------|--|---------------------------------------|------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PB[15] | PCR[31] | AF0 AF1 AF2 AF3 — | GPIO[31] E0UC[7] — CS4_0 ADC1_X[3] | SIUL eMIOS_0 — DSPI_0 ADC | I/O I/O — O I | J | Tristate | 42 | 67 |
| Port C | | | | | | | | | |
| PC[0] ⁶ | PCR[32] | AF0 AF1 AF2 AF3 | GPIO[32] — TDI — | SIUL — JTAGC — | I/O — I — | M | Input, weak pull-up | 59 | 87 |
| PC[1] ⁶ | PCR[33] | AF0 AF1 AF2 AF3 | GPIO[33] — TDO — | SIUL — JTAGC — | I/O — O — | F | Tristate | 54 | 82 |
| PC[2] | PCR[34] | AF0 AF1 AF2 AF3 — | GPIO[34] SCK_1 — — EIRQ[5] | SIUL DSPI_1 — — SIUL | I/O I/O — — I | M | Tristate | 50 | 78 |
| PC[3] | PCR[35] | AF0 AF1 AF2 AF3 — | GPIO[35] CS0_1 MA[0] — EIRQ[6] | SIUL DSPI_1 ADC — SIUL | I/O I/O O — I | S | Tristate | 49 | 77 |
| PC[4] | PCR[36] | AF0 AF1 AF2 AF3 — — | GPIO[36] — — — SIN_1 EIRQ[18] | SIUL — — — DSPI_1 SIUL | I/O — — — I I | M | Tristate | 62 | 92 |
| PC[5] | PCR[37] | AF0 AF1 AF2 AF3 — | GPIO[37] SOUT_1 — — EIRQ[7] | SIUL DSPI_1 — — SIUL | I/O O — — I | M | Tristate | 61 | 91 |
| PC[6] | PCR[38] | AF0 AF1 AF2 AF3 | GPIO[38] LIN1TX — — | SIUL LINFlex_1 — — | I/O O — — | S | Tristate | 16 | 25 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|----------|---------|------------------------------------|--|--|--------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PC[7] | PCR[39] | AF0 AF1 AF2 AF3 — — | GPIO[39] — — — LIN1RX WKPU[12] ³ | SIUL — — — LINFlex_1 WKPU | I/O — — — I I | S | Tristate | 17 | 26 |
| PC[8] | PCR[40] | AF0 AF1 AF2 AF3 | GPIO[40] LIN2TX E0UC[3] — | SIUL LINFlex_2 eMIOS_0 — | I/O O I/O — | S | Tristate | 63 | 99 |
| PC[9] | PCR[41] | AF0 AF1 AF2 AF3 — — | GPIO[41] — E0UC[7] — LIN2RX WKPU[13] ³ | SIUL — eMIOS_0 — LINFlex_2 WKPU | I/O — I/O — I I | S | Tristate | 2 | 2 |
| PC[10] | PCR[42] | AF0 AF1 AF2 AF3 | GPIO[42] — — MA[1] | SIUL — — ADC | I/O — — O | M | Tristate | 13 | 22 |
| PC[11] | PCR[43] | AF0 AF1 AF2 AF3 — | GPIO[43] — — MA[2] WKPU[5] ³ | SIUL — — ADC WKPU | I/O — — O I | S | Tristate | — | 21 |
| PC[12] | PCR[44] | AF0 AF1 AF2 AF3 — | GPIO[44] E0UC[12] — — EIRQ[19] | SIUL eMIOS_0 — — SIUL | I/O I/O — — I | M | Tristate | — | 97 |
| PC[13] | PCR[45] | AF0 AF1 AF2 AF3 | GPIO[45] E0UC[13] — — | SIUL eMIOS_0 — — | I/O I/O — — | S | Tristate | — | 98 |
| PC[14] | PCR[46] | AF0 AF1 AF2 AF3 — | GPIO[46] E0UC[14] — — EIRQ[8] | SIUL eMIOS_0 — — SIUL | I/O I/O — — I | S | Tristate | — | 3 |
| PC[15] | PCR[47] | AF0 AF1 AF2 AF3 — | GPIO[47] E0UC[15] — — EIRQ[20] | SIUL eMIOS_0 — — SIUL | I/O I/O — — I | M | Tristate | — | 4 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|---------------|---------|------------------------------------|--|---|-------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| Port D | | | | | | | | | |
| PD[0] | PCR[48] | AF0 AF1 AF2 AF3 — — | GPIO[48] — — — — WKPU[27] ³ ADC1_P[4] | SIUL — — — — WKPU ADC | — — — — | | Tristate | — | 41 |
| PD[1] | PCR[49] | AF0 AF1 AF2 AF3 — — | GPIO[49] — — — — WKPU[28] ³ ADC1_P[5] | SIUL — — — — WKPU ADC | — — — — | | Tristate | — | 42 |
| PD[2] | PCR[50] | AF0 AF1 AF2 AF3 — | GPIO[50] — — — — ADC1_P[6] | SIUL — — — — ADC | — — — — | | Tristate | — | 43 |
| PD[3] | PCR[51] | AF0 AF1 AF2 AF3 — | GPIO[51] — — — — ADC1_P[7] | SIUL — — — — ADC | — — — — | | Tristate | — | 44 |
| PD[4] | PCR[52] | AF0 AF1 AF2 AF3 — | GPIO[52] — — — — ADC1_P[8] | SIUL — — — — ADC | — — — — | | Tristate | — | 45 |
| PD[5] | PCR[53] | AF0 AF1 AF2 AF3 — | GPIO[53] — — — — ADC1_P[9] | SIUL — — — — ADC | — — — — | | Tristate | — | 46 |
| PD[6] | PCR[54] | AF0 AF1 AF2 AF3 — | GPIO[54] — — — — ADC1_P[10] | SIUL — — — — ADC | — — — — | | Tristate | — | 47 |
| PD[7] | PCR[55] | AF0 AF1 AF2 AF3 — | GPIO[55] — — — — ADC1_P[11] | SIUL — — — — ADC | — — — — | | Tristate | — | 48 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|---------------|---------|---------------------------------|--|---------------------------------------|-----------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PD[8] | PCR[56] | AF0 AF1 AF2 AF3 — | GPIO[56] — — — ADC1_P[12] | SIUL — — — ADC | I — — — I | I | Tristate | — | 49 |
| PD[9] | PCR[57] | AF0 AF1 AF2 AF3 — | GPIO[57] — — — ADC1_P[13] | SIUL — — — ADC | I — — — I | I | Tristate | — | 56 |
| PD[10] | PCR[58] | AF0 AF1 AF2 AF3 — | GPIO[58] — — — ADC1_P[14] | SIUL — — — ADC | I — — — I | I | Tristate | — | 57 |
| PD[11] | PCR[59] | AF0 AF1 AF2 AF3 — | GPIO[59] — — — ADC1_P[15] | SIUL — — — ADC | I — — — I | I | Tristate | — | 58 |
| PD[12] | PCR[60] | AF0 AF1 AF2 AF3 — | GPIO[60] CS5_0 E0UC[24] — ADC1_S[8] | SIUL DSPI_0 eMIOS_0 — ADC | I/O O I/O — I | J | Tristate | — | 60 |
| PD[13] | PCR[61] | AF0 AF1 AF2 AF3 — | GPIO[61] CS0_1 E0UC[25] — ADC1_S[9] | SIUL DSPI_1 eMIOS_0 — ADC | I/O I/O I/O — I | J | Tristate | — | 62 |
| PD[14] | PCR[62] | AF0 AF1 AF2 AF3 — | GPIO[62] CS1_1 E0UC[26] — ADC1_S[10] | SIUL DSPI_1 eMIOS_0 — ADC | I/O O I/O — I | J | Tristate | — | 64 |
| PD[15] | PCR[63] | AF0 AF1 AF2 AF3 — | GPIO[63] CS2_1 E0UC[27] — ADC1_S[11] | SIUL DSPI_1 eMIOS_0 — ADC | I/O O I/O — I | J | Tristate | — | 66 |
| Port E | | | | | | | | | |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|----------|---------|------------------------------------|--|--|-------------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PE[0] | PCR[64] | AF0 AF1 AF2 AF3 — | GPIO[64] E0UC[16] — — WKPU[6] ³ | SIUL eMIOS_0 — — WKPU | I/O I/O — — I | S | Tristate | — | 6 |
| PE[1] | PCR[65] | AF0 AF1 AF2 AF3 | GPIO[65] E0UC[17] — — | SIUL eMIOS_0 — — | I/O I/O — — | M | Tristate | — | 8 |
| PE[2] | PCR[66] | AF0 AF1 AF2 AF3 — — | GPIO[66] E0UC[18] — — — EIRQ[21] SIN_1 | SIUL eMIOS_0 — — — SIUL DSPI_1 | I/O I/O — — — I I | M | Tristate | — | 89 |
| PE[3] | PCR[67] | AF0 AF1 AF2 AF3 | GPIO[67] E0UC[19] SOUT_1 — | SIUL eMIOS_0 DSPI_1 — | I/O I/O O — | M | Tristate | — | 90 |
| PE[4] | PCR[68] | AF0 AF1 AF2 AF3 — | GPIO[68] E0UC[20] SCK_1 — EIRQ[9] | SIUL eMIOS_0 DSPI_1 — SIUL | I/O I/O I/O — I | M | Tristate | — | 93 |
| PE[5] | PCR[69] | AF0 AF1 AF2 AF3 | GPIO[69] E0UC[21] CS0_1 MA[2] | SIUL eMIOS_0 DSPI_1 ADC | I/O I/O I/O O | M | Tristate | — | 94 |
| PE[6] | PCR[70] | AF0 AF1 AF2 AF3 — | GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22] | SIUL eMIOS_0 DSPI_0 ADC SIUL | I/O I/O O O O I | M | Tristate | — | 95 |
| PE[7] | PCR[71] | AF0 AF1 AF2 AF3 — | GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23] | SIUL eMIOS_0 DSPI_0 ADC SIUL | I/O I/O O O O I | M | Tristate | — | 96 |
| PE[8] | PCR[72] | AF0 AF1 AF2 AF3 | GPIO[72] — E0UC[22] — | SIUL — eMIOS_0 — | I/O — I/O — | M | Tristate | — | 9 |

Table 5. Functional port pin descriptions (continued)

| Port pin | PCR | Alternate function ¹ | Function | Peripheral | I/O direction ² | Pad type | RESET configuration | Pin number | |
|---------------------|----------|------------------------------------|---|--|------------------------------|----------|---------------------|------------|----------|
| | | | | | | | | 64 LQFP | 100 LQFP |
| PE[9] | PCR[73] | AF0 AF1 AF2 AF3 — | GPIO[73] — E0UC[23] — WKPU[7] ³ | SIUL — eMIOS_0 — WKPU | I/O — I/O — I | S | Tristate | — | 10 |
| PE[10] | PCR[74] | AF0 AF1 AF2 AF3 — | GPIO[74] — CS3_1 — EIRQ[10] | SIUL — DSPI_1 — SIUL | I/O — O — I | S | Tristate | — | 11 |
| PE[11] | PCR[75] | AF0 AF1 AF2 AF3 — | GPIO[75] E0UC[24] CS4_1 — WKPU[14] ³ | SIUL eMIOS_0 DSPI_1 — WKPU | I/O I/O O — I | S | Tristate | — | 13 |
| PE[12] | PCR[76] | AF0 AF1 AF2 AF3 — — | GPIO[76] — — — ADC1_S[7] EIRQ[11] | SIUL — — — ADC SIUL | I/O — — — I I | S | Tristate | — | 76 |
| Port H | | | | | | | | | |
| PH[9] ⁶ | PCR[121] | AF0 AF1 AF2 AF3 | GPIO[121] — TCK — | SIUL — JTAGC — | I/O — I — | S | Input, weak pull-up | 60 | 88 |
| PH[10] ⁶ | PCR[122] | AF0 AF1 AF2 AF3 | GPIO[122] — TMS — | SIUL — JTAGC — | I/O — I — | S | Input, weak pull-up | 53 | 81 |

¹ Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

² Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

³ All WKPU pins also support external interrupt capability. See "wakeup unit" chapter of the device reference manual for further details.

⁴ NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

⁵ "Not applicable" because these functions are available only while the device is booting. Refer to "BAM" chapter of the device reference manual for details.

- ⁶ Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO. PC[0:1] are available as JTAG pins (TDI and TDO respectively). PH[9:10] are available as JTAG pins (TCK and TMS respectively). If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1 2001.

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 6](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

| Classification tag | Tag description |
|--------------------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

Electrical characteristics

4.3.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. [Table 7](#) shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 7. PAD3V5V field description

| Value ¹ | Description |
|--------------------|------------------------------|
| 0 | High voltage supply is 5.0 V |
| 1 | High voltage supply is 3.3 V |

¹ Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. [Table 8](#) shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 8. OSCILLATOR_MARGIN field description

| Value ¹ | Description |
|--------------------|---|
| 0 | Low consumption configuration (4 MHz/8 MHz) |
| 1 | High margin configuration (4 MHz/16 MHz) |

¹ Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.3.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. [Table 8](#) shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 9. WATCHDOG_EN field description

| Value ¹ | Description |
|--------------------|---------------------|
| 0 | Disable after reset |
| 1 | Enable after reset |

¹ Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.4 Absolute maximum ratings

Table 10. Absolute maximum ratings

| Symbol | | Parameter | Conditions | Value | | Unit |
|--------------------|----|---|------------|-----------------------|-----------------------|------|
| | | | | Min | Max | |
| V _{SS} | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| V _{DD} | SR | Voltage on VDD_HV pins with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| V _{SS_LV} | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS}) | — | V _{SS} - 0.1 | V _{SS} + 0.1 | V |

Table 10. Absolute maximum ratings (continued)

| Symbol | | Parameter | Conditions | Value | | Unit |
|----------------------|----|---|--|-----------------------|-----------------------|------|
| | | | | Min | Max | |
| V _{DD_BV} | SR | Voltage on VDD_BV (regulator supply) pin with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| | | | Relative to V _{DD} | V _{DD} - 0.3 | V _{DD} + 0.3 | |
| V _{SS_ADC} | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) | — | V _{SS} - 0.1 | V _{SS} + 0.1 | V |
| V _{DD_ADC} | SR | Voltage on VDD_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| | | | Relative to V _{DD} | V _{DD} - 0.3 | V _{DD} + 0.3 | |
| V _{IN} | SR | Voltage on any GPIO pin with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| | | | Relative to V _{DD} | V _{DD} - 0.3 | V _{DD} + 0.3 | |
| I _{INJPAD} | SR | Injected input current on any pin during overload condition | — | -10 | 10 | mA |
| I _{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | mA |
| I _{AVGSEG} | SR | Sum of all the static I/O current within a supply segment ¹ | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | 70 | mA |
| | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | 64 | |
| I _{CORELV} | SR | Low voltage static current sink through VDD_BV | — | — | 150 | mA |
| T _{STORAGE} | SR | Storage temperature | — | -55 | 150 | °C |

¹ Supply segments are described in [Section 4.7.5, I/O pad current specification](#).

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.5 Recommended operating conditions

Table 11. Recommended operating conditions (3.3 V)

| Symbol | | C | Parameter | Conditions | Value | | Unit |
|---------------------------------|----|---|---|------------|-----------------------|-----------------------|------|
| | | | | | Min | Max | |
| V _{SS} | SR | — | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| V _{DD} ¹ | SR | — | Voltage on VDD_HV pins with respect to ground (V _{SS}) | — | 3.0 | 3.6 | V |
| V _{SS_LV} ² | SR | — | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS}) | — | V _{SS} - 0.1 | V _{SS} + 0.1 | V |

Table 11. Recommended operating conditions (3.3 V) (continued)

| Symbol | C | Parameter | Conditions | Value | | Unit |
|----------------------------|----|---|------------------------------|------------------|----------------|------------|
| | | | | Min | Max | |
| V_{DD_BV} ³ | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS}) | — | 3.0 | 3.6 | V |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{SS_ADC} | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | $V_{SS} + 0.1$ | V |
| V_{DD_ADC} ⁴ | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS}) | — | 3.0 ⁵ | 3.6 | V |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{IN} | SR | Voltage on any GPIO pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | — | V |
| | | | Relative to V_{DD} | — | $V_{DD} + 0.1$ | |
| I_{INJPAD} | SR | Injected input current on any pin during overload condition | — | -5 | 5 | mA |
| I_{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | mA |
| TV_{DD} | SR | V_{DD} slope to ensure correct power up ⁶ | — | — | 0.25 | V/ μ s |
| $T_{A\ C-Grade\ Part}$ | SR | Ambient temperature under bias | $f_{CPU} \leq 48\text{ MHz}$ | -40 | 85 | °C |
| $T_{J\ C-Grade\ Part}$ | SR | Junction temperature under bias | | -40 | 110 | |
| $T_{A\ V-Grade\ Part}$ | SR | Ambient temperature under bias | | -40 | 105 | |
| $T_{J\ V-Grade\ Part}$ | SR | Junction temperature under bias | | -40 | 130 | |
| $T_{A\ M-Grade\ Part}$ | SR | Ambient temperature under bias | | -40 | 125 | |
| $T_{J\ M-Grade\ Part}$ | SR | Junction temperature under bias | | -40 | 150 | |

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

³ 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

⁴ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁵ Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL} , device is reset.

⁶ Guaranteed by device validation

Table 12. Recommended operating conditions (5.0 V)

| Symbol | C | Parameter | Conditions | Value | | Unit |
|----------|----|-------------------------------|------------|-------|-----|------|
| | | | | Min | Max | |
| V_{SS} | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |

Table 12. Recommended operating conditions (5.0 V) (continued)

| Symbol | C | Parameter | Conditions | Value | | Unit |
|------------------------|----|---|------------------------------|----------------|----------------|--------------------|
| | | | | Min | Max | |
| V_{DD}^1 | SR | Voltage on VDD_HV pins with respect to ground (V_{SS}) | — | 4.5 | 5.5 | V |
| | | | Voltage drop ² | 3.0 | 5.5 | |
| $V_{SS_LV}^3$ | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | $V_{SS} + 0.1$ | V |
| $V_{DD_BV}^4$ | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS}) | — | 4.5 | 5.5 | V |
| | | | Voltage drop ⁽²⁾ | 3.0 | 5.5 | |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{SS_ADC} | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | $V_{SS} + 0.1$ | V |
| $V_{DD_ADC}^5$ | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS}) | — | 4.5 | 5.5 | V |
| | | | Voltage drop ⁽²⁾ | 3.0 | 5.5 | |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{IN} | SR | Voltage on any GPIO pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | — | V |
| | | | Relative to V_{DD} | — | $V_{DD} + 0.1$ | |
| I_{INJPAD} | SR | Injected input current on any pin during overload condition | — | -5 | 5 | mA |
| I_{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | mA |
| TV_{DD} | SR | V_{DD} slope to ensure correct power up ⁶ | — | — | 0.25 | V/ μ s |
| $T_{A\ C-Grade\ Part}$ | SR | Ambient temperature under bias | $f_{CPU} \leq 48\text{ MHz}$ | -40 | 85 | $^{\circ}\text{C}$ |
| $T_{J\ C-Grade\ Part}$ | SR | Junction temperature under bias | | -40 | 110 | |
| $T_{A\ V-Grade\ Part}$ | SR | Ambient temperature under bias | | -40 | 105 | |
| $T_{J\ V-Grade\ Part}$ | SR | Junction temperature under bias | | -40 | 130 | |
| $T_{A\ M-Grade\ Part}$ | SR | Ambient temperature under bias | | -40 | 125 | |
| $T_{J\ M-Grade\ Part}$ | SR | Junction temperature under bias | | -40 | 150 | |

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.6 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

⁴ 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁶ Guaranteed by device validation

NOTE

SRAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 13. LQFP thermal characteristics¹

| Symbol | C | D | Parameter | Conditions ² | | Value | Unit |
|-----------------|----|---|--|-------------------------|---------|-------|------|
| $R_{\theta JA}$ | CC | D | Thermal resistance, junction-to-ambient natural convection ³ | Single-layer board — 1s | LQFP64 | 72.1 | °C/W |
| | | | | | LQFP100 | 65.2 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 57.3 | |
| | | | | | LQFP100 | 51.8 | |
| $R_{\theta JB}$ | CC | D | Thermal resistance, junction-to-board ⁴ | Four-layer board — 2s2p | LQFP64 | 44.1 | °C/W |
| | | | | | LQFP100 | 41.3 | |
| $R_{\theta JC}$ | CC | D | Thermal resistance, junction-to-case ⁵ | Single-layer board — 1s | LQFP64 | 26.5 | °C/W |
| | | | | | LQFP100 | 23.9 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 26.2 | |
| | | | | | LQFP100 | 23.7 | |
| Ψ_{JB} | CC | D | Junction-to-board thermal characterization parameter, natural convection | Single-layer board — 1s | LQFP64 | 41 | °C/W |
| | | | | | LQFP100 | 41.6 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 43 | |
| | | | | | LQFP100 | 43.4 | |
| Ψ_{JC} | CC | D | Junction-to-case thermal characterization parameter, natural convection | Single-layer board — 1s | LQFP64 | 11.5 | °C/W |
| | | | | | LQFP100 | 10.4 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 11.1 | |
| | | | | | LQFP100 | 10.2 | |

¹ Thermal characteristics are targets based on simulation that are subject to change per device characterization.

² $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$

³ Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-7. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} .

⁴ Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB} .

⁵ Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC} .

4.6.2 Power considerations

The average chip-junction temperature, T_J , in degrees Celsius, may be calculated using [Equation 1](#):

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \text{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD} , expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ °C}) \quad \text{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273 \text{ °C}) + R_{\theta JA} \times P_D^2 \quad \text{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from [Equation 3](#) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A .

4.7 I/O pad electrical characteristics

4.7.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Input only pads—These pads are associated to ADC channels (ADC_P[X]) providing low input leakage.

Medium pads can use slow configuration to reduce electromagnetic emission except for PC[1], that is medium only, at the cost of reducing AC performance.

4.7.2 I/O input DC characteristics

[Table 14](#) provides input DC electrical characteristics as described in [Figure 4](#).

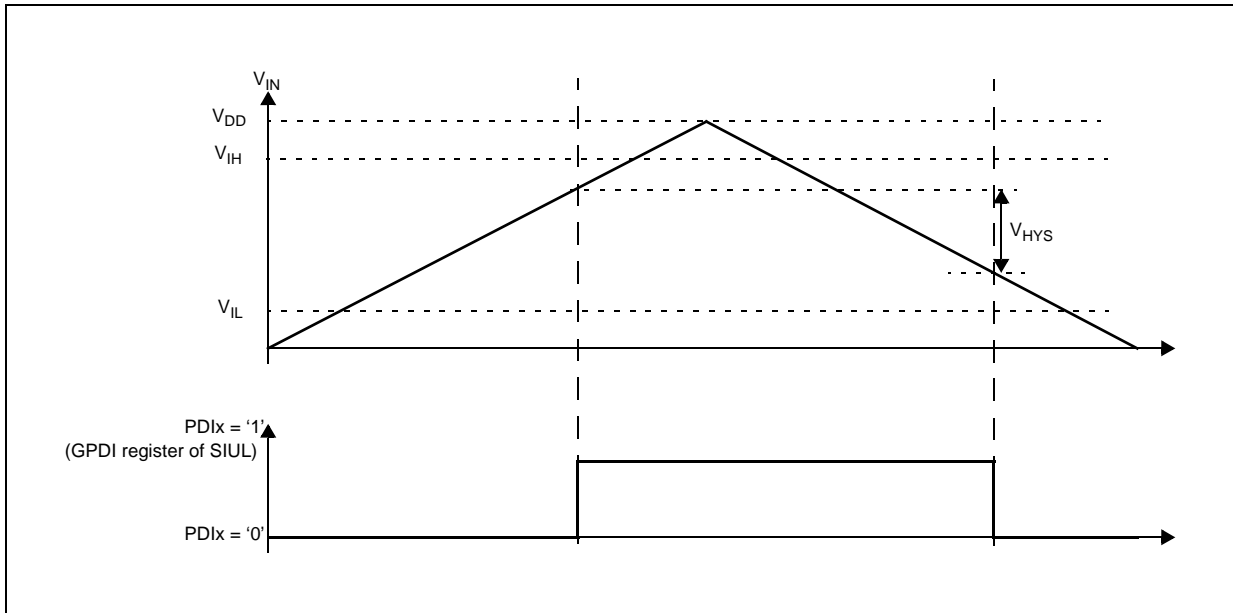


Figure 4. Input DC electrical characteristics definition

Table 14. I/O input DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|---------------------------------|----|-----------|---|------------------------------|-------------------------|-----|----------------------|------|----|
| | | | | Min | Typ | Max | | | |
| V _{IH} | SR | P | Input high level CMOS (Schmitt Trigger) | — | 0.65V _{DD} | — | V _{DD} +0.4 | V | |
| V _{IL} | SR | P | Input low level CMOS (Schmitt Trigger) | — | -0.4 | — | 0.35V _{DD} | V | |
| V _{HYS} | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | 0.1V _{DD} | — | — | V | |
| I _{LKG} | CC | D | Digital input leakage | No injection on adjacent pin | T _A = -40 °C | — | 2 | 200 | nA |
| | | | | | T _A = 25 °C | — | 2 | 200 | |
| | | | | | T _A = 85 °C | — | 5 | 300 | |
| | | | | | T _A = 105 °C | — | 12 | 500 | |
| | | | | | T _A = 125 °C | — | 70 | 1000 | |
| W _{FI} ² | SR | P | Digital input filtered pulse | — | — | — | 40 | ns | |
| W _{NFI} ⁽²⁾ | SR | P | Digital input not filtered pulse | — | 1000 | — | — | ns | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- [Table 15](#) provides weak pull figures. Both pull-up and pull-down resistances are supported.

- Table 16 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 17 provides output driver characteristics for I/O pads when in MEDIUM configuration.

Table 15. I/O pull-up/pull-down DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------------|----|---|---|----------------------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{WPU} | CC | P Weak pull-up current absolute value | V _{IN} = V _{IL} , V _{DD} = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | μA |
| | | | | PAD3V5V = 1 ² | 10 | — | 250 | |
| | | | V _{IN} = V _{IL} , V _{DD} = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |
| I _{WPD} | CC | P Weak pull-down current absolute value | V _{IN} = V _{IH} , V _{DD} = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | μA |
| | | | | PAD3V5V = 1 ⁽²⁾ | 10 | — | 250 | |
| | | | V _{IN} = V _{IH} , V _{DD} = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 16. SLOW configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-----------------|----|--|-------------------------|---|-----------------------|-----|--------------------|---|
| | | | | Min | Typ | Max | | |
| V _{OH} | CC | P Output high level SLOW configuration | Push Pull | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | — | — | V |
| | | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | — | — | |
| | | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} - 0.8 | — | — | |
| V _{OL} | CC | P Output low level SLOW configuration | Push Pull | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1V _{DD} | V |
| | | | | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽²⁾ | — | — | 0.1V _{DD} | |
| | | | | I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-----------------|----|--|-------------------------|---|-----------------------|-----|--------------------|---|
| | | | | Min | Typ | Max | | |
| V _{OH} | CC | Output high level MEDIUM configuration | Push Pull | I _{OH} = -3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | — | — | V |
| | | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | — | — | |
| | | | | I _{OH} = -1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | — | — | |
| | | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} - 0.8 | — | — | |
| | | | | I _{OH} = -100 μA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | — | — | |
| V _{OL} | CC | Output low level MEDIUM configuration | Push Pull | I _{OL} = 3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 0.2V _{DD} | V |
| | | | | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1V _{DD} | |
| | | | | I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽²⁾ | — | — | 0.1V _{DD} | |
| | | | | I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |
| | | | | I _{OL} = 100 μA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 0.1V _{DD} | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

4.7.4 Output pin transition times

Table 18. Output pin transition times

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-----------------|----|---|-------------------------|---|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| t _{tr} | CC | D Output transition time output pin ² SLOW configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 50 | ns |
| | | | C _L = 50 pF | | — | — | 100 | |
| | | | C _L = 100 pF | | — | — | 125 | |
| | | D Output transition time output pin ² MEDIUM configuration | C _L = 25 pF | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 50 | |
| | | | C _L = 50 pF | | — | — | 100 | |
| | | | C _L = 100 pF | | — | — | 125 | |
| t _{tr} | CC | D Output transition time output pin ⁽²⁾ MEDIUM configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1 | — | — | 10 | ns |
| | | | C _L = 50 pF | | — | — | 20 | |
| | | | C _L = 100 pF | | — | — | 40 | |
| | | D Output transition time output pin ⁽²⁾ SLOW configuration | C _L = 25 pF | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1 | — | — | 12 | |
| | | | C _L = 50 pF | | — | — | 25 | |
| | | | C _L = 100 pF | | — | — | 40 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in [Table 19](#).

[Table 20](#) provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 19. I/O supply segment

| Package | Supply segment | | | |
|----------|-----------------|-----------------|-----------------|-----------------|
| | 1 | 2 | 3 | 4 |
| 100 LQFP | pin 16 – pin 35 | pin 37 – pin 69 | pin 70 – pin 83 | pin 84 – pin 15 |
| 64 LQFP | pin 8 – pin 26 | pin 28 – pin 55 | pin 56 – pin 7 | — |

Table 20. I/O consumption

| Symbol | C | Parameter | Conditions ¹ | | Value | | | Unit | |
|--------------------|----|-----------|---|---|--|-----|-----|------|----|
| | | | | | Min | Typ | Max | | |
| I_{SWTSLW}^{2} | CC | D | Dynamic I/O current for SLOW configuration | $C_L = 25 \text{ pF}$ | $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ | — | — | 20 | mA |
| | | | | | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | — | — | 16 | |
| $I_{SWTMED}^{(2)}$ | CC | D | Dynamic I/O current for MEDIUM configuration | $C_L = 25 \text{ pF}$ | $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ | — | — | 29 | mA |
| | | | | | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | — | — | 17 | |
| I_{RMSLW} | CC | D | Root mean square I/O current for SLOW configuration | $C_L = 25 \text{ pF}, 2 \text{ MHz}$ | $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ | — | — | 2.3 | mA |
| | | | | $C_L = 25 \text{ pF}, 4 \text{ MHz}$ | | | | 3.2 | |
| | | | | $C_L = 100 \text{ pF}, 2 \text{ MHz}$ | | | | 6.6 | |
| | | | | $C_L = 25 \text{ pF}, 2 \text{ MHz}$ | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | — | — | 1.6 | |
| | | | | $C_L = 25 \text{ pF}, 4 \text{ MHz}$ | | | | 2.3 | |
| | | | | $C_L = 100 \text{ pF}, 2 \text{ MHz}$ | | | | 4.7 | |
| I_{RMSMED} | CC | D | Root mean square I/O current for MEDIUM configuration | $C_L = 25 \text{ pF}, 13 \text{ MHz}$ | $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ | — | — | 6.6 | mA |
| | | | | $C_L = 25 \text{ pF}, 40 \text{ MHz}$ | | | | 13.4 | |
| | | | | $C_L = 100 \text{ pF}, 13 \text{ MHz}$ | | | | 18.3 | |
| | | | | $C_L = 25 \text{ pF}, 13 \text{ MHz}$ | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | — | — | 5 | |
| | | | | $C_L = 25 \text{ pF}, 40 \text{ MHz}$ | | | | 8.5 | |
| | | | | $C_L = 100 \text{ pF}, 13 \text{ MHz}$ | | | | 11 | |
| I_{AVGSEG} | SR | D | Sum of all the static I/O current within a supply segment | $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ | | — | — | 70 | mA |
| | | | | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | | | | 65 | |

¹ $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$, unless otherwise specified

² Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 21 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 21. I/O weight¹

| Pad | 100 LQFP/64 LQFP | | | |
|--------|----------------------|---------|--------------|---------|
| | Weight 5 V | | Weight 3.3 V | |
| | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| PB[3] | 9% | 9% | 10% | 10% |
| PC[9] | 8% | 8% | 10% | 10% |
| PC[14] | 8% | 8% | 10% | 10% |
| PC[15] | 8% | 11% | 9% | 10% |
| PA[2] | 8% | 8% | 9% | 9% |
| PE[0] | 7% | 7% | 9% | 9% |
| PA[1] | 7% | 7% | 8% | 8% |
| PE[1] | 7% | 10% | 8% | 8% |
| PE[8] | 6% | 9% | 8% | 8% |
| PE[9] | 6% | 6% | 7% | 7% |
| PE[10] | 6% | 6% | 7% | 7% |
| PA[0] | 5% | 7% | 6% | 7% |
| PE[11] | 5% | 5% | 6% | 6% |
| PC[11] | 7% | 7% | 9% | 9% |
| PC[10] | 8% | 11% | 9% | 10% |
| PB[0] | 8% | 11% | 9% | 10% |
| PB[1] | 8% | 8% | 10% | 10% |
| PC[6] | 8% | 8% | 10% | 10% |
| PC[7] | 8% | 8% | 10% | 10% |
| PA[15] | 8% | 11% | 9% | 10% |
| PA[14] | 7% | 11% | 9% | 9% |
| PA[4] | 7% | 7% | 8% | 8% |
| PA[13] | 7% | 10% | 8% | 9% |
| PA[12] | 7% | 7% | 8% | 8% |
| PB[9] | 1% | 1% | 1% | 1% |
| PB[8] | 1% | 1% | 1% | 1% |
| PB[10] | 5% | 5% | 6% | 6% |
| PD[0] | 1% | 1% | 1% | 1% |
| PD[1] | 1% | 1% | 1% | 1% |
| PD[2] | 1% | 1% | 1% | 1% |
| PD[3] | 1% | 1% | 1% | 1% |
| PD[4] | 1% | 1% | 1% | 1% |

Table 21. I/O weight¹ (continued)

| Pad | 100 LQFP/64 LQFP | | | |
|--------|----------------------|---------|--------------|---------|
| | Weight 5 V | | Weight 3.3 V | |
| | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| PD[5] | 1% | 1% | 1% | 1% |
| PD[6] | 1% | 1% | 1% | 1% |
| PD[7] | 1% | 1% | 1% | 1% |
| PD[8] | 1% | 1% | 1% | 1% |
| PB[4] | 1% | 1% | 1% | 1% |
| PB[5] | 1% | 1% | 1% | 1% |
| PB[6] | 1% | 1% | 1% | 1% |
| PB[7] | 1% | 1% | 1% | 1% |
| PD[9] | 1% | 1% | 1% | 1% |
| PD[10] | 1% | 1% | 1% | 1% |
| PD[11] | 1% | 1% | 1% | 1% |
| PB[11] | 9% | 9% | 11% | 11% |
| PD[12] | 8% | 8% | 10% | 10% |
| PB[12] | 8% | 8% | 10% | 10% |
| PD[13] | 8% | 8% | 9% | 9% |
| PB[13] | 8% | 8% | 9% | 9% |
| PD[14] | 7% | 7% | 9% | 9% |
| PB[14] | 7% | 7% | 8% | 8% |
| PD[15] | 7% | 7% | 8% | 8% |
| PB[15] | 6% | 6% | 7% | 7% |
| PA[3] | 6% | 6% | 7% | 7% |
| PA[7] | 4% | 4% | 5% | 5% |
| PA[8] | 4% | 4% | 5% | 5% |
| PA[9] | 4% | 4% | 5% | 5% |
| PA[10] | 5% | 5% | 6% | 6% |
| PA[11] | 5% | 5% | 6% | 6% |
| PE[12] | 5% | 5% | 6% | 6% |
| PC[3] | 5% | 5% | 6% | 6% |
| PC[2] | 5% | 7% | 6% | 6% |
| PA[5] | 5% | 6% | 5% | 6% |
| PA[6] | 4% | 4% | 5% | 5% |
| PC[1] | 5% | 17% | 4% | 12% |

Table 21. I/O weight¹ (continued)

| Pad | 100 LQFP/64 LQFP | | | |
|--------|----------------------|---------|--------------|---------|
| | Weight 5 V | | Weight 3.3 V | |
| | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| PC[0] | 6% | 9% | 7% | 8% |
| PE[2] | 7% | 10% | 8% | 9% |
| PE[3] | 7% | 10% | 9% | 9% |
| PC[5] | 8% | 11% | 9% | 10% |
| PC[4] | 8% | 11% | 9% | 10% |
| PE[4] | 8% | 12% | 10% | 10% |
| PE[5] | 8% | 12% | 10% | 11% |
| PE[6] | 9% | 12% | 10% | 11% |
| PE[7] | 9% | 12% | 10% | 11% |
| PC[12] | 9% | 13% | 11% | 11% |
| PC[13] | 9% | 9% | 11% | 11% |
| PC[8] | 9% | 9% | 11% | 11% |
| PB[2] | 9% | 13% | 11% | 12% |

¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified

² SRC: "Slew Rate Control" bit in SIU_PCR

4.8 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

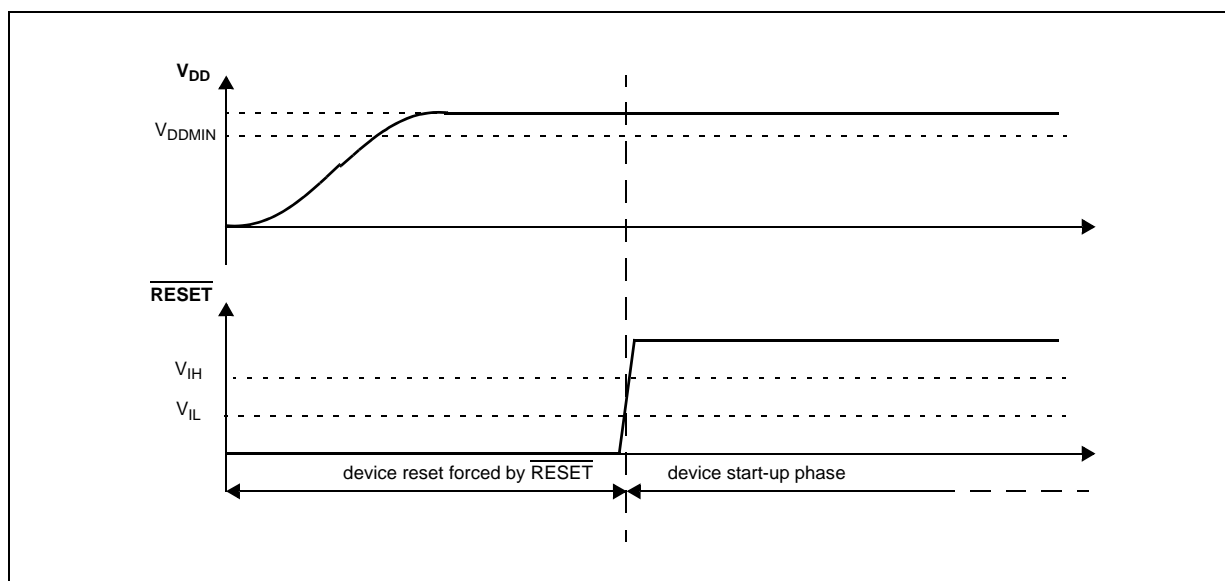


Figure 5. Start-up reset requirements

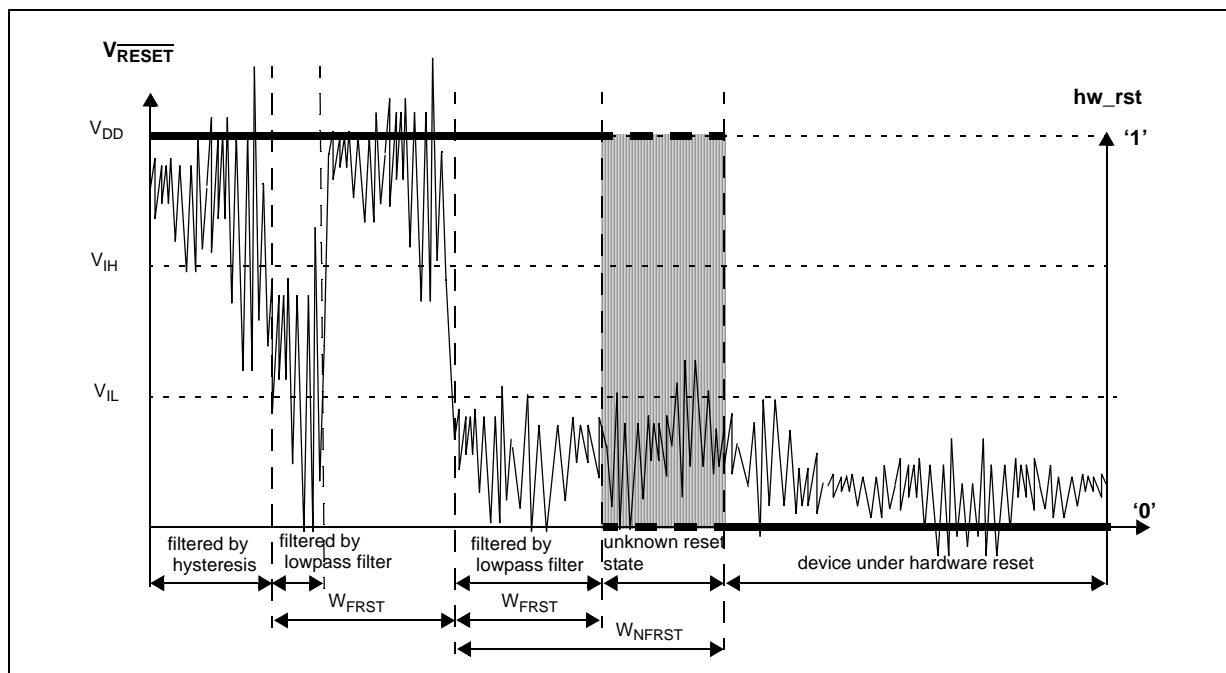


Figure 6. Noise filtering on reset signal

Table 22. Reset electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-----------|----|-----------|---|---|-----|----------------|-------------|---|
| | | | | Min | Typ | Max | | |
| V_{IH} | SR | P | Input High Level CMOS (Schmitt Trigger) | $0.65V_{DD}$ | — | $V_{DD} + 0.4$ | V | |
| V_{IL} | SR | P | Input low Level CMOS (Schmitt Trigger) | -0.4 | — | $0.35V_{DD}$ | V | |
| V_{HYS} | CC | C | Input hysteresis CMOS (Schmitt Trigger) | $0.1V_{DD}$ | — | — | V | |
| V_{OL} | CC | P | Output low level | Push Pull, $I_{OL} = 2$ mA, $V_{DD} = 5.0$ V $\pm 10\%$, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | V |
| | | | | Push Pull, $I_{OL} = 1$ mA, $V_{DD} = 5.0$ V $\pm 10\%$, PAD3V5V = 1 ² | — | — | $0.1V_{DD}$ | |
| | | | | Push Pull, $I_{OL} = 1$ mA, $V_{DD} = 3.3$ V $\pm 10\%$, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

Table 22. Reset electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|-------------|----|--|---|-------|-----|-----|---------------|
| | | | | Min | Typ | Max | |
| t_{tr} | CC | D Output transition time output pin ³ MEDIUM configuration | $C_L = 25 \text{ pF}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, PAD3V5V = 0 | — | — | 10 | ns |
| | | | $C_L = 50 \text{ pF}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, PAD3V5V = 0 | — | — | 20 | |
| | | | $C_L = 100 \text{ pF}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, PAD3V5V = 0 | — | — | 40 | |
| | | | $C_L = 25 \text{ pF}$, $V_{DD} = 3.3 \text{ V} \pm 10\%$, PAD3V5V = 1 | — | — | 12 | |
| | | | $C_L = 50 \text{ pF}$, $V_{DD} = 3.3 \text{ V} \pm 10\%$, PAD3V5V = 1 | — | — | 25 | |
| | | | $C_L = 100 \text{ pF}$, $V_{DD} = 3.3 \text{ V} \pm 10\%$, PAD3V5V = 1 | — | — | 40 | |
| W_{FRST} | SR | P $\overline{\text{RESET}}$ input filtered pulse | — | — | — | 40 | ns |
| W_{NFRST} | SR | P $\overline{\text{RESET}}$ input not filtered pulse | — | 1000 | — | — | ns |
| I_{WPU} | CC | P Weak pull-up current absolute value | $V_{DD} = 3.3 \text{ V} \pm 10\%$, PAD3V5V = 1 | 10 | — | 150 | μA |
| | | | $V_{DD} = 5.0 \text{ V} \pm 10\%$, PAD3V5V = 0 | 10 | — | 150 | |
| | | | $V_{DD} = 5.0 \text{ V} \pm 10\%$, PAD3V5V = 1 ⁴ | 10 | — | 250 | |

¹ $V_{DD} = 3.3 \text{ V} \pm 10\%$ / $5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$, unless otherwise specified

² This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).

³ C_L includes device and package capacitance ($C_{PKG} < 5 \text{ pF}$).

⁴ The configuration PAD3V5 = 1 when $V_{DD} = 5 \text{ V}$ is only transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

4.9 Power management electrical characteristics

4.9.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV} . The regulator itself is supplied by the common I/O supply V_{DD} . The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD} .
- LV: Low voltage internal power supply for core, FMPLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
 - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.

Electrical characteristics

- LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
- LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
- LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.



Figure 7. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see [Section 4.5, Recommended operating conditions](#)).

Table 23. Voltage regulator electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|------------|----|--|----------------------------|-------|-----|-----|----------|
| | | | | Min | Typ | Max | |
| C_{REGn} | SR | Internal voltage regulator external capacitance | — | 200 | — | 500 | nF |
| R_{REG} | SR | Stability capacitor equivalent serial resistance | Range: 10 kHz to 20 MHz | — | — | 0.2 | Ω |

Table 23. Voltage regulator electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|------------------------|----|--|---|------------------|------------------|------------------|------|
| | | | | Min | Typ | Max | |
| C _{DEC1} | SR | Decoupling capacitance ² ballast | V _{DD_BV} /V _{SS_LV} pair: V _{DD_BV} = 4.5 V to 5.5 V | 100 ³ | 470 ⁴ | — | nF |
| | | | V _{DD_BV} /V _{SS_LV} pair: V _{DD_BV} = 3 V to 3.6 V | 400 | | — | |
| C _{DEC2} | SR | Decoupling capacitance regulator supply | V _{DD} /V _{SS} pair | 10 | 100 | — | nF |
| V _{MREG} | CC | Main regulator output voltage | Before exiting from reset | — | 1.32 | — | V |
| | | | After trimming | 1.16 | 1.28 | — | |
| I _{MREG} | SR | Main regulator current provided to V _{DD_LV} domain | — | — | — | 150 | mA |
| I _{MREGINT} | CC | Main regulator module current consumption | I _{MREG} = 200 mA | — | — | 2 | mA |
| | | | I _{MREG} = 0 mA | — | — | 1 | |
| V _{LPREG} | CC | Low-power regulator output voltage | After trimming | 1.16 | 1.28 | — | V |
| I _{LPREG} | SR | Low power regulator current provided to V _{DD_LV} domain | — | — | — | 15 | mA |
| I _{LPREGINT} | CC | Low-power regulator module current consumption | I _{LPREG} = 15 mA; T _A = 55 °C | — | — | 600 | μA |
| | | | I _{LPREG} = 0 mA; T _A = 55 °C | — | 5 | — | |
| V _{ULPREG} | CC | Ultra low power regulator output voltage | After trimming | 1.16 | 1.28 | — | V |
| I _{ULPREG} | SR | Ultra low power regulator current provided to V _{DD_LV} domain | — | — | — | 5 | mA |
| I _{ULPREGINT} | CC | Ultra low power regulator module current consumption | I _{ULPREG} = 5 mA; T _A = 55 °C | — | — | 100 | μA |
| | | | I _{ULPREG} = 0 mA; T _A = 55 °C | — | 2 | — | |
| I _{DD_BV} | CC | In-rush average current on V _{DD_BV} during power-up ⁵ | — | — | — | 300 ⁶ | mA |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

³ This value is acceptable to guarantee operation from 4.5 V to 5.5 V.

⁴ External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

⁵ In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 μs, depending on external capacitances to be loaded).

⁶ The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

4.9.2 Low voltage detector electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as five low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27_VREG in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the $5.0\text{ V} \pm 10\%$ range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)



Figure 8. Low voltage detector vs reset

Table 24. Low voltage detector electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------------------|----|-----------|---|---|------|-----|------|---|
| | | | | Min | Typ | Max | | |
| V _{PORUP} | SR | P | Supply for functional POR module | T _A = 25 °C, after trimming | 1.0 | — | 5.5 | V |
| V _{PORH} | CC | P | Power-on reset threshold | | 1.5 | — | 2.6 | V |
| V _{LVDHV3H} | CC | T | LVDHV3 low voltage detector high threshold | | — | — | 2.95 | V |
| V _{LVDHV3L} | CC | P | LVDHV3 low voltage detector low threshold | | 2.6 | — | 2.9 | V |
| V _{LVDHV3BH} | CC | P | LVDHV3B low voltage detector high threshold | | — | — | 2.95 | V |
| V _{LVDHV3BL} | CC | P | LVDHV3B low voltage detector low threshold | | 2.6 | — | 2.9 | V |
| V _{LVDHV5H} | CC | T | LVDHV5 low voltage detector high threshold | | — | — | 4.5 | V |
| V _{LVDHV5L} | CC | P | LVDHV5 low voltage detector low threshold | | 3.8 | — | 4.4 | V |
| V _{LVDLVCORL} | CC | P | LVDLVCOR low voltage detector low threshold | | 1.08 | — | 1.16 | V |
| V _{LVDLVBKPL} | CC | P | LVDLVBKP low voltage detector low threshold | | 1.08 | — | 1.16 | V |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.10 Power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 25. Power consumption on VDD_BV and VDD_HV

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|---------------------------------|----|-----------|---|---|-------------------------|------------------|------|-------------------|----|
| | | | | Min | Typ | Max | | | |
| I _{DDMAX} ² | CC | D | RUN mode maximum average current | — | 90 | 130 ³ | mA | | |
| I _{DDRUN} ⁴ | CC | T | RUN mode typical average current ⁵ | f _{CPU} = 8 MHz | — | 7 | — | mA | |
| | | | | f _{CPU} = 16 MHz | — | 18 | — | | |
| | | | | f _{CPU} = 32 MHz | — | 29 | — | | |
| | | | | f _{CPU} = 48 MHz | — | 40 | 100 | | |
| I _{DDHALT} | CC | C | HALT mode current ⁶ | Slow internal RC oscillator (128 kHz) running | T _A = 25 °C | — | 8 | 15 | mA |
| | | | | | T _A = 125 °C | — | 14 | 25 | |
| I _{DDSTOP} | CC | P | STOP mode current ⁷ | Slow internal RC oscillator (128 kHz) running | T _A = 25 °C | — | 180 | 700 ⁸ | μA |
| | | | | | T _A = 55 °C | — | 500 | — | |
| | | | | | T _A = 85 °C | — | 1 | 6 ⁽⁸⁾ | mA |
| | | | | | T _A = 105 °C | — | 2 | 9 ⁽⁸⁾ | |
| | | | | | T _A = 125 °C | — | 4.5 | 12 ⁽⁸⁾ | |

Table 25. Power consumption on VDD_BV and VDD_HV (continued) (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|----------------------|----|-----------|-----------------------------------|---|-------------------------|-----|------|------|----|
| | | | | Min | Typ | Max | | | |
| I _{DDSTDBY} | CC | P | STANDBY mode current ⁹ | Slow internal RC oscillator (128 kHz) running | T _A = 25 °C | — | 30 | 100 | μA |
| | | | | | T _A = 55 °C | — | 75 | — | |
| | | | | | T _A = 85 °C | — | 180 | 700 | |
| | | | | | T _A = 105 °C | — | 315 | 1000 | |
| | | | | | T _A = 125 °C | — | 560 | 1700 | |
| | | D | | | | | | | |
| | | D | | | | | | | |
| | | P | | | | | | | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

³ Higher current may be sunk by device during power-up and standby exit. Please refer to in-rush average current on [Table 23](#).

⁴ RUN current measured with typical application with accesses on both flash memory and SRAM.

⁵ Only for the “P” classification: Code fetched from SRAM: serial IPs CAN and LIN in loop-back mode, DSPI as Master, PLL as system clock (3 × Multiplier) peripherals on (eMIOS/CTU/ADC) and running at maximum frequency, periodic SW/WDG timer reset enabled.

⁶ Data flash power down. Code flash in low power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: 0 ON (clocked but no reception or transmission). LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.

⁷ Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPVreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

⁸ When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

⁹ Only for the “P” classification: ULPVreg on, HP/LPVreg off, 16 KB SRAM on, device configured for minimum consumption, all possible modules switched off.

4.11 Flash memory electrical characteristics

The data flash operation depends strongly on the code flash operation. If code flash is switched-off, the data flash is disabled.

4.11.1 Program/Erase characteristics

[Table 26](#) shows the program and erase characteristics.

Table 26. Program and erase specifications (code flash)

| Symbol | C | Parameter | Value | | | | Unit | |
|-------------------|----|-----------|---|------------------|--------------------------|------------------|------|---------|
| | | | Min | Typ ¹ | Initial max ² | Max ³ | | |
| $t_{dwprogram}$ | CC | C | Double word (64 bits) program time ⁴ | — | 22 | 50 | 500 | μ s |
| $t_{16Kpperase}$ | CC | C | 16 KB block preprogram and erase time | — | 300 | 500 | 5000 | ms |
| $t_{32Kpperase}$ | CC | C | 32 KB block preprogram and erase time | — | 400 | 600 | 5000 | ms |
| $t_{128Kpperase}$ | CC | C | 128 KB block preprogram and erase time | — | 800 | 1300 | 7500 | ms |
| t_{esus} | CC | C | Erase suspend latency | — | — | 30 | 30 | μ s |

¹ Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

² Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

³ The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

⁴ Actual hardware programming times. This does not include software overhead.

Table 27. Program and erase specifications (data flash)

| Symbol | C | Parameter | Value | | | | Unit | |
|------------------|----|-----------|---|------------------|--------------------------|------------------|------|---------|
| | | | Min | Typ ¹ | Initial max ² | Max ³ | | |
| $t_{swprogram}$ | CC | C | Single word (32 bits) program time ⁴ | — | 30 | 70 | 300 | μ s |
| $t_{16Kpperase}$ | CC | C | 16 KB block preprogram and erase time | — | 700 | 800 | 1500 | ms |
| t_{Bank_D} | CC | C | 64 KB block preprogram and erase time | — | 1900 | 2300 | 4800 | ms |

¹ Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

² Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

³ The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

⁴ Actual hardware programming times. This does not include software overhead.

Table 28. Flash module life

| Symbol | C | Parameter | Conditions | Value | | | Unit |
|-----------|----|---|---------------------------------------|---------|---------|-----|--------|
| | | | | Min | Typ | Max | |
| P/E | CC | Number of program/erase cycles per block over the operating temperature range (T _J) | 16 KB blocks | 100,000 | — | — | cycles |
| | | | 32 KB blocks | 10,000 | 100,000 | — | cycles |
| | | | 128 KB blocks | 1,000 | 100,000 | — | cycles |
| Retention | CC | Minimum data retention at 85 °C average ambient temperature ¹ | Blocks with 0–1,000 P/E cycles | 20 | — | — | years |
| | | | Blocks with 1,001–10,000 P/E cycles | 10 | — | — | |
| | | | Blocks with 10,001–100,000 P/E cycles | 5 | — | — | |

¹ Ambient temperature averaged over application duration. It is recommended not to exceed the product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing

| Symbol | C | Parameter | Conditions ¹ | Max | Unit |
|---------------------|----|--|-------------------------|-----|------|
| f _{CFREAD} | CC | Maximum working frequency for reading code flash memory at given number of wait states in worst conditions | 2 wait states | 48 | MHz |
| | | | 0 wait states | 20 | |
| f _{DFREAD} | CC | Maximum working frequency for reading data flash memory at given number of wait states in worst conditions | 6 wait states | 48 | MHz |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 30 shows the power supply DC characteristics on external supply.

NOTE

Power supply for data flash is actually provided by code flash; this means that data flash cannot work if code flash is not powered.

Table 30. Flash power supply DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|---------------------|----|--|--|------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{CFREAD} | CC | Sum of the current consumption on V _{DDHV} and V _{DDBV} on read access | Flash module read f _{CPU} = 48 MHz | Code flash | — | — | 33 | mA |
| I _{DFREAD} | CC | | | Data flash | — | — | 4 | |
| I _{CFMOD} | CC | Sum of the current consumption on V _{DDHV} and V _{DDBV} on matrix modification (program/erase) | Program/Erase on-going while reading flash registers, f _{CPU} = 48 MHz | Code flash | — | — | 33 | mA |
| I _{DFMOD} | CC | | | Data flash | — | — | 6 | |

Table 30. Flash power supply DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|--------------------|----|-----------|--|------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{FLPW} | CC | D | Sum of the current consumption on V _{DDHV} and V _{DDBV} during flash low-power mode | — | — | 910 | μA | |
| I _{CFPWD} | CC | D | Sum of the current consumption on V _{DDHV} and V _{DDBV} during flash power-down mode | Code flash | — | — | 125 | μA |
| I _{DFPWD} | CC | D | | Data flash | — | — | 25 | μA |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.11.3 Start-up/Switch-off timings

Table 31. Start-up time/Switch-off time

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-------------------------|----|-----------|--|------------|-----|-----|------------------|----|
| | | | | Min | Typ | Max | | |
| t _{FLARSTEXIT} | CC | T | Delay for flash module to exit reset mode | Code flash | — | — | 125 | μs |
| | | | | Data flash | — | — | 150 | μs |
| t _{FLALPEXIT} | CC | T | Delay for flash module to exit low-power mode ² | Code flash | — | — | 0.5 | μs |
| t _{FLAPDEXIT} | CC | T | Delay for flash module to exit power-down mode | Code flash | — | — | 30 | μs |
| | | | | Data flash | — | — | 30 ³ | μs |
| t _{FLALPENTRY} | CC | T | Delay for flash module to enter low-power mode | Code flash | — | — | 0.5 | μs |
| t _{FLAPDENTRY} | CC | T | Delay for flash module to enter power-down mode | Code flash | — | — | 1.5 | μs |
| | | | | Data flash | — | — | 4 ⁽³⁾ | μs |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Data flash does not support low-power mode

³ If code flash is already switched-on.

4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:

Electrical characteristics

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.
To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 32. EMI radiated emission measurement^{1 2}

| Symbol | C | Parameter | Conditions | Value | | | Unit | | |
|--------------------|----|-----------------------|------------|---|-----------------------------|------|------|------|------|
| | | | | Min | Typ | Max | | | |
| — | SR | Scan range | — | 0.150 | — | 1000 | MHz | | |
| f _{CPU} | SR | Operating frequency | — | — | 48 | — | MHz | | |
| V _{DD_LV} | SR | LV operating voltages | — | — | 1.28 | — | V | | |
| S _{EMI} | CC | T | Peak level | V _{DD} = 5 V, T _A = 25 °C, 100 LQFP package Test conforming to IEC 61967-2, f _{OSC} = 8 MHz/f _{CPU} = 48 MHz | No PLL frequency modulation | — | — | 18 | dBμV |
| | | | | ± 2% PLL frequency modulation | — | — | 14 | dBμV | |

¹ EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

² For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 33. ESD absolute maximum ratings^{1 2}

| Symbol | | C | Ratings | Conditions | Class | Max value | Unit |
|----------------|----|---|--|--|-------|---------------|------|
| $V_{ESD(HBM)}$ | CC | T | Electrostatic discharge voltage (Human Body Model) | $T_A = 25\text{ °C}$ conforming to AEC-Q100-002 | H1C | 2000 | V |
| $V_{ESD(MM)}$ | CC | T | Electrostatic discharge voltage (Machine Model) | $T_A = 25\text{ °C}$ conforming to AEC-Q100-003 | M2 | 200 | V |
| $V_{ESD(CDM)}$ | CC | T | Electrostatic discharge voltage (Charged Device Model) | $T_A = 25\text{ °C}$ conforming to AEC-Q100-011 | C3A | 500 | V |
| | | | | | | 750 (corners) | V |

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.12.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 34. Latch-up results

| Symbol | | C | Parameter | Conditions | Class |
|--------|----|---|-----------------------|--|------------|
| LU | CC | T | Static latch-up class | $T_A = 125\text{ °C}$ conforming to JESD 78 | II level A |

4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 9 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 35 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

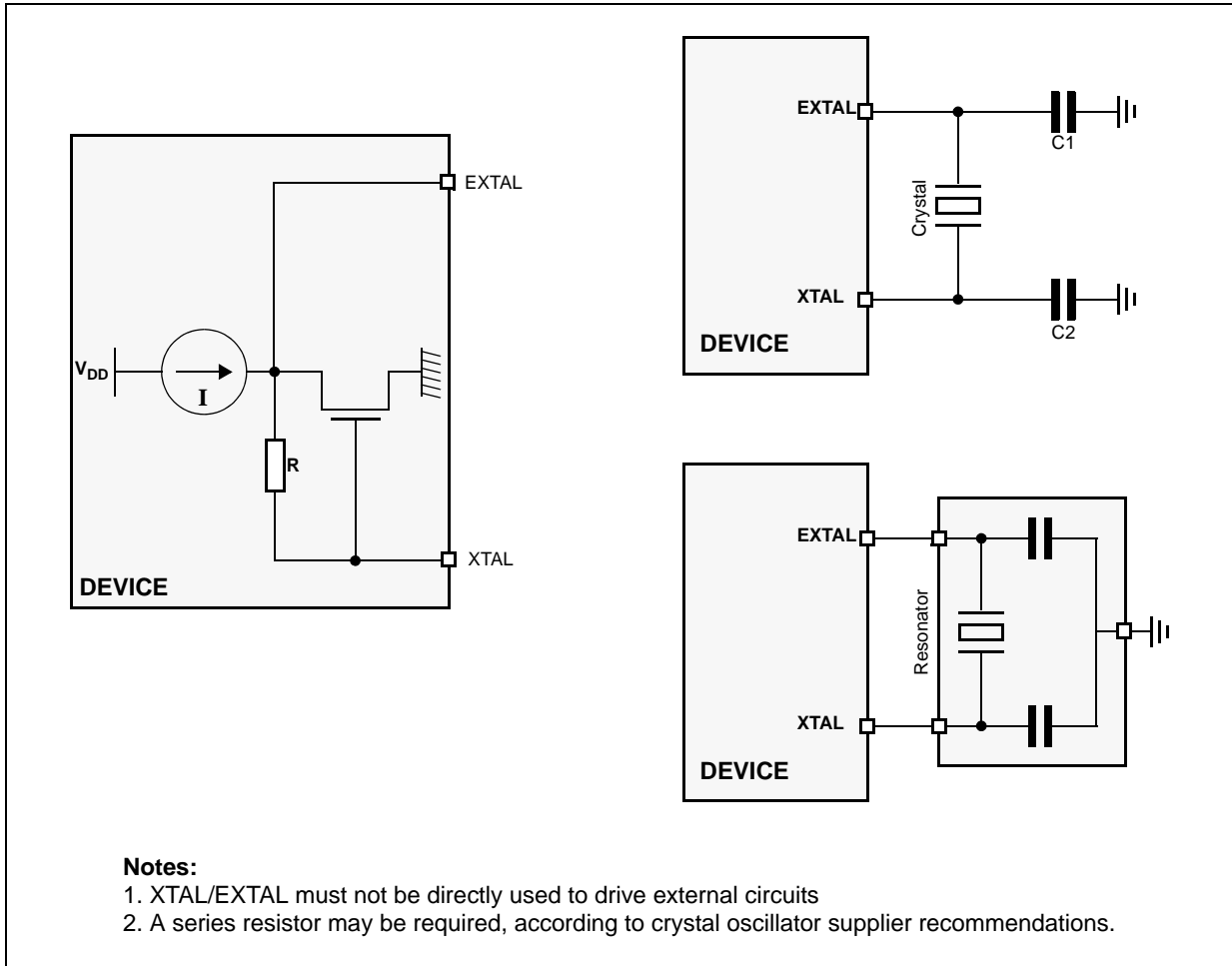


Figure 9. Crystal oscillator and resonator connection scheme

Table 35. Crystal description

| Nominal frequency (MHz) | NDK crystal reference | Crystal equivalent series resistance (ESR) Ω | Crystal motional capacitance (C_m) fF | Crystal motional inductance (L_m) mH | Load on xtalin/xtalout $C_1 = C_2$ (pF) ¹ | Shunt capacitance between xtalout and xtalin C_0^2 (pF) |
|-------------------------|-----------------------|---|---|--|--|---|
| 4 | NX8045GB | 300 | 2.68 | 591.0 | 21 | 2.93 |
| 8 | NX5032GA | 300 | 2.46 | 160.7 | 17 | 3.01 |
| 10 | | 150 | 2.93 | 86.6 | 15 | 2.91 |
| 12 | | 120 | 3.11 | 56.5 | 15 | 2.93 |
| 16 | | 120 | 3.90 | 25.3 | 10 | 3.00 |

¹ The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

² The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

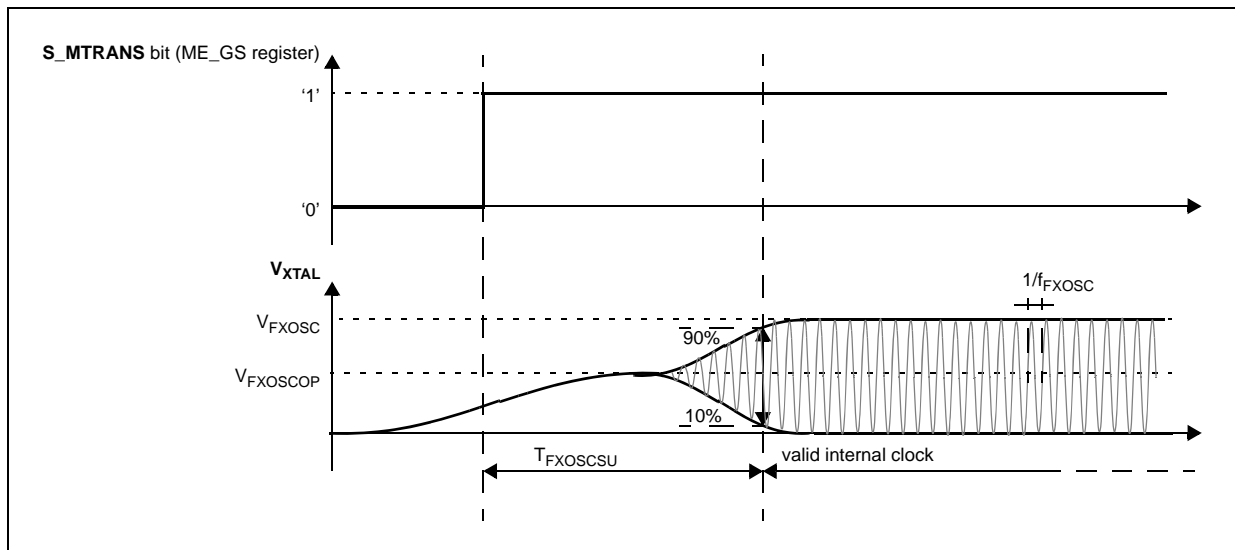


Figure 10. Fast external crystal oscillator (4 to 16 MHz) timing diagram

Table 36. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|---------------------------------|----|-----------|---|--|---------------------|------|----------------------|------|
| | | | | Min | Typ | Max | | |
| f _{FXOSC} | SR | — | Fast external crystal oscillator frequency | — | 4.0 | — | 16.0 | MHz |
| g _{mFXOSC} | CC | C | Fast external crystal oscillator transconductance | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0 | 2.2 | — | 8.2 | mA/V |
| | CC | P | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0 | 2.0 | — | 7.4 | |
| | CC | C | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1 | 2.7 | — | 9.7 | |
| | CC | C | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1 | 2.5 | — | 9.2 | |
| V _{FXOSC} | CC | T | Oscillation amplitude at EXTAL | f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0 | 1.3 | — | — | V |
| | | | | f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1 | 1.3 | — | — | |
| V _{FXOSCOF} | CC | P | Oscillation operating point | — | — | 0.95 | — | V |
| I _{FXOSC} ² | CC | T | Fast external crystal oscillator consumption | — | — | 2 | 3 | mA |
| t _{FXOSCSU} | CC | T | Fast external crystal oscillator start-up time | f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0 | — | — | 6 | ms |
| | | | | f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1 | — | — | 1.8 | |
| V _{IH} | SR | P | Input high level CMOS (Schmitt Trigger) | Oscillator bypass mode | 0.65V _{DD} | — | V _{DD} +0.4 | V |
| V _{IL} | SR | P | Input low level CMOS (Schmitt Trigger) | Oscillator bypass mode | -0.4 | — | 0.35V _{DD} | V |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

4.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 37. FMPLL electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|------------------------|----|-----------|---|---|-----|-----|---------|
| | | | | Min | Typ | Max | |
| f_{PLLIN} | SR | — | FMPLL reference clock ² | — | — | — | MHz |
| Δ_{PLLIN} | SR | — | FMPLL reference clock duty cycle ⁽²⁾ | — | — | — | % |
| $f_{PULLOUT}$ | CC | D | FMPLL output clock frequency | — | — | — | MHz |
| f_{VCO} ³ | CC | P | VCO frequency without frequency modulation | — | — | — | MHz |
| | | | VCO frequency with frequency modulation | — | — | — | |
| f_{CPU} | SR | — | System clock frequency | — | — | — | MHz |
| f_{FREE} | CC | P | Free-running frequency | — | — | — | MHz |
| t_{LOCK} | CC | P | FMPLL lock time | Stable oscillator ($f_{PLLIN} = 16$ MHz) | | | μ s |
| Δt_{LTJIT} | CC | — | FMPLL long term jitter | $f_{PLLIN} = 16$ MHz (resonator), f_{PLLCLK} at 48 MHz, 4,000 cycles | | | ns |
| I_{PLL} | CC | C | FMPLL consumption | $T_A = 25$ °C | | | mA |

¹ $V_{DD} = 3.3$ V \pm 10% / 5.0 V \pm 10%, $T_A = -40$ to 125 °C, unless otherwise specified.

² PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN} .

³ Frequency modulation is considered \pm 4%.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|---------------------------|----|-----------|---|------------------------|-----|-----|---------|
| | | | | Min | Typ | Max | |
| f_{FIRC} | CC | P | Fast internal RC oscillator high frequency | $T_A = 25$ °C, trimmed | | | MHz |
| | SR | — | | — | — | — | |
| I_{FIRCUN} ² | CC | T | Fast internal RC oscillator high frequency current in running mode | $T_A = 25$ °C, trimmed | | | μ A |
| $I_{FIRCPWD}$ | CC | D | Fast internal RC oscillator high frequency current in power down mode | $T_A = 25$ °C | | | μ A |

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|------------------------|----|-----------|---|-------------------------------|-----------------|-----|------|-----|----|
| | | | | Min | Typ | Max | | | |
| I _{FIRCSTOP} | CC | T | Fast internal RC oscillator high frequency and system clock current in stop mode | T _A = 25 °C | sysclk = off | — | 500 | — | μA |
| | | | | | sysclk = 2 MHz | — | 600 | — | |
| | | | | | sysclk = 4 MHz | — | 700 | — | |
| | | | | | sysclk = 8 MHz | — | 900 | — | |
| | | | | | sysclk = 16 MHz | — | 1250 | — | |
| t _{FIRCSU} | CC | C | Fast internal RC oscillator start-up time | V _{DD} = 5.0 V ± 10% | | — | 1.1 | 2.0 | μs |
| Δ _{FIRC} PRE | CC | C | Fast internal RC oscillator precision after software trimming of f _{FIRC} | T _A = 25 °C | | -1 | — | 1 | % |
| Δ _{FIRC} TRIM | CC | C | Fast internal RC oscillator trimming step | T _A = 25 °C | | — | 1.6 | | % |
| Δ _{FIRC} VAR | CC | C | Fast internal RC oscillator variation in temperature and supply with respect to f _{FIRC} at T _A = 55 °C in high-frequency configuration | — | | -5 | — | 5 | % |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|--------------------------------|----|-----------|--|---|-----|-----|------|-----|----|
| | | | | Min | Typ | Max | | | |
| f _{SIRC} | CC | P | Slow internal RC oscillator low frequency | T _A = 25 °C, trimmed | — | 128 | — | kHz | |
| | SR | | | — | 100 | — | 150 | | |
| I _{SIRC} ² | CC | C | Slow internal RC oscillator low frequency current | T _A = 25 °C, trimmed | | — | — | 5 | μA |
| t _{SIRCSU} | CC | P | Slow internal RC oscillator start-up time | T _A = 25 °C, V _{DD} = 5.0 V ± 10% | | — | 8 | 12 | μs |
| Δ _{SIRC} PRE | CC | C | Slow internal RC oscillator precision after software trimming of f _{SIRC} | T _A = 25 °C | | -2 | — | 2 | % |
| Δ _{SIRC} TRIM | CC | C | Slow internal RC oscillator trimming step | — | | — | 2.7 | — | |

Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|---------------------------|----|-----------|---|------------------------------|-----|-----|------|---|
| | | | | Min | Typ | Max | | |
| Δ_{SIRCVAR} | CC | P | Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at $T_A = 55\text{ °C}$ in high frequency configuration | High frequency configuration | -10 | — | 10 | % |

¹ $V_{\text{DD}} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ °C}$, unless otherwise specified.

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides a 12-bit Successive Approximation Register (SAR) analog-to-digital converter.

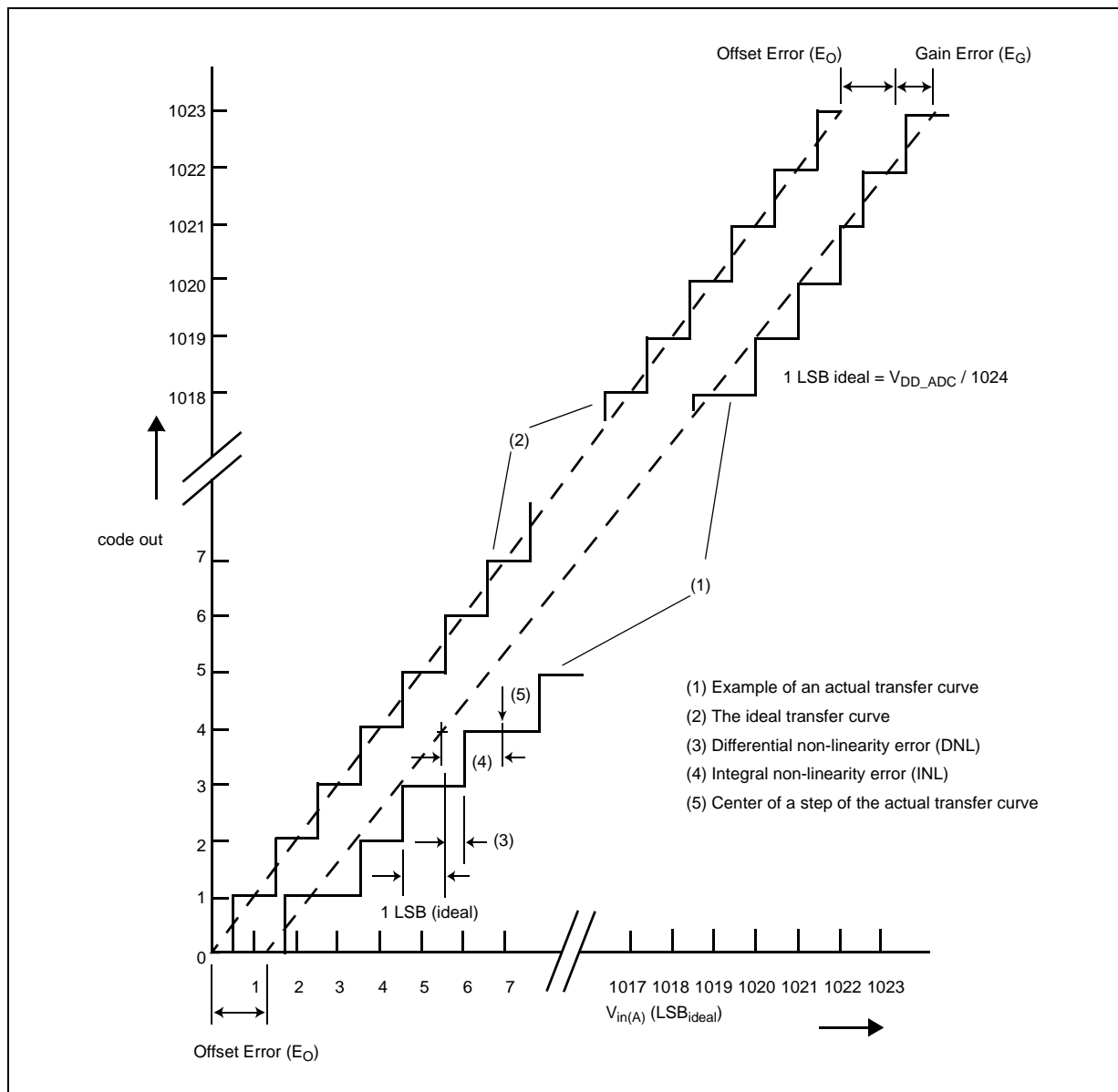


Figure 11. ADC characteristics and error definitions

4.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 k Ω is obtained ($R_{EQ} = 1 / (f_c \times (C_S+C_{p2}))$), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of $R_S + R_F$, the external circuit must be designed to respect the [Equation 4](#):

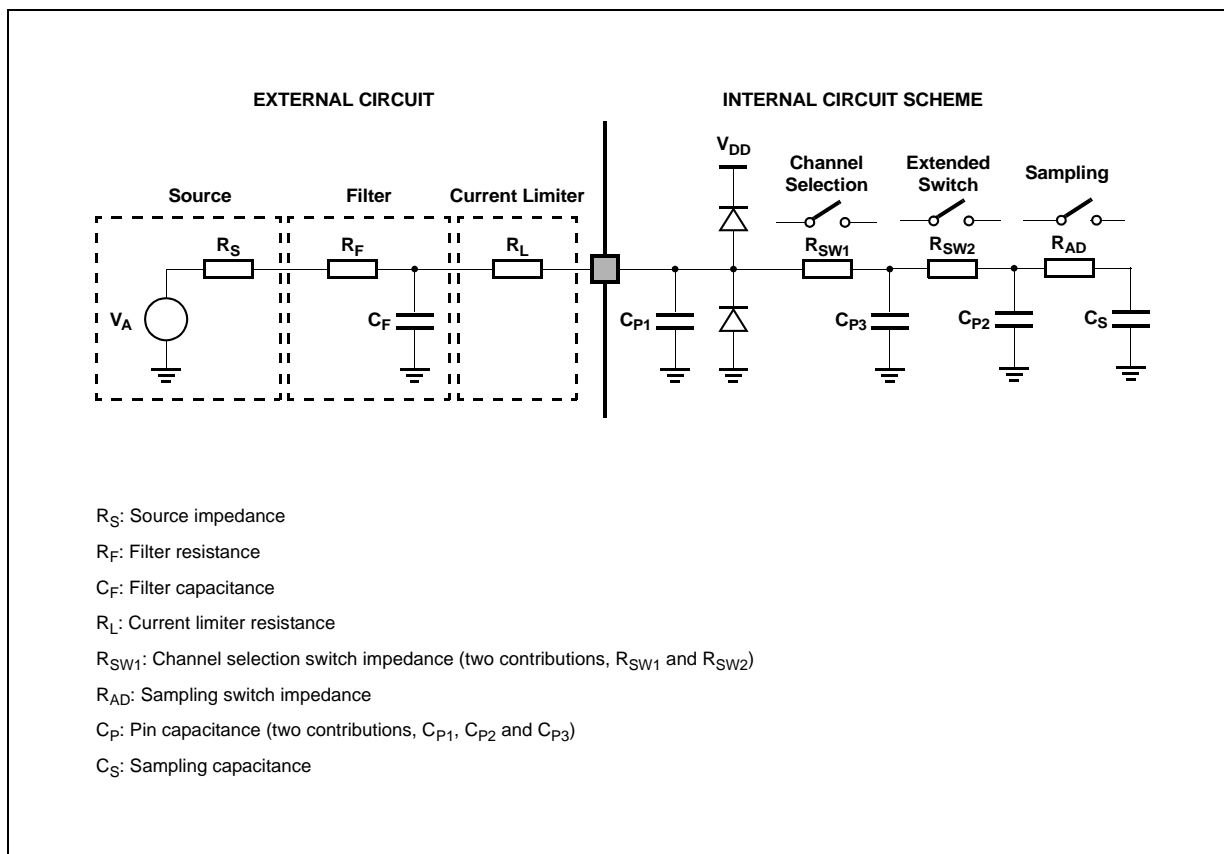
Eqn. 4

$$V_A \cdot \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

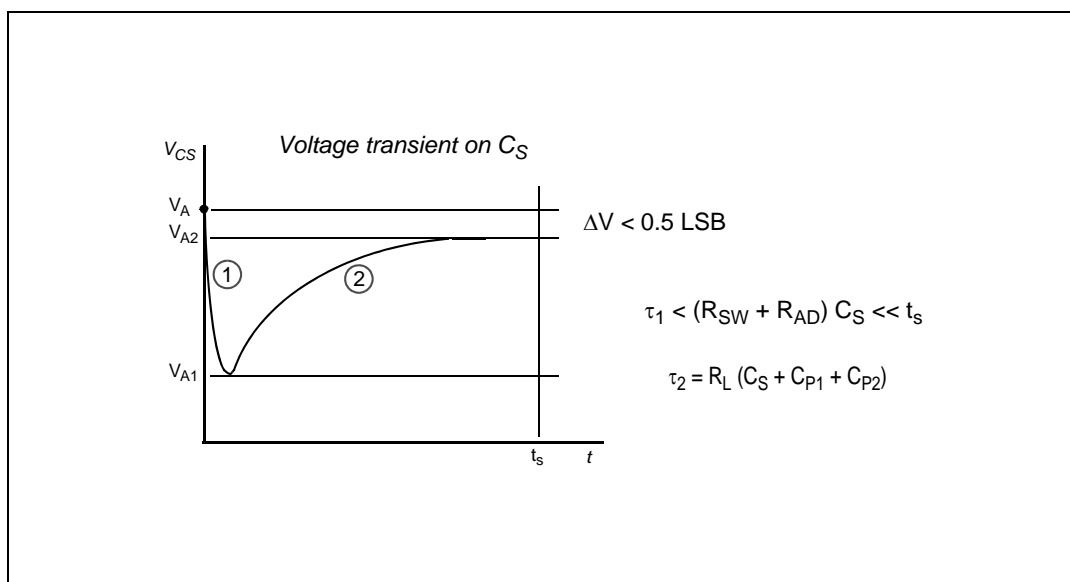
[Equation 4](#) generates a constraint for external network design, in particular on a resistive path.



Figure 12. Input equivalent circuit (precise channels)


Figure 13. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in Figure 13): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).


Figure 14. Transient behavior during sampling phase

Electrical characteristics

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

Eqn. 5

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll t_s$$

Eqn. 6

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

Eqn. 7

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

Eqn. 8

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s , a constraints on R_L sizing is obtained:

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < t_s$$

Eqn. 9

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

Eqn. 10

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

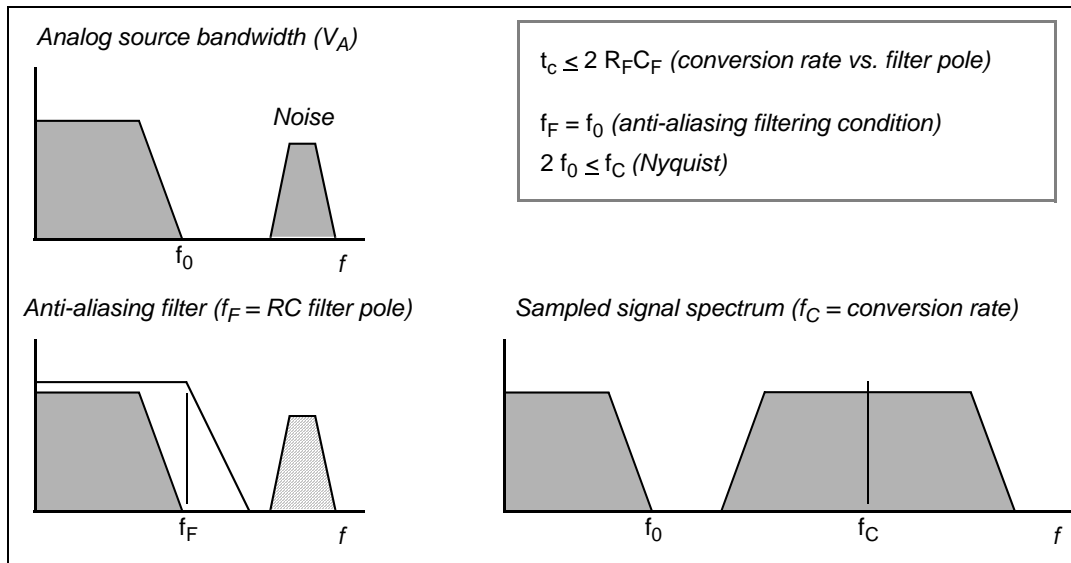


Figure 15. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s , so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive [Equation 11](#) between the ideal and real sampled voltage on C_S :

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \cdot C_S$$

4.17.3 ADC electrical characteristics

Table 40. ADC input leakage current

| Symbol | C | Parameter | Conditions | Value | | | Unit | |
|------------------|----|-----------------------|-------------------------|--------------------------------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{LKG} | CC | Input leakage current | T _A = -40 °C | No current injection on adjacent pin | — | 1 | — | nA |
| | | | T _A = 25 °C | | — | 1 | — | |
| | | | T _A = 105 °C | | — | 8 | 200 | |
| | | | T _A = 125 °C | | — | 45 | 400 | |

Table 41. ADC conversion characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|----------------------|----|-----------|--|---|------|---------------------------|---------|-----|
| | | | | Min | Typ | Max | | |
| V _{SS_ADC} | SR | — | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) ² | — | — | 0.1 | V | |
| V _{DD_ADC} | SR | — | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS}) | — | — | V _{DD} + 0.1 | V | |
| V _{AINx} | SR | — | Analog input voltage ³ | — | — | V _{DD_ADC} + 0.1 | V | |
| f _{ADC} | SR | — | ADC analog frequency | V _{DD} = 5.0 V | 3.33 | — | 32 + 4% | MHz |
| | | | | V _{DD} = 3.3 V | 3.33 | — | 20 + 4% | |
| Δ _{ADC_SYS} | SR | — | ADC clock duty cycle (ipg_clk) | ADCLKSEL = 1 ⁴ | 45 | — | 55 | % |
| t _{ADC_PU} | SR | — | ADC power up delay | — | — | — | 1.5 | μs |
| t _s | CC | T | Sampling time ⁵ V _{DD} = 3.3 V | f _{ADC} = 20 MHz, INPSAMP = 12 | 600 | — | — | ns |
| | | | | f _{ADC} = 3.33 MHz, INPSAMP = 255 | — | — | 76.2 | μs |
| | | T | Sampling time ⁽⁵⁾ V _{DD} = 5.0 V | f _{ADC} = 24 MHz, INPSAMP = 13 | 500 | — | — | ns |
| | | | | f _{ADC} = 3.33 MHz, INPSAMP = 255 | — | — | 76.2 | μs |

Table 41. ADC conversion characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-------------------|----|---|--|--|-------------------------------|-----|------|-----|----|
| | | | | Min | Typ | Max | | | |
| t _c | CC | P | Conversion time ⁶ V _{DD} = 3.3 V | f _{ADC} = 20 MHz, INPCMP = 0 | 2.4 | — | — | μs | |
| | | | | f _{ADC} = 13.33 MHz, INPCMP = 0 | — | — | 3.6 | | |
| | P | Conversion time ⁽⁶⁾ V _{DD} = 5.0 V | f _{ADC} = 32 MHz, INPCMP = 0 | 1.5 | — | — | μs | | |
| | | | f _{ADC} = 13.33 MHz, INPCMP = 0 | — | — | 3.6 | | | |
| C _S | CC | D | ADC input sampling capacitance | — | 5 | | | pF | |
| C _{P1} | CC | D | ADC input pin capacitance 1 | — | 3 | | | pF | |
| C _{P2} | CC | D | ADC input pin capacitance 2 | — | 1 | | | pF | |
| C _{P3} | CC | D | ADC input pin capacitance 3 | — | 1.5 | | | pF | |
| R _{SW1} | CC | D | Internal resistance of analog source | — | — | — | 1 | kΩ | |
| R _{SW2} | CC | D | Internal resistance of analog source | — | — | — | 2 | kΩ | |
| R _{AD} | CC | D | Internal resistance of analog source | — | — | — | 0.3 | kΩ | |
| I _{INJ} | SR | — | Input current Injection | Current injection on one ADC input, different from the converted one | V _{DD} = 3.3 V ± 10% | —5 | — | 5 | mA |
| | | | | | V _{DD} = 5.0 V ± 10% | —5 | — | 5 | |
| INLP | CC | T | Absolute Integral non-linearity-precise channels | No overload | — | 1 | 3 | LSB | |
| INLX | CC | T | Absolute Integral non-linearity-extended channels | No overload | — | 1.5 | 5 | LSB | |
| DNL | CC | T | Absolute Differential non-linearity | No overload | — | 0.5 | 1 | LSB | |
| E _O | CC | T | Absolute Offset error | — | — | 2 | — | LSB | |
| E _G | CC | T | Absolute Gain error | — | — | 2 | — | LSB | |
| TUEP ⁷ | CC | P | Total unadjusted error for precise channels, input only pins | Without current injection | —6 | — | 6 | LSB | |
| | | T | | With current injection | —8 | — | 8 | | |

Table 41. ADC conversion characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|---------------------|----|-----------|---|---------------------------|-----|-----|------|
| | | | | Min | Typ | Max | |
| TUEX ⁽⁷⁾ | CC | T | Total unadjusted error for extended channel | Without current injection | | 10 | LSB |
| | | | | With current injection | -12 | 12 | |

- ¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified.
- ² Analog and digital V_{SS} **must** be common (to be tied together externally).
- ³ V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFFF.
- ⁴ Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.
- ⁵ During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sampling time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
- ⁶ This parameter does not include the sampling time t_S , but only the time for determining the digital result and the time to load the result's register with the conversion result.
- ⁷ Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 42. On-chip peripherals current consumption¹

| Symbol | C | Parameter | Conditions | Typical value ² | Unit | | |
|---------------------|----|-----------|--|---|---|-----------------------------------|---------------|
| $I_{DD_BV(CAN)}$ | CC | T | CAN (FlexCAN) supply current on V_{DD_BV} | 500 Kbyte/s | Total (static + dynamic) consumption: <ul style="list-style-type: none"> • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 μs | $8 \times f_{\text{periph}} + 85$ | μA |
| | | | | 125 Kbyte/s | | $8 \times f_{\text{periph}} + 27$ | μA |
| $I_{DD_BV(eMIOS)}$ | CC | T | eMIOS supply current on V_{DD_BV} | Static consumption: <ul style="list-style-type: none"> • eMIOS channel OFF • Global prescaler enabled | $29 \times f_{\text{periph}}$ | μA | |
| | | | | Dynamic consumption: <ul style="list-style-type: none"> • It does not change varying the frequency (0.003 mA) | 3 | μA | |
| $I_{DD_BV(SCI)}$ | CC | T | SCI (LINFlex) supply current on V_{DD_BV} | Total (static + dynamic) consumption: <ul style="list-style-type: none"> • LIN mode • Baudrate: 20 Kbyte/s | $5 \times f_{\text{periph}} + 31$ | μA | |

Table 42. On-chip peripherals current consumption¹ (continued)

| Symbol | C | Parameter | Conditions | | Typical value ² | Unit | |
|-----------------------------|----|-----------|--|---|--|-------------------------------|----|
| I _{DD_BV(SPI)} | CC | T | SPI (DSPI) supply current on V _{DD_BV} | Ballast static consumption (only clocked) | 1 | μA | |
| | | | | Ballast dynamic consumption (continuous communication): | 16 × f _{periph} | μA | |
| | | | | <ul style="list-style-type: none"> • Baudrate: 2 Mbit/s • Transmission every 8 μs • Frame: 16 bits | | | |
| I _{DD_BV(ADC)} | CC | T | ADC supply current on V _{DD_BV} | V _{DD} = 5.5 V | Ballast static consumption (no conversion) | 41 × f _{periph} | μA |
| | | | | | Ballast dynamic consumption (continuous conversion) ³ | 5 × f _{periph} | μA |
| I _{DD_HV_ADC(ADC)} | CC | T | ADC supply current on V _{DD_HV_ADC} | V _{DD} = 5.5 V | Analog static consumption (no conversion) | 2 × f _{periph} | μA |
| | | | | | Analog dynamic consumption (continuous conversion) | 75 × f _{periph} + 32 | μA |
| I _{DD_HV(FLASH)} | CC | T | CFlash + DFlash supply current on V _{DD_HV} | V _{DD} = 5.5 V | — | 8.21 | mA |
| I _{DD_HV(PLL)} | CC | T | PLL supply current on V _{DD_HV} | V _{DD} = 5.5 V | — | 30 × f _{periph} | μA |

¹ Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 48 MHz

² f_{periph} is an absolute value.

³ During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) × f_{periph}.

4.18.2 DSPI characteristics

Table 43. DSPI characteristics¹

| No. | Symbol | C | Parameter | | DSPI0/DSPI1 | | | Unit | |
|-----|-------------------|----|-----------|-----------------------------------|------------------------|-----|------------------|------|----|
| | | | | | Min | Typ | Max | | |
| 1 | t _{SCK} | SR | D | SCK cycle time | Master mode (MTFE = 0) | 125 | — | — | ns |
| | | | | | Slave mode (MTFE = 0) | 125 | — | — | |
| | | | | | Master mode (MTFE = 1) | 83 | — | — | |
| | | | | | Slave mode (MTFE = 1) | 83 | — | — | |
| — | f _{DSPI} | SR | D | DSPI digital controller frequency | — | — | f _{CPU} | MHz | |

Table 43. DSPI characteristics¹ (continued)

| No. | Symbol | C | D | Parameter | DSPI0/DSPI1 | | | Unit | |
|-----|------------------|----|---|--|-------------|-------------------|-------------|--------------------|----|
| | | | | | Min | Typ | Max | | |
| — | Δt_{CSC} | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode | Master mode | — | — | 130 ² | ns |
| — | Δt_{ASC} | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→1 | Master mode | — | — | 130 ⁽²⁾ | ns |
| 2 | t_{CSCext}^3 | SR | D | CS to SCK delay | Slave mode | 32 | — | — | ns |
| 3 | t_{ASCext}^4 | SR | D | After SCK delay | Slave mode | $1/f_{DSPI} + 5$ | — | — | ns |
| 4 | t_{SDC} | CC | D | SCK duty cycle | Master mode | — | $t_{SCK}/2$ | — | ns |
| | | SR | D | | Slave mode | $t_{SCK}/2$ | — | — | |
| 5 | t_A | SR | D | Slave access time | — | $1/f_{DSPI} + 70$ | — | — | ns |
| 6 | t_{DI} | SR | D | Slave SOUT disable time | — | 7 | — | — | ns |
| 7 | t_{PCSC} | SR | D | PCSS to PCSx time | — | 0 | — | — | ns |
| 8 | t_{PASC} | SR | D | PCSS to PCSx time | — | 0 | — | — | ns |
| 9 | t_{SUI} | SR | D | Data setup time for inputs | Master mode | 43 | — | — | ns |
| | | | | | Slave mode | 5 | — | — | |
| 10 | t_{HI} | SR | D | Data hold time for inputs | Master mode | 0 | — | — | ns |
| | | | | | Slave mode | 2 ⁵ | — | — | |
| 11 | t_{SUO}^6 | CC | D | Data valid after SCK edge | Master mode | — | — | 32 | ns |
| | | | | | Slave mode | — | — | 52 | |
| 12 | $t_{HO}^{(6)}$ | CC | D | Data hold time for outputs | Master mode | 0 | — | — | ns |
| | | | | | Slave mode | 8 | — | — | |

¹ Operating conditions: $C_{OUT} = 10$ to 50 pF, $Slew_{IN} = 3.5$ to 15 ns

² Maximum is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM pad

³ The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext} .

⁴ The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext} .

⁵ This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR.

⁶ SCK and SOUT configured as MEDIUM pad

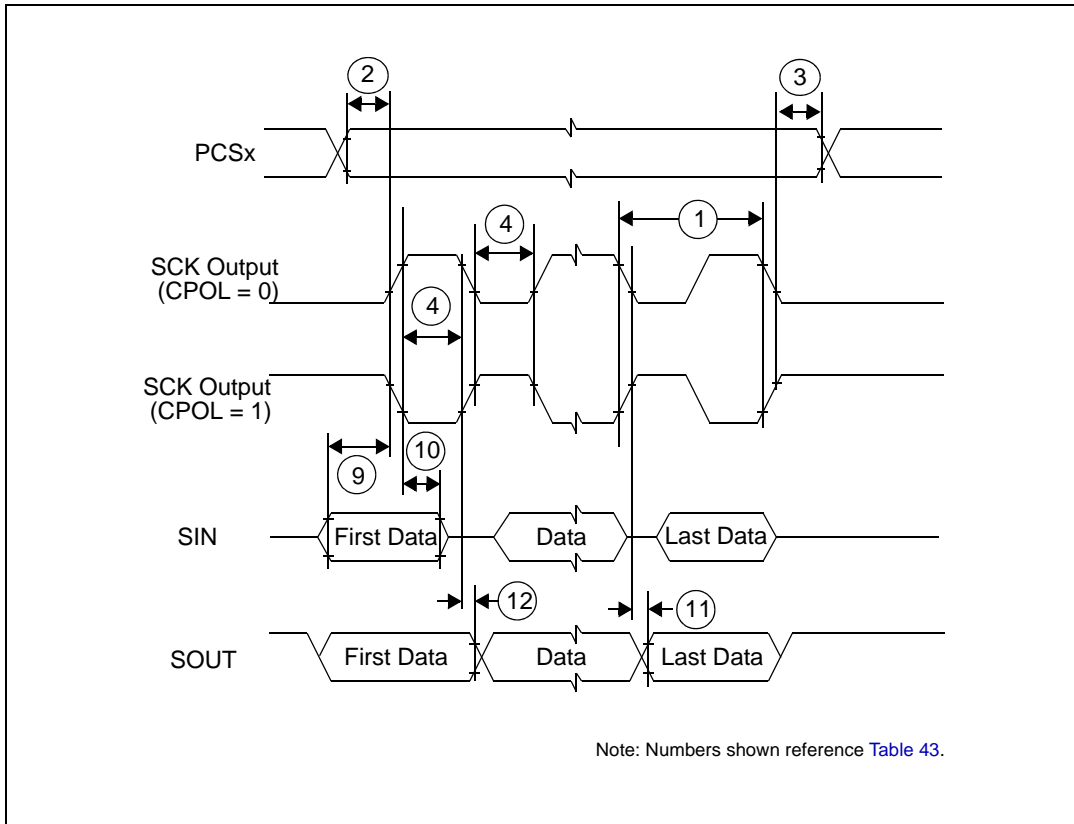


Figure 16. DSPI classic SPI timing – master, CPHA = 0

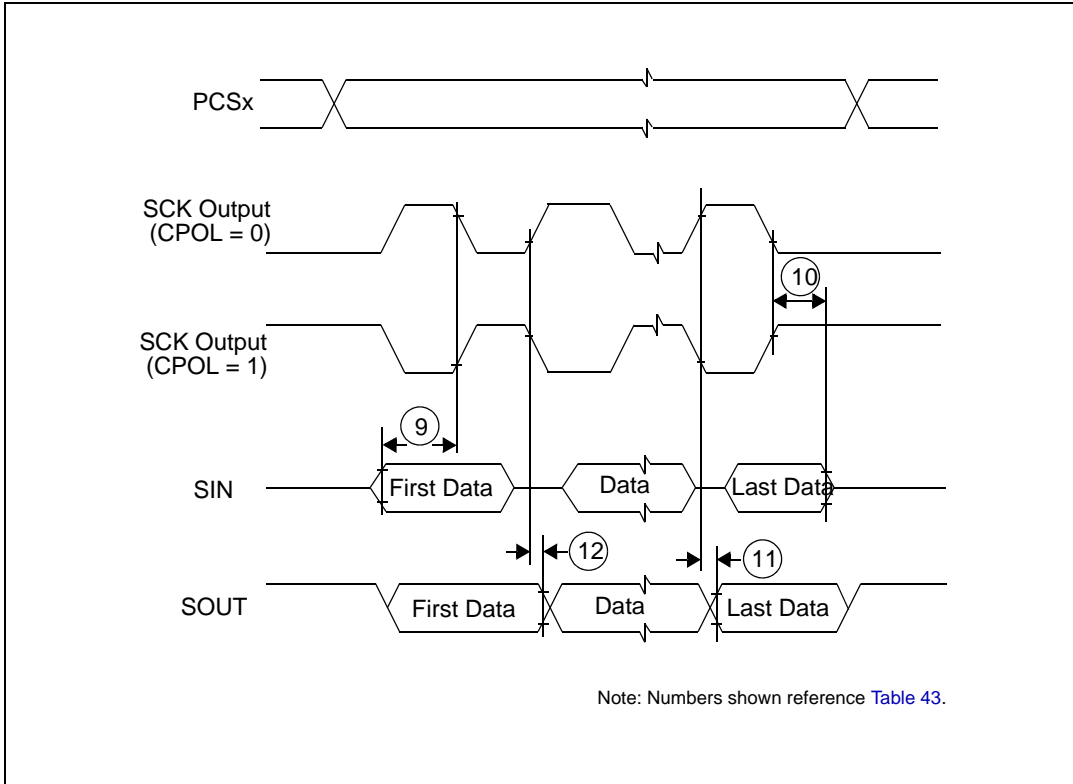


Figure 17. DSPI classic SPI timing – master, CPHA = 1

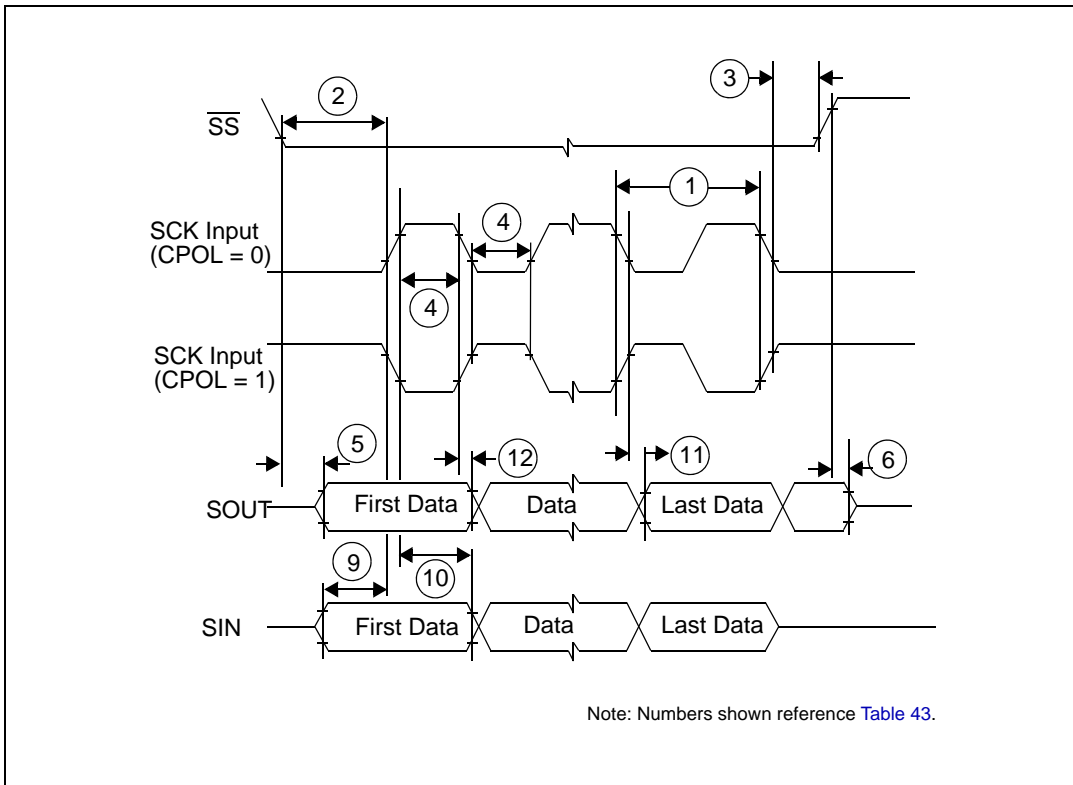


Figure 18. DSPI classic SPI timing – slave, CPHA = 0

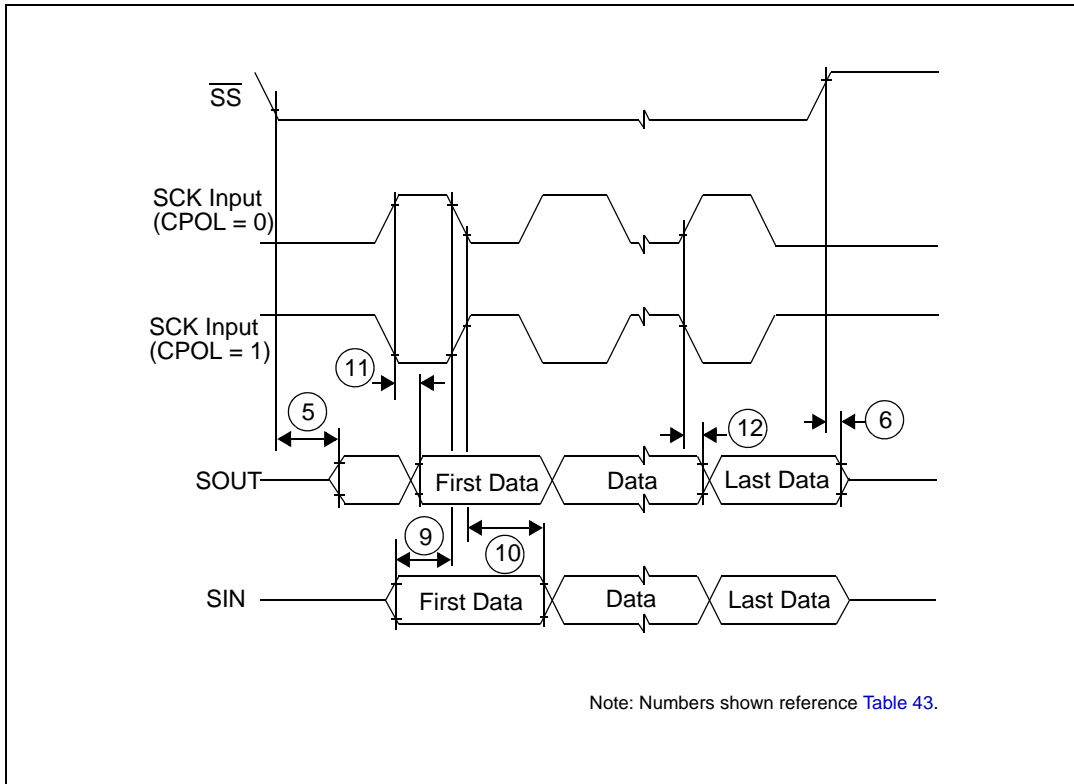


Figure 19. DSPI classic SPI timing – slave, CPHA = 1

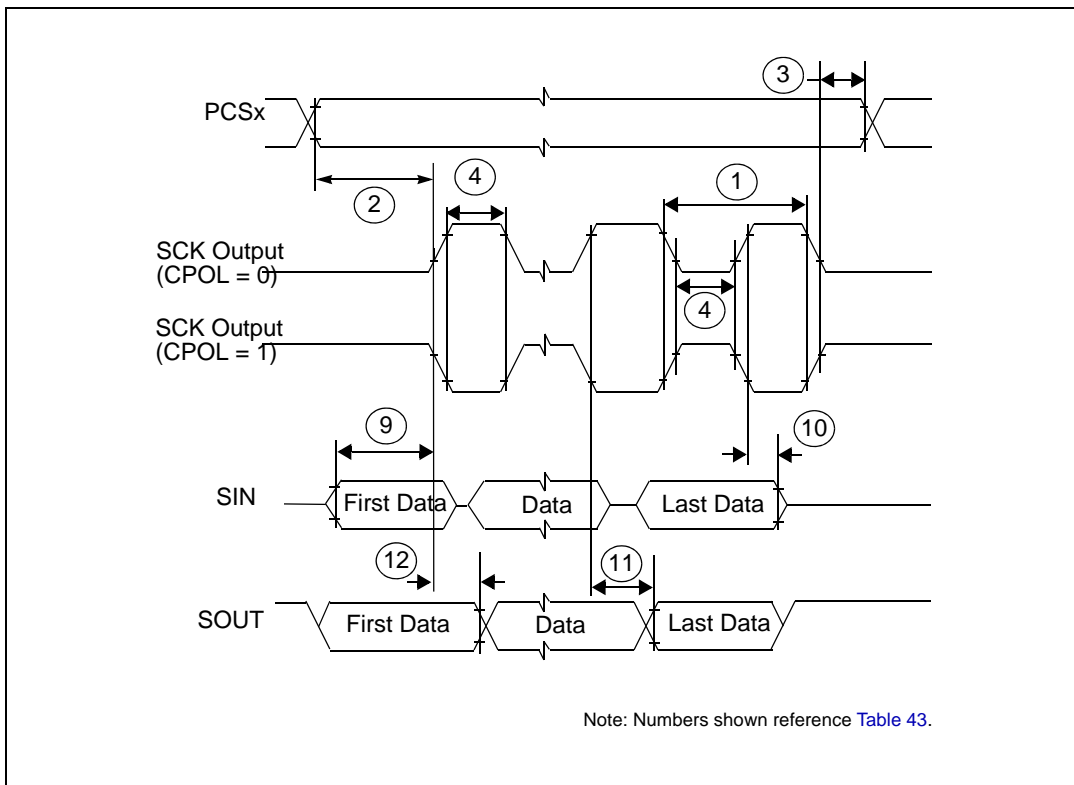


Figure 20. DSPI modified transfer format timing – master, CPHA = 0

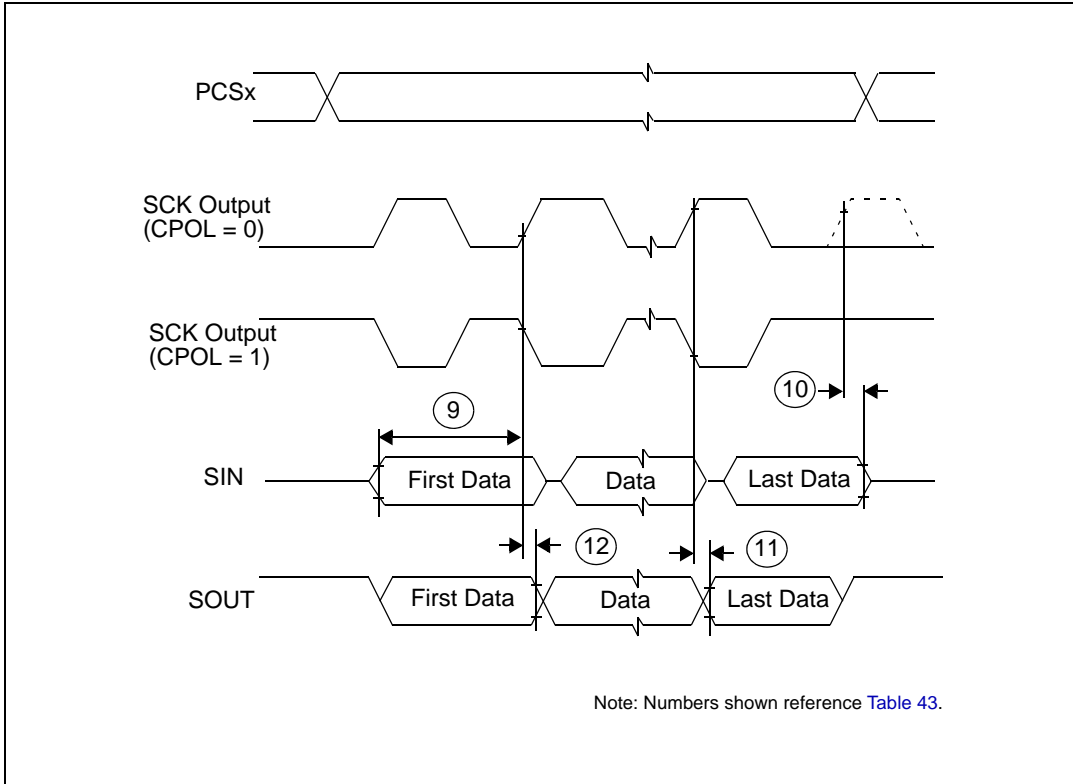


Figure 21. DSPI modified transfer format timing – master, CPHA = 1

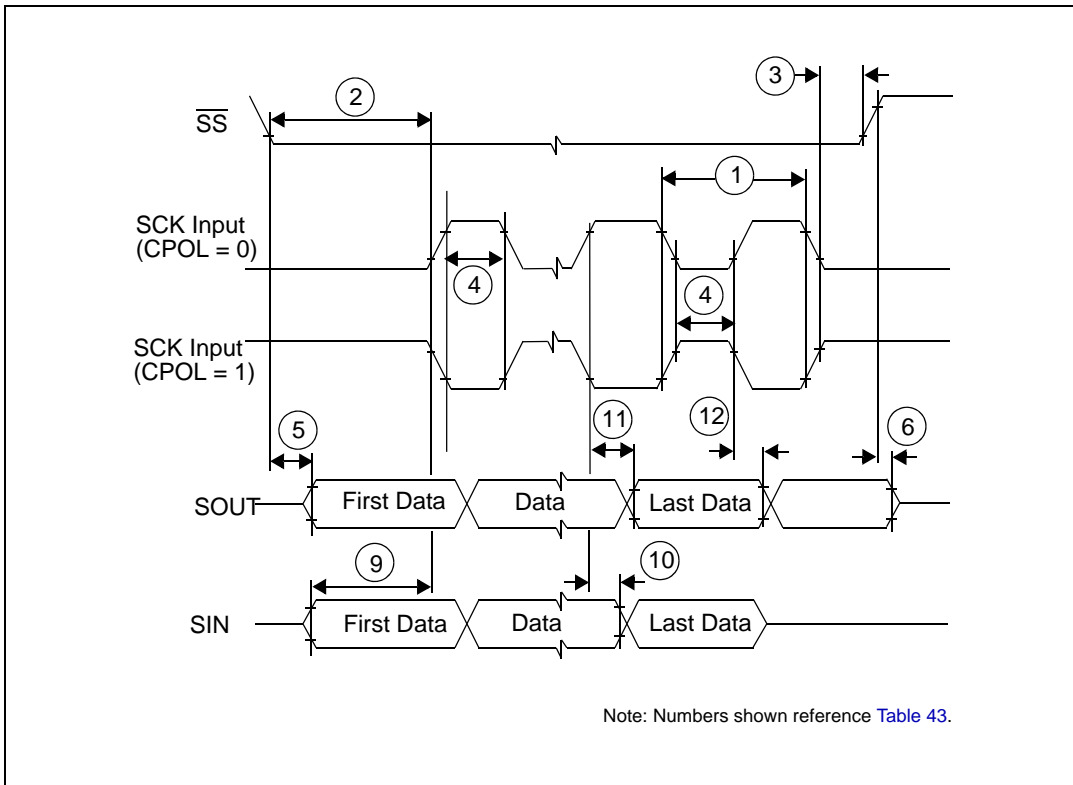


Figure 22. DSPI modified transfer format timing – slave, CPHA = 0

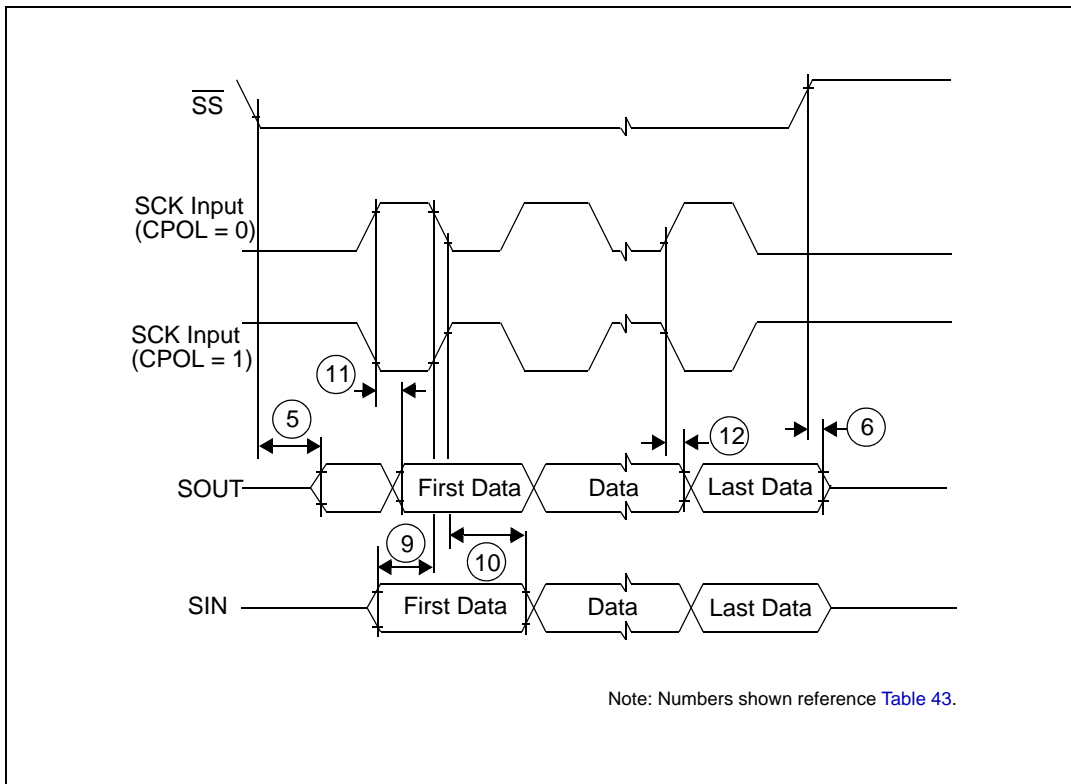


Figure 23. DSPI modified transfer format timing – slave, CPHA = 1

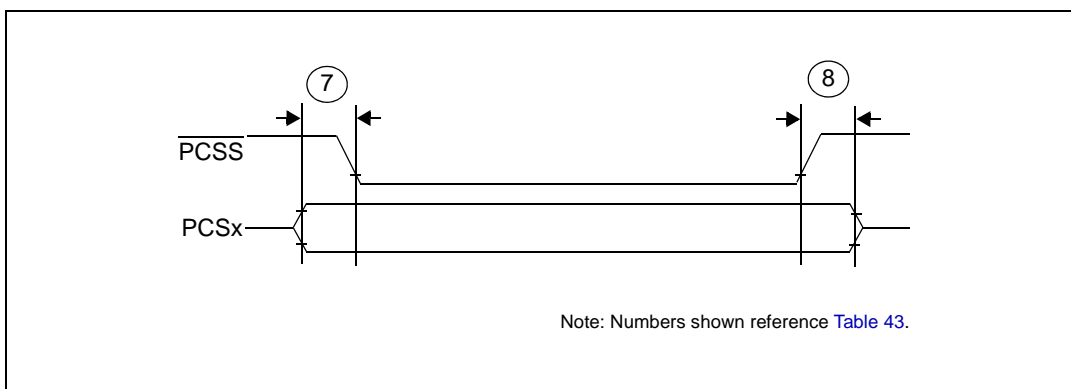


Figure 24. DSPI PCS strobe (PCSS) timing

4.18.3 JTAG characteristics

Table 44. JTAG characteristics

| No. | Symbol | C | Parameter | Value | | | Unit | |
|-----|------------|----|-----------|------------------------|-------|-----|------|----|
| | | | | Min | Typ | Max | | |
| 1 | t_{JCYC} | CC | D | TCK cycle time | 83.33 | — | — | ns |
| 2 | t_{TDIS} | CC | D | TDI setup time | 15 | — | — | ns |
| 3 | t_{TDIH} | CC | D | TDI hold time | 5 | — | — | ns |
| 4 | t_{TMSS} | CC | D | TMS setup time | 15 | — | — | ns |
| 5 | t_{TMSH} | CC | D | TMS hold time | 5 | — | — | ns |
| 6 | t_{TDOV} | CC | D | TCK low to TDO valid | — | — | 49 | ns |
| 7 | t_{TDOI} | CC | D | TCK low to TDO invalid | 6 | — | — | ns |

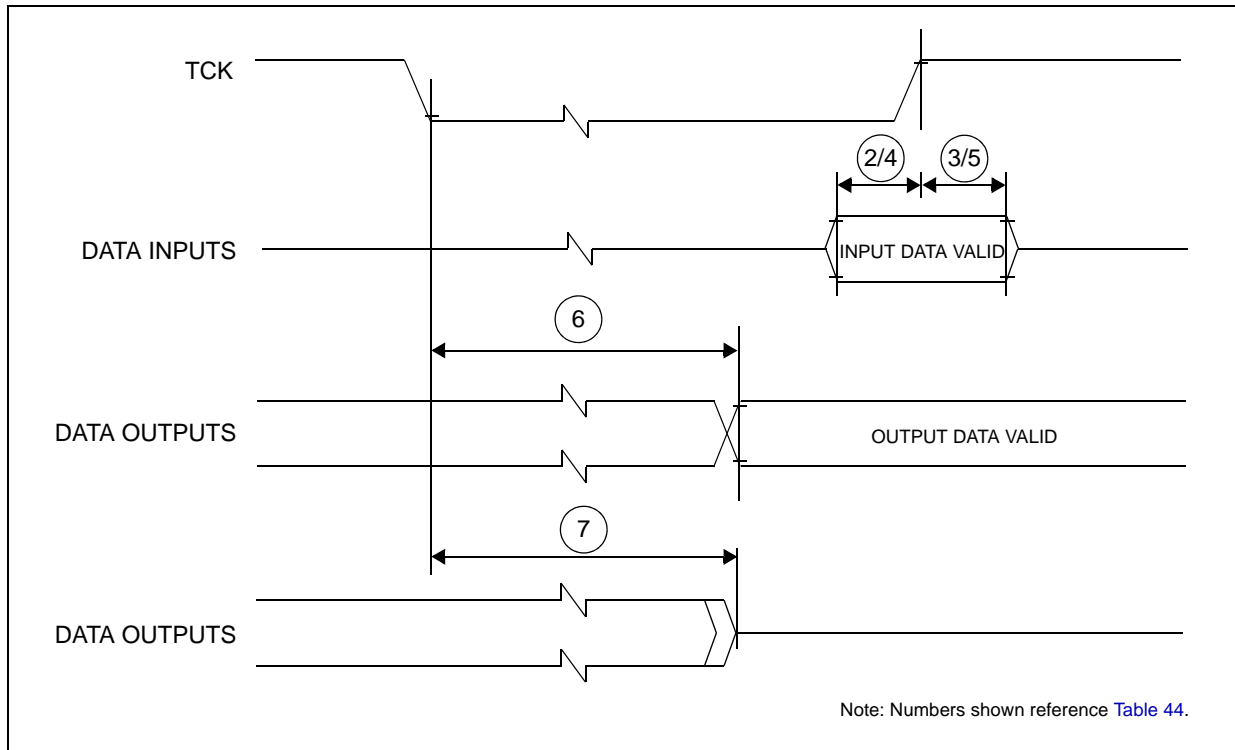


Figure 25. Timing diagram – JTAG boundary scan

5 Package characteristics

5.1 Package mechanical data

5.1.1 100 LQFP



Figure 26. 100 LQFP package mechanical drawing (Part 1 of 3)



Figure 27. 100 LQFP package mechanical drawing (Part 2 of 3)

| | | | | |
|--|---|---------------------|--------------------------|-----|
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| | | | PAGE: | 983 |
| | DO NOT SCALE THIS DRAWING | | REV: | H |
| <p>NOTES:</p> <ol style="list-style-type: none"> 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994. 3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H. 4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM. 5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH. 6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM. 7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A. | | | | |
| TITLE: | | CASE NUMBER: 983-02 | | |
| <p style="text-align: center;">100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK</p> | | STANDARD: NON-JEDEC | | |
| | | PACKAGE CODE: 8264 | SHEET: | 3 |

Figure 28. 100 LQFP package mechanical drawing (Part 3 of 3)

5.1.2 64 LQFP

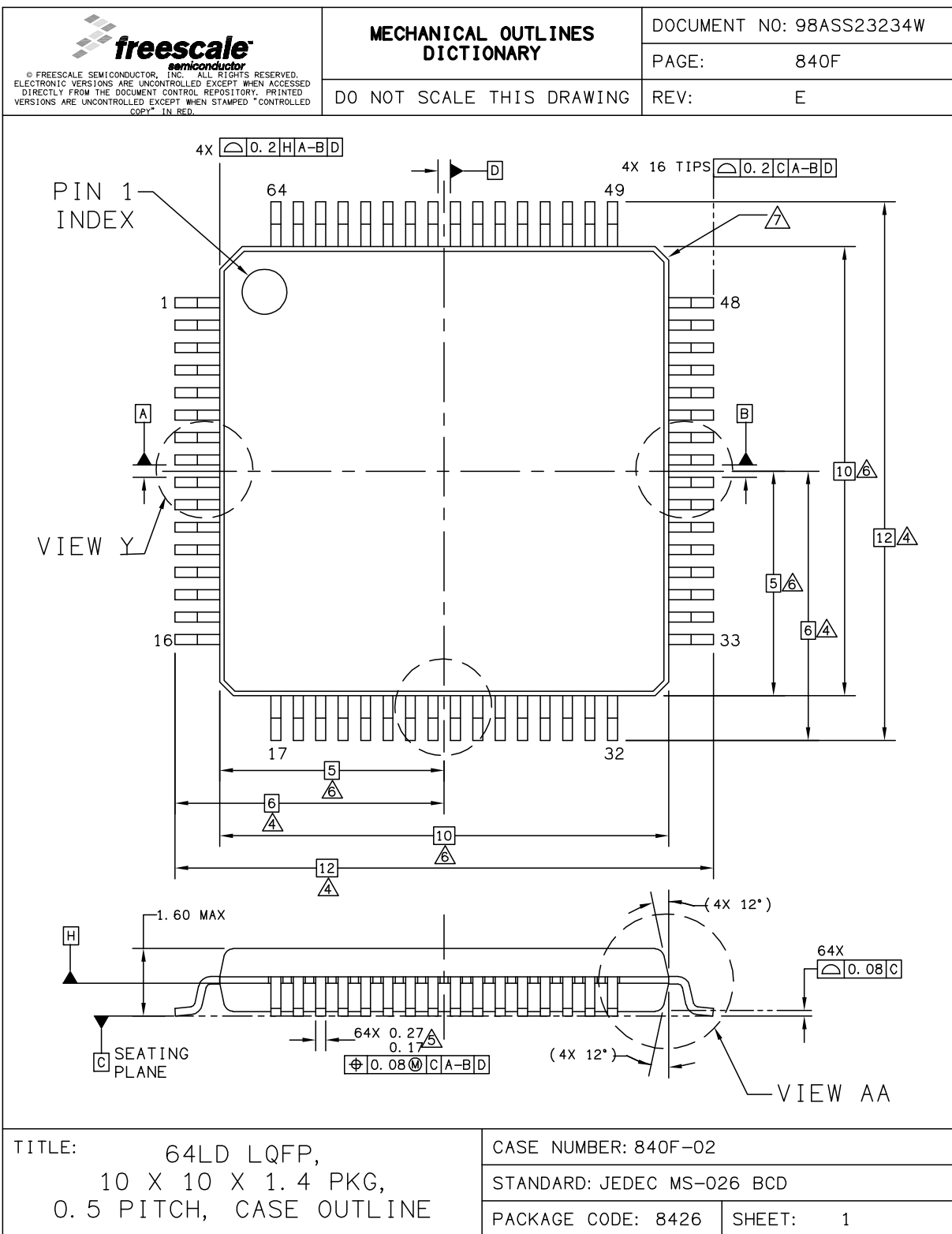


Figure 29. 64 LQFP mechanical drawing (part 1 of 3)

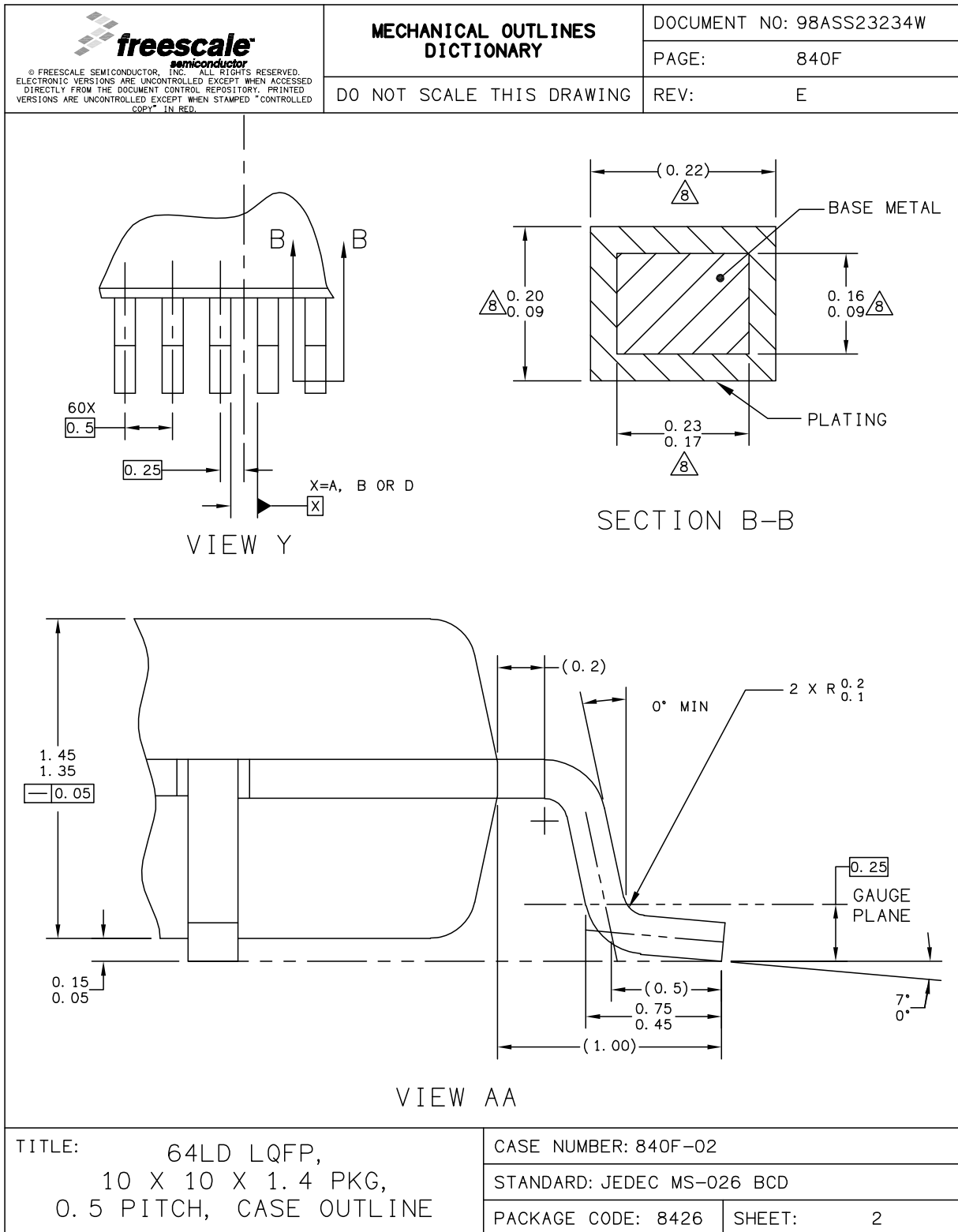


Figure 30. 64 LQFP mechanical drawing (part 2 of 3)

Package characteristics

| | | | |
|---|---|----------------------------|----------|
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| | DO NOT SCALE THIS DRAWING | PAGE: | 840F |
| | | REV: | E |
| <p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H. 4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C. 5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm. 6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH. 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL. 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP. | | | |
| TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE | | CASE NUMBER: 840F-02 | |
| | | STANDARD: JEDEC MS-026 BCD | |
| | | PACKAGE CODE: 8426 | SHEET: 3 |

Figure 31. 64 LQFP mechanical drawing (part 3 of 3)

6 Ordering information

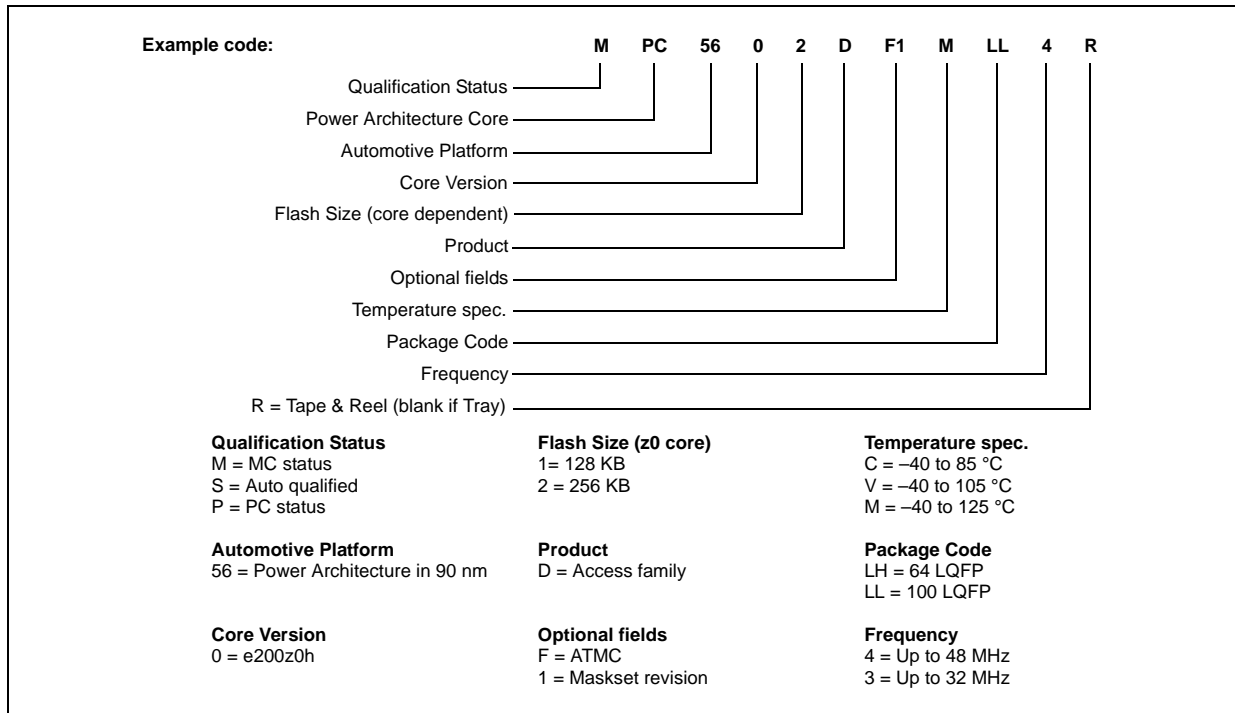


Figure 32. Commercial product code structure

7 Document revision history

Table 45 summarizes revisions to this document.

Table 45. Revision history

| Revision | Date | Description of Changes |
|------------------|-------------|---|
| 1 | 30 Sep 2009 | Initial release |
| 2 | 18 Feb 2010 | Updated the following tables: <ul style="list-style-type: none"> - Absolute maximum ratings - Low voltage power domain electrical characteristics; - On-chip peripherals current consumption - DSPI characteristics; - JTAG characteristics; - ADC conversion characteristics; Inserted a note on “Flash power supply DC characteristics” section. |
| 3 | 10 Aug 2010 | <p>“Features” section: Updated information concerning eMIOS, ADC, LINFlex, Nexus and low power capabilities</p> <p>“MPC5602D device comparison” table: updated the “Execution speed” row</p> <p>“MPC5602D series block diagram” figure:</p> <ul style="list-style-type: none"> • updated max number of Crossbar Switches • updated Legend <p>“MPC5602D series block summary” table: added contents concernig the eDMA block</p> <p>“100 LQFP pin configuration (top view)” figure:</p> <ul style="list-style-type: none"> • removed alternate functions • updated supply pins <p>“64 LQFP pin configuration (top view)” figure: removed alternate functions</p> <p>Added “Pin muxing” section</p> <p>“NVUSRO register” section: Deleted “NVUSRO[WATCHDOG_EN] field description” section</p> <p>“Recommended operating conditions (3.3 V)” table:</p> <ul style="list-style-type: none"> • $T_{V_{DD}}$: deleted min value • In footnote No. 3, changed capacitance value between V_{DD_BV} and V_{SS_LV} <p>“Recommended operating conditions (5.0 V)” table: deleted $T_{V_{DD}}$ min value</p> <p>“LQFP thermal characteristics” table: changed $R_{\theta_{JC}}$ values</p> <p>“I/O input DC electrical characteristics” table:</p> <ul style="list-style-type: none"> • W_{FI}: updated max value • W_{NFI}: updated min value <p>“I/O consumption” table: removed I_{DYNSEG} row</p> <p>Added “I/O weight” table</p> <p>“Program and erase specifications (Code Flash)” table: deleted T_{Bank_C} row</p> <p>Updated the following tables:</p> <ul style="list-style-type: none"> • “Voltage regulator electrical characteristics” • “Low voltage monitor electrical characteristics” • “Low voltage power domain electrical characteristics” • “Start-up time/Switch-off time” • “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” • “FMPLL electrical characteristics” • “Fast internal RC oscillator (16 MHz) electrical characteristics” • “ADC conversion characteristics” • “On-chip peripherals current consumption” • “DSPI characteristics” <p>“DSPI characteristics” section: removed “DSPI PCS strobe (PCSS) timing” figure</p> |
| 3 (continued) | 10 Aug 2010 | “Ordering information” section: removed “Orderable part number summary” table |

Table 45. Revision history (continued)

| Revision | Date | Description of Changes |
|----------|-------------|---|
| 3.1 | 23 Feb 2011 | Deleted the "Freescale Confidential Proprietary" label (the document is public) |

Table 45. Revision history (continued)

| Revision | Date | Description of Changes |
|----------|-------------|---|
| 4 | 14 Jul 2011 | <p>Formatting and editorial changes throughout</p> <p>Device comparison table: for the "Total timer I/O eMIOS", changed "13 ch" to "14 ch"</p> <p>Features: Replaced "e200z0" with "e200z0h"; added an explanation of which LINFlex modules support master mode and slave</p> <p>MPC5601D/MPC5602D series block summary:</p> <ul style="list-style-type: none"> added definition for "AUTOSAR" acronym <p>changed "System watchdog timer" to "Software watchdog timer"</p> <p>64 LQFP pin configuration (top view): changed pin 6 from VPP_TEST to VSS_HV</p> <p>Added section "Pad configuration during reset phases"</p> <p>Added section "Voltage supply pins"</p> <p>Added section "Pad types"</p> <p>Added section "System pins"</p> <p>Renamed and updated section "Functional ports" (was previously section "Pin muxing"); update includes replacing all instances of WKUP with WKPU (WKPU is the correct abbreviation for Wakeup Unit)</p> <p>Section "NVUSRO register": edited content to separate configuration into electrical parameters and digital functionality</p> <p>Added section "NVUSRO[WATCHDOG_EN] field description"</p> <p>Absolute maximum ratings: Removed "C" column from table</p> <p>Replaced "TBD" with "—" in T_{VDD} min value cell of 3.3 V and 5 V recommended operating conditions tables</p> <p>LQFP thermal characteristics: removed $R_{\theta JB}$ single layer board conditions; updated footnote 4</p> <p>I/O input DC electrical characteristics: removed footnote "All values need to be confirmed during device validation"; updated I_{LKG} characteristics</p> <p>MEDIUM configuration output buffer electrical characteristics: changed "$I_{OH} = 100 \mu A$" to "$I_{OL} = 100 \mu A$" in V_{OL} conditions</p> <p>I/O consumption: replaced instances of "Root medium square" with "Root mean square"</p> <p>Updated section "Voltage regulator electrical characteristics"</p> <p>Section "Low voltage detector electrical characteristics": changed title (was "Voltage monitor electrical characteristics"); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of "Low voltage monitor" with "Low voltage detector"; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table</p> <p>Updated and renamed section "Power consumption" (was previously section "Low voltage domain power consumption")</p> <p>Program and erase specifications (code flash): updated symbols; updated t_{ESUS} values</p> <p>Updated Flash memory read access timing</p> <p>EMI radiated emission measurement: updated S_{EMI} values</p> <p>Updated FMPLL electrical characteristics</p> <p>Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor</p> <p>Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values</p> <p>Section "Input impedance and ADC accuracy": changed "V_A/V_{A2}" to "V_{A2}/V_A" in Equation 13</p> <p>ADC conversion characteristics:</p> <ul style="list-style-type: none"> updated conditions for sampling time $V_{DD} = 5.0 V$ updated conditions for conversion time $V_{DD} = 5.0 V$ <p>Commercial product code structure: added character for frequency; updated optional fields character and description</p> <p>Restored the revision history table and added an entry for Rev. 3.1</p> <p>Updated Abbreviations</p> |

Table 45. Revision history (continued)

| Revision | Date | Description of Changes |
|----------|-------------|--|
| 5 | — | Rev. 5 not published. |
| 6 | 29 Jan 2013 | Removed all instances of table footnote “All values need to be confirmed during device validation” Section 4.1, “Introduction, removed Caution note. In Table 42, On-chip peripherals current consumption, replaced “TBD” with “8.21 mA” in $I_{DD_HV(FLASH)}$ cell. Updated Section 4.17.2, “Input impedance and ADC accuracy In Table 24, changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ from 2.7 V to 2.6 V. Revised the Table 28 (Flash module life) Updated Table 43, DSPI characteristics, to add specifications 7 and 8, t_{PCSC} and t_{PASC} . Inserted Figure 24, DSPI PCS strobe (PCSS) timing. |

Appendix A Abbreviations

Table A-1 lists abbreviations used in this document.

Table A-1. Abbreviations

| Abbreviation | Meaning |
|--------------|--|
| APU | Auxilliary processing unit |
| CMOS | Complementary metal–oxide–semiconductor |
| CPHA | Clock phase |
| CPOL | Clock polarity |
| CS | Peripheral chip select |
| DAOC | Double action output compare |
| ECC | Error code correction |
| EVTO | Event out |
| GPIO | General purpose input/output |
| IPM | Input period measurement |
| IPWM | Input pulse width measurement |
| MB | Message buffer |
| MC | Modulus counter |
| MCB | Modulus counter buffered (up / down) |
| MCKO | Message clock out |
| MDO | Message data out |
| MSEO | Message start/end out |
| MTFE | Modified timing format enable |
| NVUSRO | Non-volatile user options register |
| OPWFMB | Output pulse width and frequency modulation buffered |
| OPWMB | Output pulse width modulation buffered |

Table A-1. Abbreviations (continued)

| Abbreviation | Meaning |
|--------------|--|
| OPWMCB | Center aligned output pulse width modulation buffered with dead time |
| OPWMT | Output pulse width modulation trigger |
| PWM | Pulse width modulation |
| SAIC | Single action input capture |
| SAOC | Single action output compare |
| SCK | Serial communications clock |
| SOUT | Serial data out |
| TBD | To be defined |
| TCK | Test clock input |
| TDI | Test data input |
| TDO | Test data output |
| TMS | Test mode select |

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Document Number: MPC5602D

Rev. 6

01/2013



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