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# LC79430KNE

CMOS LSI

## Dot-Matrix LCD Drivers

### Overview

The LC79430KNE is a large-scale dot matrix LCD common driver LSI. The LC79430KNE contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79430KNE can be used in conjunction with segment driver LC79401KNE (QIP100E) to drive a wide-screen LCD panel.

### Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support a further increases in bit number
- Supports externally supplied bias voltage
- On-chip 80-bit bidirectional shift register (supports 40-bit × 2 division)
- Supports single mode (80-bit shift register) and dual mode (40-bit × 2 shift register) applications
  - (1) O1 → O80      } Single mode
  - (2) O80 → O1     }
  - (3) O1 → O40 and O41 → O80      } Dual mode
  - (4) O80 → O41 and O40 → O1     }

All four of the shift direction selection listed above all supported
- Operating power supply voltage/operating temperature include
  - V<sub>DD</sub> (Logic section) : 2.7 to 5.5V/-20 to +85°C
  - V<sub>DD</sub>-V<sub>EE</sub> (LCD section) : 12 to 32V/-20 to +85°C
- CMOS process
- 100-pin flat plastic package (QIP100E)

# LC79430KNE

## Specifications

**Absolute Maximum Ratings** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

| Parameter                      | Symbol              | Conditions | Ratings              | unit             |
|--------------------------------|---------------------|------------|----------------------|------------------|
| Maximum supply voltage (Logic) | $V_{DD}$ max        |            | -0.3 to +7.0         | V                |
| Maximum supply voltage (LCD)   | $V_{DD}-V_{EE}$ max | *1         | 0 to 35              | V                |
| Maximum input voltage          | $V_I$ max           |            | -0.3 to $V_{DD}+0.3$ | V                |
| Storage temperature            | Tstg                |            | -40 to +125          | $^\circ\text{C}$ |

Note \*1 The following relations between elements should be maintained:  $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$ ,  $V_{DD}-V_2 \leq 7\text{V}$ ,  $V_5-V_{EE} \leq 7\text{V}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operating Ranges** at  $T_a = -20$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

| Parameter                | Symbol          | Conditions   | min         | typ | max         | unit |
|--------------------------|-----------------|--|-------------|-----|-------------|------|
| Supply voltage (Logic)   | $V_{DD}$        |  | 2.7         |     | 5.5         | V    |
| Supply voltage (LCD)     | $V_{DD}-V_{EE}$ | *2, 3  | 12          |     | 32          | V    |
| Input high level voltage | $V_{IH}$        | DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF                       | $0.8V_{DD}$ |     |             | V    |
| Input low level voltage  | $V_{IL}$        | DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF                       |             |     | $0.2V_{DD}$ | V    |
| CP Shift clock           | $f_{CP}$        | CP   |             |     | 1           | MHz  |
| CP pulse width           | $t_{WC}$        | CP   | 63          |     |             | ns   |
| Setup time               | $t_{SETUP}$     | DIO1 $\rightarrow$ CP, DIO80 $\rightarrow$ CP, DMIN $\rightarrow$ CP | 100         |     |             | ns   |
| Hold time                | $t_{HOLD}$      | DIO1 $\rightarrow$ CP, DIO80 $\rightarrow$ CP, DMIN $\rightarrow$ CP | 100         |     |             | ns   |
| CP rise time             | $t_R$           | CP   |             |     | 50          | ns   |
| CP fall time             | $t_F$           | CP   |             |     | 50          | ns   |

Note \*2 The following relations between elements should be maintained:  $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$ ,  $V_{DD}-V_2 \leq 7\text{V}$ ,  $V_5-V_{EE} \leq 7\text{V}$

\*3 When the power supply is turned on, power to the LCD driver is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

**Electrical Characteristics** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$

| Parameter                    | Symbol      | Conditions   | min          | typ | max | unit             |
|------------------------------|-------------|--|--------------|-----|-----|------------------|
| Input high level current     | $I_{IH}$    | $V_{IN}=V_{DD}$ , $V_{DD}=5.5\text{V}$ , DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF        |              |     | 1   | $\mu\text{A}$    |
| Input low level current      | $I_{IL}$    | $V_{IN}=V_{SS}$ , $V_{DD}=5.5\text{V}$ , DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF        | -1           |     |     | $\mu\text{A}$    |
| Output high level voltage    | $V_{OH}$    | $I_{OH}=-0.4\text{mA}$ , DIO1, DIO80   | $V_{DD}-0.4$ |     |     | V                |
| Output low level voltage     | $V_{OL}$    | $I_{OL}=0.4\text{mA}$ , DIO1, DIO80  |              |     | 0.4 | V                |
| Driver on resistance         | $R_{ON(1)}$ | $V_{DD}-V_{EE}=30\text{V}$ , $ V_{DE}-V_O =0.5\text{V}$<br>$V_{DD}=4.5\text{V}$ , O1 to O80 *4 |              |     | 1.0 | $\text{k}\Omega$ |
|                              | $R_{ON(2)}$ | $V_{DD}-V_{EE}=20\text{V}$ , $ V_{DE}-V_O =0.5\text{V}$<br>$V_{DD}=4.5\text{V}$ , O1 to O80 *4 |              |     | 1.0 | $\text{k}\Omega$ |
| Consumable current drain (1) | $I_{SS}$    | $V_{DD}-V_{EE}=30\text{V}$ , CP=14kHz<br>no-load, $V_{DD}=5.5\text{V}$ ; $V_{SS}$              |              |     | 100 | $\mu\text{A}$    |
| Consumable current drain (2) | $I_{EE}$    | $V_{DD}-V_{EE}=30\text{V}$ , CP=14kHz<br>no-load, $V_{DD}=5.5\text{V}$ ; $V_{EE}$              |              |     | 100 | $\mu\text{A}$    |
| Input capacitance            | CI          | f=1MHz; CP   |              | 8   |     | pF               |

Note \*4  $V_{DE} = V_1$  or  $V_2$  or  $V_5$  or  $V_{EE}$ ,  $V_1 = V_{DD}$ ,  $V_2 = 16/17 (V_{DD}-V_{EE})$ ,  $V_5 = 1/17 (V_{DD}-V_{EE})$

**Switching Characteristics** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$

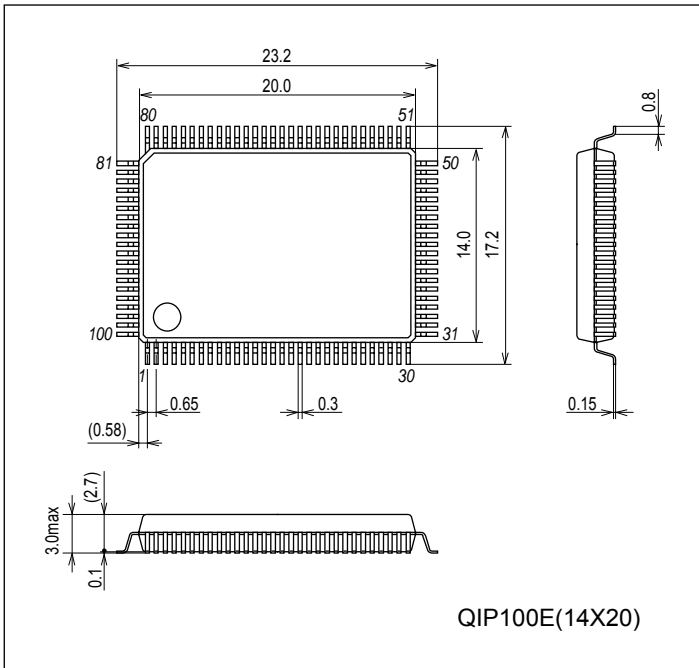
| Parameter         | Symbol    | Conditions   | min | typ | max | unit |
|-------------------|-----------|--|-----|-----|-----|------|
| Output delay time | $t_{PLH}$ | CL=15pF; CP $\rightarrow$ DIO1, CP $\rightarrow$ DIO80 |     |     | 250 | ns   |
|                   | $t_{PHL}$ | CL=15pF; CP $\rightarrow$ DIO1, CP $\rightarrow$ DIO80 |     |     | 250 | ns   |

# LC79430KNE

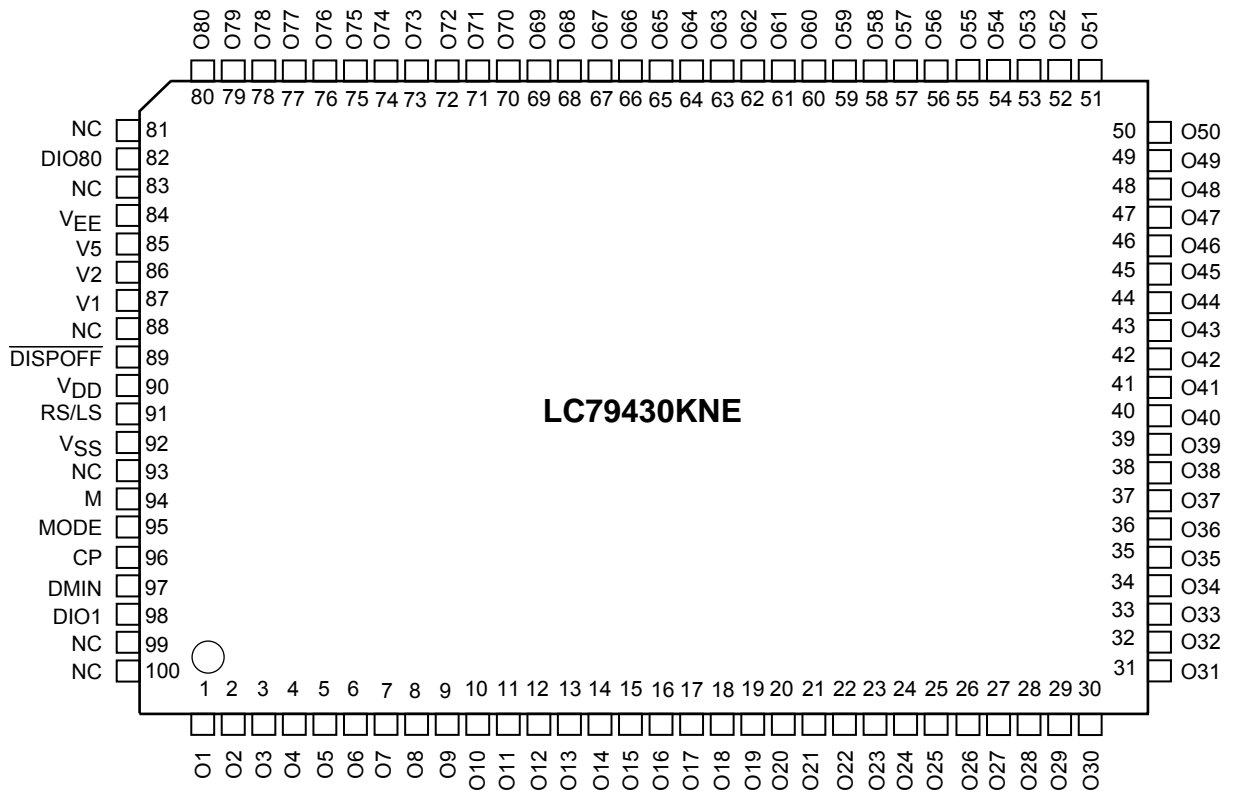
## Package Dimensions

unit:mm (typ)

3151A



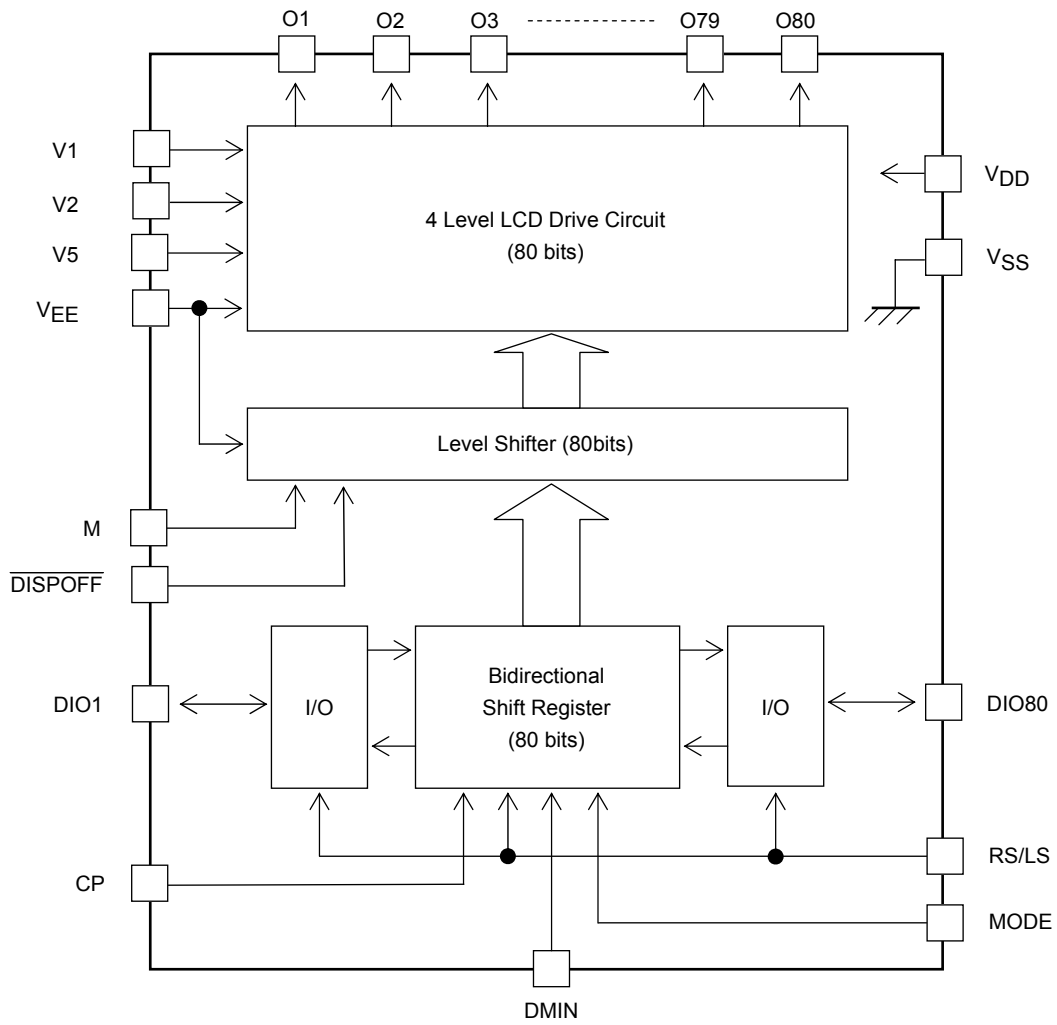
## Pin Assignment



Top view

# LC79430KNE

## Equivalent Circuit Block Diagram



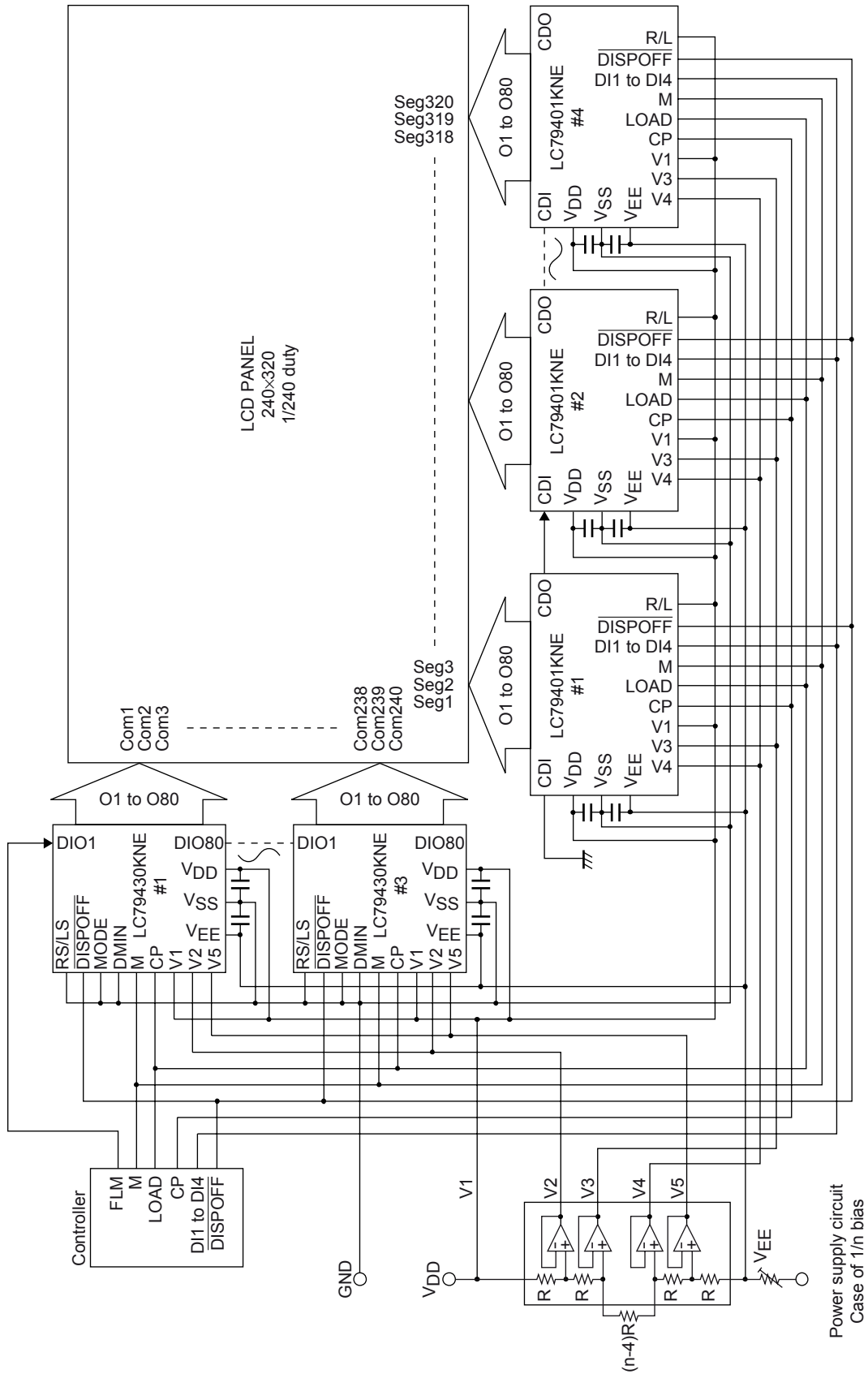
# LC79430KNE

## Pin Function

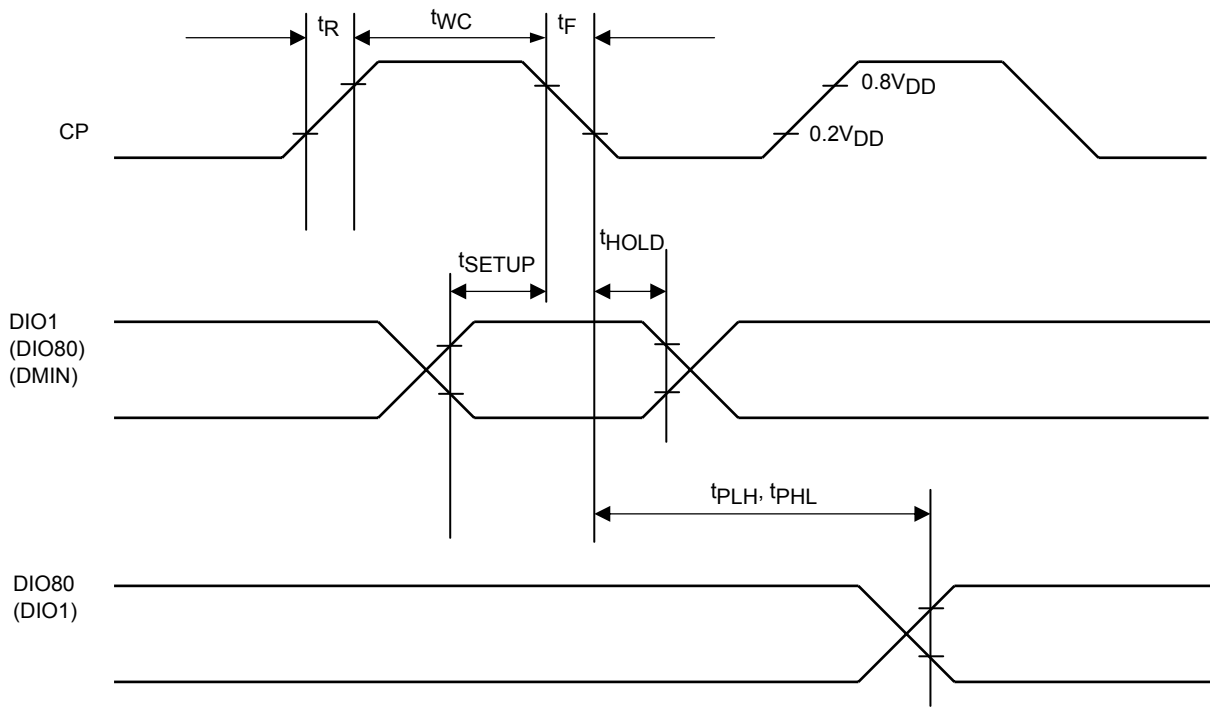
| Pin No        | Symbol                      | I/O                         | Function  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
|---------------|-----------------------------|-----------------------------|---|------|-------|-----------------------------|--------|-------|------|---------------|-----------------|----------|----|-----|-----------------|----------------|----------|-----|----|---|-------------|-----------------|----------|----|-----|----|-----------|----------------|-----------|-----|----|----|----------|
| 90            | V <sub>DD</sub>             | Supply                      | V <sub>DD</sub> -V <sub>SS</sub> : Logic power supply<br>V <sub>DD</sub> -V <sub>EE</sub> : LCD drive circuit power supply  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 92            | V <sub>SS</sub>             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 84            | V <sub>EE</sub>             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 87            | V1                          | Supply                      | LCD drive level power supply<br>V1, V <sub>EE</sub> : Selected level<br>V2, V5 : Unselected level   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 86            | V2                          |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 85            | V5                          |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 96            | CP                          | I                           | Bidirectional shift register shift clock (falling edge trigger)   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 98            | DIO1                        | I/O                         | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">MODE</th> <th style="width: 15%;">RS/LS</th> <th style="width: 20%;">Data Transfer Direction</th> <th style="width: 10%;">DIO1</th> <th style="width: 10%;">DIO80</th> <th style="width: 10%;">DMIN</th> </tr> </thead> <tbody> <tr> <td rowspan="2" style="text-align: center;">L<br/>(Single)</td> <td>L (Shift right)</td> <td style="text-align: center;">O1 → O80</td> <td style="text-align: center;">IN</td> <td style="text-align: center;">OUT</td> <td style="text-align: center;">*</td> </tr> <tr> <td>H (Shift left)</td> <td style="text-align: center;">O80 → O1</td> <td style="text-align: center;">OUT</td> <td style="text-align: center;">IN</td> <td style="text-align: center;">*</td> </tr> <tr> <td rowspan="4" style="text-align: center;">H<br/>(Dual)</td> <td rowspan="2" style="text-align: center;">L (Shift right)</td> <td style="text-align: center;">O1 → O40</td> <td rowspan="2" style="text-align: center;">IN</td> <td rowspan="2" style="text-align: center;">OUT</td> <td rowspan="2" style="text-align: center;">IN</td> </tr> <tr> <td style="text-align: center;">O41 → O80</td> </tr> <tr> <td rowspan="2" style="text-align: center;">H (Shift left)</td> <td style="text-align: center;">O80 → O41</td> <td rowspan="2" style="text-align: center;">OUT</td> <td rowspan="2" style="text-align: center;">IN</td> <td rowspan="2" style="text-align: center;">IN</td> </tr> <tr> <td style="text-align: center;">O40 → O1</td> </tr> </tbody> </table> <p>* Don't care (May be set to either "H" or "L")</p> | MODE | RS/LS | Data Transfer Direction     | DIO1   | DIO80 | DMIN | L<br>(Single) | L (Shift right) | O1 → O80 | IN | OUT | *               | H (Shift left) | O80 → O1 | OUT | IN | * | H<br>(Dual) | L (Shift right) | O1 → O40 | IN | OUT | IN | O41 → O80 | H (Shift left) | O80 → O41 | OUT | IN | IN | O40 → O1 |
| MODE          | RS/LS                       | Data Transfer Direction     |   | DIO1 | DIO80 | DMIN                        |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| L<br>(Single) | L (Shift right)             | O1 → O80                    |   | IN   | OUT   | *                           |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
|               | H (Shift left)              | O80 → O1                    |   | OUT  | IN    | *                           |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| H<br>(Dual)   | L (Shift right)             | O1 → O40                    |   | IN   | OUT   | IN                          |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
|               |                             | O41 → O80                   |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
|               | H (Shift left)              | O80 → O41                   | OUT   | IN   | IN    |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
|               |                             | O40 → O1                    |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 82            | DIO80                       | I/O                         |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 91            | RS/LS                       | I                           |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 95            | MODE                        | I                           |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 97            | DMIN                        | I                           |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 94            | M                           | I                           | LCD drive output alternation signal   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 89            | $\overline{\text{DISPOFF}}$ | I                           | O1 to O80 output controlling input pins.  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 1<br>⋮<br>80  | O1<br>⋮<br>O80              | O                           | <p>LCD drive outputs</p> <p>The output levels are determined by the combination of the output the data, The M signal, and the <math>\overline{\text{DISPOFF}}</math> pin as shown in the table.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">M</th> <th style="width: 15%;">Data</th> <th style="width: 15%;"><math>\overline{\text{DISPOFF}}</math></th> <th style="width: 55%;">Output</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">L</td> <td style="text-align: center;">L</td> <td style="text-align: center;">H</td> <td style="text-align: center;">V2</td> </tr> <tr> <td style="text-align: center;">L</td> <td style="text-align: center;">H</td> <td style="text-align: center;">H</td> <td style="text-align: center;">V<sub>EE</sub></td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">L</td> <td style="text-align: center;">H</td> <td style="text-align: center;">V5</td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">H</td> <td style="text-align: center;">H</td> <td style="text-align: center;">V1</td> </tr> <tr> <td style="text-align: center;">*</td> <td style="text-align: center;">*</td> <td style="text-align: center;">L</td> <td style="text-align: center;">V1</td> </tr> </tbody> </table> <p>* Don't care (May be set to either "H" or "L")</p>   | M    | Data  | $\overline{\text{DISPOFF}}$ | Output | L     | L    | H             | V2              | L        | H  | H   | V <sub>EE</sub> | H              | L        | H   | V5 | H | H           | H               | V1       | *  | *   | L  | V1        |                |           |     |    |    |          |
| M             | Data                        | $\overline{\text{DISPOFF}}$ | Output  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| L             | L                           | H                           | V2  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| L             | H                           | H                           | V <sub>EE</sub>   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| H             | L                           | H                           | V5  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| H             | H                           | H                           | V1  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| *             | *                           | L                           | V1  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 81            | NC                          | -                           | Must be left open.  |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 83            |                             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 88            |                             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 93            |                             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 99            |                             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |
| 100           |                             |                             |   |      |       |                             |        |       |      |               |                 |          |    |     |                 |                |          |     |    |   |             |                 |          |    |     |    |           |                |           |     |    |    |          |

# LC79430KNE

## Application Example (LC79401KNE/LC79430KNE)



Switching Characteristics Diagram



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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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