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Evaluating 16-Lead SOIC and 16-Lead QSOP Digital Isolators

FEATURES

- Convenient connections for power through screw terminal blocks
- Add-on BNC connector for 50 Ω signal sources
- On-board signal routing
- Support for signal wrap back
- Simple signal paths to reduce transmission line effects
- Pull-up and pull-down provided for control lines
- Support for *iso*Power
- Project area that supports surface-mount and through-hole devices

GENERAL DESCRIPTION

The EVAL-ADuMQSEBZ can be used with most *i*Coupler® isolation products in the 16-lead, wide-body SOIC and QSOP packages. The evaluation board supports the common pad positions for power, ground, and I/O pins found in nearly all of the *i*Coupler products and is a configurable board that can be adapted to many *i*Coupler products.

SUPPORTED *i*Coupler MODELS

- ADuM130x
- ADuM131x
- ADuM140x
- ADuM141x
- ADuM1510
- ADuM240x
- ADuM330x
- ADuM340x
- ADuM344x
- ADuM440x
- ADuM5000
- ADuM520x
- ADuM540x
- ADuM6000
- ADuM620x
- ADuM640x
- ADuM744x
- ADuM7510

EVALUATION BOARD

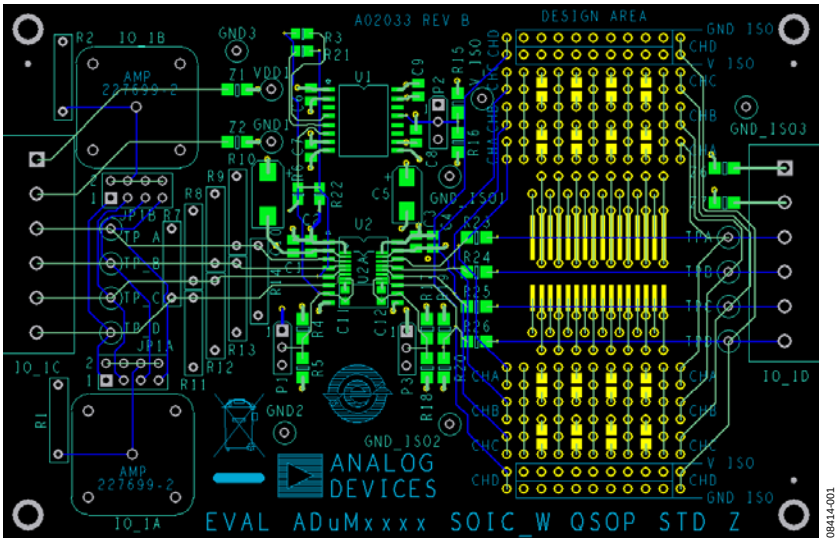

Figure 1.

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REVISION HISTORY

12/10—Rev. 0 to Rev. A

Changes to Supported *i*Coupler Models Section 1

1/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

PAD LAYOUT FOR THE DUT

The evaluation board has a pad layout in U2 that accommodates 16-lead, wide-body SOIC devices, as well as QSOP miniature packages, as shown in Figure 2. Power and ground connections connect to capacitor pads for Side 1 and Side 2.

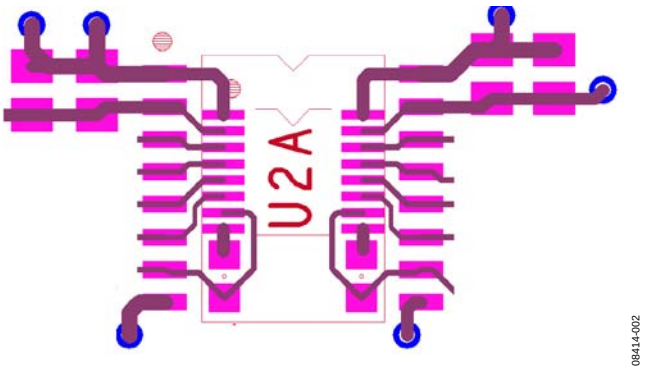

Figure 2. DUT Pad Layout Component U2

Three low inductance, surface-mount bypass capacitors are provided for each side. A 100 nF capacitor is installed on each side in Capacitor C2 and Capacitor C3. Additional bypass capacitors required for QSOP packages are below the QSOP pads and within the pad layout of the SOIC package. They cannot be installed if the SOIC is used.

In addition, there are 10 µF ceramic X7R capacitors, C1 on Side 1 and C4 on Side 2, that provide high frequency bypassing and ripple reduction. For further ripple reduction in *iso*Power® devices like the ADuM540x, tantalum capacitors are added to C10 as a 68 µF value on Side 1 and to C5 as a 22 µF value on Side 2. These large value ceramic and tantalum bypass capacitors are not necessary for non-*iso*Power devices.

Many of the *i*Coupler devices have configuration pins that allow outputs to be disabled or default levels to be set. These pins are usually located at Pin 7 and Pin 10 in the wide-body package. Pull-up 0 Ω resistors on SM Pad R4 and SM Pad R17 are provided to pull these pins high. These pull-up resistors can be removed, and pull-down resistors can be installed on R5 and R18.

In addition to the U2 DUT space, an additional pad layout is provided at U1, specifically to accommodate an ADuM5000 *iso*Power device, as shown in Figure 3. This is a power supply only device that can be used to provide secondary power for any *i*Coupler in standalone mode or as a slave to boost power to the ADuM520x or ADuM540x devices. The surface-mount resistor pads that are used to control these functions are not populated.

An ADuM5000 is not installed at Position U1; it is left to the user to obtain and install this device if required. As shown in Figure 3, the power and ground connections for this device are different from the rest of the *i*Coupler components. The C6 to C9 pad positions for bypass capacitors are provided but not populated (0.1 µF X7R ceramic capacitors are recommended).

Pull-up, pull-down, and connecting resistor pads are provided (but not populated) to connect the ADuM5000 in master or slave mode, as well as to set the output voltage. See the ADuM5000 data sheet for descriptions of the pin functions.

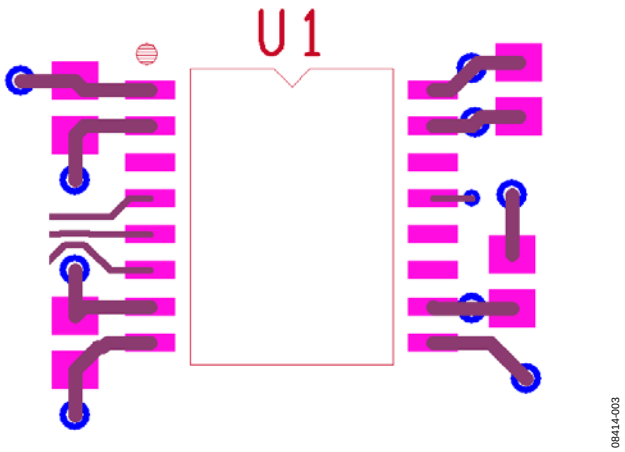

Figure 3. ADuM5000 Pad Layout Component U1

Grounding Scheme

The board consists of two separate ground and power systems. Each side of the DUT can be operated from an independent power and ground reference. This allows simulation of conditions similar to the target application. The board provides for board creepage and clearance typical of most 2.5 kV circuit boards. It is not recommended for use above 2.5 kV rms transient voltages or for isolation voltage testing above 2500 V rms.

EMI and EMC Measurements

The signal path has been made as simple as possible while still providing flexibility. The board is not intended for detailed characterization of system noise, EMI, or EMC. It may be useful for initial bench work in these areas, but Analog Devices, Inc., does not guarantee that board results will be indicative of the final system performance in these areas. The board includes some of the structures discussed in the AN-0971 Application Note for radiated EMI mitigation.

TERMINALS

Side 1 Power Supply Inputs

Power is supplied to the board via a set of terminal block connectors labeled IO_1C, as shown in Figure 4. Power is connected to the Pin 1 top terminal, and ground is connected to the Pin 2 top terminal. Provisions for adding in-line inductors for noise isolation have been made with the inclusion of Z1 and Z2, which are 1206 size surface-mount components. These positions are populated with 0 Ω resistors to connect power to the board. If ferrite inductors are required for noise control, these components should be removed and replaced with appropriate inductors.

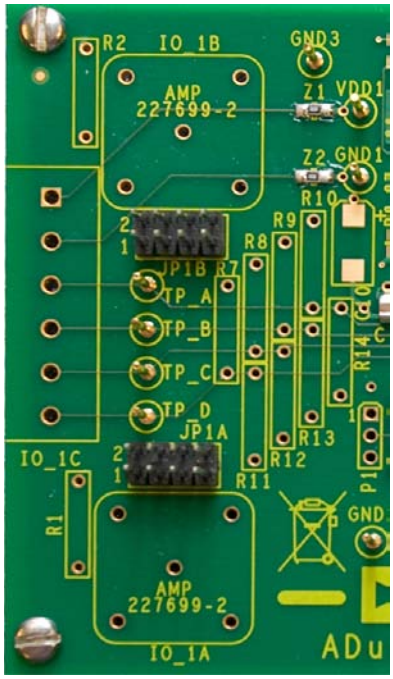

Figure 4. Side 1 Terminal Block Connector

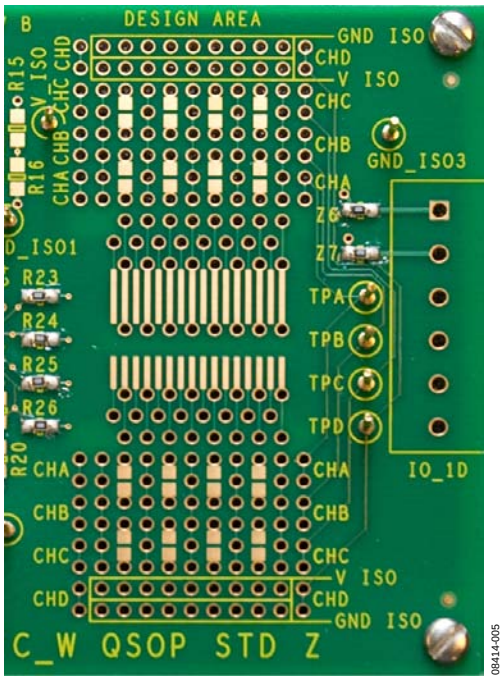

Figure 5. Side 2 Terminal Block Connector

The power and ground from the screw terminal block (if installed) are connected to the Side 1 power and ground pads of the DUT and provide power and ground to pull-up and pull-down resistors and terminations.

The ADuM640x devices differ from the rest of the *iso*Power devices in that they have an additional power supply input on Pin 7. This replaces the RC_{OUT} pin present on the ADuM5401, ADuM5402, ADuM5403, and ADuM5404. This pin must be bypassed and connected to VDD1 for proper operation of the ADuM640x. It is recommended that a 0.1 µF capacitor be installed at R5 and a 0 W resistor at R4. The ADuM640x devices are not compatible with power sharing; therefore, an ADuM5000 should not be installed at U1 when using the ADuM640x.

Side 2 Power Supply Connections

The Side 2 connections are different from those on Side 1. With standard *i*Coupler devices, these connections are power supply inputs for Side 2. However, with *iso*Power devices such as the ADuM540x, these same connections can be power outputs for off-board circuits. In addition, they can be configured as an independent power supply for the project area.

Power is connected to the terminal block connector (if installed) labeled IO_1D, as shown in Figure 5. Power is connected to IO_1D Pin 1 at the top, and ground is connected to Pin 2. Provisions for adding in-line inductors for noise isolation or for isolating the jacks from the on-board power connections have been made with the inclusion of Z6 and Z7. These positions are populated with 0 Ω resistors to connect power from the ADuM540x to the IO_1D terminal block.

When standard *i*Coupler isolators are installed, the Z6 and Z7 pads should be populated with 0 Ω resistors to connect the power jacks to the power pins of the DUT. Replace these resistors with inductors if noise isolation is required.

When *iso*Power devices are installed on the board, the power configuration required can vary greatly, depending on the demands of the application. With 0 Ω resistors or inductors installed at Z6 and Z7, the power jacks can provide power from the *iso*Power device to an external device.

DATA I/O CONNECTIONS

Side 1 Data I/O

Signals can be provided to the board and routed to the required input pins through the IO_1C terminal block connector, as shown in Figure 4. Four channel inputs/outputs can be connected from IO_1C Pin 3 through IO_1C Pin 6 to the respective A, B, C, and D channels of the ADuM540x.

Signals from the IO_1C terminal block connector channels can also be routed to some of the other data lines through the JP1A and JP1B jumper blocks (these jumper blocks correspond to BNC Channel A and Channel B, if you populate them). Each jumper block allows a channel signal from the IO_1C terminal block to be connected to additional data input lines by configuring the jumpers. The jumper blocks can also be used to wrap signals from an *i*Coupler output back to an input by using the JP1A or JP1B block to cross-connect inputs and outputs.

A common way to provide signals is with a function generator through 50 Ω coax cables. The ADuM540x board has a layout position at IO_1A and IO_1B for adding two BNC connectors, but these are not provided with the board. You can purchase the coax cables (Tyco AMP 227699-2) and populate these BNC connectors. In addition, to have 50 Ω terminations on the board for the added BNC connectors, a 50 Ω through-hole resistor should be added at the R1 and R2 positions. It is possible to route data outputs to this connector as well, but it is not recommended because proper termination is not possible for logic level signals, and improper termination can cause severe ringing on the output lines.

The Side 1 I/O structure also includes pull-up/pull-down/load positions, R7 through R14. Discrete through-hole resistors and capacitors can be installed at these positions to simulate most loading conditions or to provide pull-ups for open collector outputs.

Side 2 Data I/O

Signals can be provided to the board and routed to the required input pins through the IO_1D terminal block connector, as shown in Figure 5. It consists of terminal block connections that operate like the Side 1 structures. The terminal block connections can also be used to wrap signals from an *i*Coupler output back to an input.

In addition to the off-board I/O connections, each data channel is provided with through-hole connections to the design area.

DESIGN AREA

The design area of the evaluation board is provided to allow breadboarding of application components such as RS-485 and CAN transceivers, ADC or DAC components with direct interconnects. The design area, as shown in Figure 6, accepts most surface-mount narrow- and wide-body components with 50 mil and 100 mil pitch, as well as narrow- and wide-body 300 mil DIP through-hole devices. These surface-mount discrete components and jumper wires can be used to complete a wide variety of circuits.

The design area has convenient connection points to the primary data path, CHA to CHD, of the *i*Coupler, as well as power connections for V_{ISO} and GND_{ISO}. To allow signals from the design area to be routed to the IO_1D terminal block, remove the 0 Ω resistors for R23 through R26. Note that no ground plane is provided in the design area.

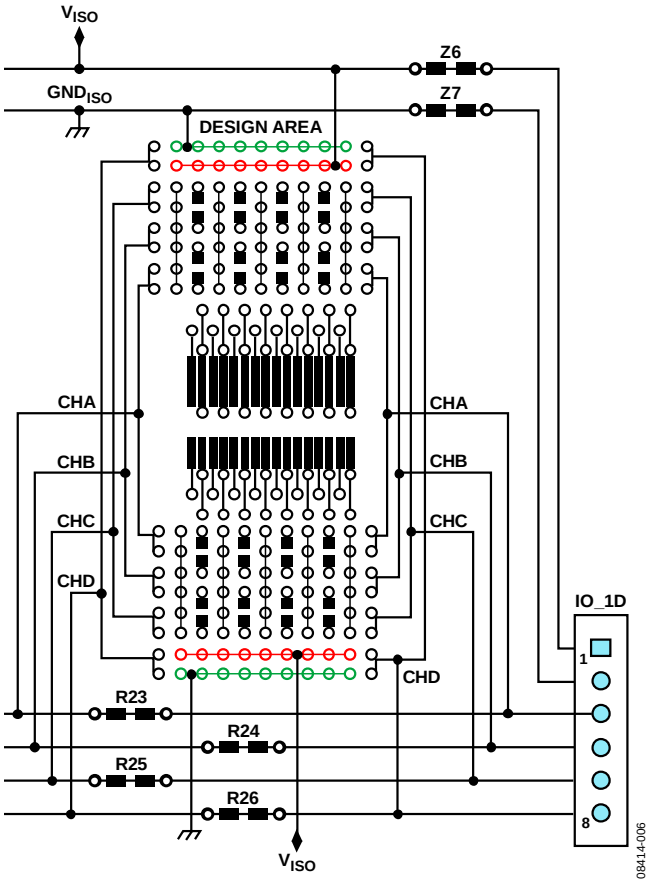

Figure 6. Design Area

EVALUATION BOARD SCHEMATICS AND LAYOUT

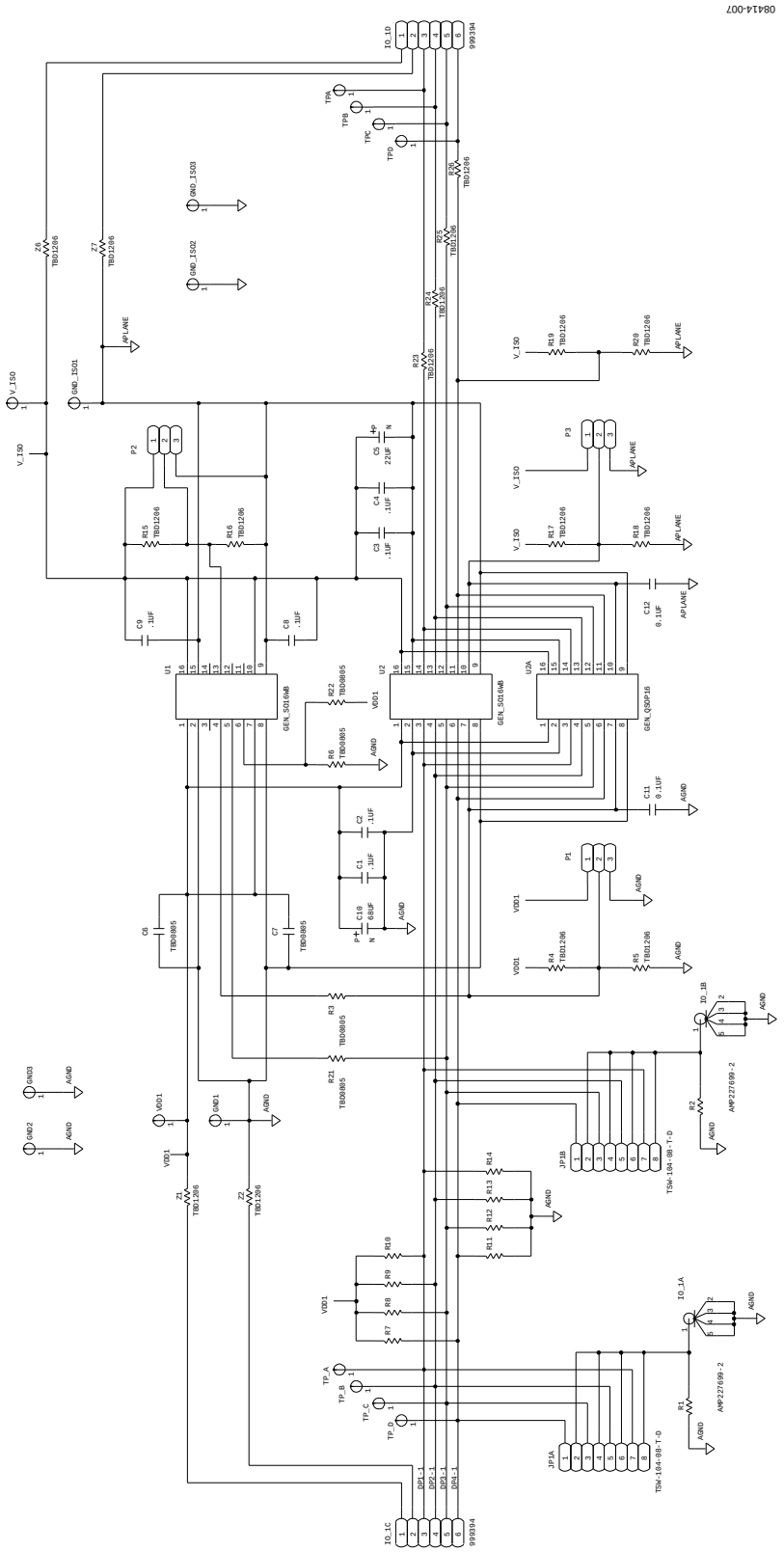

Figure 7. Schematic of ADuM540x Evaluation Board

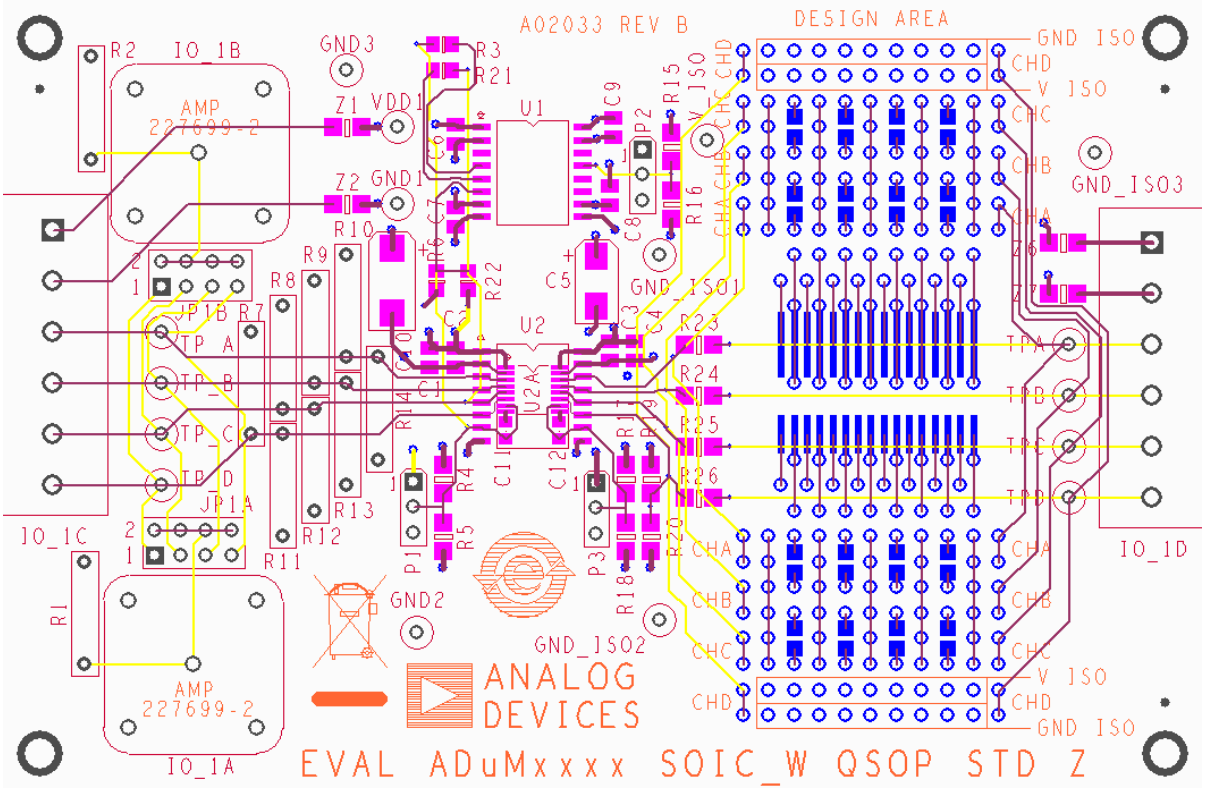

Figure 8. Evaluation Board Layout

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Supplier/Part Number
2	IO_1C, IO_1D	CONN-PCB terminal; not populated	Weidmuller/999394
0	U1	ADuM5000; not populated	N/A
0	U2	Supported *i*Coupler models SO16WB; not populated	N/A
1	C10	CAP TANT chip 68 µF; not populated	KEMET/T495X686K020AS
1	C5	CAP TANT chip 22 µF; not populated	AVX/TAJC226K020R
2	C1, C4	CAP CER X5R 10 µF; not populated	Panasonic/ECJ-2FB0J106M
2	C2, C3	CAP CER X7R 0.1 µF	Murata/GRM21BR71E104KA01L
0	C6 to C9, C11, C12	CAP CER SMD 0805; not populated	N/A
0	IO_1A, IO_1B	CONN-PCB coax BNC; not populated	Tyco AMP/227699-2
2	JP1A, JP1B	CONN-PCB header, 8-pin double row	SAMTEC/TSW-104-08-T-D
17	TP_A, TP_B, TP_C, TP_D, TPA, TPB, TPC, TPD, GND3, GND2, GND1, GND_ISO, GND_ISO1, GND_ISO2, GND_ISO3, VDD1, V_ISO	Test points	VECTOR/K24A/M
2	P1, P2	Jumper	FCI/65474-001LF
0	R3 to R6, R21, R22	RES chip SMD 0805; not populated	N/A
6	R17, R23 to R26	RES chip SMD 0805; 0 Ω	Panasonic/ERJ-6GEY0R00V
4	Z1, Z2, Z6, Z7	RES chip SMD 0805; 0 Ω	Panasonic/ERJ-6GEY0R00V
0	R15, R16, R18 to R20	RES chip SMD 0805; not populated	N/A
0	R1, R2, R7 to R14	RES SPACER_400; not populated	N/A

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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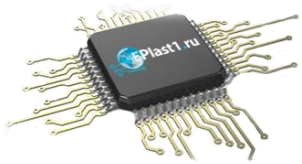

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