



PSMN4R0-40YS

N-channel LFPACK 40 V 4.2 m Ω standard level MOSFET

Rev. 02 — 12 July 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in LFPACK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low R_{DSon} and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPACK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	40	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	106	W
T _j	junction temperature		-55	-	175	°C

Static characteristics

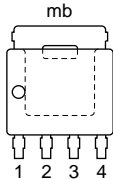
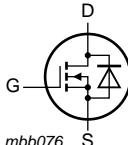
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; see Figure 12	-	-	5.6	m Ω
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see Figure 12 ; see Figure 13	-	3.2	4.2	m Ω

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$;	-	7	-	nC
$Q_{G(\text{tot})}$	total gate charge	$V_{DS} = 20\text{ V}$; see Figure 14 ; see Figure 15	-	38	-	nC
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{\text{sup}} \leq 40\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	77	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	drain		

SOT669 (LPAK)

3. Ordering information

Table 3. Ordering information

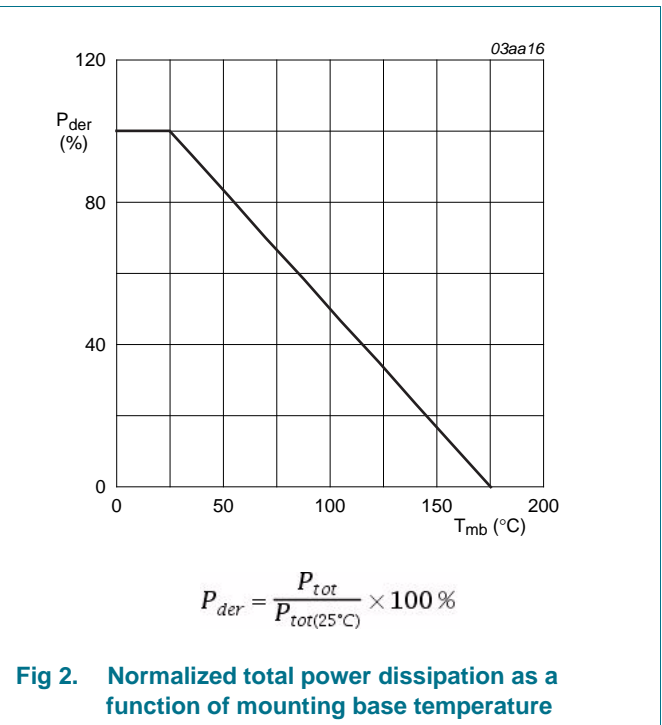
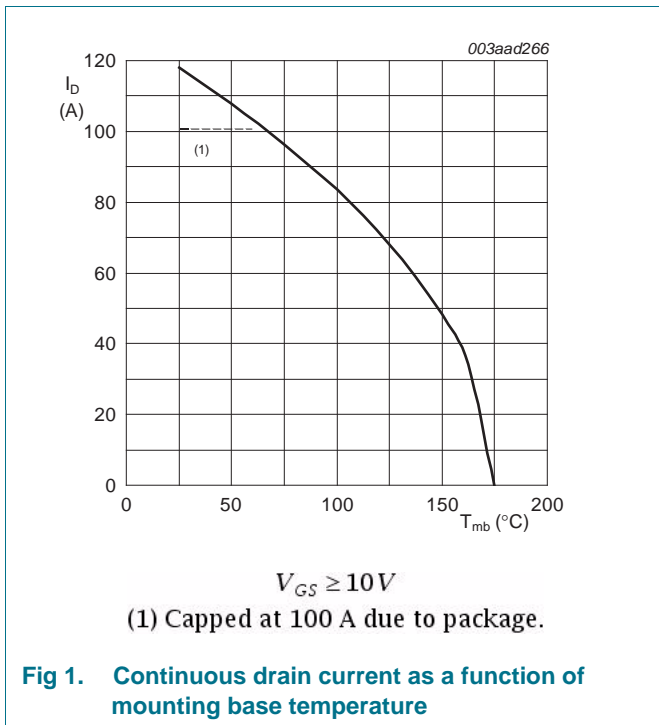
Type number	Package		Version
	Name	Description	
PSMN4R0-40YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	40	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	40	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	83	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	-	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	472	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	106	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	472	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(initial)} = 25 °C; I _D = 100 A; V _{sup} ≤ 40 V; unclamped; R _{GS} = 50 Ω	-	77	mJ



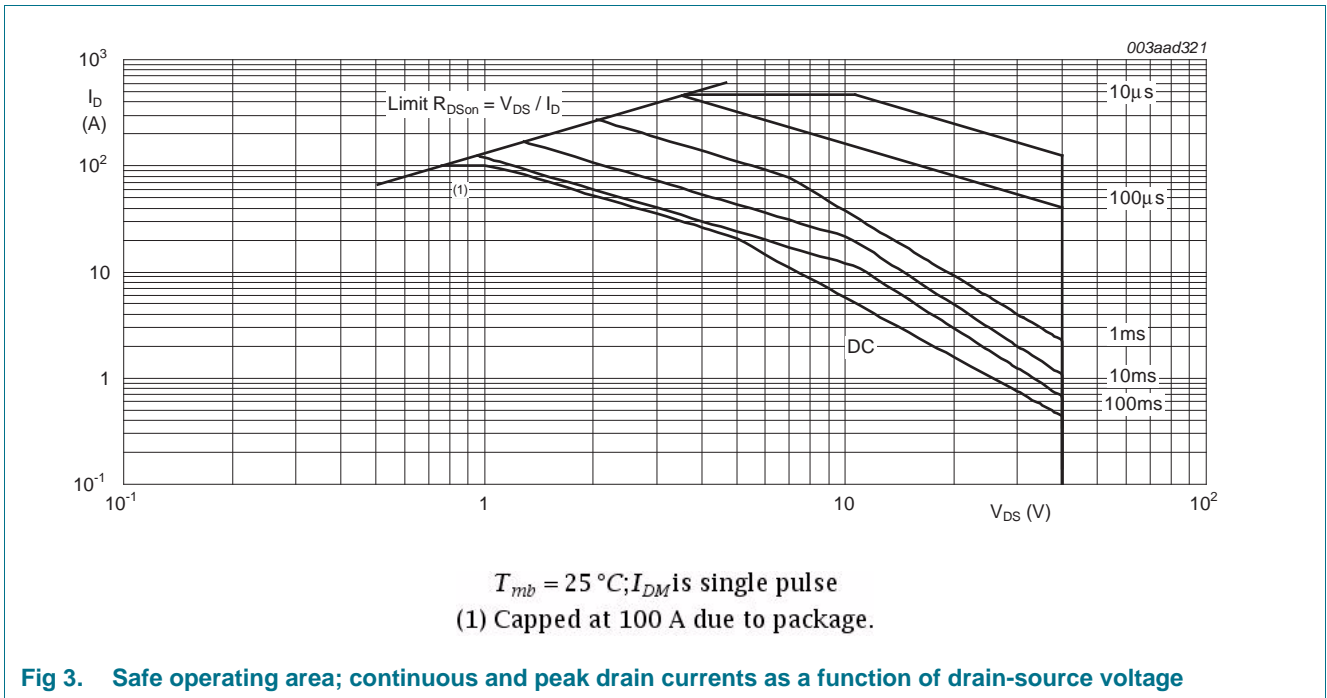


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.54	1.42	K/W

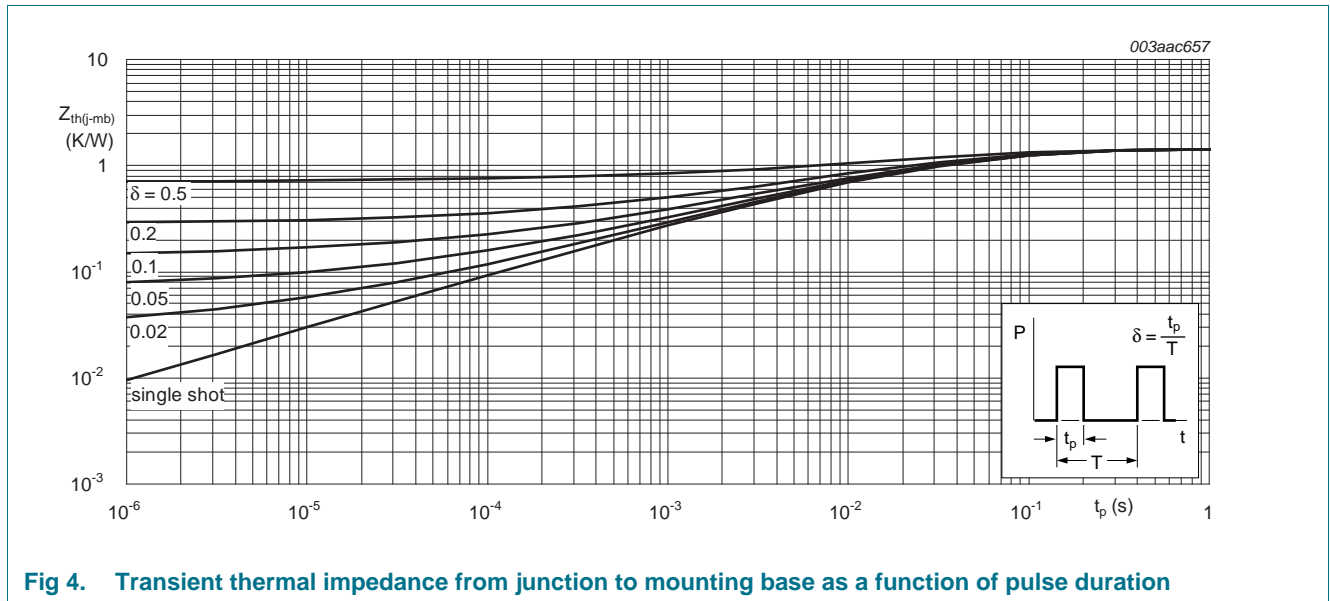


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ\text{C}$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-	-	3	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ\text{C}$	-	-	40	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12	-	-	5.6	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12	-	-	8	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	3.2	4.2	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.62	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	31	-	nC
		$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$ see Figure 14 ; see Figure 15	-	38	-	nC
Q_{GS}	gate-source charge	see Figure 14 ; see Figure 15	-	12	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$ see Figure 14	-	7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$ see Figure 14 ; see Figure 15	-	7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 20 V;$ see Figure 14	-	4.8	-	V
C_{iss}	input capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	2410	-	pF
C_{oss}	output capacitance		-	504	-	pF
C_{rss}	reverse transfer capacitance		-	266	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 V; R_L = 0.8 \text{ } \Omega; V_{GS} = 10 V;$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	18	-	ns
t_r	rise time		-	19	-	ns
$t_{d(off)}$	turn-off delay time		-	34	-	ns
t_f	fall time		-	12	-	ns

Table 6. Characteristics ...continued
 Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.83	1.2	V
t_{rr}	reverse recovery time	$I_S = 50\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	42	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	45	-	nC

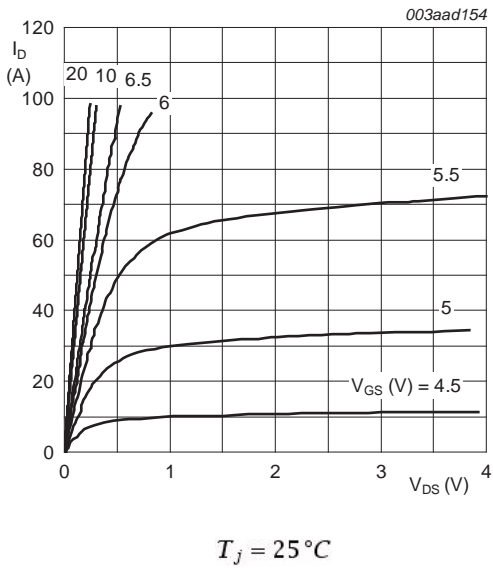


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

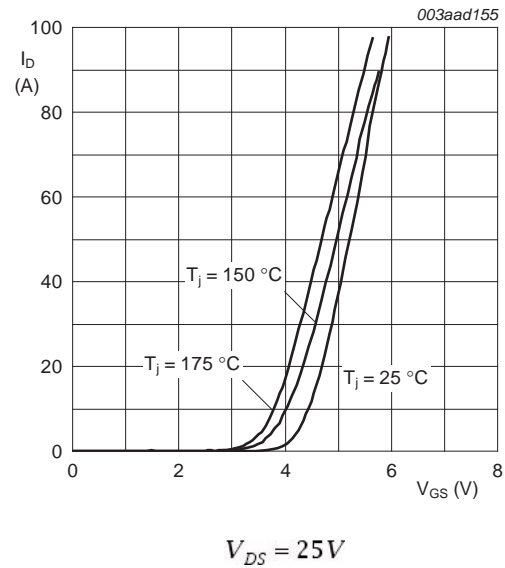


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

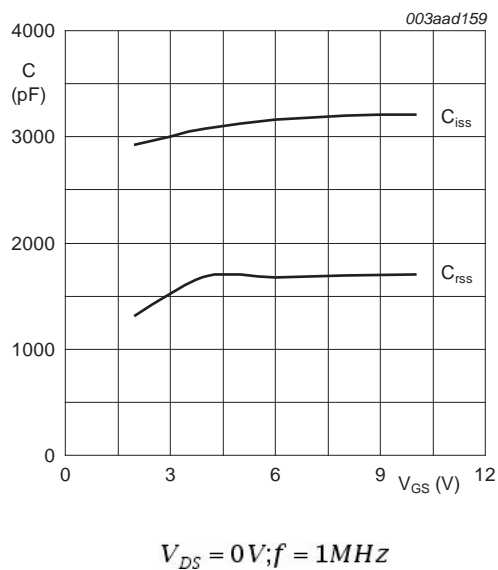


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

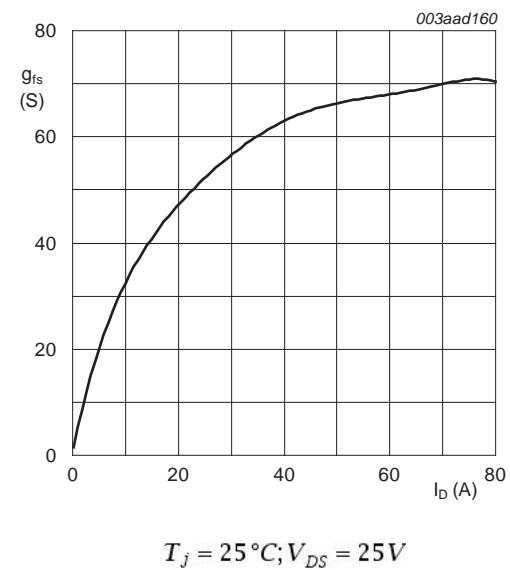
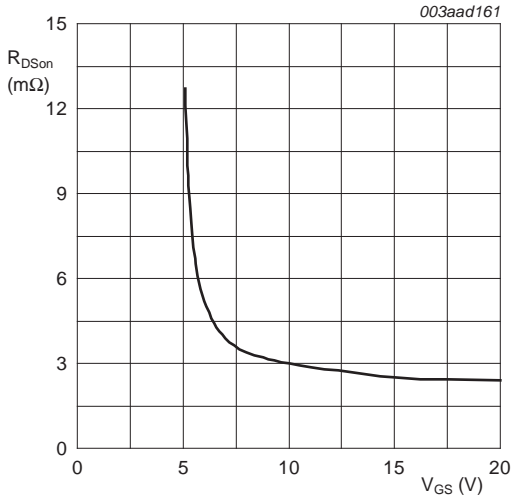
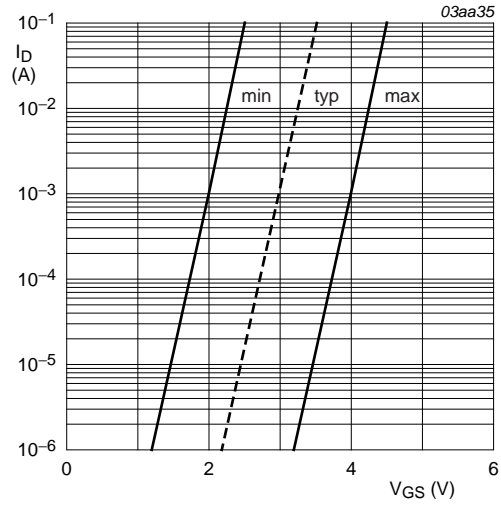


Fig 8. Forward transconductance as a function of drain current; typical values



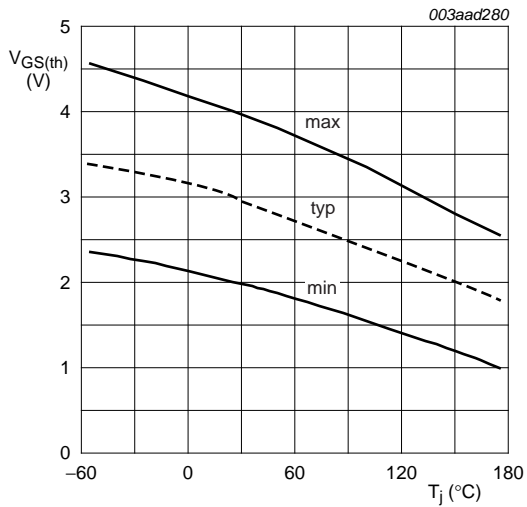
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



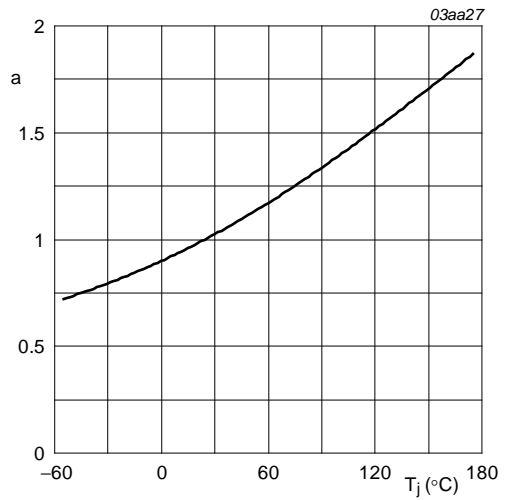
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



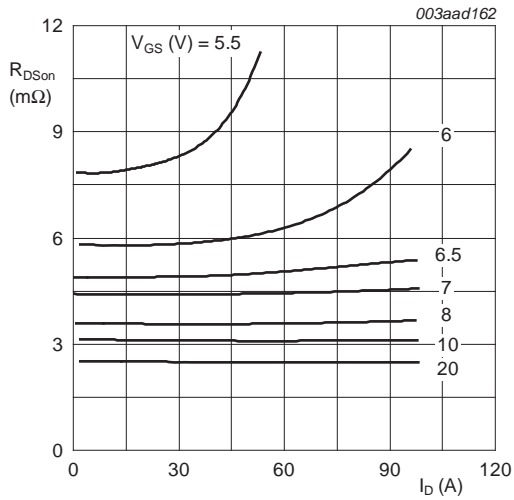
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

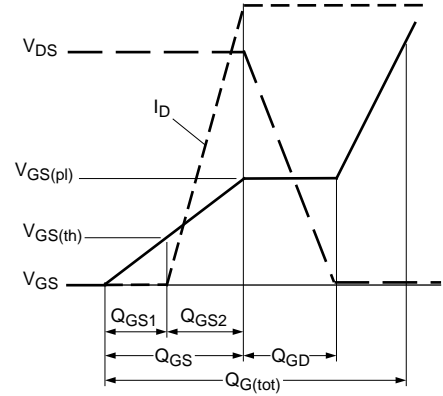
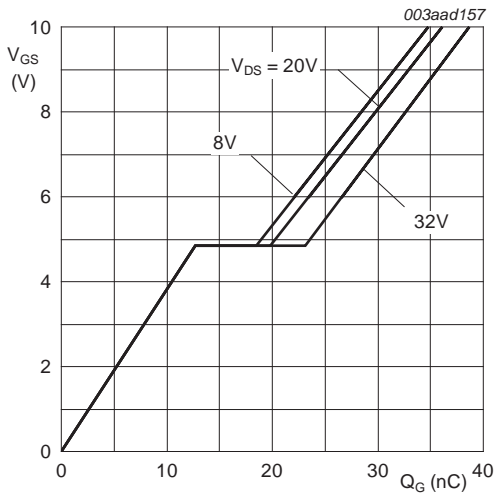
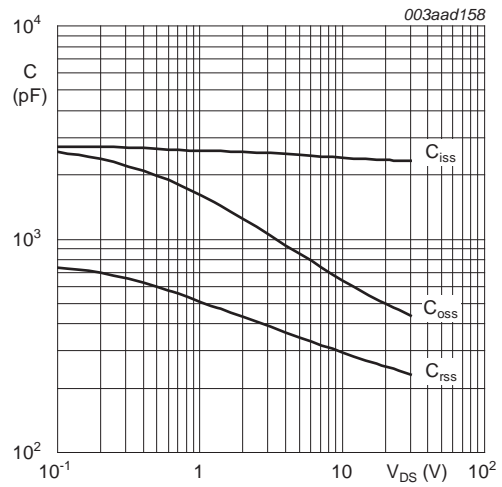


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ C; I_D = 25A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

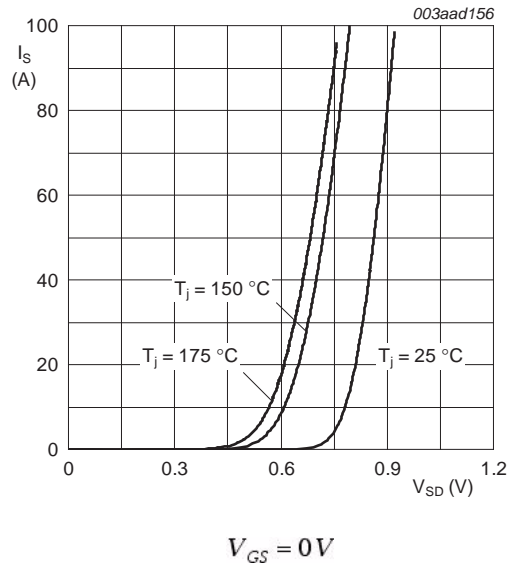


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

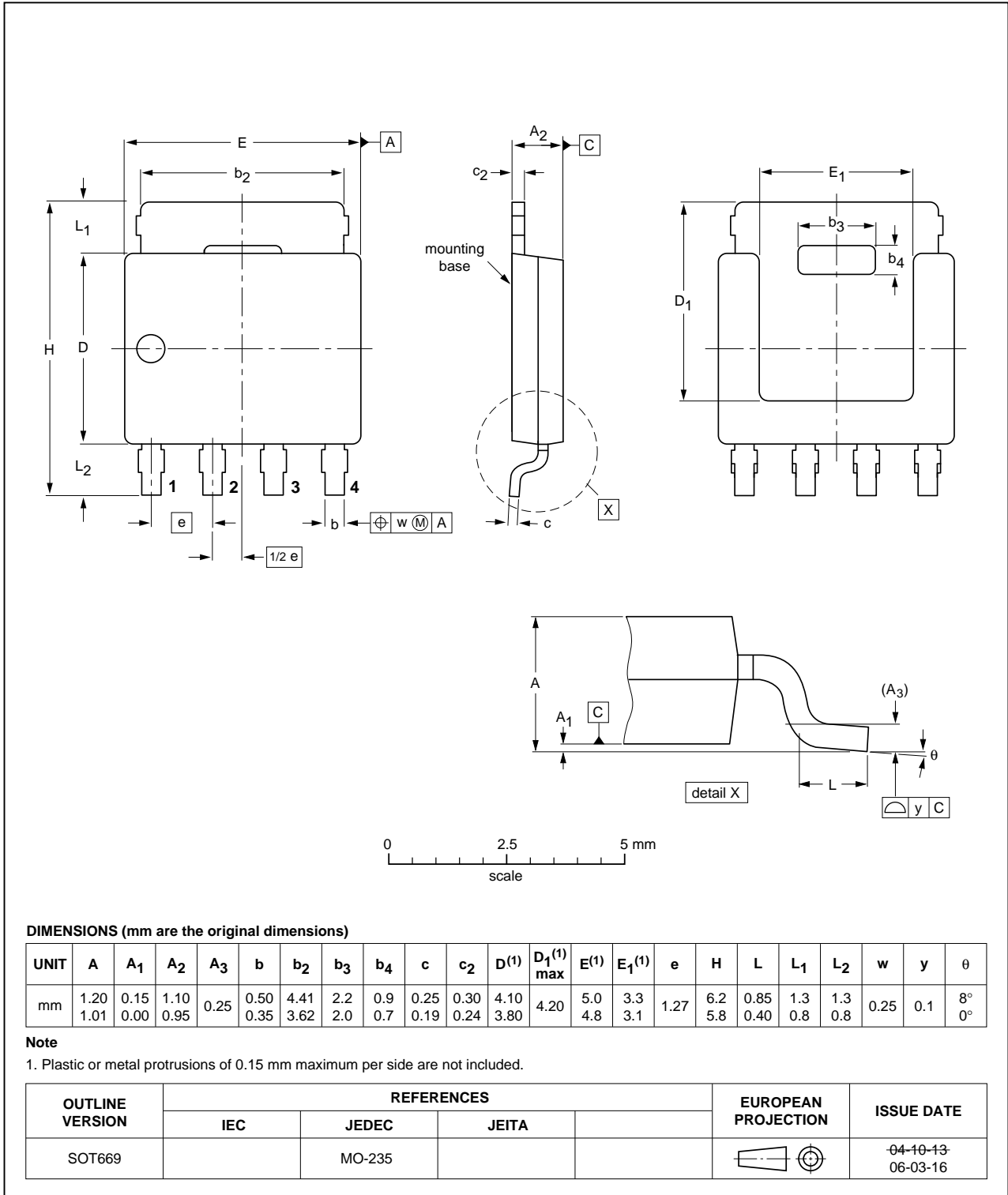


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R0-40YS v.2	20100712	Product data sheet	-	PSMN4R0-40YS v.1
Modifications:	• Various changes to content.			
PSMN4R0-40YS v.1	20090625	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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