KAF-50100

8176 (H) x 6132 (V) Full Frame CCD Image Sensor

Description

The KAF−50100 Image Sensor is a high performance, 50-megapixel CCD. Based on the TRUESENSE 6.0 micron Full Frame CCD Platform, the sensor features ultra-high resolution, broad dynamic range, and a four-output architecture. A lateral overflow drain suppresses image blooming, while an integrated Pulse Flush Gate clears residual charge on the sensor with a single electrical pulse. A Fast Dump Gate can be used to selectively remove a line of charge to facilitate partial image readout. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

The sensor shares a common pin-out and electrical configuration with the KAF−40000 Image Sensor, allowing a single camera design to support both members of this sensor family.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD (Square Pixels)
Total Number of Pixels	8304 (H) × 6220 (V) = 51.6 Mp
Number of Effective Pixels	8208 (H) × 6164 (V) = 50.5 Mp
Number of Active Pixels	8176 (H) × 6132 (V) = 50.1 Mp
Pixel Size	6.0 μm (H) × 6.0 μm (V)
Active Image Size	49.1 mm (H) × 36.8 mm (V) 61.3 mm (Diagonal), 645 1.1x Optical Format
Aspect Ratio	4:3
Horizontal Outputs	4
Saturation Signal	40.3 ke$^-$
Output Sensitivity	31 μV/e$^-$
Quantum Efficiency KAF−50100−CAA KAF−50100−AAA KAF−50100−ABA (with Lens)	 22%, 22%, 16% (Peak R, G, B) 25% 62%
Read Noise (f = 18 MHz)	12.5 e$^-$
Dark Signal (T = 60°C)	42 pA/cm^2
Dark Current Doubling Temperature	5.7°C
Dynamic Range (f = 18 MHz)	70.2 dB
Estimated Linear Dynamic Range (f = 18 MHz)	69.3 dB
Charge Transfer Efficiency Horizontal Vertical	 0.999995 0.999999
Blooming Protection (4 ms Exposure Time)	800X Saturation Exposure
Maximum Date Rate	18 MHz
Package	Ceramic PGA
Cover Glass	MAR Coated, 2 Sides

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

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Figure 1. KAF−50100 Full Frame CCD Image Sensor

Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- Ultra-High Resolution
- Board Dynamic Range
- Low Noise Architecture
- Large Active Imaging Area

Applications

- Digitization
- Mapping/Aerial
- Photography
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

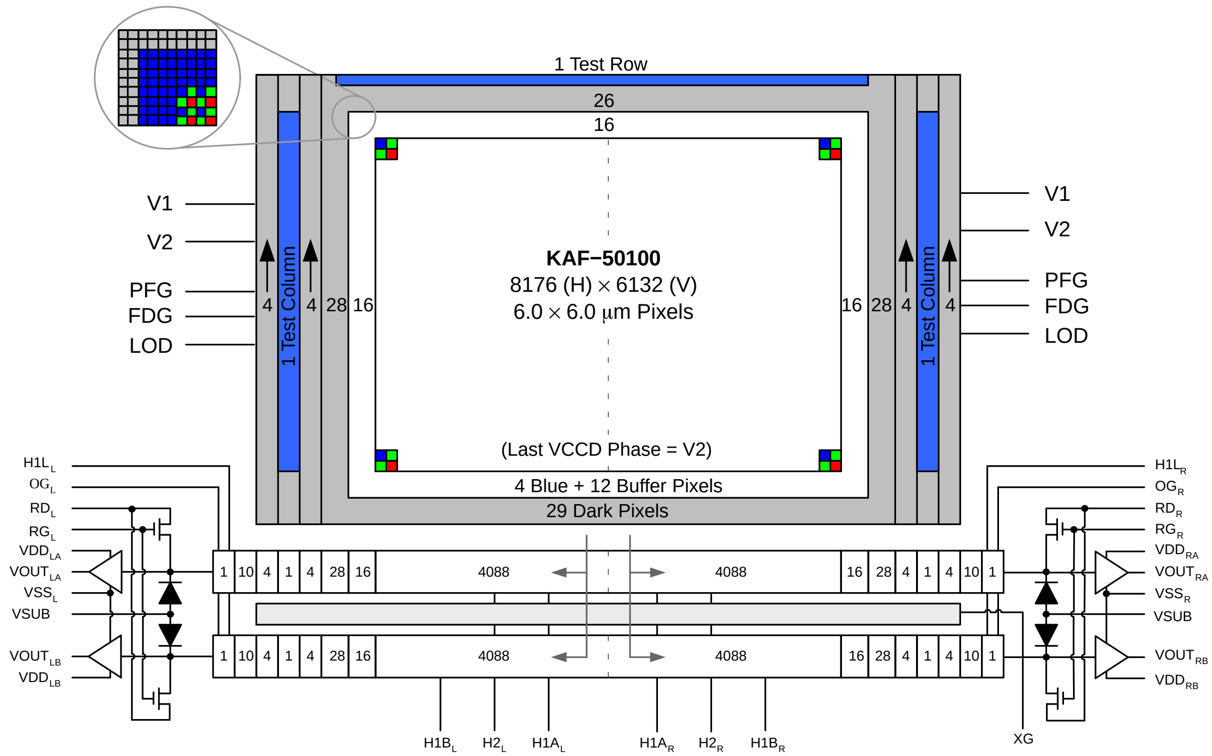
Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAF−50100−CAA−JD−AA	Color (Bayer RGB), No Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAF−50100−CAA Serial Number
KAF−50100−CAA−JD−AE	Color (Bayer RGB), No Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAF−50100−AAA−JD−BA	Monochrome, No Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAF−50100−AAA Serial Number
KAF−50100−AAA−JD−AE	Monochrome, No Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAF−50100−ABA−JR−BA	Monochrome, Microlens, Enhanced, ESD, Ceramic PGA, Taped-Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAF−50100−ABA Serial Number
KAF−50100−ABA−JR−AE	Monochrome, Microlens, Enhanced, ESD, Ceramic PGA, Taped-Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture



NOTE: Showing the filter pattern of the color version.

Figure 2. Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region are light shielded pixels that include 28 leading dark pixels on every line. There are also 29 full dark lines at the start and 26 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Dummy Pixels

Within each horizontal shift register there are 20 leading pixels. These are designated as *dummy pixels* and should not be used to determine a dark reference level.

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 16 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non-uniformities. For the leading 16 active column pixels, the first 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B). The filter description is for the color version only. No filter pattern is provided for the monochrome version.

CTE Monitor Pixels

Two CTE test columns, at the leading end of each output, and one CTE test row are included for manufacturing test purposes. The filter description is for the color version only. No filter pattern is provided for the monochrome version.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs (charge) within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel’s capacity is reached, excess electrons are discharged into the lateral overflow drain (LOD) to prevent crosstalk or ‘blooming’. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each pixel in the Vertical CCD (VCCD) is transported to the output using a two-step process. Each remaining line (row) of charge is first transported from the VCCD to a dual parallel split horizontal register (HCCD) using the V1 and V2 register clocks. The transfer to the HCCD occurs on the falling edge of V2 while H1A is held high. This line of charge may be readout immediately (dual split) or may be passed through a transfer gate (XG) into a second (B) HCCD register while the next line loads into the first (A) HCCD register (dual parallel split). Readout of each line in the HCCD is always split at the middle and, thus, either two or four outputs are used. Left (or right) outputs carry image content from pixels in the left (or right) columns of the VCCD. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the output amplifier. On each falling edge of H1L, a new charge packet is sensed by the output amplifier. Left and right HCCDs are electrically isolated from each other except for the common transfer gate (XG).

Pulsed Flush Gate/Fast Dump Gate

The Pulsed Flush Gate (PFG) feature is used to drain the charge of all pixels prior to exposure. The exception is pixels in the Fast Dump Gate (FDG) row that are drained using the separate FDG pin. Draining is accomplished by first clocking V2 high while V1 is held low. This forces all charge into the V2 phase of the pixel. While V2 is high, PFG (or FDG) may be clocked high to begin draining the signal from the pixel to the LOD. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus some characteristic time.

Horizontal Register

Output Structure

The output consists of a floating diffusion connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 4.

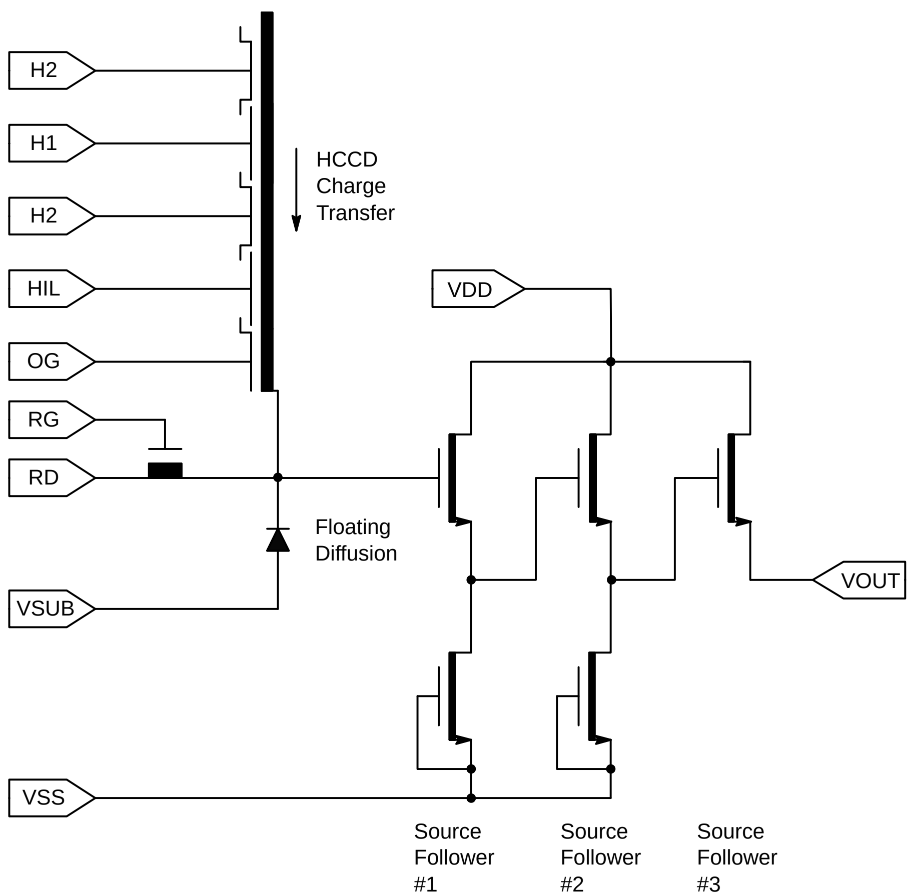
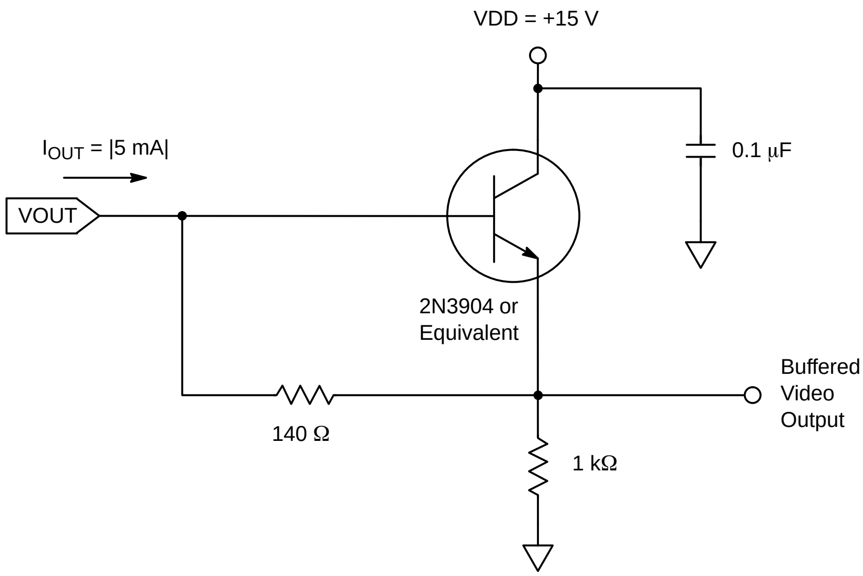


Figure 3. Output Architecture (Each Output)

Output Load



NOTE: Component values may be revised based on operating conditions and other design considerations.

Figure 4. Recommended Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation

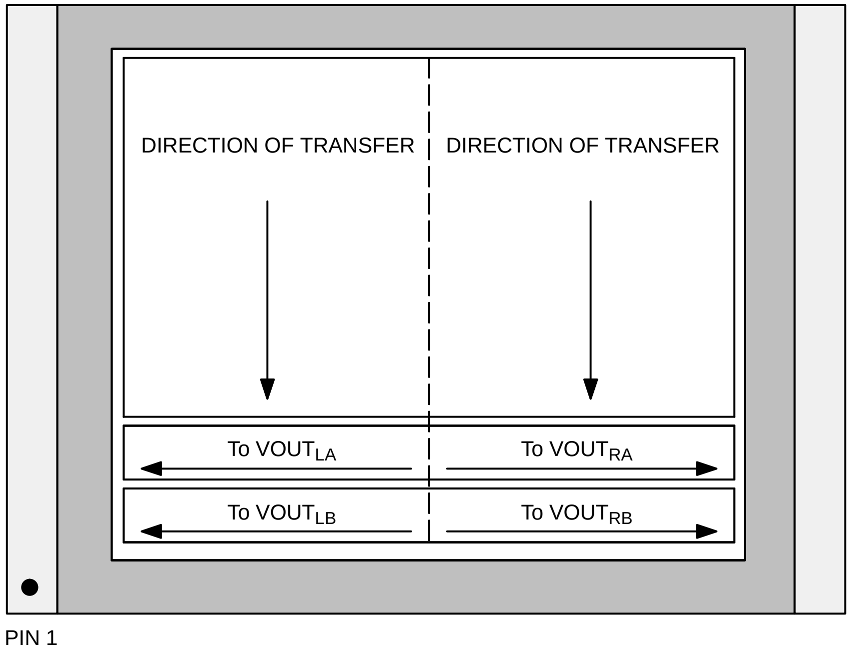
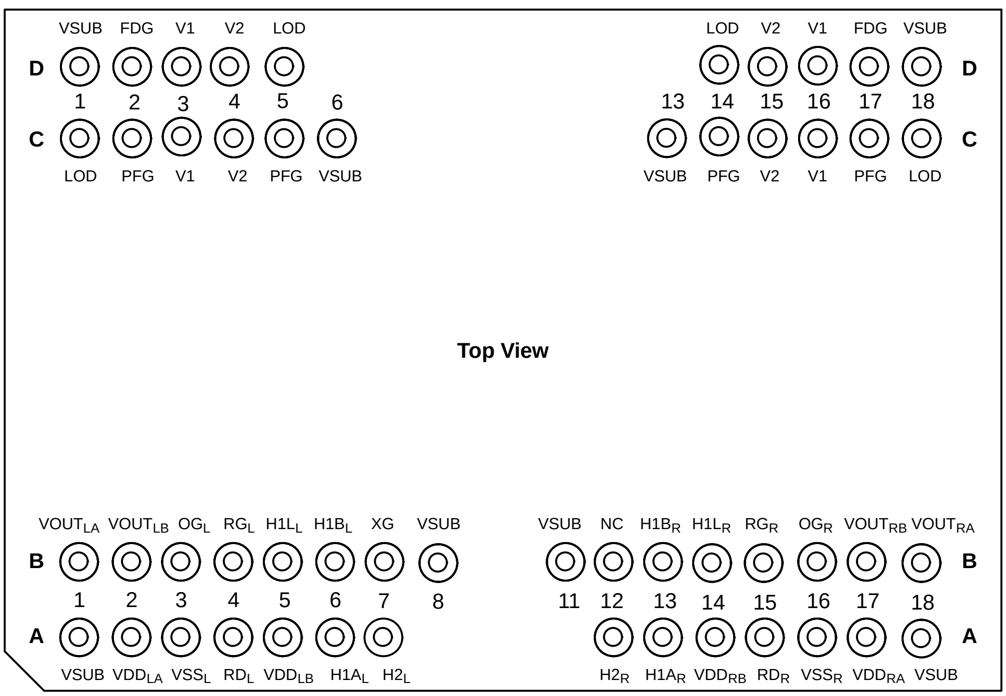


Figure 5. Image Transfer Diagram



Notes:
1. Pins with the same name are nominally tied together on the circuit board and have the same operating conditions. In addition, pins labeled with left (‘L’) and (‘R’) designations may also be tied together except for VOUT pins.
2. To achieve optimal output signal matching, electrical layout of the PCB should be made as symmetrical as possible relative to the left and right sides of the sensor.

Figure 6. Pinout Diagram

Table 3. PIN DESCRIPTION

Pin	Name	Description
A1	VSUB	Substrate
A2	VDD_{LA}	Output Amplifier Supply, Left A
A3	VSS_{L}	Output Amplifier Return, Left
A4	RD_{L}	Reset Drain, Left
A5	VDD_{LB}	Output Amplifier Supply, Left B
A6	$H1A_{L}$	Horizontal Phase 1, A Left
A7	$H2_{L}$	Horizontal Phase 2, Left
A12	$H2_{R}$	Horizontal Phase 2, Right
A13	$H1A_{R}$	Horizontal Phase 1, A Right
A14	VDD_{RB}	Output Amplifier Supply, Right B
A12	RD_{R}	Reset Drain, Right
A16	VSS_{R}	Output Amplifier Return, Right
A17	VDD_{RA}	Output Amplified Supply, Right A
A18	VSUB	Substrate

B1	$VOUT_{LA}$	Video Output, Left A
B2	$VOUT_{LB}$	Video Output, Left B
B3	OG_{L}	Output Gate, Left
B4	RG_{L}	Reset Gate, Left
B5	$H1L_{L}$	Horizontal Phase 1, Last Gate, Left
B6	$H1B_{L}$	Horizontal Phase 1, B Left
B7	XG	Horizontal Transfer Gate
B8	VSUB	Substrate
B11	VSUB	Substrate
B12	NC	No Connection
B13	$H1B_{R}$	Horizontal Phase 1, B Right
B14	$H1L_{R}$	Horizontal Phase 1, Last Gate, Right
B15	RG_{R}	Reset Gate, Right
B16	OG_{R}	Output Gate, Right
B17	$VOUT_{RB}$	Video Output, Right B
B18	$VOUT_{RA}$	Video Output, Right A

Pin	Name	Description
C1	LOD	Lateral Overflow Drain
C2	PFG	Pulse Flush Gate
C3	V1	Vertical Phase 1
C4	V2	Vertical Phase 2
C5	PFG	Pulse Flush Gate
C6	VSUB	Substrate
C13	VSUB	Substrate
C14	PFG	Pulse Flush Gate
C15	V2	Vertical Phase 2
C16	V1	Vertical Phase 1
C17	PFG	Pulse Flush Gate
C18	LOD	Lateral Overflow Drain

D1	VSUB	Substrate
D2	FDG	Fast Dump Gate
D3	V1	Vertical Phase 1
D4	V2	Vertical Phase 2
D5	LOD	Lateral Overflow Drain
D14	LOD	Lateral Overflow Drain
D15	V2	Vertical Phase 2
D16	V1	Vertical Phase 1
D17	FDG	Fast Dump Gate
D18	VSUB	Substrate

NOTE: The leads are on a 0.100″ spacing.

IMAGING PERFORMANCE

Table 4. TYPICAL OPERATIONAL CONDITIONS

Description	Test Condition − Unless Otherwise Noted	Units	Notes
Frame Time ($t_{READOUT}$ + t_{INT})	1,001 1,754	ms	Dual Parallel Split Dual Split
Integration Time (t_{INT})	Variable		
Horizontal Clock Frequency	18	MHz	
Temperature	25	°C	Room Temperature
Operation	Nominal Operating Levels		

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan[15]
Saturation Signal	N_{SAT} N_{e^-SAT} Q/V	1,075 − −	1,250 40.3 31	− − −	mV ke− μV/e−	1	Die
Quantum Efficiency (Color) Red Green Blue	QE_{MAX}	 − − −	 22 22 16	 − − −	% QE		Design
Quantum Efficiency (Monochrome) @ 450 nm	QE_{MAX}	 −	 25	 −	% QE		Design
Photoresponse Non-Linearity	PRNL	−	5	10	%	2	Die
Photoresponse Non-Uniformity	PRNU	−	8.5	25	% p−p	3	Die
Readout Dark Signal	$V_{DARK,READ}$	−	18	30	mV/s	4	Die
Integration Dark Signal	$V_{DARK,INT}$	−	3	10	mV/s	5	Die
Dark Signal Non-Uniformity	DSNU	−	1	4	mV p−p	6, 16	Die
Dark Signal Doubling Temperature	ΔT	−	5.7	−	°C	4	Design
Read Noise	NR	−	12.5	−	e− rms	7	Design
Dynamic Range	DR	−	70.2	−	dB	8	Design
Estimated Linear Dynamic Range	DR_{LIN} (Est.)	−	69.3	−	dB		Design
Red-Green Hue Shift Blue-Green Hue Shift (Color Version)	$RG_{HueUnif}$ $BG_{HueUnif}$	− −	5 5	12 12	%	9	Die
Horizontal Charge Transfer Efficiency	HCTE	−	0.999995	−		10	Design
Vertical Charge Transfer Efficiency	VCTE	−	0.999999	−			Die
Blooming Protection	X_{AB}	−	800		x Esat	11	Design
DC Offset, Output Amplifier	V_{ODC}	−	7.5	−	V	12	Die
Output Amplifier Bandwidth	f_{-3dB}	−	220	−	MHz	13	Design

Table 5. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan[15]
Output Impedance, Amplifier	R_{OUT}	−	145	−	Ω		Die
Reset Feedthrough	V_{RFT}	−	0.5	−	V	14	Design

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst-case deviation (from 15 mV & 90% N_{SAT} min) relative to a linear fit applied between 0 and 65% of V_{SAT}.
3. Difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor on a per color basis as a % of average signal level.
4. T = 60°C. t_{INT} = 0. Average non-illuminated signal with respect to over-clocked horizontal register signal.
5. T = 60°C. Average non-illuminated signal with respect to over-clocked vertical register signal.
6. T = 60°C. Absolute difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor.
7. rms deviation of horizontal over-clocked pixels measured in the dark.
8. 20Log (N_{e^-SAT} / NR)
9. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (168 × 168 blocks) within the sensor. The specification refers to the largest value of the response difference.
10. Measured per transfer above and below (~70% V_{SAT} min) saturation exposure levels. Typically, no degradation in HCCD CTE is observed up to 18 MHz.
11. X_{AB} is the number of times above the V_{SAT} illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_{AB} is measured at 4 ms.
12. Video level offset with respect to ground.
13. Last stage only. Assumes 5 pF off-chip load.
14. Amplitude of feed-through in VOUT during RG clocking.
15. A “die” parameter is measured on every sensor during production testing. A “design” parameter is quantified during design verification and not guaranteed by specification.
16. t_{INT} = 1,000 ms

TYPICAL PERFORMANCE CURVES

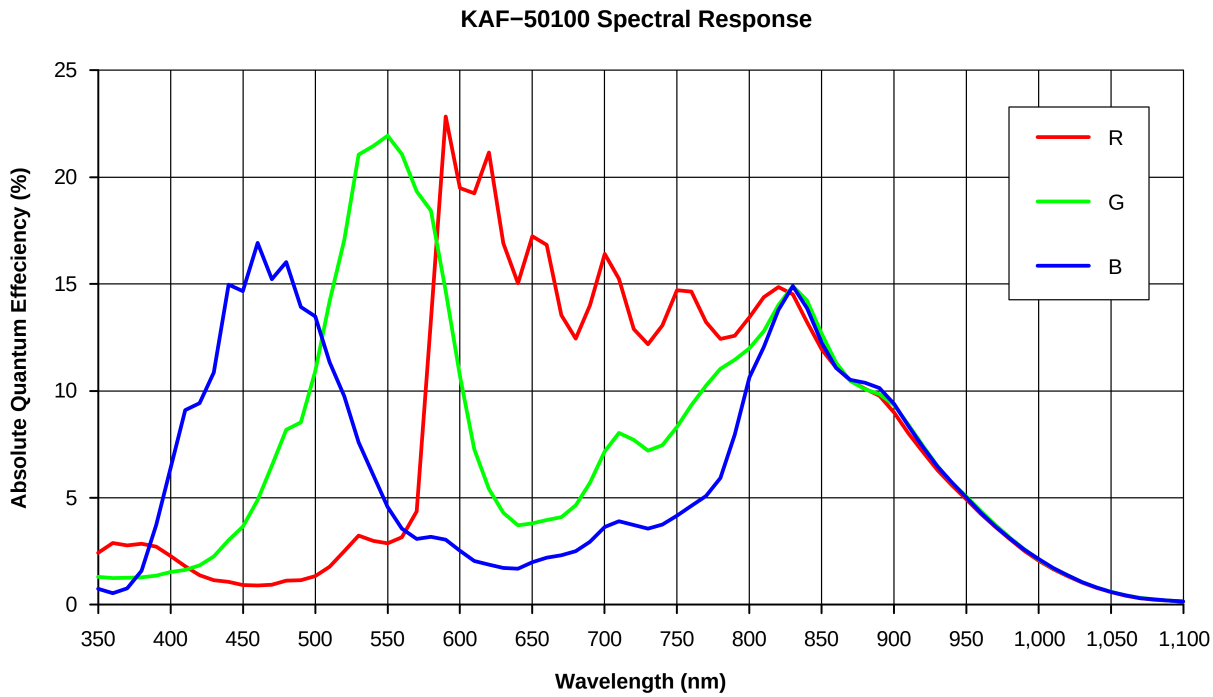


Figure 7. Spectral Response (KAF−50100−CAA Version)

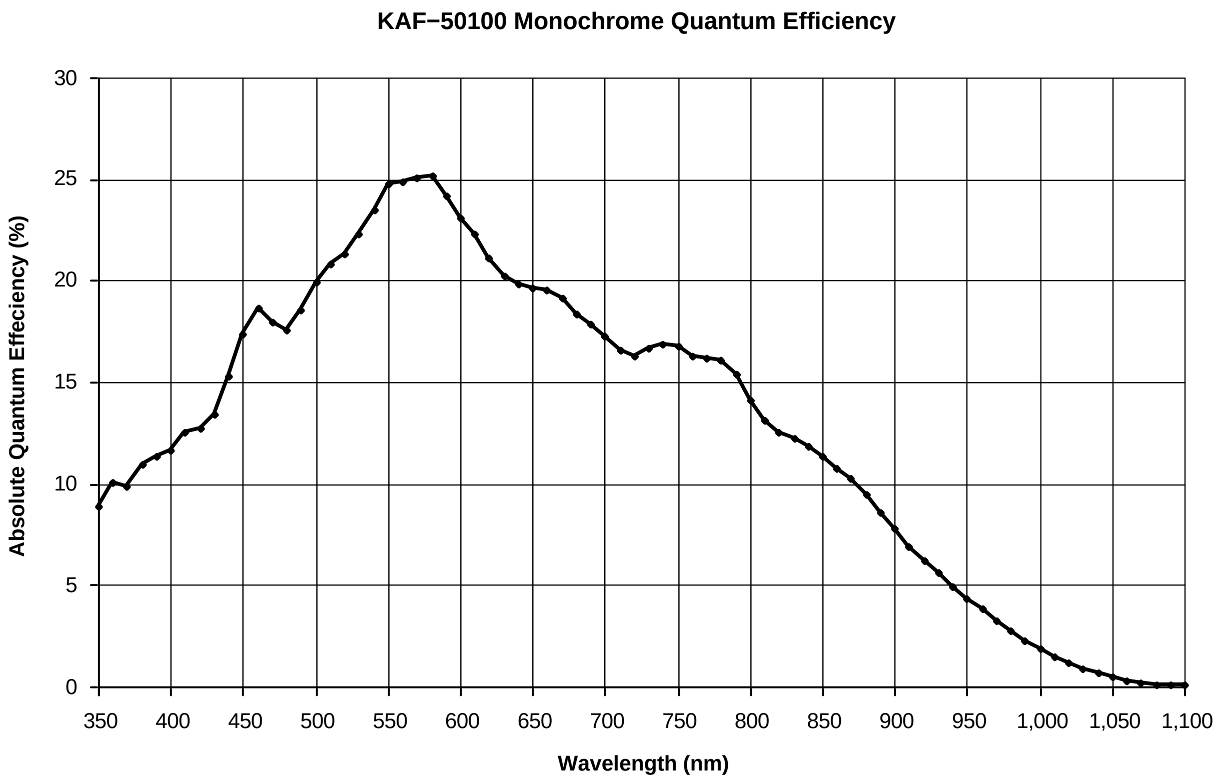


Figure 8. Spectral Response (KAF−50100−AAA Version)

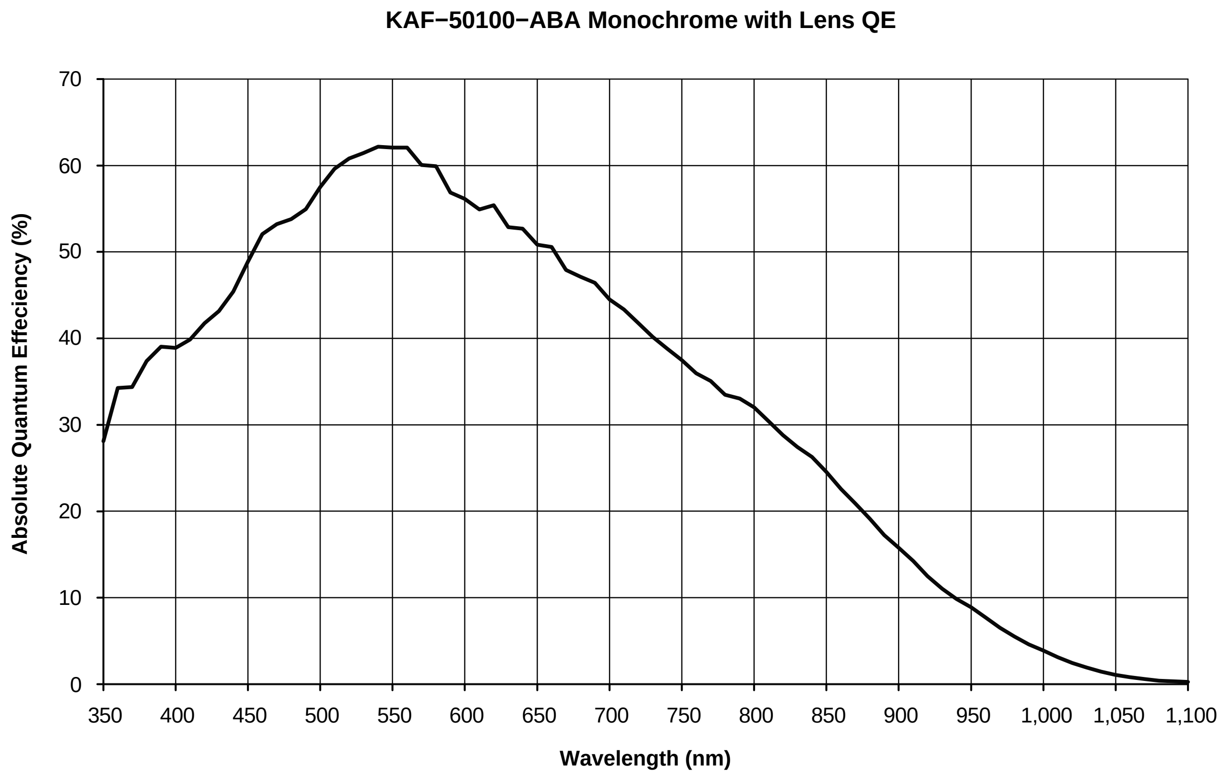


Figure 9. Spectral Response (KAF−50100−ABA Version)

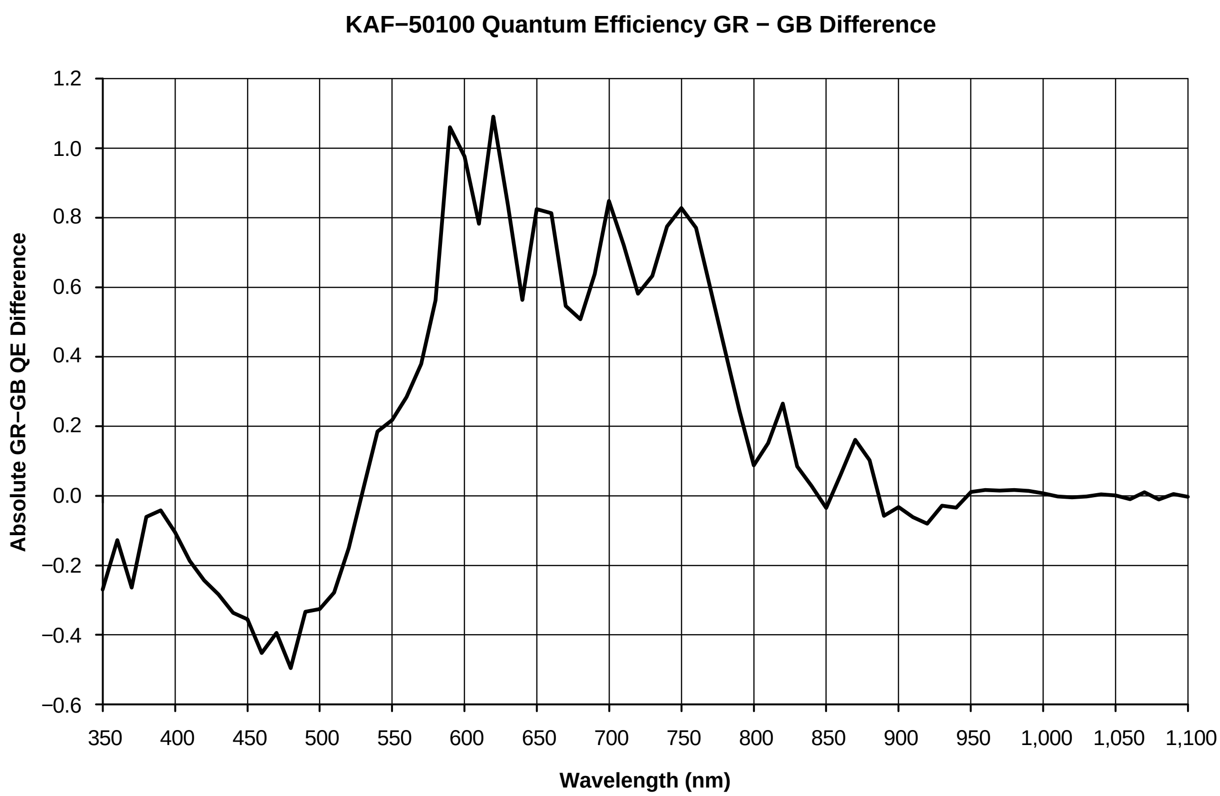


Figure 10. Typical GR − GB QE Difference (KAF−50100−CAA Version)

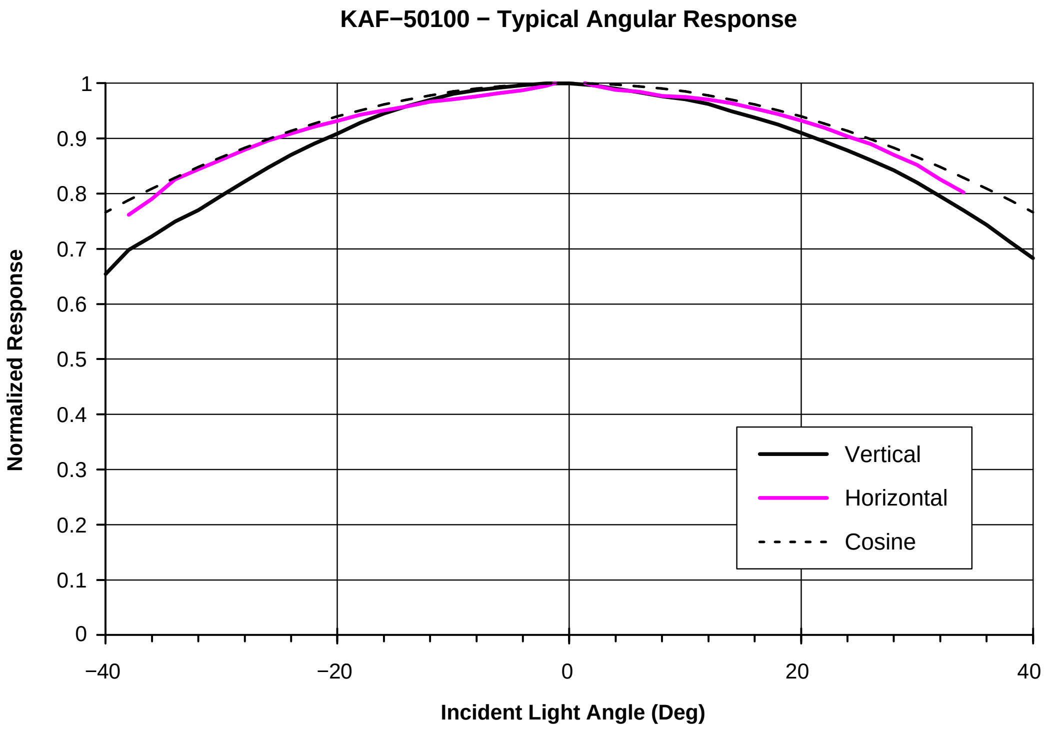


Figure 11. Typical Normalized Angle Response (KAF−50100−CAA Version)

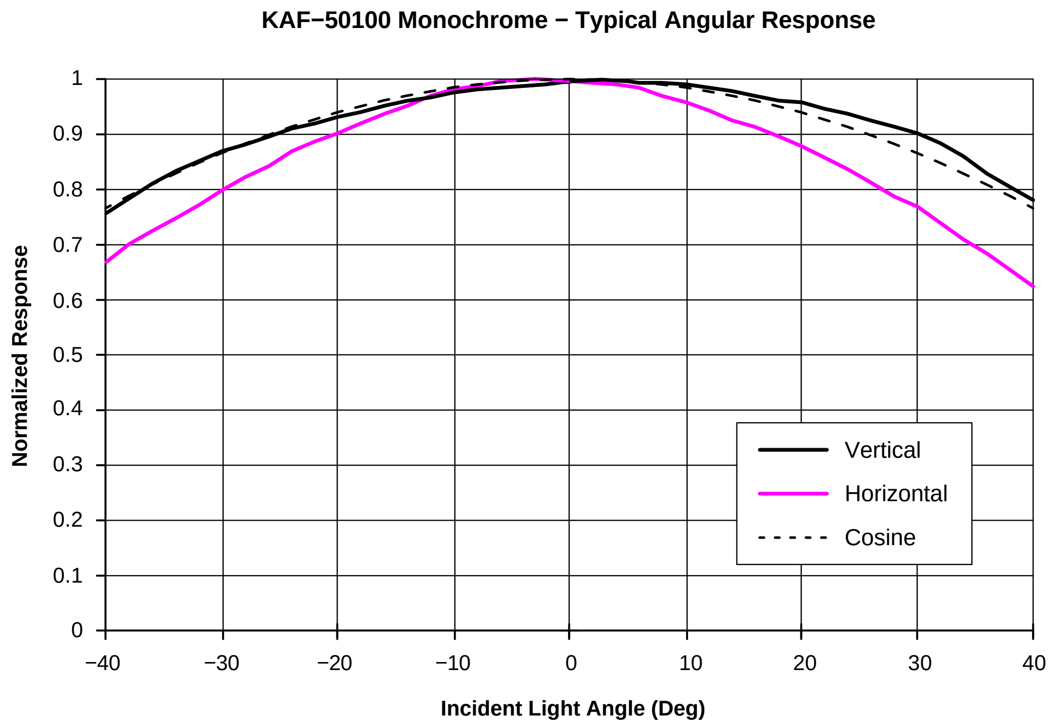


Figure 12. Typical Normalized Angle Response (KAF−50100−AAA Version)

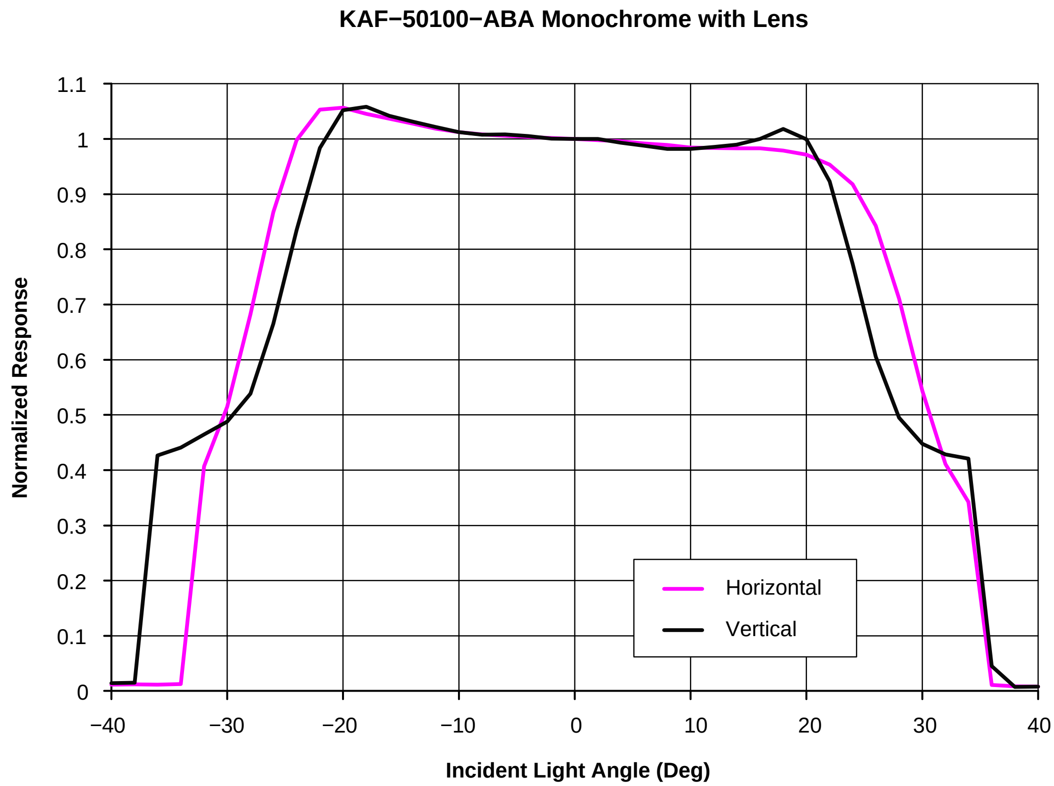


Figure 13. Typical Normalized Angle Response (KAF−50100−ABA Version)

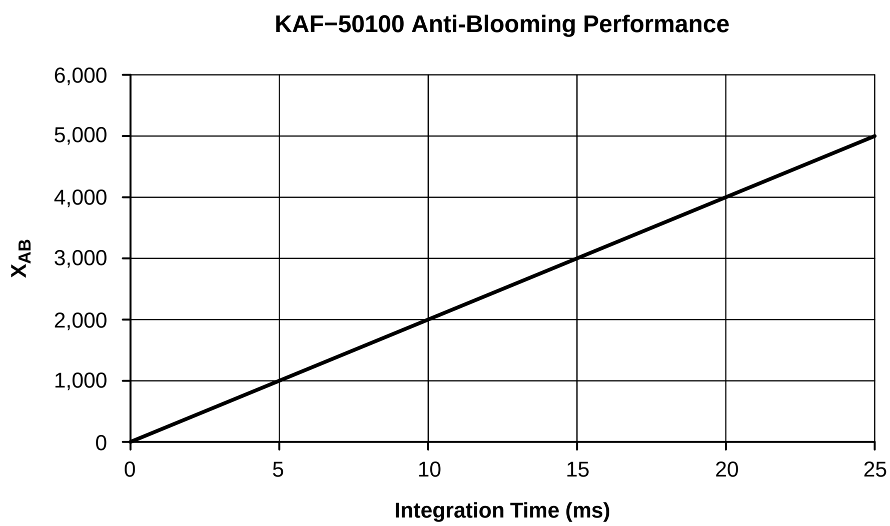


Figure 14. Typical Anti-Blooming Performance

DEFECT DEFINITIONS

Operating Conditions

Bright defect tests performed at T = 25°C, t_{INT} = 250 ms and $t_{READOUT}$ = 2,527 ms.
Dark defect tests performed at T = 25°C, t_{INT} = 1,000 ms and $t_{READOUT}$ = 2,527 ms.

Table 6. SPECIFICATIONS

Classification	Points	Clusters	Columns	Includes Dead Columns
Standard Grade	< 4,000	< 50	< 20	Yes

Point Defects

A pixel that deviates by more than 36 mV above neighboring pixels under non-illuminated conditions.

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of not more than 10 adjacent point defects.

Cluster defects are separated by no less than 4 good pixels in any direction.

Column Defect

A grouping of more than 10 point defects along a single column.

A column that deviates by more that 1.2 mV above neighboring columns under non-illuminated conditions.

A column that deviates by more that 1.5% above or below neighboring columns under illuminated conditions.

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Dead Column

A column that deviates by more than 50% below neighboring columns under illuminated conditions.

Saturated Column

A column that deviates by more than 120 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{DIODE}	−0.5	20	V	1, 2
Gate Pin Voltages	V_{GATE1}	−14.3	14.5	V	1, 3
RG Pin Voltage	V_{RG}	−0.5	14.5	V	1
Overlapping Gate Voltages	V_{1-2}	−14.3	14.5	V	4
Non-Overlapping Gate Voltages	V_{g-g}	−14.3	14.5	V	5
Output Bias Current	I_{OUT}	–	−30	mA	6
LOD Diode Voltage	V_{LODT}	−0.5	13.5	V	1
Operating Temperature	T_{OP}	0	60	°C	7

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin VSUB.
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1A, H1B, H1L, H2, OG, PFG, FDG, XG.
4. Voltage difference between overlapping gates. Includes: V1 to V2, H1/H1L to H2, H1L to OG, V1 to H2, PFG to V1/V2, FDG to V1/V2, XG to H1A/H1B/H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1A/H1B/H1L, V2 to XG, H2 to PFG/FDG, PFG to FDG.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF (Mean Time to Failure).
7. Noise performance will degrade at higher temperatures.

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	11.3	11.5	11.7	V	I_{RD} = 0.01	1
Output Amplifier Return	V_{SS}	0.5	0.7	1.0	V	I_{SS} = 3.0	1
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V	$I_{OUT} + I_{SS}$	1
Substrate	V_{SUB}	–	0	–	V	0.01	
Output Gate	V_{OG}	−2.2	−2.0	−1.8	V	0.01	1
Lateral Drain	V_{LOD}	9.8	10.0	10.2	V	0.01	1
Video Output Current	I_{OUT}	–	5	10	mA		2

1. Subscripts (L, R, LA, LB, RA, RB, T, B) have not been included in the symbol list.
2. An output load sink must be applied to VOUT to activate output amplifier – see Figure 4.

AC Operating Conditions

Table 9. CLOCK LEVELS

Pin Description for Clocked Signal	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance (Note 1)	Notes
V1 (4 Pins Total)	V1L	Low	−9.2	−9.0	−8.8	V	568 nF	2
	V1H	High	2.3	2.5	2.7	V	568 nF	2
V2 (4 Pins Total)	V2L	Low	−9.2	−9.0	−8.8	V	645 nF	2
	V2H	High	3.3	3.5	3.7	V	645 nF	2
$H1A_L$ and $H1A_R$	H1L	Low	−4.2	−4.0	−3.8	V	491 pF	2
	H1H	High	1.8	2.0	2.2	V	491 pF	2
$H1B_L$ and $H1B_R$	H1L	Low	−4.2	−4.0	−3.8	V	541 pF	2
	H1H	High	1.8	2.0	2.2	V	541 pF	2
$H1L_L$ and $H1L_R$	$H1L_{LOW}$	Low	−6.2	−6.0	−5.8	V	17 pF	2
	$H1L_{HIGH}$	High	1.8	2.0	2.2	V	17 pF	2
$H2_L$ and $H2_R$	H2L	Low	−4.2	−4.0	−3.8	V	1,025 pF	2
	H2H	High	1.8	2.0	2.2	V	1,025 pF	2
RG_L and RG_R	V_{RGL}	Low	0.8	1.0	1.2	V	15 pF	2
	V_{RGH}	High	7.8	8.0	8.2	V	15 pF	2
PFG (2 Pins Total)	PFGL	Low	−9.2	−9.0	−8.8	V	322 nF	2
	PFGH	High	4.8	5.0	5.2	V	322 nF	2
FDG (2 Pins Total)	FDGL	Low	−9.2	−9.0	−8.8	V	120 pF	2
	FDGH	High	4.8	5.0	5.2	V	120 pF	2
XG	XGL	Low	−4.7	−4.5	−4.3	V	265 pF	2
	XGH	High	2.8	3.0	3.2	V	265 pF	2

1. All pins shown are expected to draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).
2. Pins with the same name are nominally tied together on the circuit board and have the same operating conditions. For pin description entries with more than one pin for this clocked signal, the capacitance value shown is for all pins in the row tied together.

TIMING

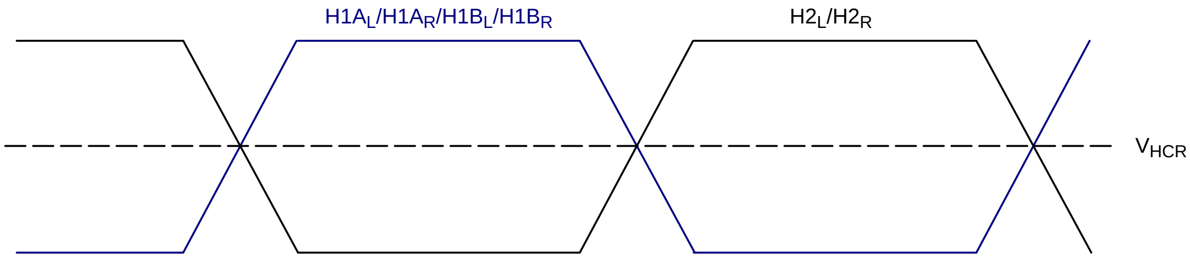
Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
H1, H2 Clock Frequency	f_H	–	–	18	MHz	1, 2
V1, V2 Clock Frequency	f_V	–	–	25	kHz	1, 2
V1−V2 Cross-over	V_{VCR}	0	1.0	2.7	V	
H1−H2 Cross-over	V_{HCR}	−2.0	−1.0	0	V	
H1, H2 Setup Time	t_{HS}	5	–	–	μs	
V2−H1A Delay	t_{D1}	5	–	–	μs	
H1A−XG Delay	t_{D2}	30	–	–	μs	
XG−V2 Delay	t_{D3}	5	–	–	μs	
H1, H2 Rise, Fall Times	t_{H1r}, t_{H1f}	5	–	10	%	5, 6
H1L Rise − H2 Fall Cross-over	V_{H1LCR}	−2.0	−1.0	1.0	V	9
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	5	–	10	%	5
RG Clock Pulse Width	t_{RGw}	5	–	–	ns	7
RG Rise, Fall Times	t_{RGr}, t_{RGf}	5	–	10	%	5
V1, V2 Clock Pulse Width	t_{Vw}	20	–	–	μs	2, 3, 4
Pixel Period (1 Count)	t_e	55.56	–	–	ns	2
H1L−VOUT Delay	t_{HV}	–	10	–	ns	
RG−VOUT Delay	t_{RV}	–	5	–	ns	
Readout Time	$t_{READOUT}$ − DS $t_{READOUT}$ − DPS	1.71 0.98	– –	– –	s	8
Frame Rate	t_F − DS t_F − DPS	0.6 1.0	– –	– –	fps	8
Line Rate	t_{LINEDS} − DS t_{LINEDP} − DPS	275.7 315.7	– –	– –	μs	8
PFG Holdoff Time	t_{PFG}	180	–	–	μs	
FDG Holdoff Time	t_{FDG}	20	–	–	μs	

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Longer times will degrade noise performance.
4. Measured where V_{CLOCK} is at 0 V.
5. Relative to the pulse width (based on 50% of high/low levels).
6. The maximum specification or 10 ns whichever is greater based on the frequency of the horizontal clocks.
7. RG should be clocked continuously.
8. DS = Dual Split DPS = Dual Parallel Split.
9. The charge capacity near the output could be degraded if the voltage at the clock crossover point is outside this range.

Edge Alignment

Horizontal Clock



Vertical Clock

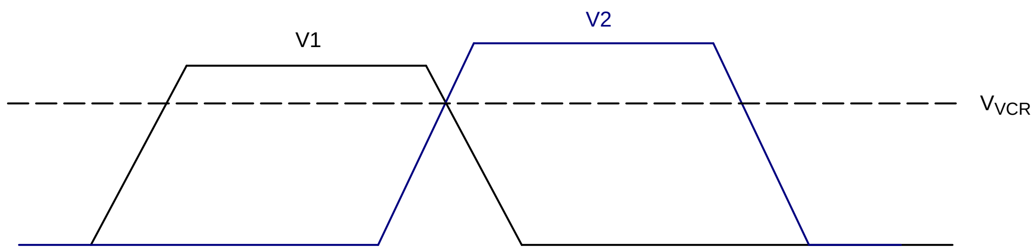


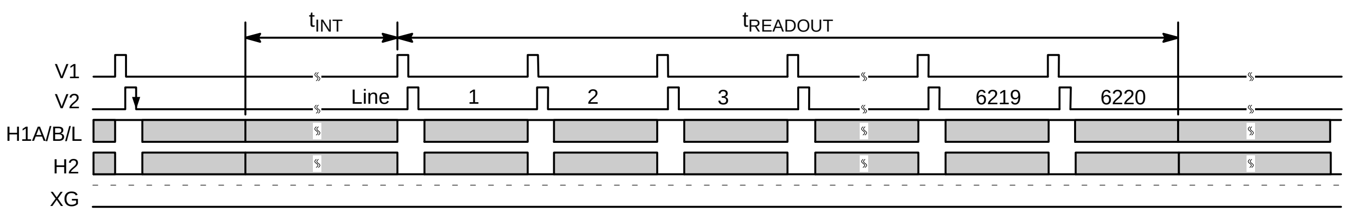
Figure 15. Timing Edge Alignment

Frame Timing

Dual split timing reads the pixels out of $VOUT_{LA}$ and $VOUT_{RA}$. H1B may be grounded in this operating mode.

Dual-Parallel Split timing reads pixels out of all four outputs with even lines reading out of $VOUT_{LA}$ and $VOUT_{RA}$ and odd lines reading out of $VOUT_{LB}$ and $VOUT_{RB}$.

Frame Timing − Dual Split



Frame Timing − Dual-Parallel Split

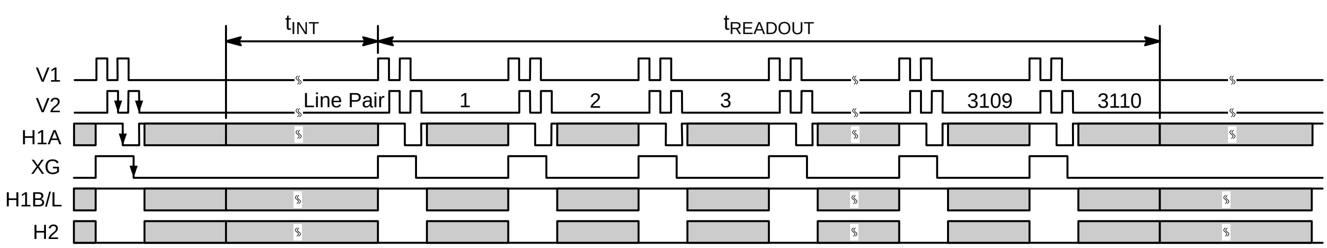


Figure 16. Frame Timing

Frame Timing Detail

Vertical Clocks

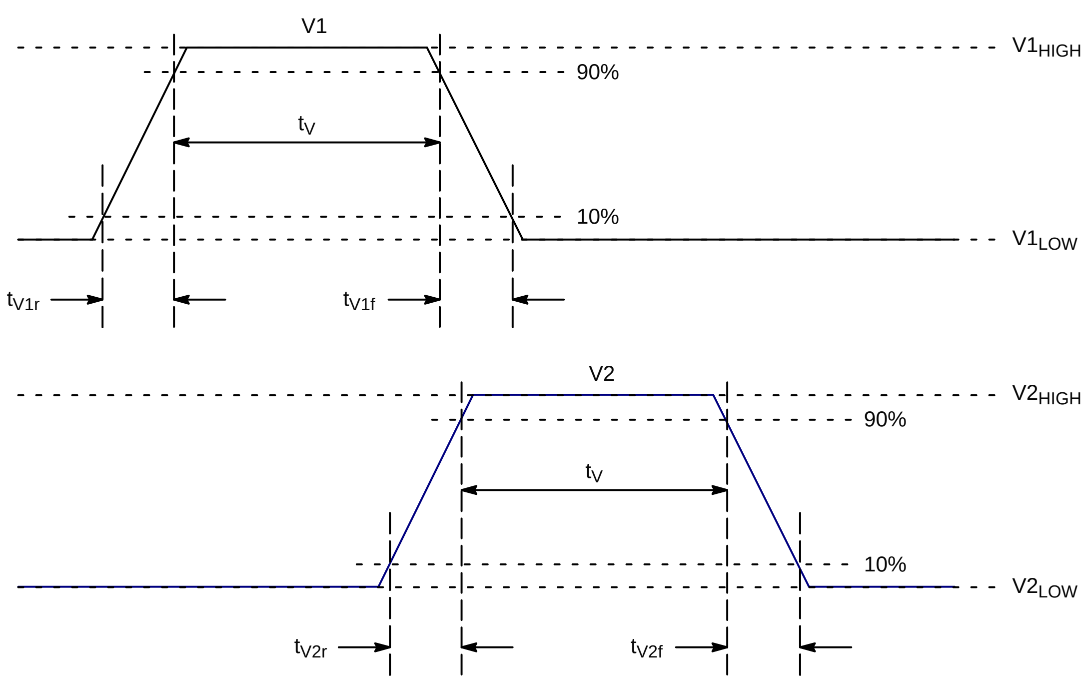
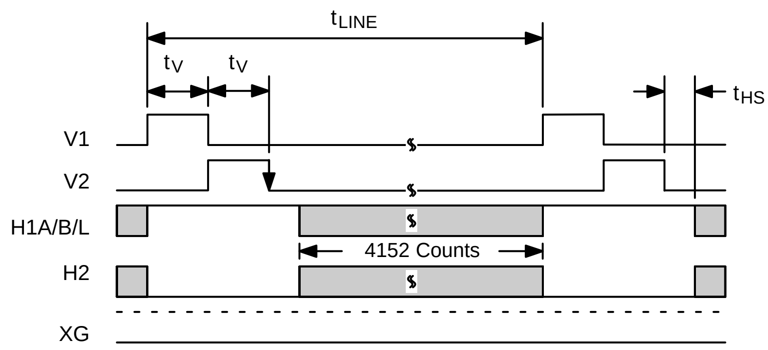


Figure 17. Frame Timing Detail

Line Timing (Each Output)

XG is held low unless the Dual-Parallel Split timing is required. While operating in Dual-Parallel Split mode, full resolution rows are passed from V2 (t_{D1}), through H1A (t_{D2}), and then passed through XG (t_{D3}) and into H1B. During this time, the second, full resolution, row will load into H1A at the second falling edge of V2 following the characteristic delay t_{HD}.

Line Timing − Dual Split



Line Timing − Dual-Parallel Split

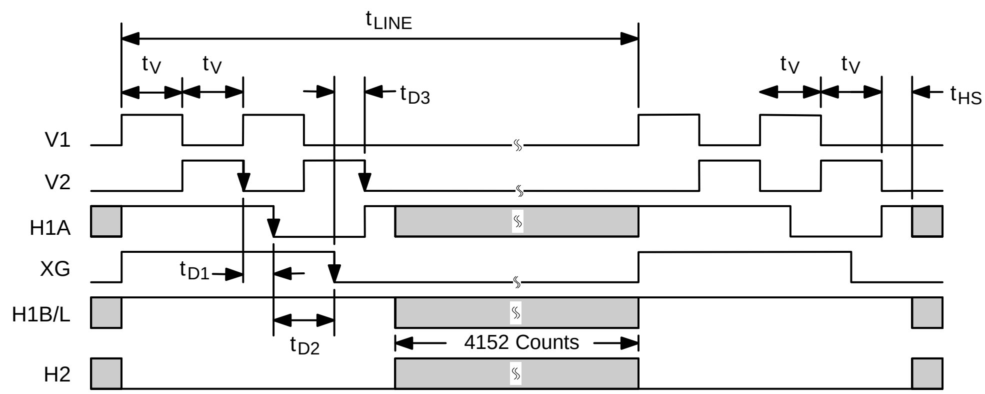


Figure 18. Line Timing

Pixel Timing

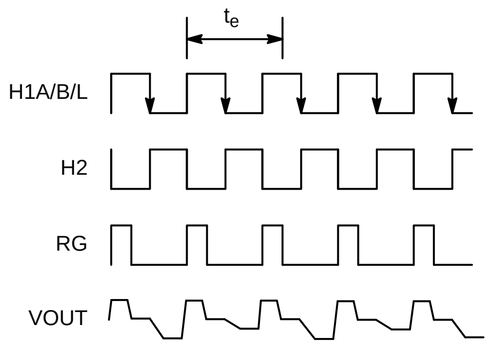
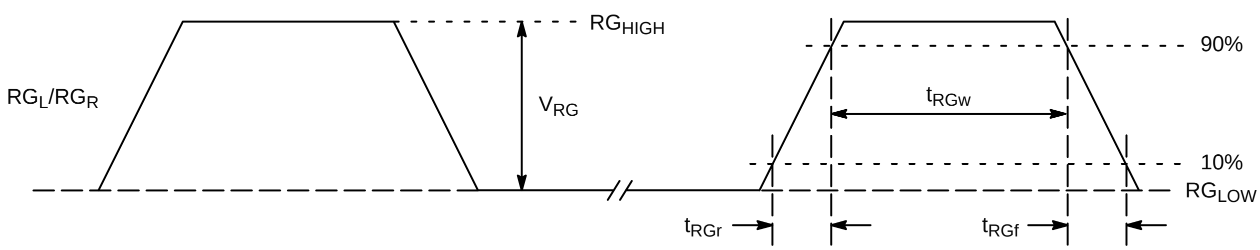


Figure 19. Pixel Timing

Pixel Timing Detail

Reset Clock



Horizontal Clocks

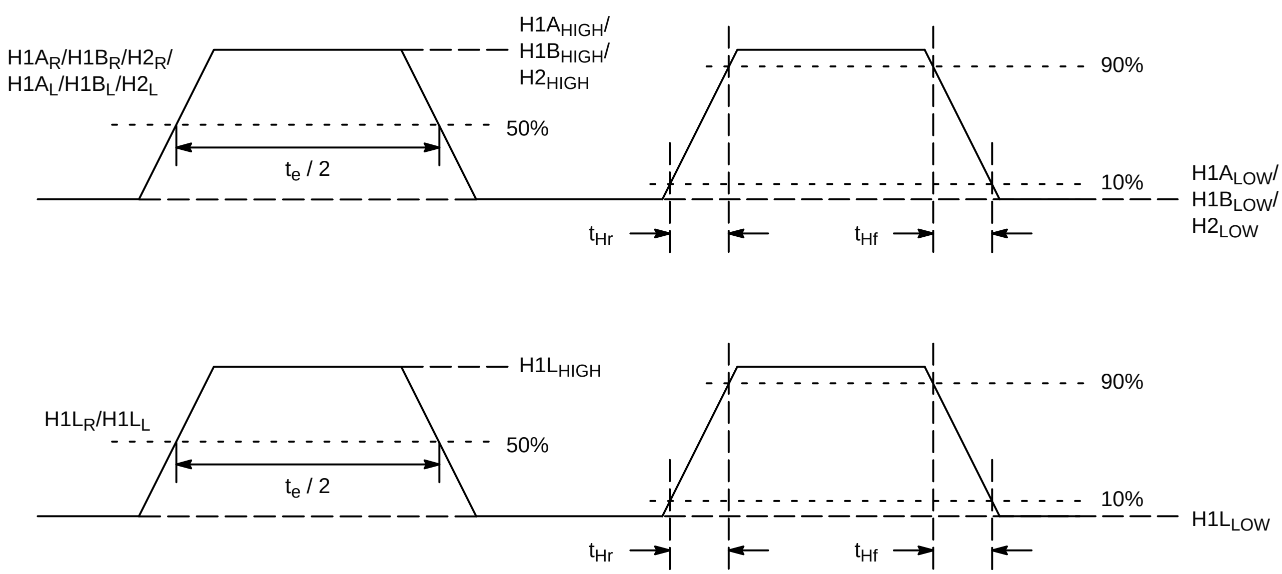


Figure 20. Pixel Timing Detail

MODE OF OPERATION

Power-Up Flush Cycle

Pulse Flush Gate Timing

The PFG clock resets all pixels in the array (except the FDG row). Charge transfer out of the pixel is fully completed only after V2 has been clocked low as shown.

Frame Timing − Pulse Flush Operation

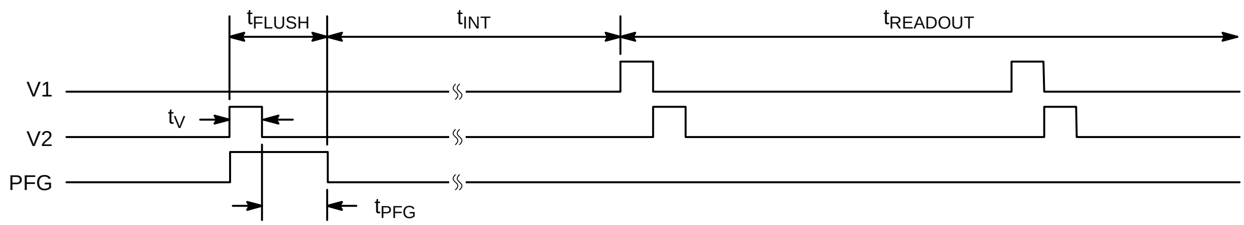


Figure 21. Pulse Flush Gate Timing

Fast Dump Gate (FDG) Timing

The FDG clock only resets pixels that happen to be in the FDG row. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus the characteristic time period (t_{FDG}). The position of the FDG row is illustrated in Figures 23–25, including the timing required for a simple 1 line dump operation. Pixels colored in yellow represent dumped pixels.

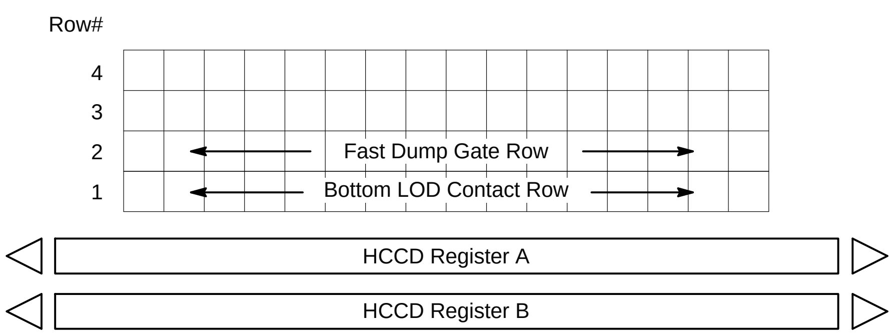


Figure 22. Fast Line Dump Layout

Line Timing − Fast Dump Gate

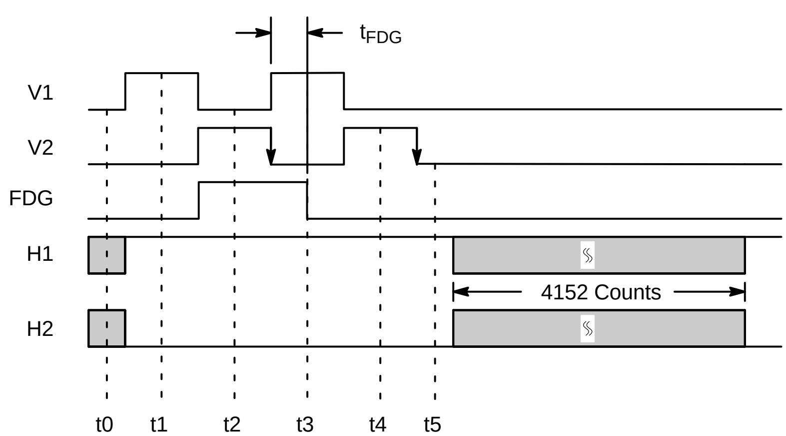


Figure 23. One Line Dump Timing Example

Line Timing − Fast Dump Gate (3 Line Dump)

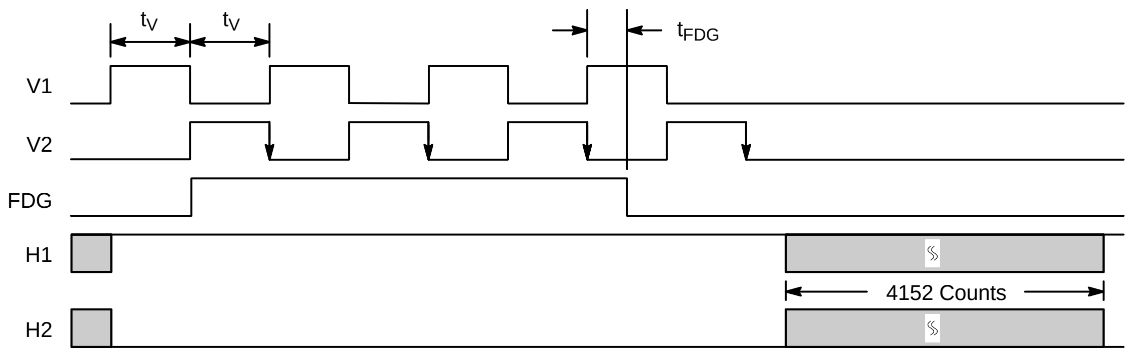
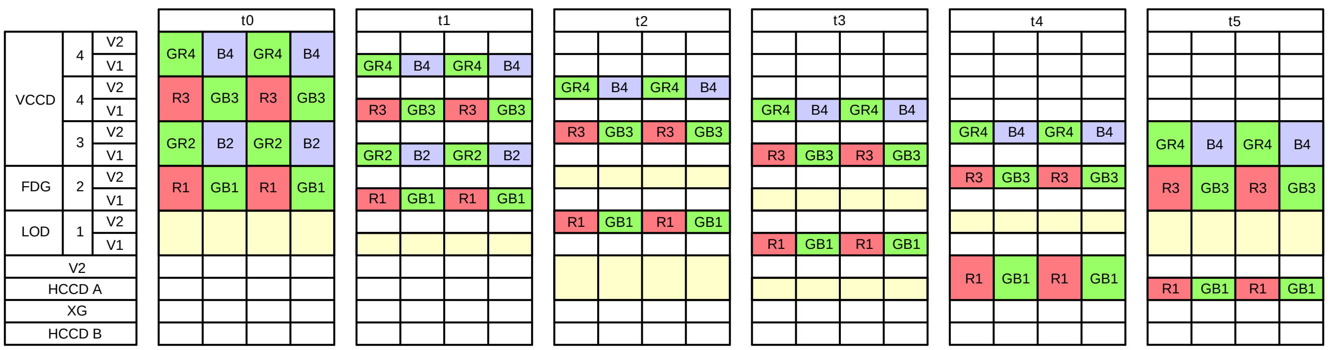


Figure 24. Line Dump Timing Example

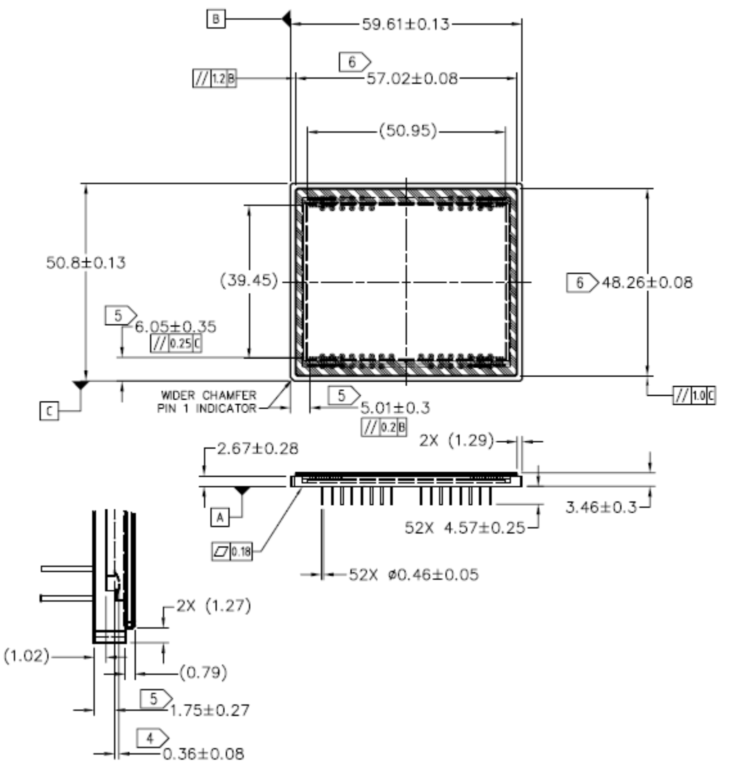


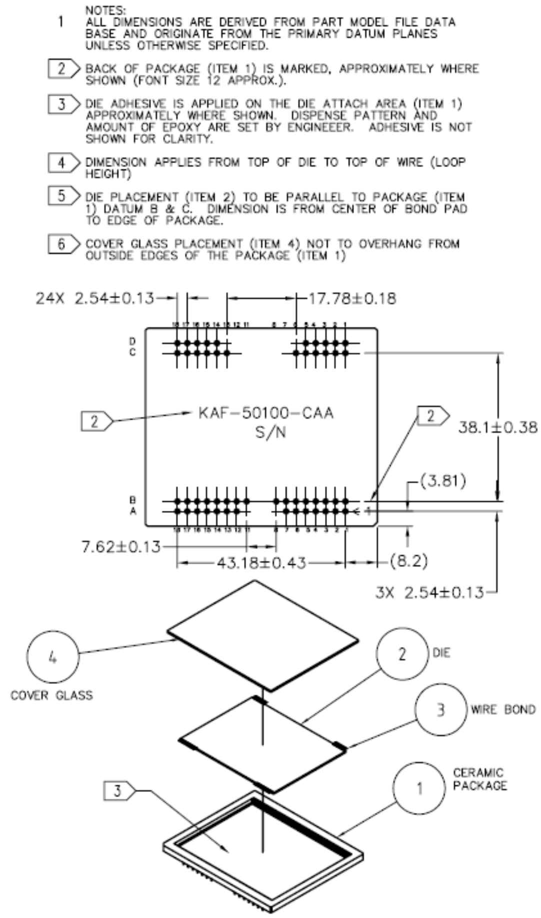
NOTE: Areas highlighted in yellow represent pixels drained of charge.

Figure 25. One Line Dump Pixel Illustration using Color Filter Designation

MECHANICAL DRAWINGS

Completed Assembly





Notes:

1. Device marking for the monochrome no-lens version is “KAF−50100−AAA”.
2. Device marking for the monochrome version with lens is “KAF−50100−ABA”.

Figure 26. Completed Assembly Drawing

Cover Glass Specification

1. Substrate material Schott D263T eco or equivalent.
2. 10 μm max. scratch/dig specification on the glass. No defect in the glass that exceeds 10 μm in any X−Y dimension.
3. Multilayer anti-reflective coating.

Table 11.

Wavelength	Total Reflectance
420−450	≤ 2%
450−630	≤ 1%
630−680	≤ 2%

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

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