

N-channel 650 V, 0.099 Ω typ., 22.5 A MDmesh™ V Power MOSFET in PowerFLAT™ 8x8 HV package

Datasheet - production data

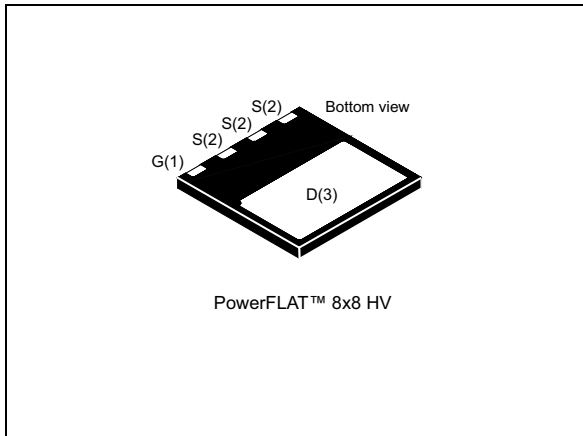
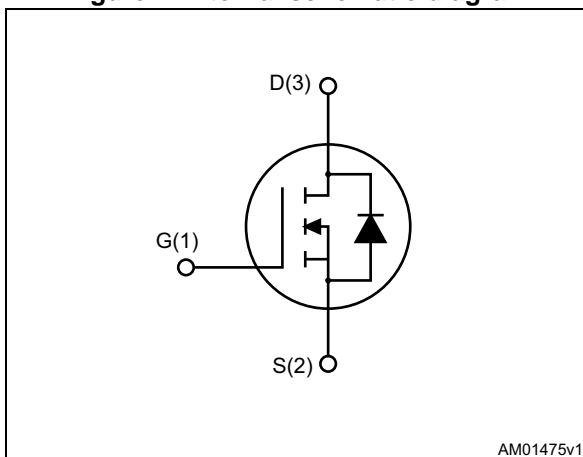


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D
STL34N65M5	710 V	0.120 Ω	22.5 A ⁽¹⁾

1. The value is rated according to $R_{thj-case}$ and limited by package.

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL34N65M5	34N65M5	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	15	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	90	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	3.2	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	510	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu.
4. $I_{SD} \leq 22.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$		0.099	0.120	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2700	-	pF
C_{oss}	Output capacitance		-	75	-	pF
C_{riss}	Reverse transfer capacitance		-	6.3	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0$ to $80\% V_{(BR)DSS}$	-	63	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	220	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.95	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 14\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	62.5	-	nC
Q_{gs}	Gate-source charge		-	17	-	nC
Q_{gd}	Gate-drain charge		-	28	-	nC

- $C_{o(er)}^{(1)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to $80\% V_{DSS}$
- $C_{o(tr)}^{(2)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to $80\% V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400 \text{ V}$, $I_D = 18 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 19)	-	59	-	ns
$t_{r(v)}$	Voltage rise time		-	8.7	-	ns
$t_{f(i)}$	Current fall time		-	7.5	-	ns
$t_{c(off)}$	Crossing time		-	12	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		90	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 22.5 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 22.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see Figure 16)	-	330		ns
Q_{rr}	Reverse recovery charge		-	5.3		μC
I_{RRM}	Reverse recovery current		-	32.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 22.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16)	-	412		ns
Q_{rr}	Reverse recovery charge		-	7.3		μC
I_{RRM}	Reverse recovery current		-	35.5		A

1. The value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

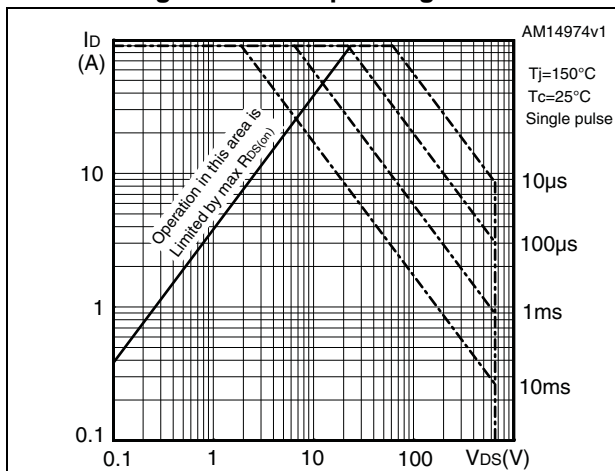


Figure 3. Thermal impedance

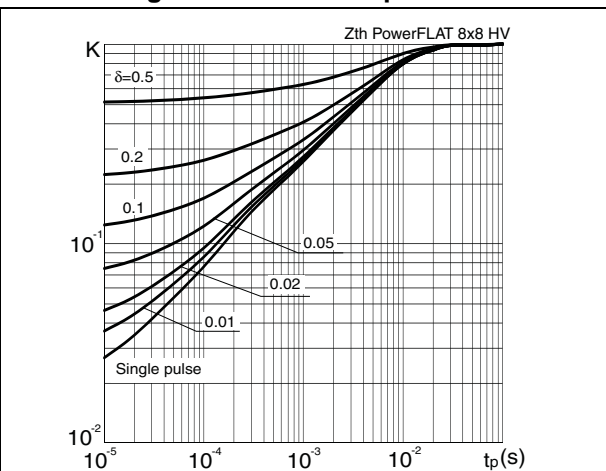


Figure 4. Output characteristics

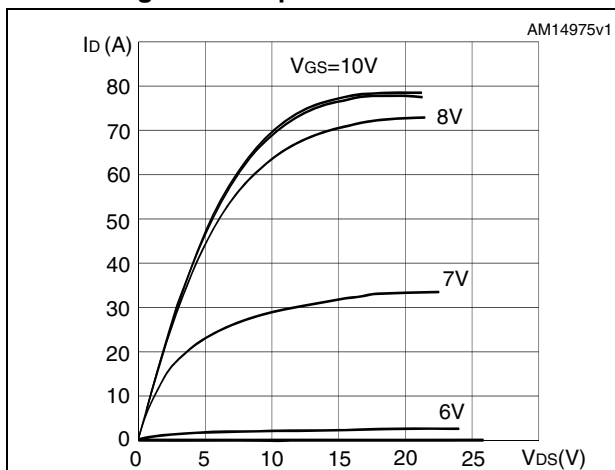


Figure 5. Transfer characteristics

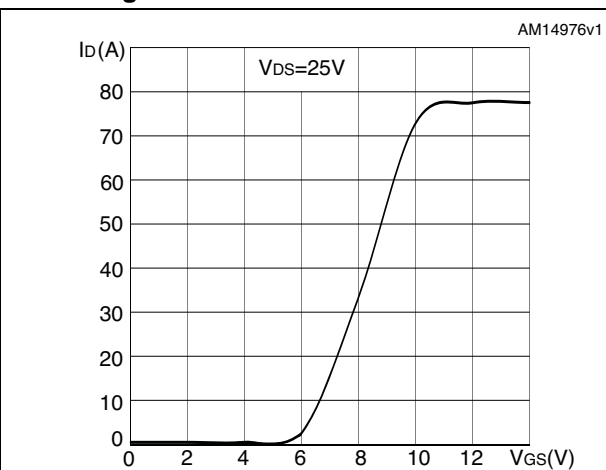


Figure 6. Gate charge vs gate-source voltage

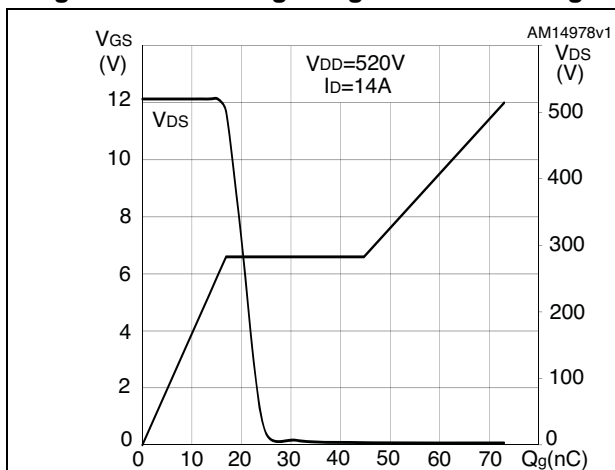


Figure 7. Static drain-source on-resistance

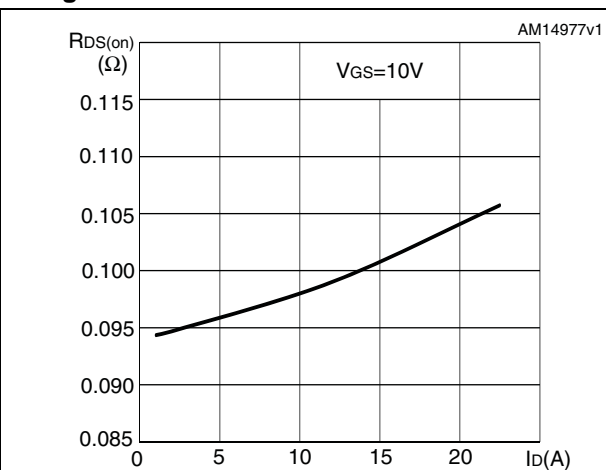


Figure 8. Capacitance variations

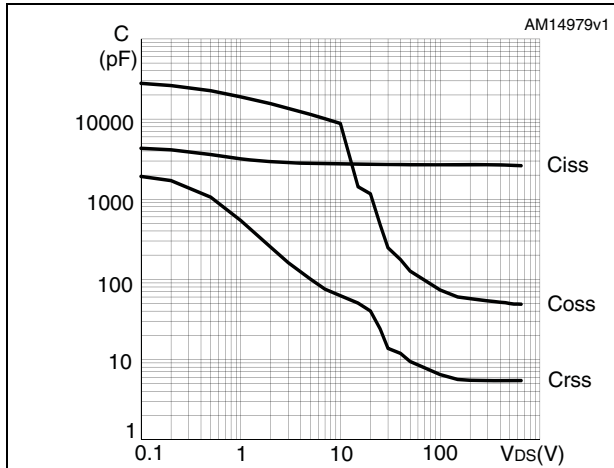


Figure 9. Output capacitance stored energy

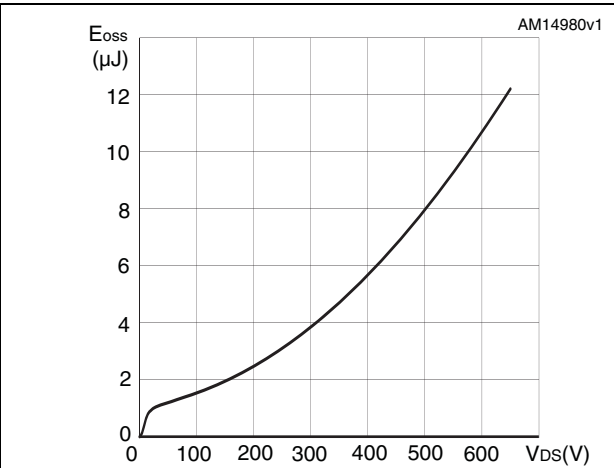


Figure 10. Normalized gate threshold voltage vs temperature

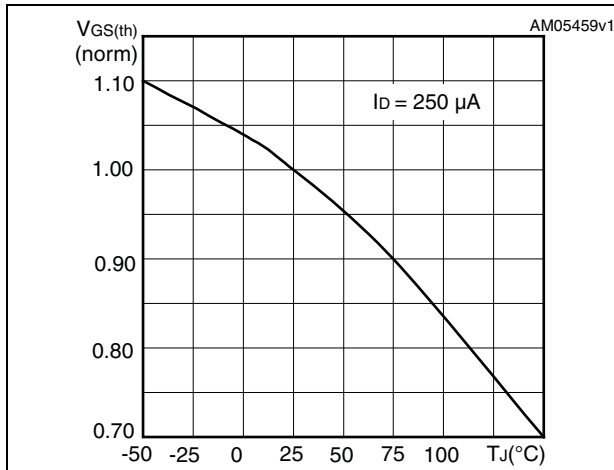


Figure 11. Normalized on-resistance vs temperature

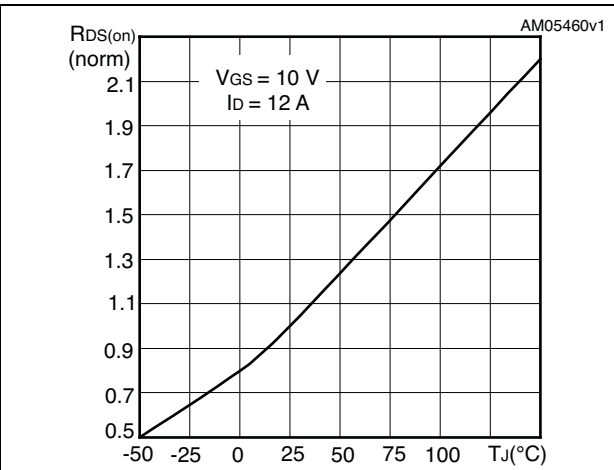


Figure 12. Switching losses vs gate resistance (1)

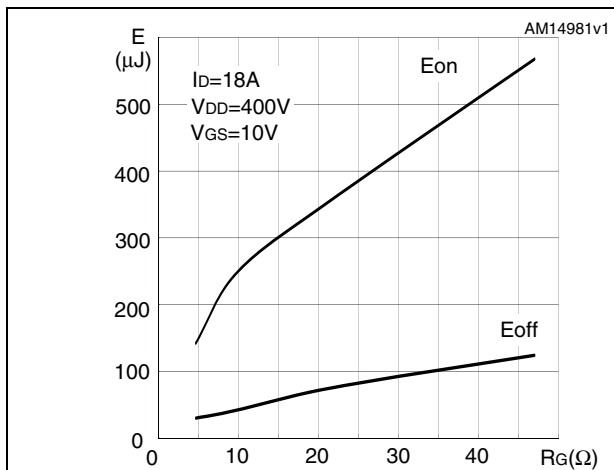
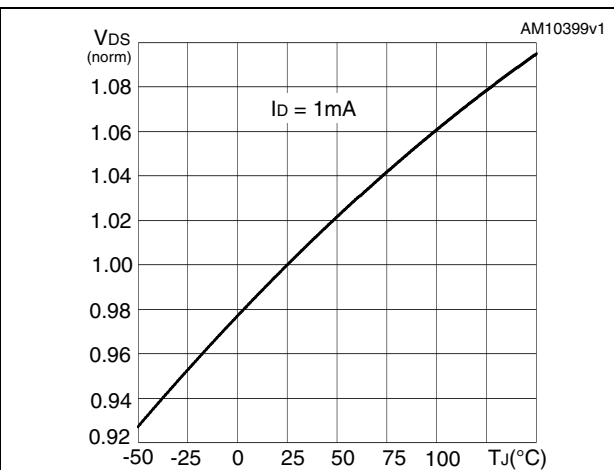


Figure 13. Normalized VDS vs temperature



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 14. Switching times test circuit for resistive load

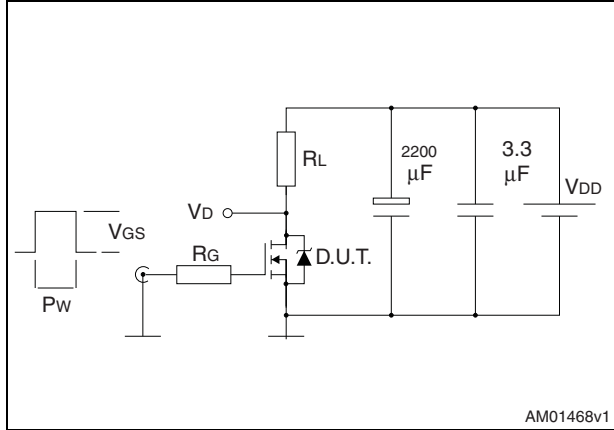


Figure 15. Gate charge test circuit

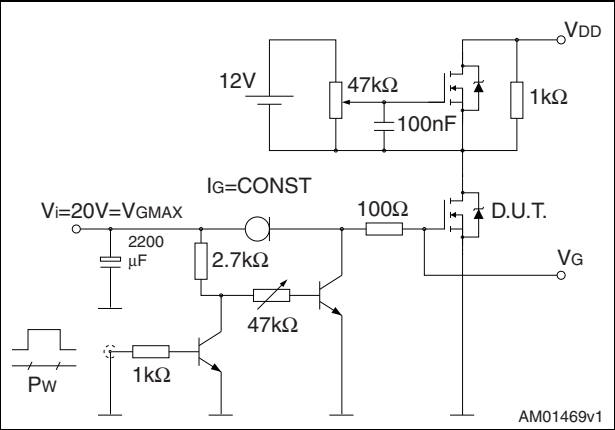


Figure 16. Test circuit for inductive load switching and diode recovery times

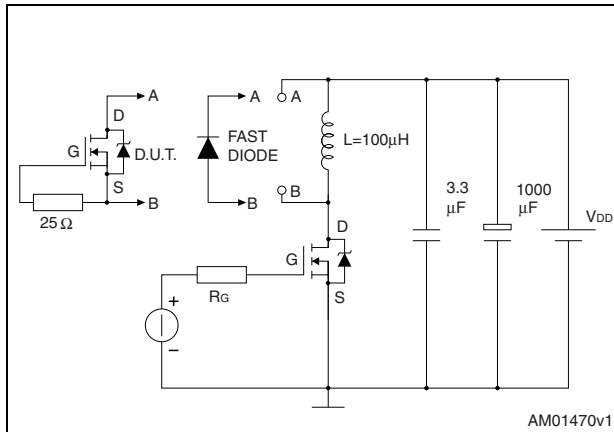


Figure 17. Unclamped inductive load test circuit

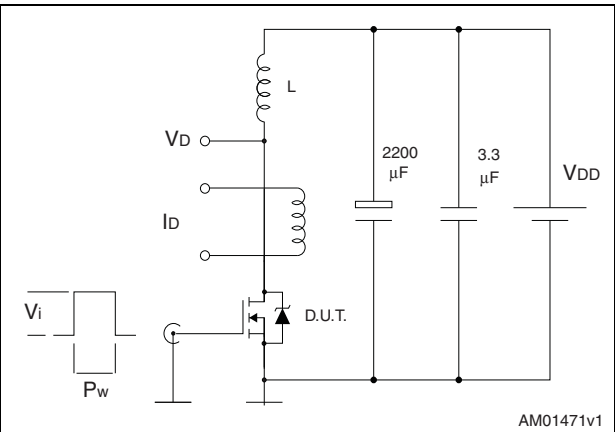


Figure 18. Unclamped inductive waveform

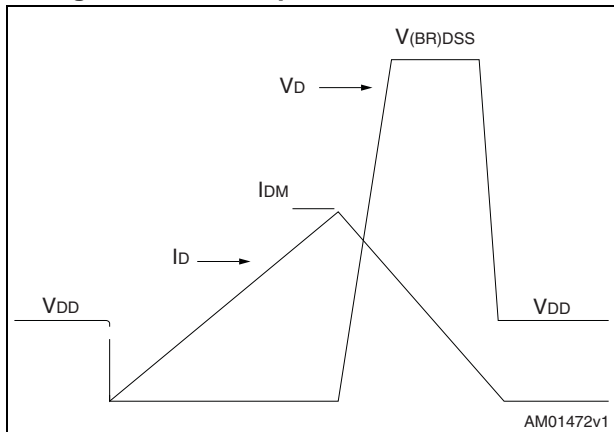
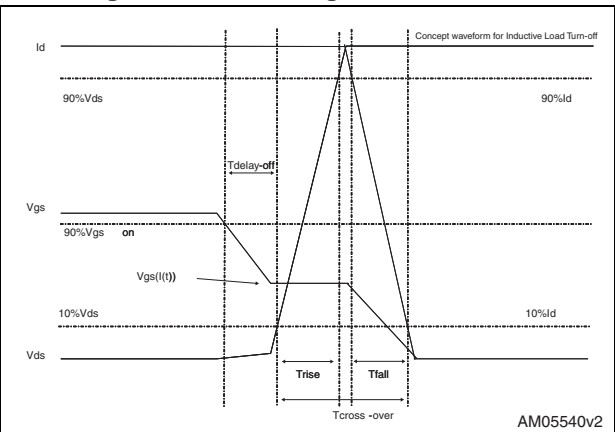


Figure 19. Switching time waveform



4 Package mechanical data

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Figure 20. PowerFLAT™ 8x8 HV drawing mechanical data

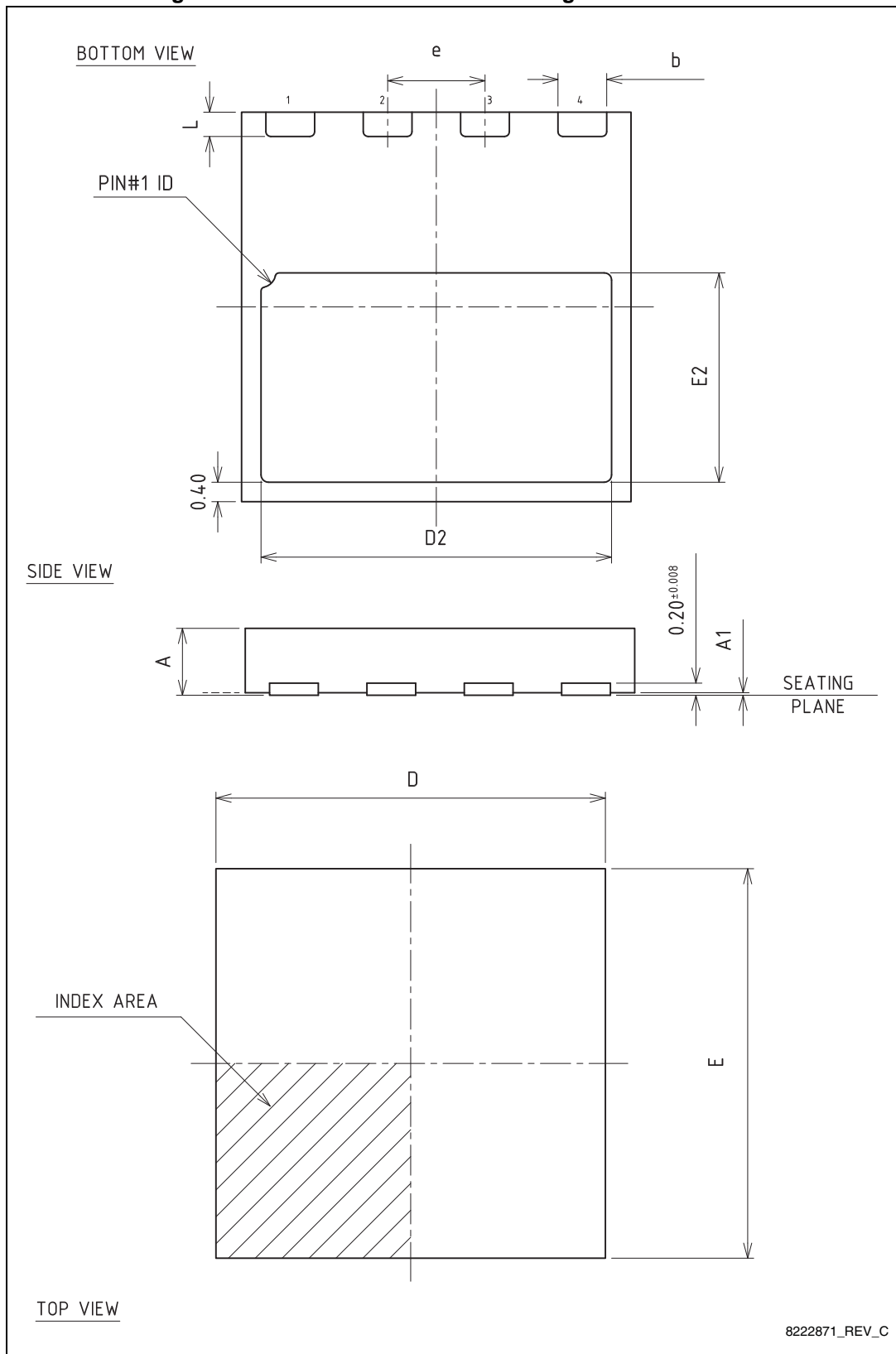
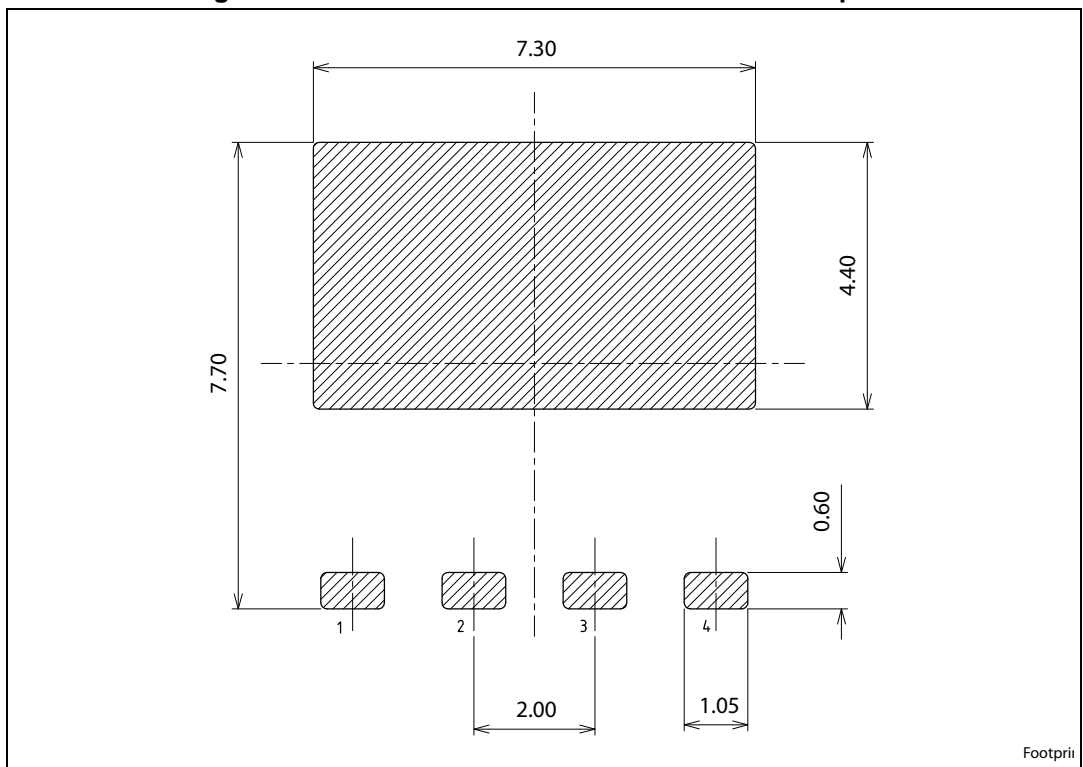


Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 21. PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

Figure 22. PowerFLAT™ 8x8 HV tape

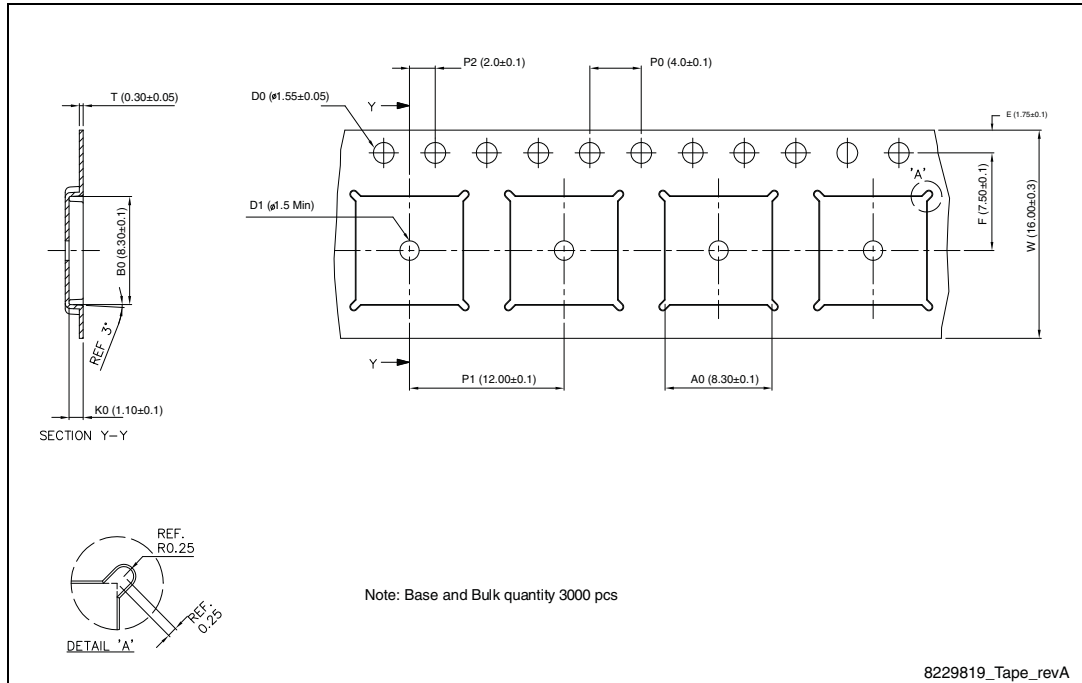


Figure 23. PowerFLAT™ 8x8 HV package orientation in carrier tape.

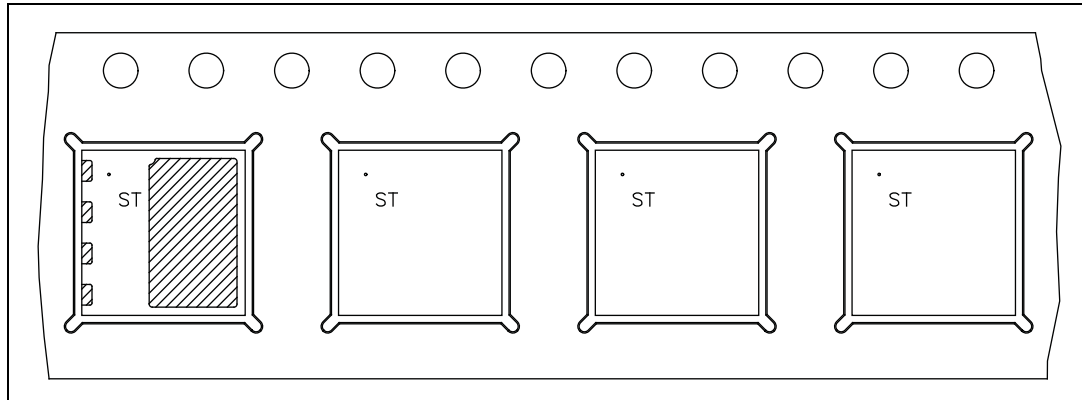
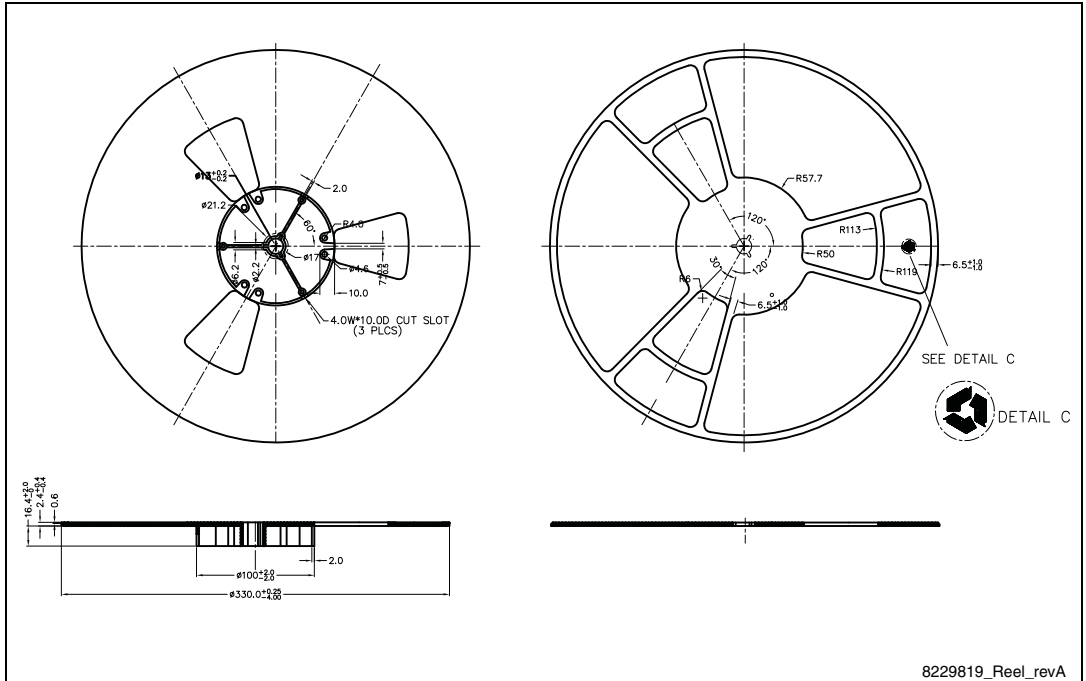


Figure 24. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Apr-2014	1	First release.

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