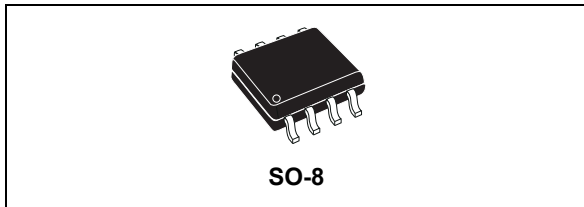


High voltage high- and low-side driver for automotive applications

Datasheet - production data



Features

- High voltage rail up to 550 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability
 - 400 mA source
 - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1 nF load
- CMOS/TTL Schmitt-trigger inputs with hysteresis and pull down
- Internal bootstrap diode

- Outputs in phase with inputs
- Interlocking function
- AECQ100 automotive qualified

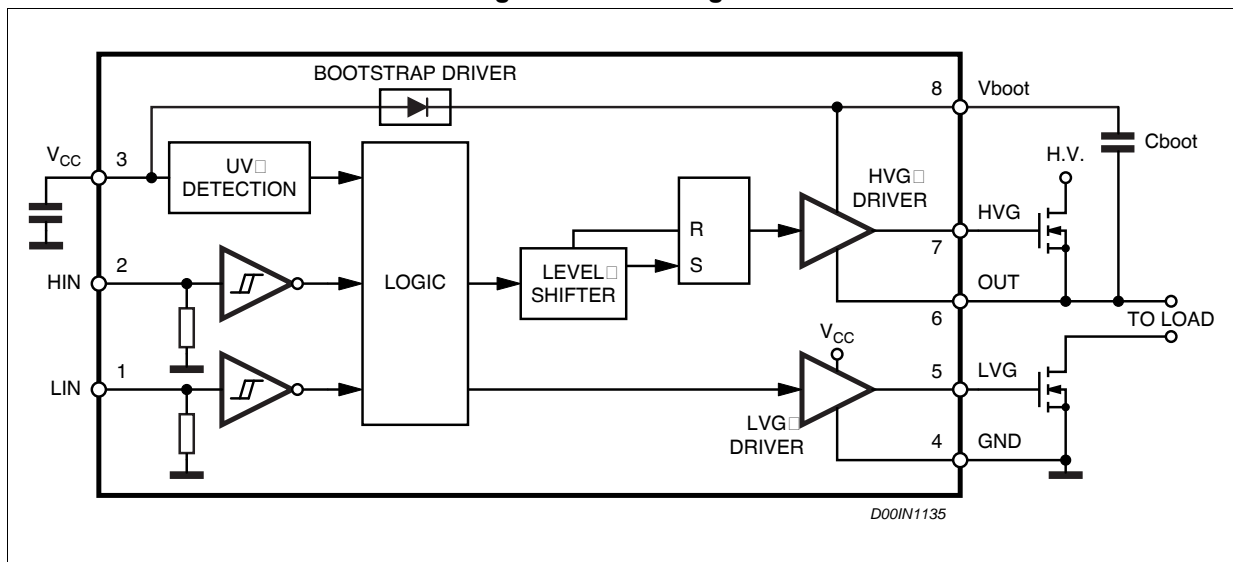
Applications

- Drive inverters for HEV and EV
- HID ballasts, power supply units
- Motion driver for home appliances, factory automation, industrial drives

Description

The A6387 is a high voltage device, manufactured with the BCD™ “offline” technology. It is a single chip half-bridge gate driver for N-channel Power MOSFETs or IGBTs. The high-side (floating) section is designed to stand a voltage rail of up to 550 V. The logic inputs are CMOS/TTL compatible for easy interfacing of the microcontroller or DSP.

Figure 1. Block diagram



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1 Electrical data

1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---------------|--|-----------------|------------------|------|
| V_{CC} | Supply voltage | - 0.3 | 18 | V |
| V_{out} | Output voltage | $V_{boot} - 18$ | $V_{boot} + 0.3$ | V |
| V_{boot} | Bootstrap voltage | - 0.3 | 568 | V |
| V_{hvg} | High-side gate output voltage | $V_{out} - 0.3$ | $V_{boot} + 0.3$ | V |
| V_{lvg} | Low-side gate output voltage | - 0.3 | $V_{CC} + 0.3$ | V |
| V_i | Logic input voltage | - 0.3 | $V_{CC} + 0.3$ | V |
| dV_{out}/dt | Allowed output slew rate | | 50 | V/ns |
| P_{tot} | Total power dissipation ($T_A = 85\text{ °C}$) | | 750 | mW |
| T_j | Junction temperature | | 150 | °C |
| T_{stg} | Storage temperature | -50 | 150 | °C |
| ESD | Human Body Model | 2 | | kV |

1.2 Thermal data

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|--------------|--|-------|------|
| $R_{th(JA)}$ | Thermal resistance junction to ambient | 150 | °C/W |

1.3 Recommended operating conditions

Table 3. Recommended operating conditions

| Symbol | Pin | Parameter | Test condition | Min. | Max. | Unit |
|----------------|-------|-------------------------|-----------------------------------|-------------------|------|------|
| V_{CC} | 3 | Supply voltage | | 6.3 | 17 | V |
| $V_{BO}^{(1)}$ | 8 - 6 | Floating supply voltage | | | 17 | V |
| V_{out} | 7 | Output voltage | | -6 ⁽²⁾ | 530 | V |
| f_{sw} | | Switching frequency | HVG, LVG load $C_L = 1\text{ nF}$ | | 400 | kHz |
| T_j | | Junction temperature | | -40 | 125 | °C |

1. $V_{BO} = V_{boot} - V_{out}$.

2. LVG off. $V_{CC} = 12\text{ V}$.

2 Pin connection

Figure 2. Pin connection (top view)

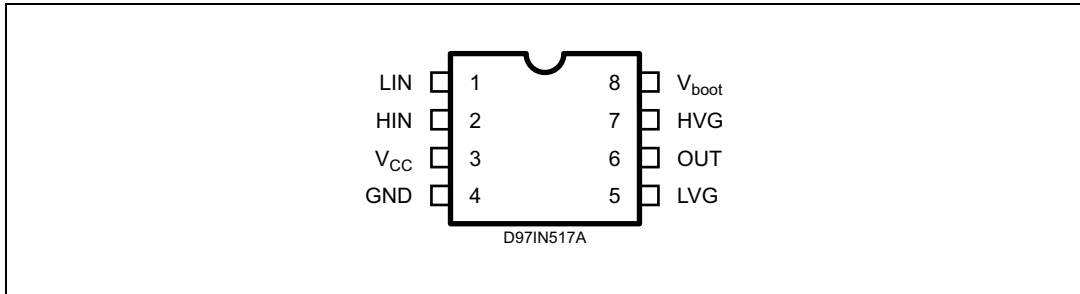


Table 4. Pin description

| No. | Pin | Type | Function |
|-----|--------------------|------|-------------------------------------|
| 1 | LIN | I | Low-side driver logic input |
| 2 | HIN | I | High-side driver logic input |
| 3 | V _{CC} | P | Low voltage power supply |
| 4 | GND | P | Ground |
| 5 | LVG ⁽¹⁾ | O | Low-side driver output |
| 6 | OUT | P | High-side driver floating reference |
| 7 | HVG ⁽¹⁾ | O | High-side driver output |
| 8 | V _{boot} | P | Bootstrap supply voltage |

1. The circuit provides less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA). This allows the omitting of the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

3 Electrical characteristics

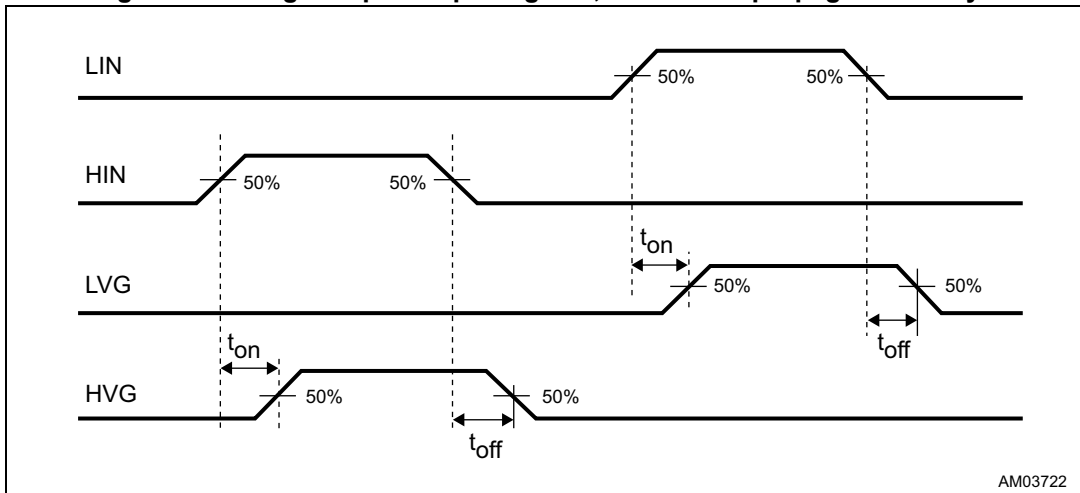
3.1 AC operation

$V_{CC} = 15\text{ V}$; $T_J = -40\text{ }^\circ\text{C} \div 125\text{ }^\circ\text{C}$, unless otherwise specified.

Table 5. AC operation electrical characteristics

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------|--------------------|---|--|------|------|------|------|
| t_{on} | 1 vs. 5 2 vs. 7 | High/low-side driver turn-on propagation delay | $V_{out} = 0\text{ V}$ $V_{boot} = V_{CC}$ $C_L = 1\text{ nF}$ | 40 | 120 | 240 | ns |
| t_{off} | 1 vs. 5 2 vs. 7 | High/low-side driver turn-off propagation delay | | 40 | 110 | 210 | ns |
| t_r | 5, 7 | Rise time | $C_L = 1\text{ nF}$ | | 50 | 100 | ns |
| t_f | 5, 7 | Fall time | | | 30 | 80 | ns |

Figure 3. Timing of input/output signals; turn-on/off propagation delays



3.2 DC operation

V_{CC} = 15 V; T_J = -40 °C ÷ 125 °C, unless otherwise specified

Table 6. DC operation electrical characteristics

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|------|---|---|------|------|------|------|
| Low supply voltage section | | | | | | | |
| V _{CC_thON} | 3 | V _{CC} UV turn-on threshold | | 5.5 | 6 | 6.3 | V |
| V _{CC_thOFF} | | V _{CC} UV turn-off threshold | | 5 | 5.5 | 6 | V |
| V _{CC_hys} | | V _{CC} UV hysteresis | | 0.3 | 0.5 | 0.7 | V |
| I _{qccu} | | Undervoltage quiescent supply current | V _{CC} ≤ 5 V | | 150 | 220 | μA |
| I _{qcc} | | Quiescent current | | | 250 | 320 | μA |
| R _{DSon} | | Bootstrap driver on resistance ⁽¹⁾ | LVG ON | | 125 | | Ω |
| Bootstrapped supply voltage section ⁽²⁾ | | | | | | | |
| I _{QBO} | 8 | V _{BO} quiescent current | HVG ON | | | 100 | μA |
| I _{LK} | | High voltage leakage current | V _{hvg} = V _{out} = V _{boot} = 550 V | | | 10 | μA |
| High/low-side driver | | | | | | | |
| I _{so} | 5, 7 | High/low-side source short-circuit current | V _{IN} = V _{ih} (t _p < 10 μs) | 300 | 400 | | mA |
| I _{si} | | High/low-side sink short-circuit current | V _{IN} = V _{il} (t _p < 10 μs) | 450 | 650 | | mA |
| Logic inputs | | | | | | | |
| V _{il} | 1,2 | Low level logic threshold voltage | | | | 1.4 | V |
| V _{ih} | | High level logic threshold voltage | | 3.2 | | | V |
| I _{ih} | | High level logic input current | V _{IN} = 15 V | 8 | 20 | 40 | μA |
| I _{il} | | Low level logic input current | V _{IN} = 0 V | | | 1 | μA |

1. R_{DS(on)} is tested in the following way:

$$R_{DS(on)} = \frac{(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})}{I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})}$$

where I₁ is pin 8 current when V_{BOOT} = V_{BOOT1}, I₂ when V_{BOOT} = V_{BOOT2}.

2. V_{BO} = V_{boot} - V_{out}.

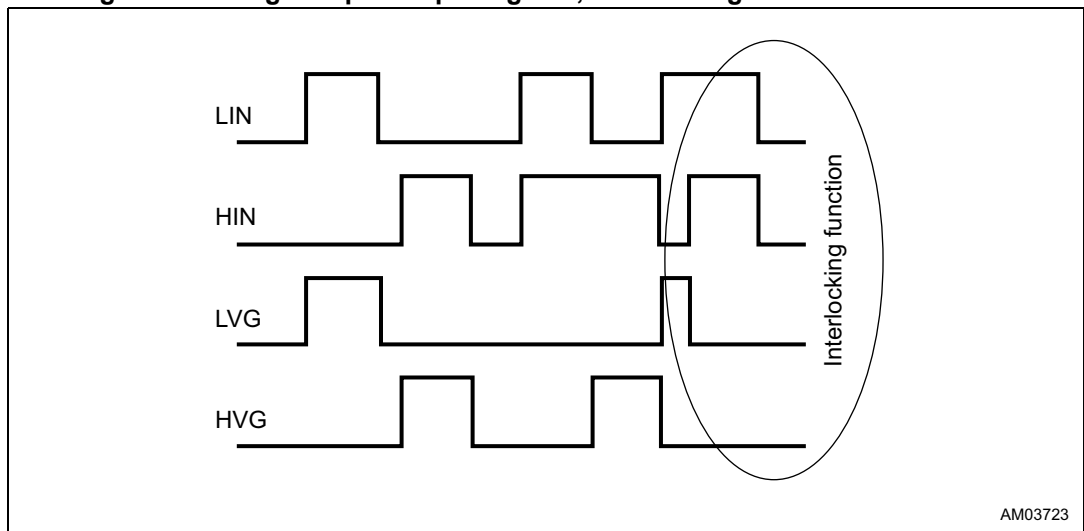
4 Input logic

The A6387 input logic is V_{CC} (17 V) compatible. An interlocking feature is offered (see [Table 7](#)) to avoid undesired simultaneous turn-on of both power switches driven.

Table 7. Input logic

| Input | | Output | |
|-------|-----|--------|-----|
| HIN | LIN | HVG | LVG |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Figure 4. Timing of input/output signals; interlocking waveforms definition



5 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 5 a*). In the A6387 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 5 b*. An internal charge pump (*Figure 5 b*) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be:

$$C_{BOOT} \gg C_{EXT}$$

For example: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With $C_{BOOT} = 100$ nF the drop would be 300 mV.

If HVG must be supplied for a long period, the C_{BOOT} selection must take into account also the leakage and quiescent losses.

For example: HVG steady-state consumption is lower than 100 μ A, therefore, if HVG T_{ON} is 5 ms, C_{BOOT} must supply 0.5 μ C to C_{EXT} . This charge on a 1 μ F capacitor means a voltage drop of 0.5 V.

The internal bootstrap driver offers a big advantage: the external fast recovery diode can be avoided (it usually has very high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, in the meantime, the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 125 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

Equation 2 is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{DSon} is the ON-resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

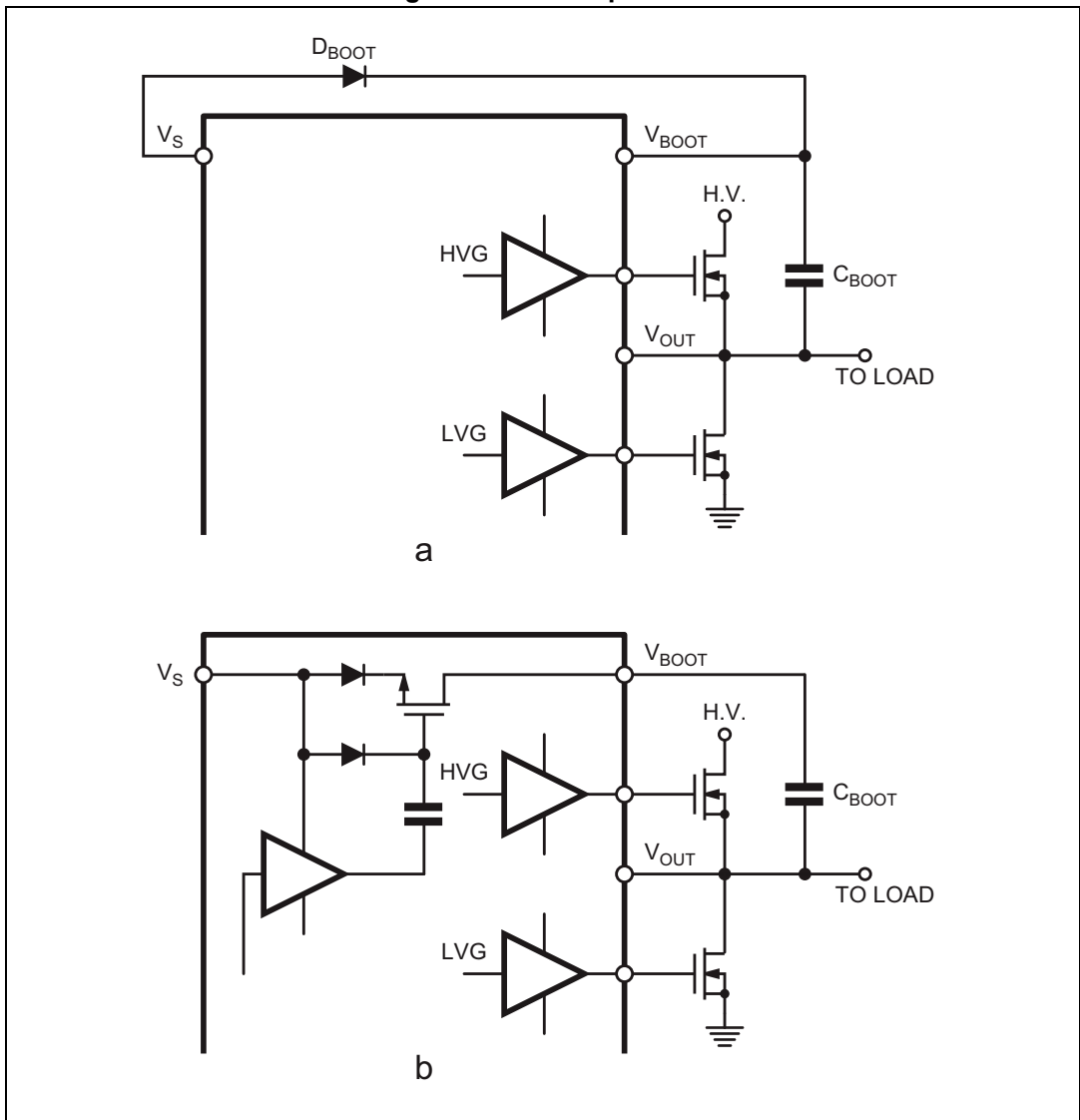
For example: using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μs . In fact:

Equation 3

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 125\Omega \sim 0.8\text{V}$$

V_{drop} should be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 5. Bootstrap driver



6 Typical characteristic

Figure 6. Typical rise and fall times vs. load capacitance

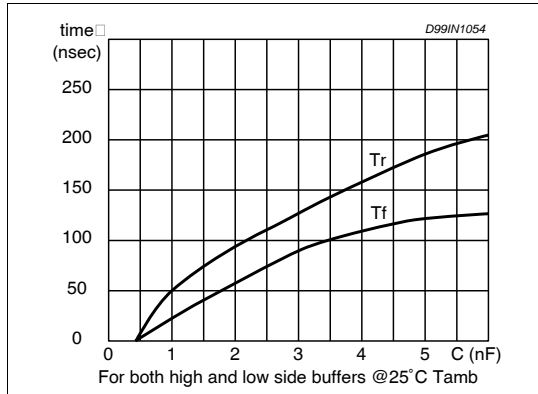


Figure 7. Quiescent current vs. supply voltage

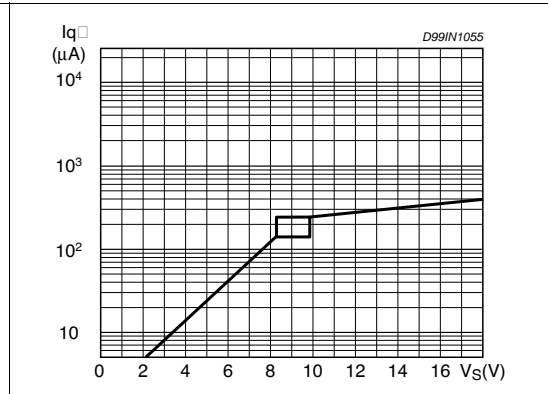


Figure 8. Turn-on time vs. temperature

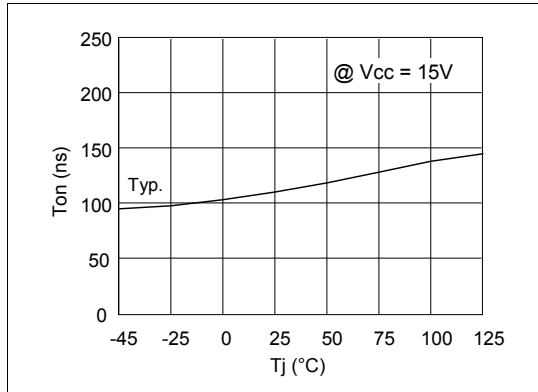


Figure 9. Turn-off time vs. temperature

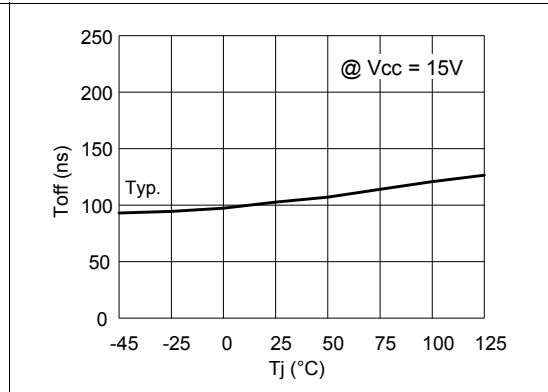


Figure 10. Output source current vs. temperature

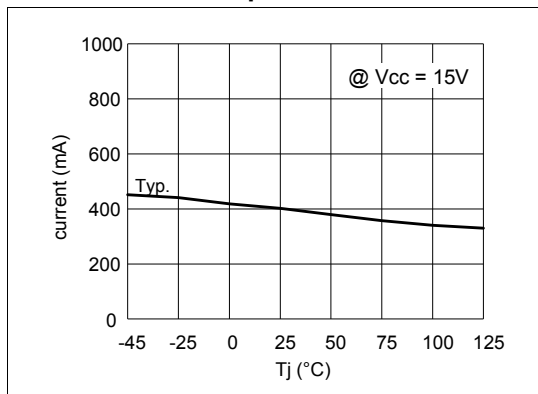
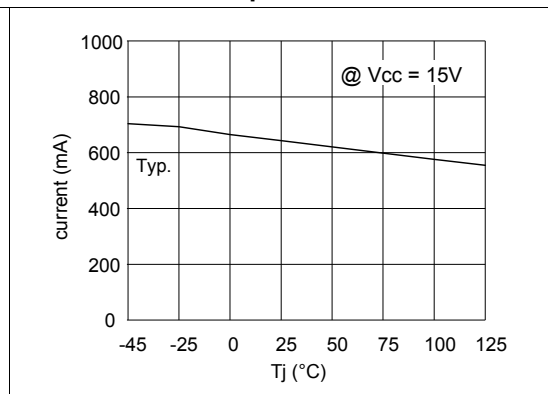


Figure 11. Output sink current vs. temperature



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 12. SO-8 package outline

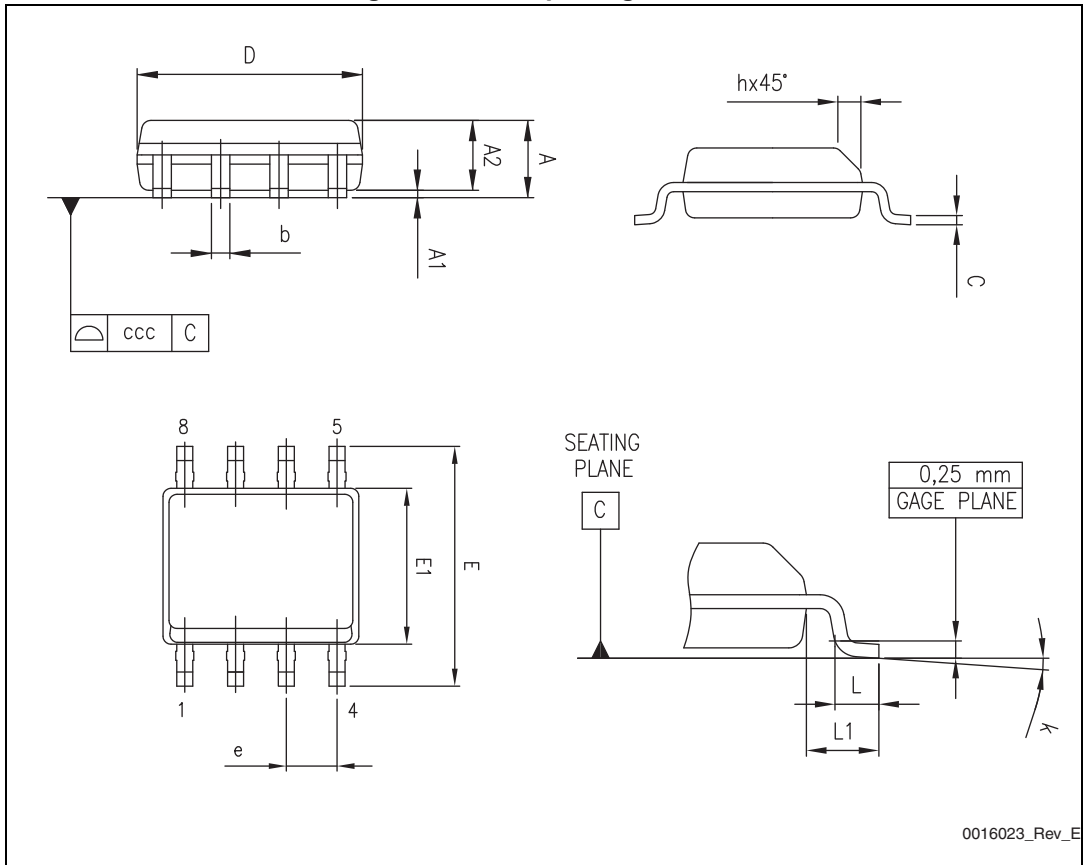


Table 8. SO-8 package mechanical data

| Symbol | Dimensions (mm) | | |
|--------|-----------------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.28 | | 0.48 |
| c | 0.17 | | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

8 Ordering information

Table 9. Ordering information

| Order code | Package | Packaging |
|------------|---------|---------------|
| A6387D | SO-8 | Tube |
| A6387DTR | SO-8 | Tape and reel |

9 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 05-Jul-2012 | 1 | First release |
| 10-Oct-2013 | 2 | Updated: Section : Features on page 1 (added "AECQ100 compliant"). Section : Applications on page 1 added: – Drive inverters for HEV and EV, – HID ballasts, power supply units, – Motion driver for home appliances, factory automation, industrial drives. Table 1 on page 3 (removed note below Table 1). Minor corrections throughout document. |
| 22-Oct-2013 | 3 | Updated Section : Features on page 1 ("replaced AECQ100 compliant" by "AECQ100 automotive qualified"). |
| 14-Apr-2014 | 4 | Updated Section 3.1: AC operation on page 5 (added Figure 3). Updated Section 4: Input logic on page 7 (added Figure 4). |
| 04-Feb-2015 | 5 | Updated Table 1 (added <i>Human Body Model</i> parameter). Updated minimum supply voltage in Table 3 and maximum V_{CC} UV turn-on threshold voltage in Table 6 . Corrected typo in $R_{DS(on)}$ testing equation in footnote of Table 6 . Updated Figure 5: Bootstrap driver . |

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