

NTD6415ANL, NVD6415ANL

N-Channel Power MOSFET 100 V, 23 A, 56 mΩ, Logic Level

Features

- Low $R_{DS(on)}$
- 100% Avalanche Tested
- AEC-Q101 Qualified
- AEC Q101 Qualified – NVD6415ANL
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	100	V
Gate-to-Source Voltage – Continuous			V _{GS}	± 20	V
Continuous Drain Current	Steady State	T _C = 25°C	I _D	23	A
		T _C = 100°C		16	
Power Dissipation	Steady State	T _C = 25°C	P _D	83	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	80	A
Operating and Storage Temperature Range			T _J , T _{stg}	–55 to +175	°C
Source Current (Body Diode)			I _S	23	A
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 50 Vdc, V _{GS} = 10 Vdc, I _{L(pk)} = 23 A, L = 0.3 mH, R _G = 25 Ω)			E _{AS}	79	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			T _L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) – Steady State	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	39	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

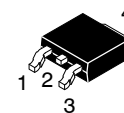
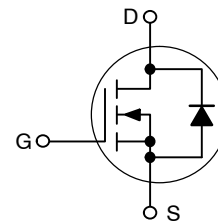
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



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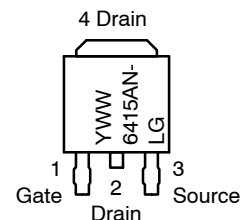
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	56 mΩ @ 4.5 V	23 A
	52 mΩ @ 10 V	



DPAK
CASE 369AA
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



6415ANL = Device Code
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}, T_J = -40^\circ\text{C}$	100 92			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			115		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$		1.0 100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.8		mV/ $^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		44	56	m Ω
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		43	52	
Forward Transconductance	g_{FS}	$V_{DS} = 5.0\text{ V}, I_D = 10\text{ A}$		24		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1024		pF
Output Capacitance	C_{OSS}			156		
Reverse Transfer Capacitance	C_{RSS}			70		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 80\text{ V}, I_D = 23\text{ A}$		20		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	Q_{GS}			3.1		
Gate-to-Drain Charge	Q_{GD}			14		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 80\text{ V}, I_D = 23\text{ A}$		35		nC

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 80\text{ V},$ $I_D = 23\text{ A}, R_G = 6.1\text{ }\Omega$		11		ns
Rise Time	t_r			91		
Turn-Off Delay Time	$t_{d(off)}$			40		
Fall Time	t_f			71		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 23\text{ A}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	0.87 0.74	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 23\text{ A}$		64		ns
Charge Time	T_a			40		
Discharge Time	T_b			24		
Reverse Recovery Charge	Q_{RR}			152		nC

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTD6415ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD6415ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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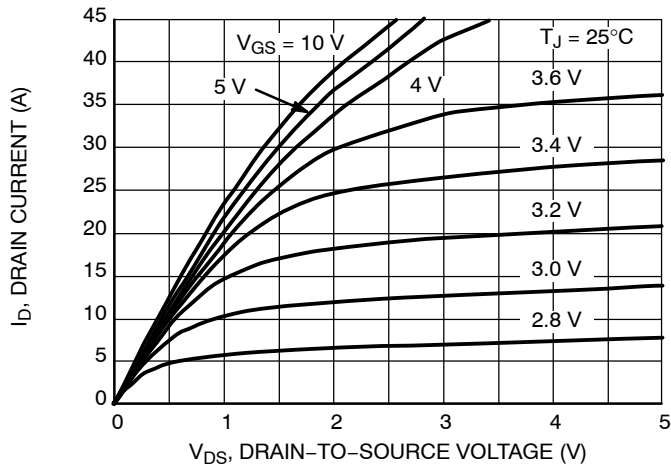


Figure 1. On-Region Characteristics

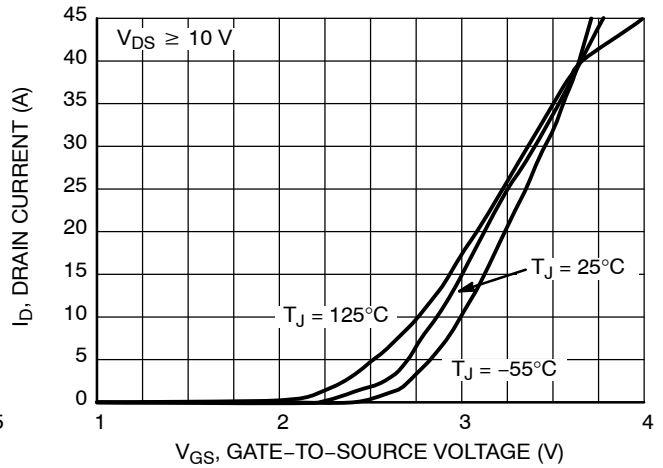


Figure 2. Transfer Characteristics

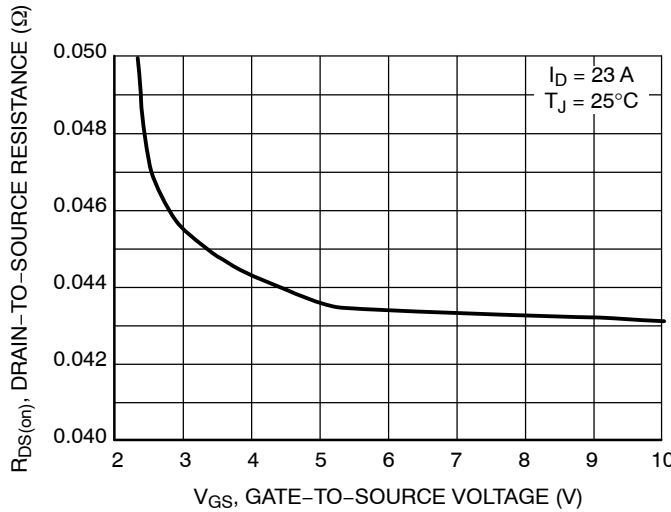


Figure 3. On-Region versus Gate Voltage

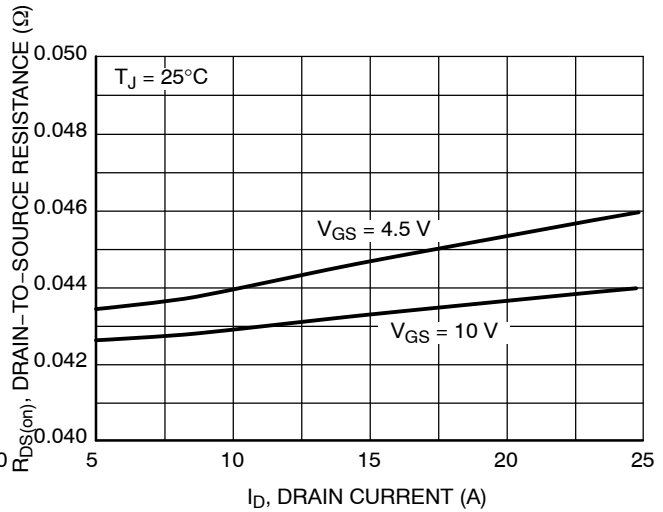


Figure 4. On-Resistance versus Drain Current and Gate Voltage

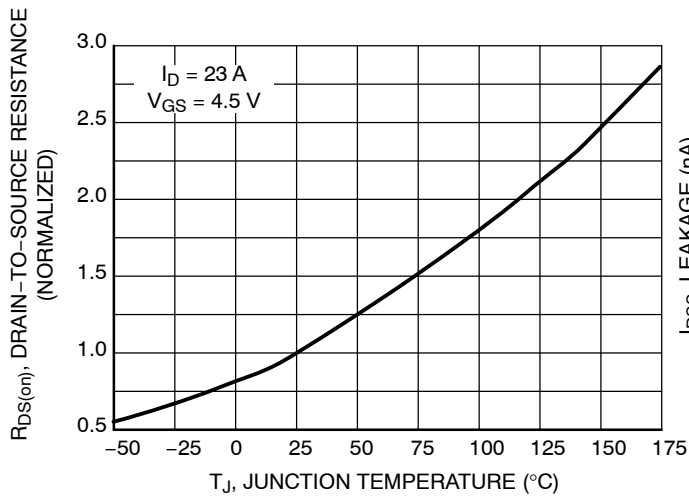


Figure 5. On-Resistance Variation with Temperature

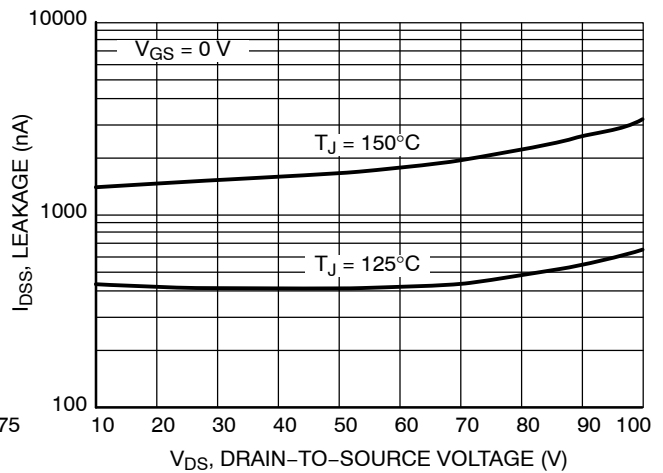


Figure 6. Drain-to-Source Leakage Current versus Voltage

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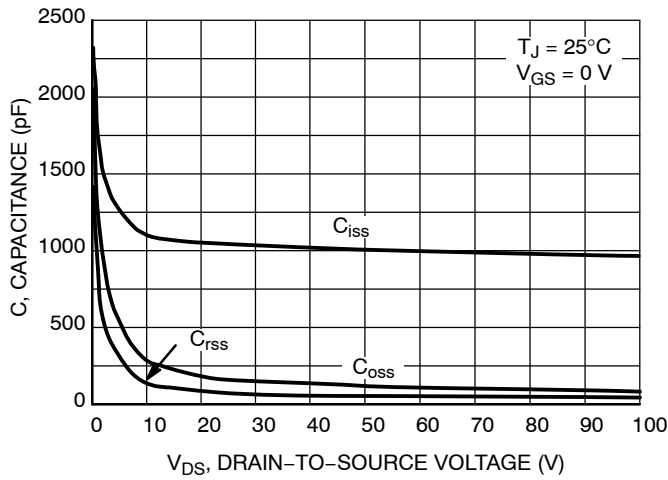


Figure 7. Capacitance Variation

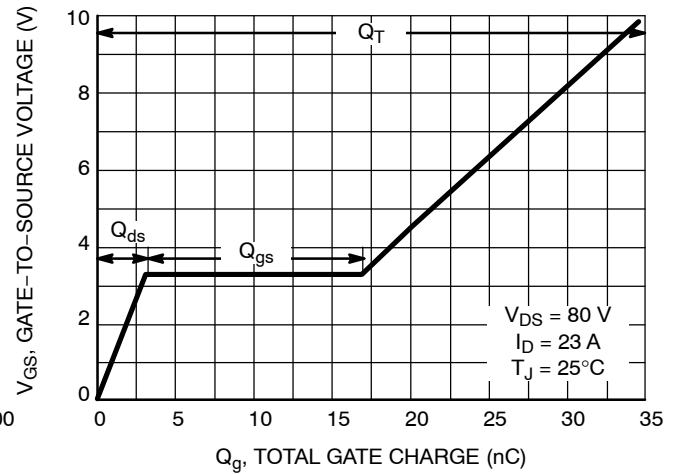


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

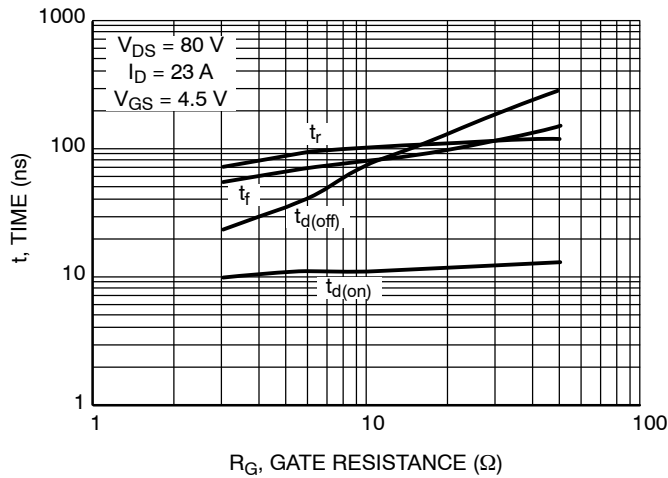


Figure 9. Resistive Switching Time Variation versus Gate Resistance

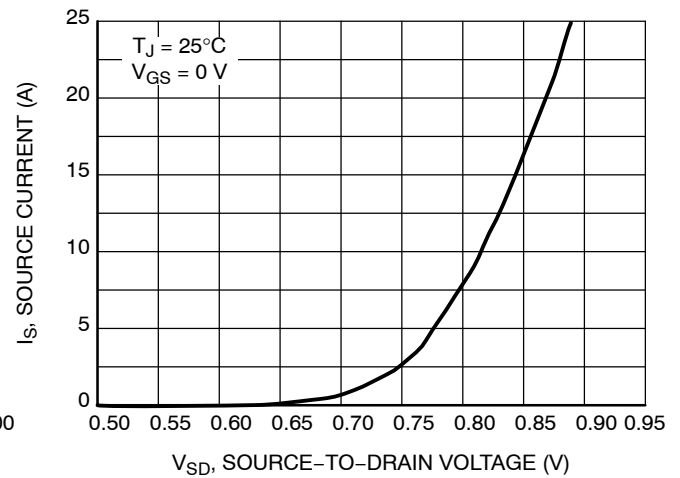


Figure 10. Diode Forward Voltage versus Current

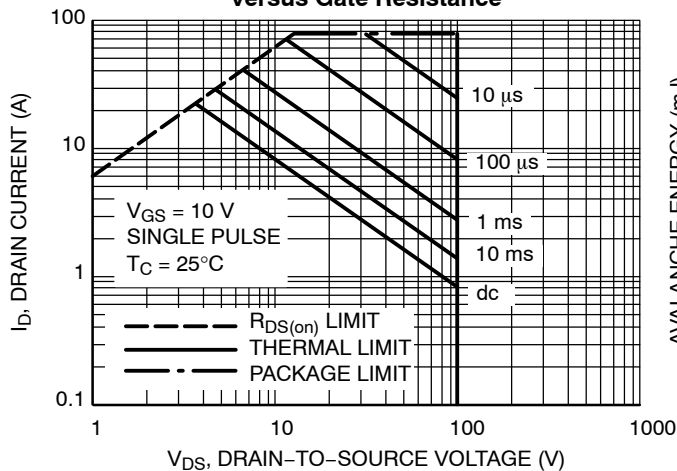


Figure 11. Maximum Rated Forward Biased Safe Operating Area

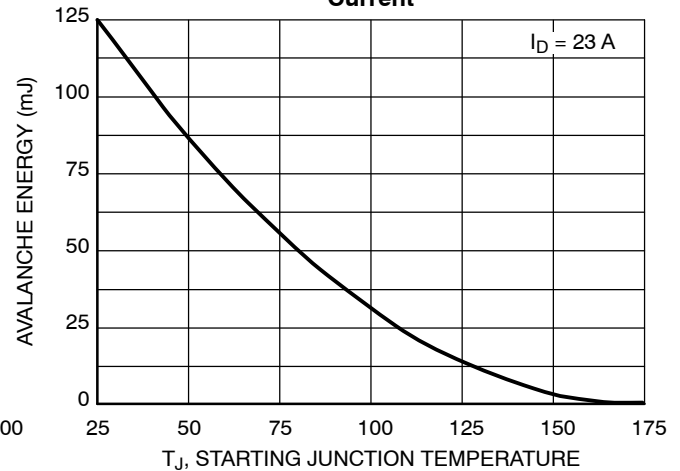


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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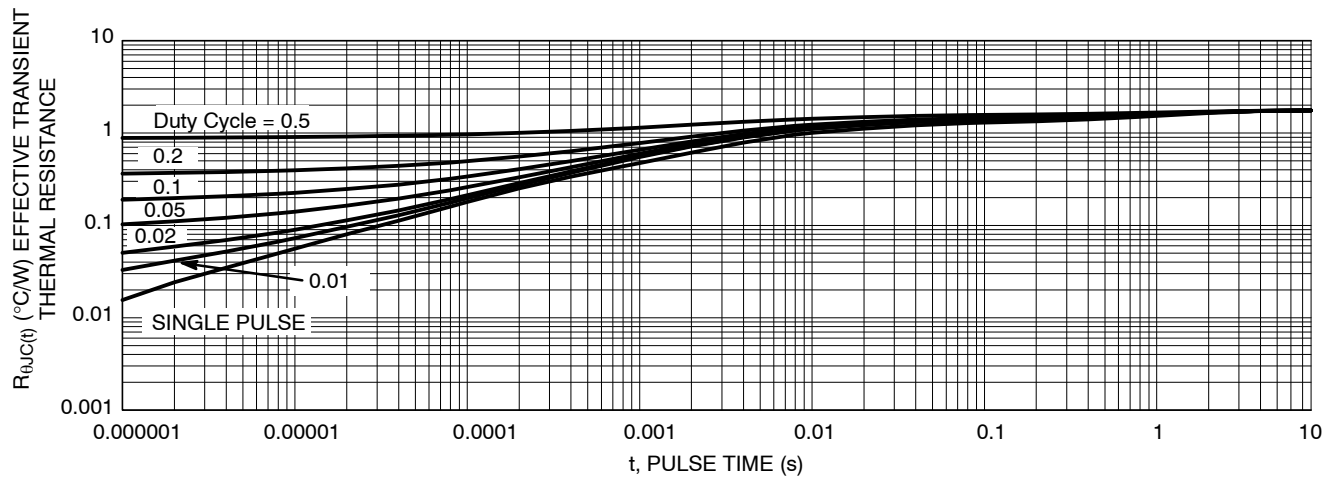


Figure 13. Thermal Response

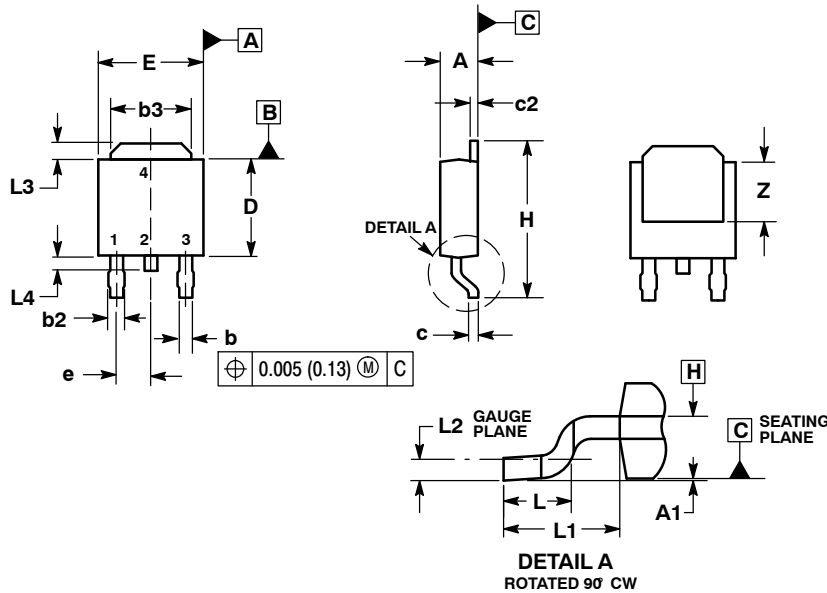
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PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE)

CASE 369AA-01

ISSUE B

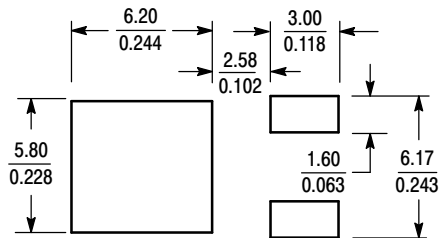


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NTD6415ANL/D



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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.