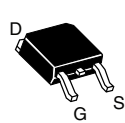




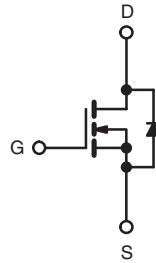
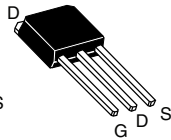
## Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	600
R <sub>DS(on)</sub> (Max.) (Ω)	V <sub>GS</sub> = 10 V   7.0
Q <sub>g</sub> (Max.) (nC)	14
Q <sub>gs</sub> (nC)	2.7
Q <sub>gd</sub> (nC)	8.1
Configuration	Single

PAK (TO-252)



IPAK (TO-251)



N-Channel MOSFET

### FEATURES

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT  
HALOGEN  
FREE  
Available

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- Power Factor Correction

### TYPICAL SMPS TOPOLOGIES

- Low Power Single Transistor Flyback

ORDERING INFORMATION					
Package	PAK (TO-252)	PAK (TO-252)	PAK (TO-252)	PAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR1N60A-GE3	SiHFR1N60ATRL-GE3 <sup>a</sup>	SiHFR1N60ATR-GE3 <sup>a</sup>	SiHFR1N60ATRR-GE3 <sup>a</sup>	SiHFU1N60A-GE3
Lead (Pb)-free	IRFR1N60APbF	IRFR1N60ATRLPbF <sup>a</sup>	IRFR1N60ATRPbF <sup>a</sup>	IRFR1N60ATRRPbF <sup>a</sup>	IRFU1N60APbF
	SiHFR1N60A-E3	SiHFR1N60ATL-E3 <sup>a</sup>	SiHFR1N60AT-E3 <sup>a</sup>	SiHFR1N60ATR-E3 <sup>a</sup>	SiHFU1N60A-E3

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>		600	V	
Gate-Source Voltage	V <sub>GS</sub>		± 30		
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	1.4	A	
		T <sub>C</sub> = 100 °C	0.89		
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>		5.6		
Linear Derating Factor			0.28	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>		93	mJ	
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>		1.4	A	
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>		3.6	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	36	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	3.8	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300		

#### Notes


- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Starting T<sub>J</sub> = 25 °C, L = 95 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 1.4 A (see fig. 12).  
 c. I<sub>SD</sub> ≤ 1.4 A, di/dt ≤ 180 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.  
 d. 1.6 mm from case.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.5	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 0.84\text{ A}^b$	-	-	7.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 0.84\text{ A}$	0.88	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5	-	229	-	pF
Output Capacitance	$C_{oss}$		-	32.6	-	
Reverse Transfer Capacitance	$C_{rss}$		-	2.4	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$ , $f = 1.0\text{ MHz}$	-	320	-
			$V_{DS} = 480\text{ V}$ , $f = 1.0\text{ MHz}$	-	11.5	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to }480\text{ V}^c$	-	130	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 1.4\text{ A}$ , $V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	14	nC
Gate-Source Charge	$Q_{gs}$		-	-	2.7	
Gate-Drain Charge	$Q_{gd}$		-	-	8.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$ , $I_D = 1.4\text{ A}$ , $R_g = 2.15\text{ }\Omega$ , $R_D = 178\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	9.8	-	ns
Rise Time	$t_r$		-	14	-	
Turn-Off Delay Time	$t_{d(off)}$		-	18	-	
Fall Time	$t_f$		-	20	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.4	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	5.6	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 1.4\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 1.4\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	290	440	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	510	760	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DS}$ .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

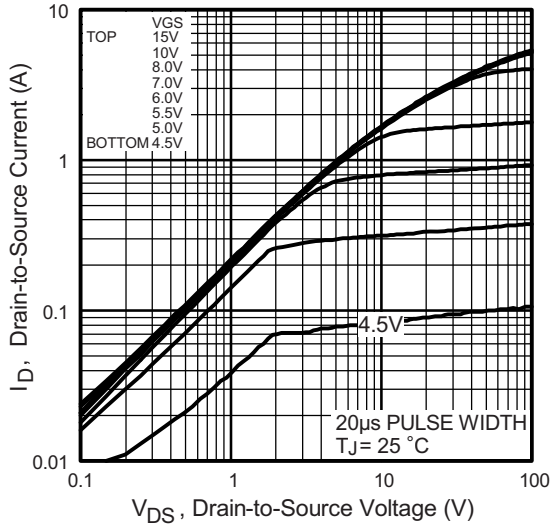


Fig. 1 - Typical Output Characteristics

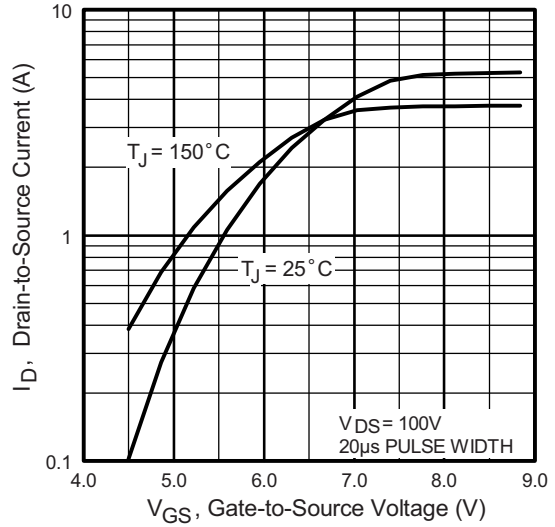


Fig. 3 - Typical Transfer Characteristics

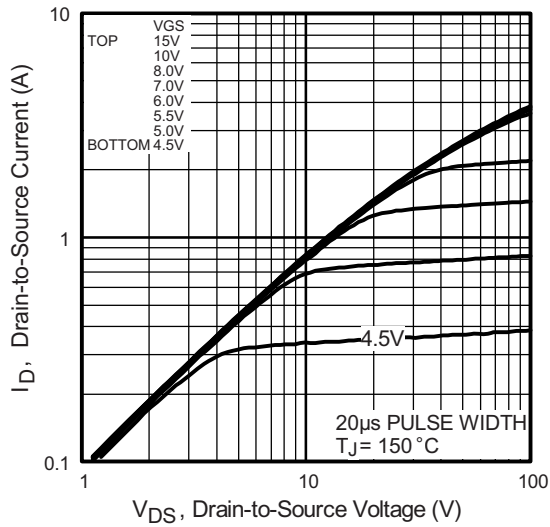


Fig. 2 - Typical Output Characteristics

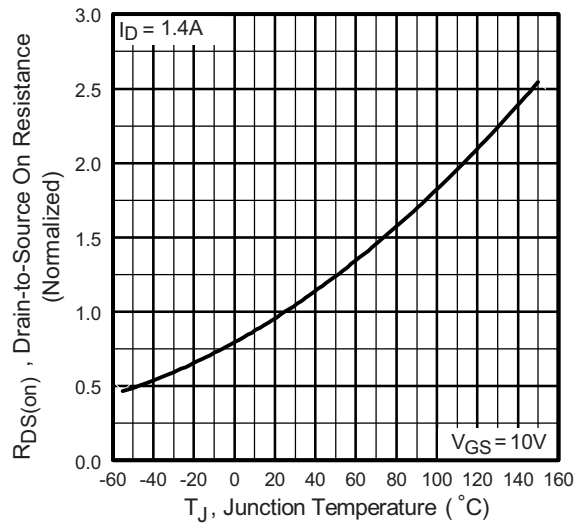


Fig. 4 - Normalized On-Resistance vs. Temperature

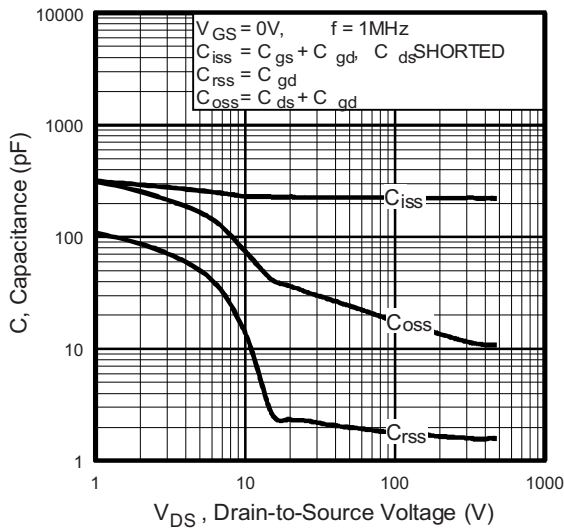


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

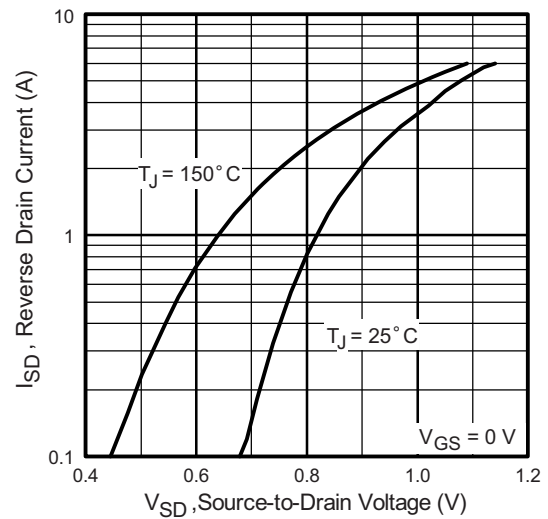


Fig. 7 - Typical Source-Drain Diode Forward Voltage

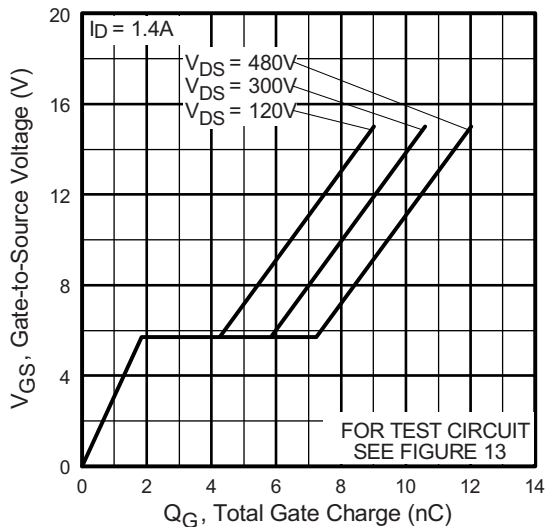


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

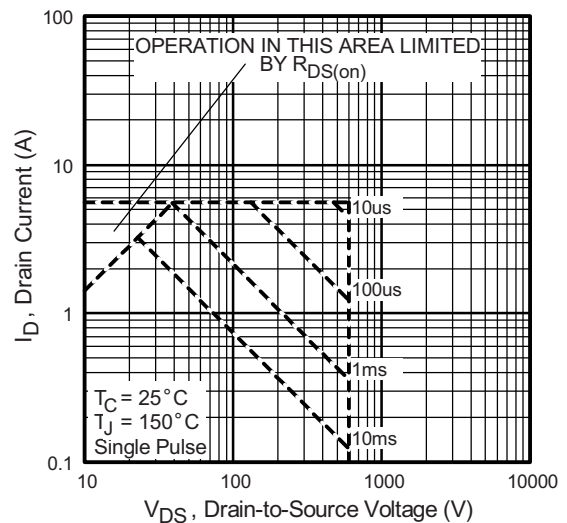
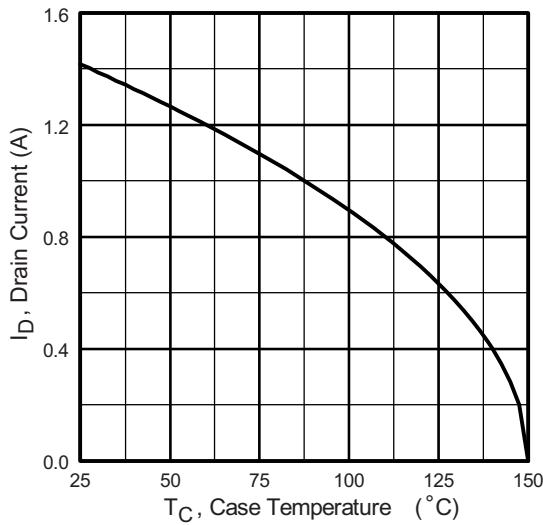
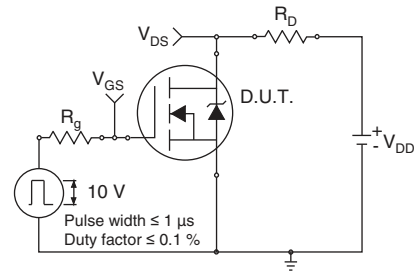


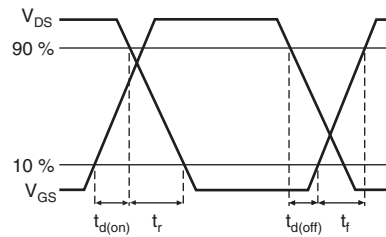
Fig. 8 - Maximum Safe Operating Area



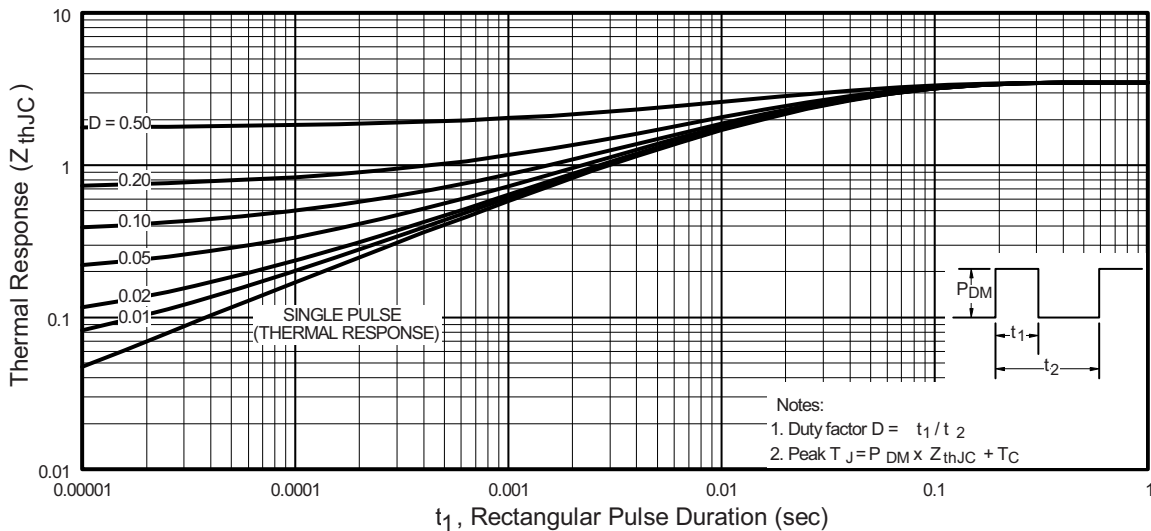
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



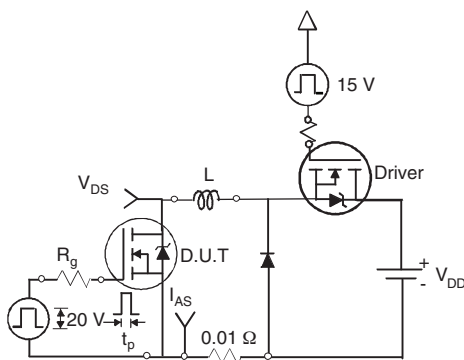
**Fig. 10a - Switching Time Test Circuit**



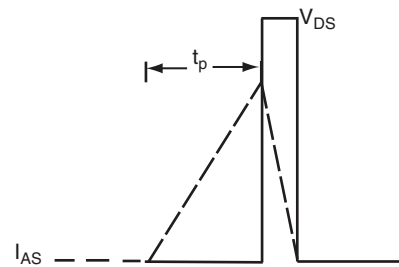
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

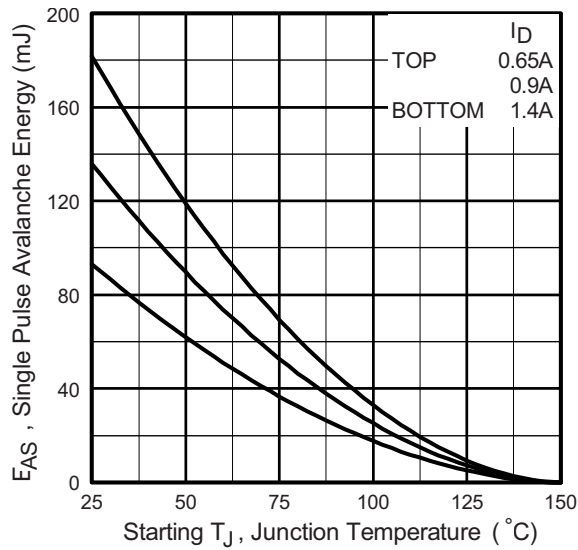


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

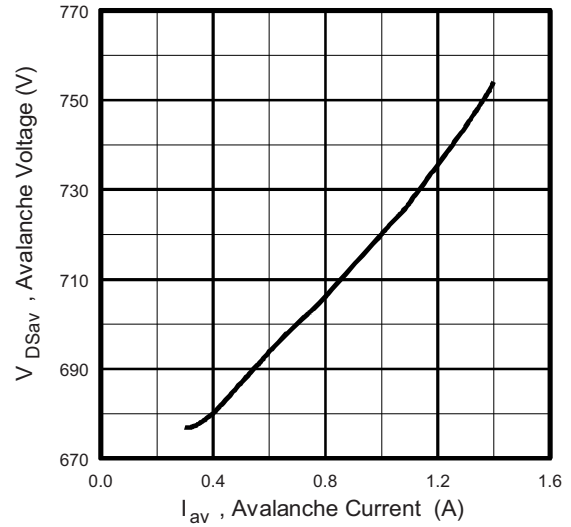


Fig. 12d - Basic Gate Charge Waveform

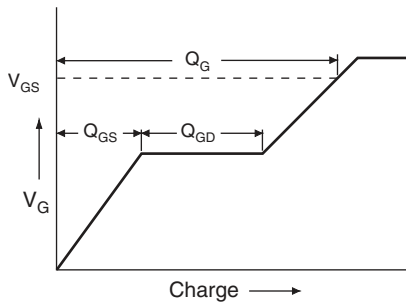


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

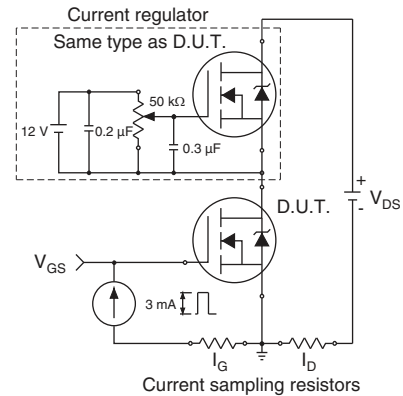
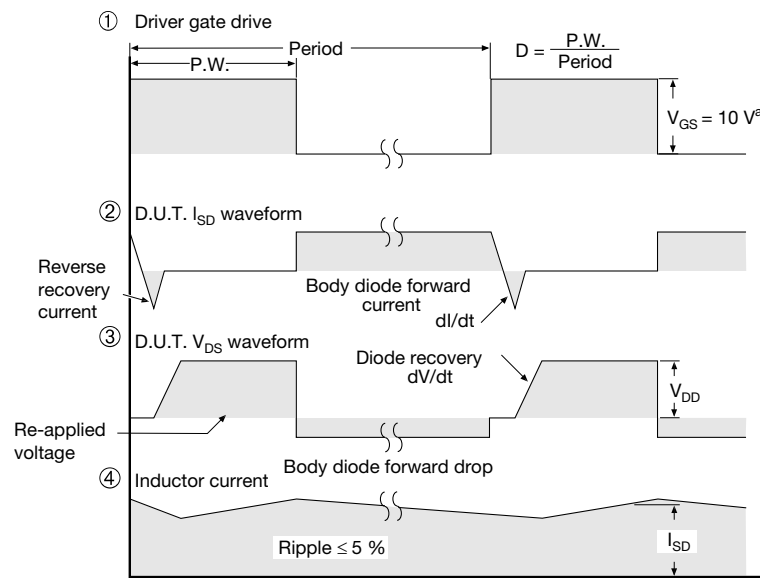
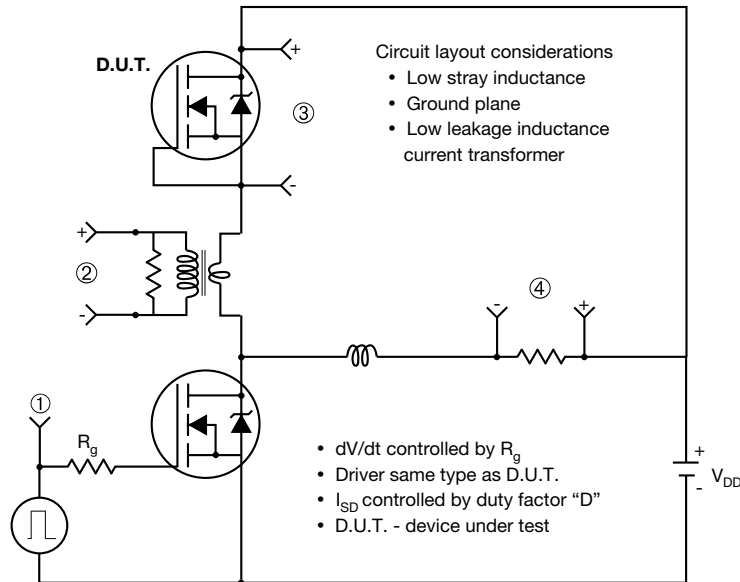


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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## TO-252AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
E	6.40	6.73	0.252	0.265
L	1.40	1.77	0.055	0.070
L1	2.743 REF		0.108 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.89	1.27	0.035	0.050
L4	0.64	1.01	0.025	0.040
D	6.00	6.22	0.236	0.245
H	9.40	10.40	0.370	0.409
b	0.64	0.88	0.025	0.035
b2	0.77	1.14	0.030	0.045
b3	5.21	5.46	0.205	0.215
e	2.286 BSC		0.090 BSC	
A	2.20	2.38	0.087	0.094
A1	0.00	0.13	0.000	0.005
c	0.45	0.60	0.018	0.024
c2	0.45	0.58	0.018	0.023
D1	5.30	-	0.209	-
E1	4.40	-	0.173	-
θ	0'	10'	0'	10'

ECN: S-81965-Rev. A, 15-Sep-08  
 DWG: 5973

### Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.



### TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08  
DWG: 5968

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**



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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.