



**Absolute Maximum Ratings**

|  |   |
|--|---|
| Voltage on HVD, MIRIN, MIRCAP, and MIROUT<br>Relative to HVGND .....-0.3V to +79V                    | Continuous Power Dissipation (T <sub>A</sub> = +70°C)<br>TQFN (derate 15.4mW/°C above +70°C).....1228.9mW |
| Voltage on V <sub>CC</sub> and AVCC to GND .....-0.3V to + 4.3V                                      | Storage Temperature Range..... -65°C to +150°C  |
| Voltage on All Other Pins Relative<br>to GND.....-0.3V to (V <sub>CC</sub> + 0.3V) Not to Exceed +4V | Lead Temperature (soldering, 10s) .....+300°C   |
|  | Soldering Temperature (reflow).....+260°C   |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Electrical Characteristics**

(V<sub>MIRIN</sub> = 15V to 76V, V<sub>CC</sub> = 2.85V to 3.63V, T<sub>A</sub> = -40°C to +95°C, unless otherwise noted.) (Note 1)

| PARAMETER  | SYMBOL                | CONDITIONS  | MIN                       | TYP  | MAX                   | UNITS |    |
|--|-----------------------|---|---------------------------|------|-----------------------|-------|----|
| Low Voltage Supply   | V <sub>CC</sub>       |   | 2.85                      |      | 3.63                  | V     |    |
| Low Voltage Current  | I <sub>CC</sub>       | (Note 2)  |                           | 8    | 16                    | mA    |    |
| MIRIN Quiescent Current  | I <sub>MIRIN</sub>    | V <sub>MIRIN</sub> = 60V,<br>ISRC/SHDN =<br>30kΩ to GND       | I <sub>MIROUT</sub> = 0μA | 1    | 2                     | mA    |    |
|  |                       |   | I <sub>MIROUT</sub> = 1mA | 3.2  | 4                     |       |    |
| MIRIN Voltage  | V <sub>MIRIN</sub>    |   | 15                        |      | 76                    | V     |    |
| HV FET On-Resistance   | R <sub>DSONHV</sub>   | V <sub>GS</sub> = 3.0V, I <sub>D</sub> = 170mA                |                           | 0.85 | 2                     | Ω     |    |
| HVG Voltage  | V <sub>GSHV</sub>     |   | 0                         |      | V <sub>CC</sub> + 0.3 | V     |    |
| HVD Voltage  | V <sub>DHV</sub>      |   |                           |      | 76                    | V     |    |
| HVD Leakage  | I <sub>ILHV</sub>     |   | -1                        |      | +1                    | μA    |    |
| Logic-Input Thresholds (DIFFEN, DISCHARGE, GAIN, HVG, SEN, SENXOR) | V <sub>IL</sub>       |   |                           |      | 0.3 x V <sub>CC</sub> | V     |    |
|  | V <sub>IH</sub>       |   | 0.7 x V <sub>CC</sub>     |      |                       |       |    |
| ISRC/SHDN Threshold  | V <sub>IL_SHDN</sub>  |   |                           |      | 1.4                   | V     |    |
|  | V <sub>IH_SHDN</sub>  |   | V <sub>CC</sub> - 0.2     |      |                       |       |    |
| ISRC/SHDN Resistor   | R <sub>ISRC</sub>     | (Note 3)  | 29.7                      | 30   | 30.3                  | kΩ    |    |
| Maximum MIROUT Current   | I <sub>CLAMP</sub>    | ISRC/SHDN = low   | R <sub>LIM</sub> = 40.2kΩ | 1.4  | 2                     | 2.8   | mA |
|  |                       |   | R <sub>LIM</sub> = 24.9kΩ | 2.5  | 3.2                   | 4.1   |    |
|  |                       | ISRC/SHDN = high  |                           |      |                       | 0.01  |    |
| MIROUT Capacitive Load   | C <sub>MIROUT</sub>   | Total capacitance on MIROUT to achieve accuracy specification | 330                       |      | 500                   | pF    |    |
| Logic Output Levels (I <sub>LIMS</sub> )                           | V <sub>OL_ILIMS</sub> | I <sub>LIMS</sub> = -2mA                                      |                           |      | 0.45                  | V     |    |
|  | V <sub>OH_ILIMS</sub> | I <sub>LIMS</sub> = +2mA                                      | V <sub>CC</sub> - 0.45    |      |                       |       |    |

**Electrical Characteristics (continued)**(V<sub>MIRIN</sub> = 15V to 76V, V<sub>CC</sub> = 2.85V to 3.63V, T<sub>A</sub> = -40°C to +95°C, unless otherwise noted.) (Note 1)

| PARAMETER  | SYMBOL                                   | CONDITIONS   | MIN                   | TYP   | MAX   | UNITS |
|--|--|--|-----------------------|-------|-------|-------|
| Logic Output Levels (GAIN Has 3.5kΩ Internal Nominal Impedance)                  | V <sub>OL</sub>                          | I <sub>GAIN</sub> = -30μA  |                       |       | 0.4   | V     |
|  | V <sub>OH</sub>                          | I <sub>GAIN</sub> = +30μA  | V <sub>CC</sub> - 0.4 |       |       |       |
| ILIMS Output Time  | t <sub>ILIMS</sub>                       | (Note 4)   |                       | 1     |       | μs    |
| IOOUT to MIROUT Ratio  | K <sub>IOOUT</sub>                       | I <sub>MIROUT</sub> = 1mA  | 0.090                 | 0.100 | 0.110 | A/A   |
| VIP1 to MIROUT Ratio   | K <sub>VIP1</sub>                        | I <sub>MIROUT</sub> = 1mA  | 0.720                 | 0.800 | 0.880 | A/A   |
| VIP2 to MIROUT Ratio   | K <sub>VIP2</sub>                        | I <sub>MIROUT</sub> = 1mA  | 0.180                 | 0.200 | 0.220 | A/A   |
| K <sub>VIP1</sub> , K <sub>VIP2</sub> , and K <sub>IOOUT</sub> Voltage Variation | K <sub>VAR</sub>                         | V <sub>MIRIN</sub> = 40V ± 10%   |                       | ±0.3  | ±2.5  | %     |
| Mirror Voltage Drop Monitor Load Capacitance                                     | V <sub>APDV:CAP</sub>                    | External capacitance required on APDV  | 50                    |       | 250   | pF    |
| Mirror Voltage Drop  | V <sub>MIRIN</sub> - V <sub>MIROUT</sub> | Current limit not exceeded, V <sub>SHDN</sub> = Hi-Z, I <sub>MIRIN</sub> = 1mA |                       | 4     |       | V     |
| Shutdown Temperature   | T <sub>SHDN</sub>                        |  |                       | 150   |       | °C    |
| Shutdown Temperature Hysteresis  | T <sub>HYS</sub>                         |  |                       | 20    |       | °C    |
| VIP1 Offset Current  | I <sub>VIP1OFF</sub>                     | R <sub>ISRC</sub> = 30kΩ   |                       | 20    | 40    | μA    |
| VIP2 Offset Current  | I <sub>VIP2OFF</sub>                     | R <sub>ISRC</sub> = 30kΩ   |                       | 19    | 30    | μA    |
| IOOUT Offset Current   | I <sub>OUTOFF</sub>                      | R <sub>ISRC</sub> = 30kΩ   |                       | 18    | 25    | μA    |

## Sample and Hold Parameters

( $V_{MIRIN}$  = 15V to 76V,  $V_{CC}$  = 2.85V to 3.63V,  $T_A$  = -40°C to +95°C,  $R_{ISRC}$  = 30k $\Omega$ , DISCHARGE = high, unless otherwise noted.)  
(Note 1)

| PARAMETER                                   | SYMBOL       | CONDITIONS  | MIN  | TYP       | MAX  | UNITS      |
|---|--------------|---|------|-----------|------|------------|
| Output Error (Total Error from All Sources) | $V_{ERR}$    | $I_{MIROUT}$ from 600 $\mu$ A to 60 $\mu$ A (Note 5)                                    |      | $\pm 5.5$ |      | %          |
|   |              | $I_{MIROUT}$ from 20 $\mu$ A to 500 $\mu$ A (Note 5)                                    | -9.0 |           | +9.0 |            |
| Output Voltage                              | $V_{OUT}$    | $V_{OUT} = V_{VOP} - V_{VON}$ ,<br>100k $\Omega$ output load                            | 0    |           | 2.5  | V          |
| Output Voltage Common Mode                  | $V_{OUTCM}$  | $V_{DIFFEN} = \text{High}$  |      | 1.4       |      | V          |
| Output Impedance                            | $R_{OUT}$    |   |      |           | 1    | k $\Omega$ |
| VOP Output Capacitive Load                  | $C_{LD}$     | Capacitance for stable operation  |      |           | 50   | pF         |
| Gain Selection Threshold                    | $V_{GTHR}$   |   | 320  | 400       | 460  | mV         |
| GAIN Impedance                              | $R_G$        | (Note 6)  | 2.1  | 3.5       | 4.9  | k $\Omega$ |
| Sample Time                                 | $t_S$        | 1k $\Omega$ resistors connected to VIP1 and VIP2 (Note 7)                               | 300  |           |      | ns         |
| Delay Time                                  | $t_{DEL}$    | (Note 7)  | 10   |           |      | ns         |
| Output Valid Time                           | $t_{O\_VAL}$ | Less than 1% change from the time the output is valid, $C_{LD} = 50$ pF (Notes 7 and 8) | 9    |           | 109  | $\mu$ s    |

Note 1: Limits are 100% tested at  $T_A = +25^\circ\text{C}$ . Limits over the operating temperature range and relevant supply voltage rating are guaranteed by design and characterization.

Note 2: ISRC/SHDN is not connected; HV FET is driven by a 100 $\Omega$  source at 250kHz with a 2.97V square wave; HVD is connected to GND.

Note 3: External resistor connected to GND. This value guarantees accuracy of DS3923.  $I_{ISRC} = (6/R_{ISRC}) \pm 6\%$ .

Note 4: Resistor connected to RLIM for 1mA clamp limit.  $I_{MIROUT}$  step from 10 $\mu$ A to 10mA. Time measured from  $I_{MIROUT}$  step to  $I_{MIROUT} < 1.1$ mA (see the [Typical Application Circuit](#)).  $C_3 = 47$ pF,  $C_1 = C_2 = 0.1$  $\mu$ F,  $V_{VC1} = 30$ V,  $R_1 = 100$  $\Omega$ .

Note 5: Output Error =  $VOP - 4 \times (VIP1 \text{ or } VIP2)$  and sampled at  $t_{OUT}$ . Measured at +25°C with offset removed.

Note 6: To change internal gain selection, external driver must be capable of meeting the GAIN input logic level with the GAIN impedance connected to either  $V_{CC}$  or GND.

Note 7: See Figure 1 for more detail on timing.

Note 8: Time referenced to SENINT falling edge when output is valid at  $VOP - VON$  if  $DIFFEN = \text{High}$  or  $VOP$  if  $DIFFEN = \text{Low}$ .

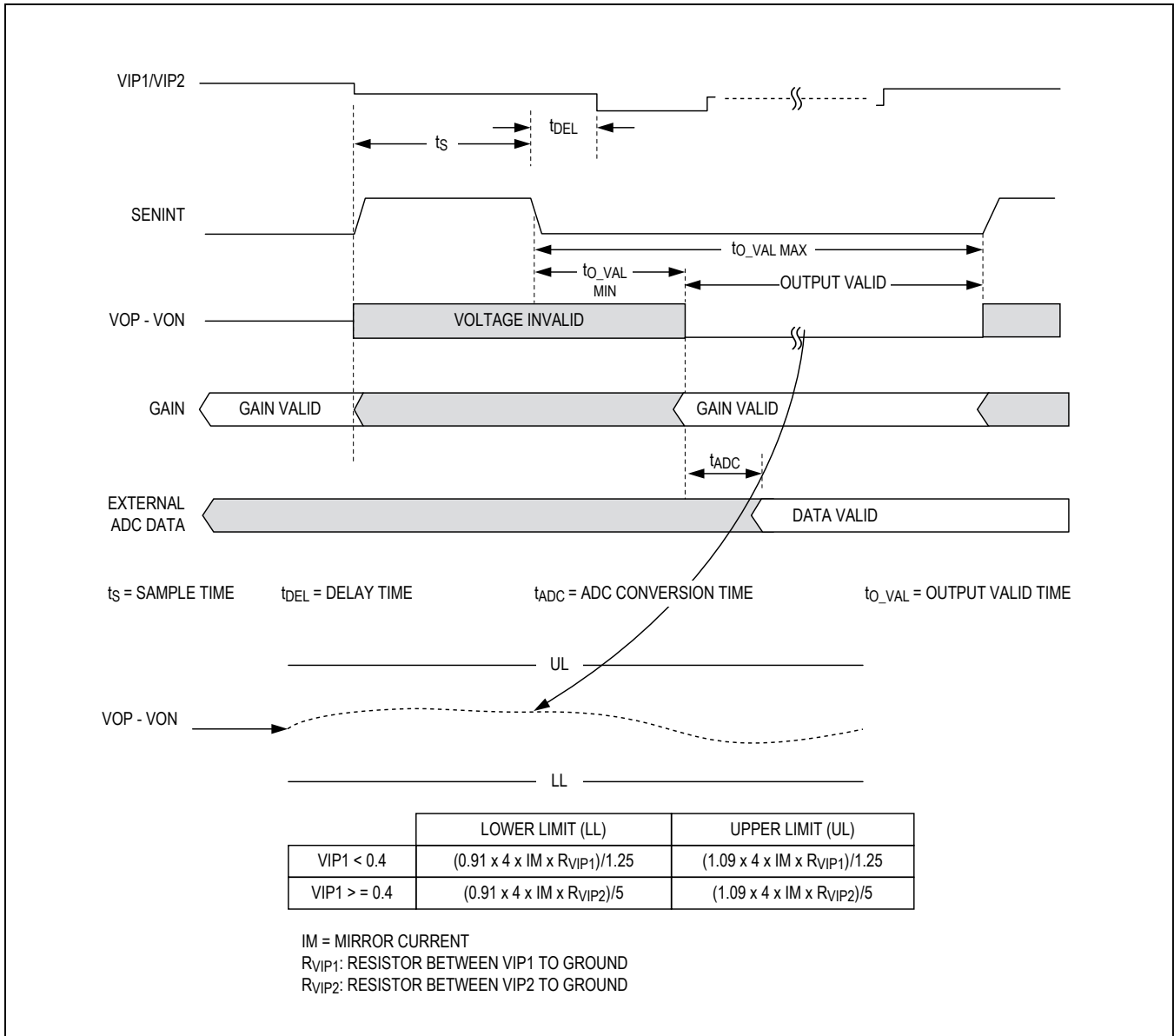
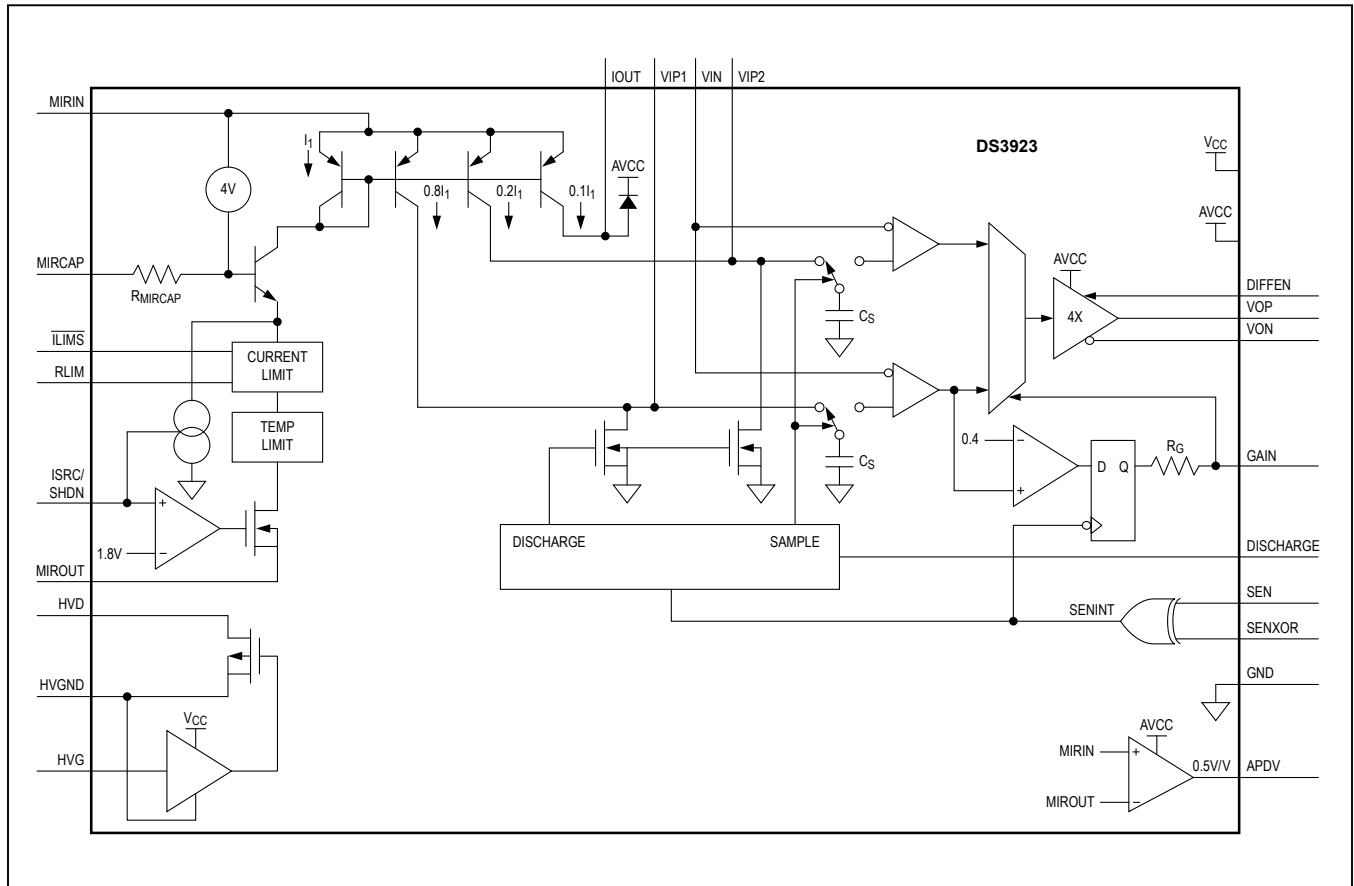


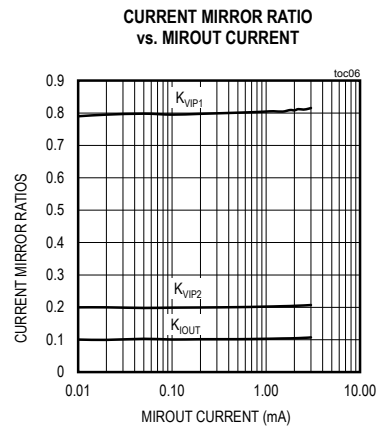
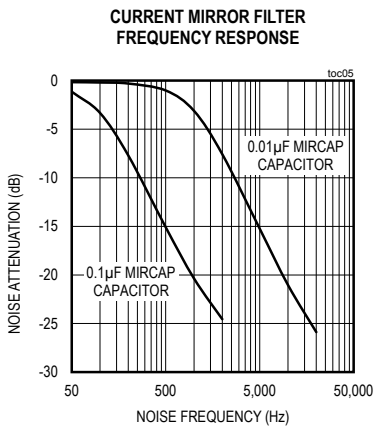
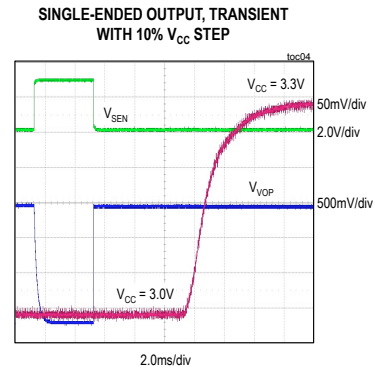
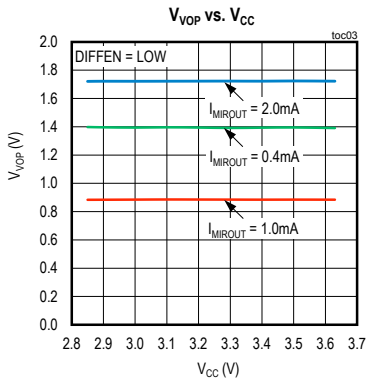
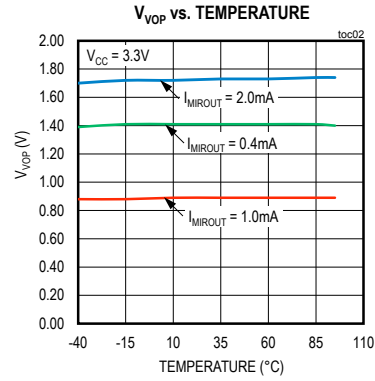
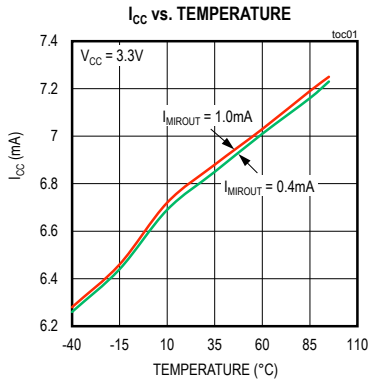
Figure 1. DS3923 Sample/Hold Timing Diagram

Block Diagram

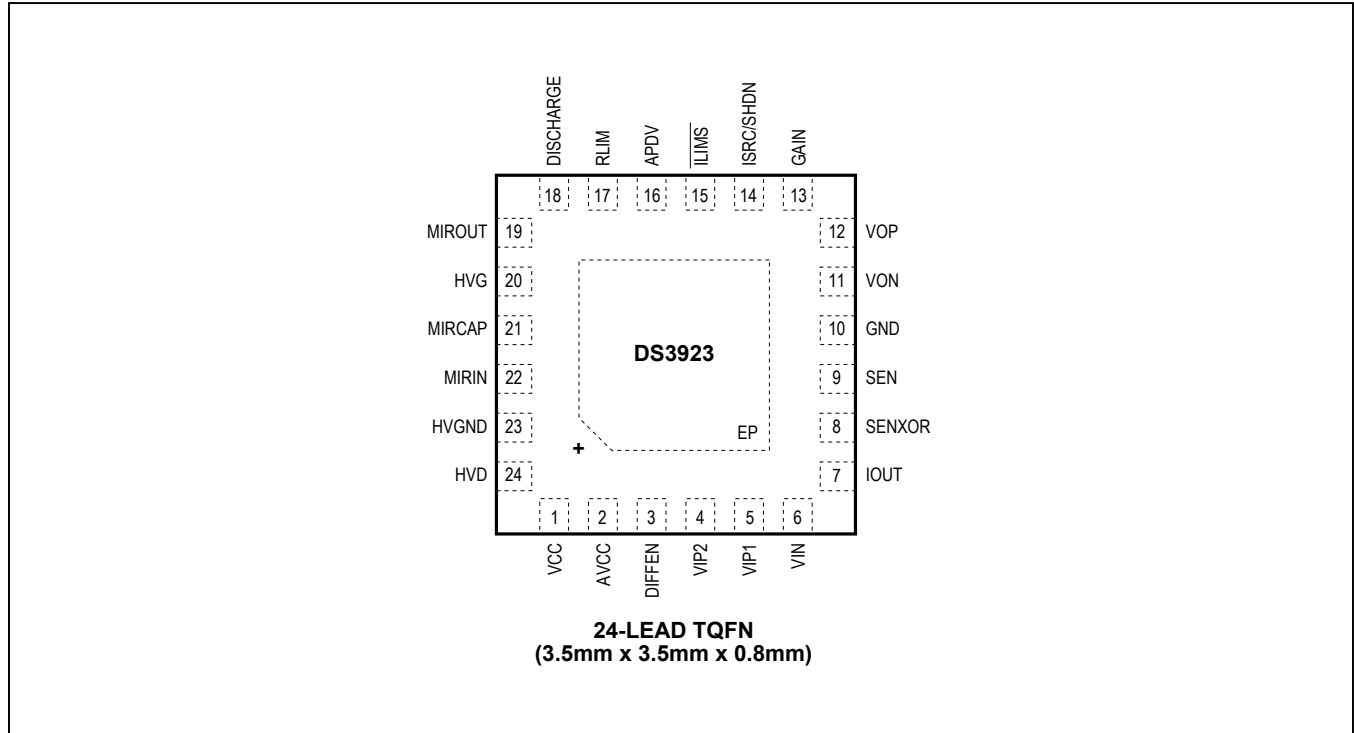


Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



Pin Configuration



Pin Description

| PIN | NAME             | FUNCTION  |
|-----|------------------|---|
| 1   | V <sub>CC</sub>  | Digital 3.3V (Nominal) Supply   |
| 2   | AV <sub>CC</sub> | Analog 3.3V (Nominal) Supply  |
| 3   | DIFFEN           | Sample/Hold Single-Mode/Differential Mode Selection. When logic input is:<br>Low: Single-mode sample/hold output<br>High: Differential mode sample/hold output.   |
| 4   | VIP2             | 20% Current Mirror Output. Connect to resistor to ground.   |
| 5   | VIP1             | 80% Current Mirror Output. Connect to resistor to ground.   |
| 6   | VIN              | Negative Voltage Input. Connect to the same ground point as resistors connected to VIP1 and VIP2.   |
| 7   | IOUT             | 10% Current Mirror Output. If unused, do not connect.   |
| 8   | SENXOR           | Sample Enable XOR. The start and stop of the sampling depend on the logic input of SENXOR and SEN.<br>When SENXOR is low, the rising edge of the SEN pulse activates sampling, and the falling edge of the SEN pulse deactivates sampling.<br>When SENXOR is high, the falling edge of the SEN pulse activates sampling, and the rising edge of the SEN pulse deactivates sampling. <b>Note:</b> If SENXOR is high, the discharge function should not be used.<br>See <a href="#">Figure 3</a> for more detail. |
| 9   | SEN              | Sample Enable Pulse. Logic input. See the description of SENXOR and <a href="#">Figure 3</a> for more detail.   |



## Pin Description (continued)

| PIN | NAME           | FUNCTION  |
|-----|----------------|---|
| 10  | GND            | Ground  |
| 11  | VON            | Negative Sample/Hold Voltage Output. Do not connect for single-ended mode.  |
| 12  | VOP            | Sample/Hold Voltage Output. Positive output in differential mode. Also used for single-ended output.  |
| 13  | GAIN           | Hold Amplifier Gain Indicator. Both as output and logic input. Indicates which current mirror's output is active. 3.5kΩ input/output impedance.<br>Pin as input (mirror selection for sample/hold):<br>Low: Sample/hold Conversion from Current Mirror 1 (VIP1);<br>High: Sample/hold Conversion from Current Mirror 2 (VIP2).<br>Pin as output (mirror indication for sample/hold):<br>Low: Sample/hold Conversion from Current Mirror 1 (VIP1);<br>High: Sample/hold Conversion from Current Mirror 2 (VIP2).   |
| 14  | ISRC/<br>SHDN  | Dual-Purpose Pin.<br>ISRC: A resistor connected to this pin controls the amount of current flowing through a current source connected to MIROUT. ( <b>Note:</b> During this mode of operation, the microcontroller pin (if connected) should be in the high impedance.)<br>SHDN: If pulled high, sets MIROUT to high-impedance.   |
| 15  | ILIMS          | Current-Limit Status. Active-low signal indicating that the current-limit threshold is exceeded.  |
| 16  | APDV           | APD Voltage Monitor. Provides output voltage used to calculate the voltage on the APD.  |
| 17  | RLIM           | Resistor Limit. Connect a resistor between RLIM and GND to set the current clamp limit.   |
| 18  | DIS-<br>CHARGE | Discharge Enable.<br>When sampling is deactivated and the DISCHARGE pin logic input is low, the discharge function is disabled.<br>When sampling is deactivated and the DISCHARGE pin logic input is high, the discharge function is enabled, and the DS3923 pulls current mirror outputs VIP1 and VIP2 low to ensure accurate sampling.<br>During the sample time, the pin discharge is internally disabled by the DS3923. See <a href="#">Figure 4</a> and <a href="#">Figure 5</a> for more detail.<br><b>Note:</b> The discharge function should not be used if SENXOR is a logic-high. |
| 19  | MIROUT         | Current Mirror Output. Connect to APD.  |
| 20  | HVG            | High-Voltage NMOS FET Gate. Connect to ground if unused.  |
| 21  | MIRCAP         | Mirror Filter. Connect external capacitor to filter voltage at MIROUT.  |
| 22  | MIRIN          | Current Mirror Input. Connect to high voltage supply.   |
| 23  | HVGND          | High-Voltage NMOS FET Source  |
| 24  | HVD            | High-Voltage NMOS FET Drain. Connect to HVGND if unused.  |
| —   | EP             | Exposed Pad. Connect to ground with a minimum of 9 vias for thermal conductivity improvement. It is acceptable to use solder mask between the IC and the ground pad. It is not necessary to electrically connect the exposed pad ground.  |

**Detailed Description**

The DS3923 contains circuits to monitor the APD bias current. The device includes three current mirrors, which allow for a wide dynamic monitoring range. The mirror response time is fast enough to comply with GPON Rx burst-mode monitoring requirements. The device has a built-in current-limiting feature to protect APDs. This current limit is adjustable using an external resistor. The APD current can also be shut down by ISRC/SHDN or thermal shutdown. The internal HV FET may be used as a fast APD shutdown. A dual range sample/hold circuit with a range selection multiplexer is included to hold the analog voltage while an external ADC performs the conversion.

**Current Mirrors**

The DS3923 includes three current mirrors as shown in Figure 2. One is a 10:1 (10%) mirror connected at IOUT. The other two are a 1.25:1 (80%) and the 5:1 (20%) mirror connected to VIP1 and VIP2 as well as the internal sample/hold circuit. On pin VIP1 and VIP2, resistors to ground should be selected such that the maximum voltage is 0.625V (2.5V after the 4x gain of the built-in amplifier).

For example, if the maximum monitored current through the APD is 1mA, the mirror is 1.25:1 ratio, and then the correct resistor is approximately 780Ω.

**Current Mirror Filter**

The DS3923 includes a filter to stabilize the MIROUT voltage. An external capacitor must be connected to pin MIRCAP. See specification  $t_{MIRCAP}$  in the [Electrical Characteristics](#) table for filter and capacitor settings.

**Current Source for Mirror Bias**

The current mirror response time is improved by providing a continuous current source. This source is adjustable by changing the resistor connected to the ISRC/SHDN pin. However, only one value is allowed to guarantee performance (see [Electrical Characteristics](#) table).

$$I_{ISRC} = (6 / R_{ISRC}) \pm 6\%$$

Typical  $R_{ISRC}$  value should be 30kΩ.

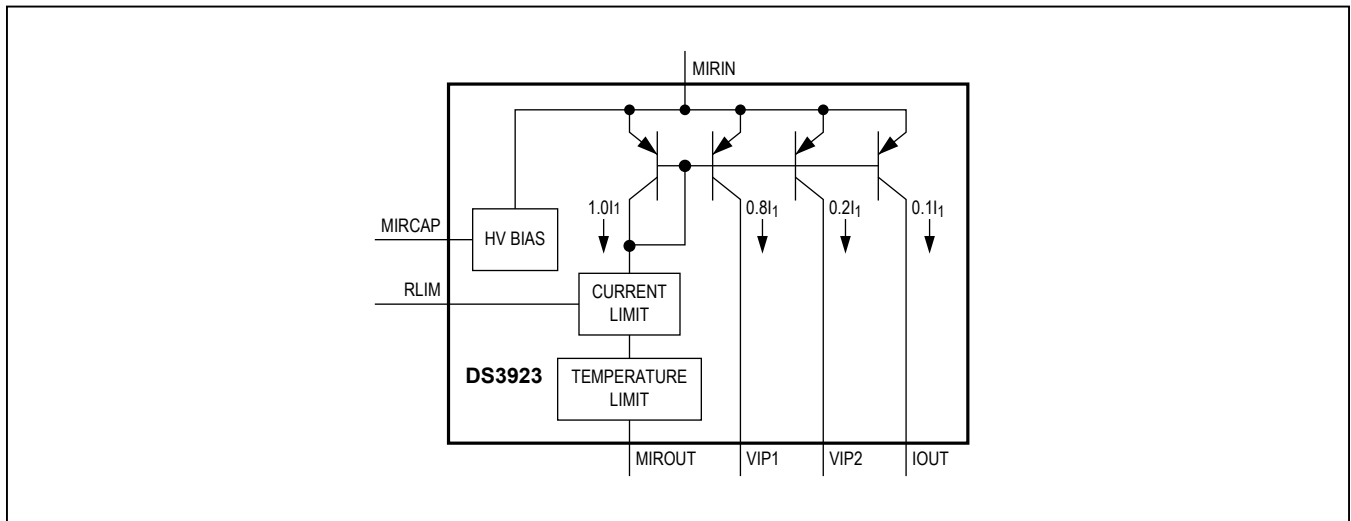


Figure 2. DS3923 Current Mirrors

**Current Mirror Voltage Drop Monitor**

The DS3923 includes a voltage monitor that indicates the voltage drop across the current mirror. This signal is output on APDV. This signal should be used to accurately maintain the correct APD bias voltage in conjunction with the feedback resistors for the APD bias boost converter.

$$APDV = (V_{MIRIN} - V_{MIROUT})/2$$

**Current Clamp**

The DS3923 has a current clamping circuit to protect the APD by limiting the amount of current from MIROUT. The current limit is defined by a resistor ( $R_{LIM}$ ) connected between the RLIM pin and ground. A larger  $R_{LIM}$  results in a lower current clamp limit (see [Electrical Characteristics](#) table).

**Shutdown**

The MIROUT output can be set to a high-impedance state using the ISRC/SHDN pin, effectively disabling the APD. The ISRC/SHDN pin is active-high.

**Sample/Hold**

As shown in the block diagram, the DS3923 Sample/Hold consists of sampling capacitors ( $C_S$ ), control logic and a differential output amplifier. The control logic selects the current mirror for the sample/hold. Additionally, it controls

the sample time by taking a logic input from SENXOR pin as shown in [Figure 4](#). The sample/hold has a discharge circuit to discharge parasitic capacitance on the mirror outputs VIP1, VIP2,  $V_{IN}$  and the sample capacitor before it starts sampling.

During the sample time ( $t_S$ ) the sample/hold capacitor is connected to sample/hold input for sampling of the input signal either from VIP1 or VIP2 which is selected by the sample/hold control circuit. As shown below in [Figure 3](#), the sampling start and stop depends upon the logic input of SENXOR and SEN. Sampling stops at the SEN falling edge (when SENXOR is low) or rising edge (when SENXOR is high), and the voltage stored at the sampling capacitors is then amplified by the hold amplifier.

The voltage at current mirrors VIP1, VIP2, and IOUT pins can be shown as:

$$VIP1 = 0.8 \times I1 \times R4$$

$$VIP2 = 0.2 \times I1 \times R5$$

$$I_{OUT} = 0.1 \times I1 \times R6$$

$I1$ ,  $R4$ ,  $R5$ , and  $R6$  are shown in the [Typical Application Circuit](#).

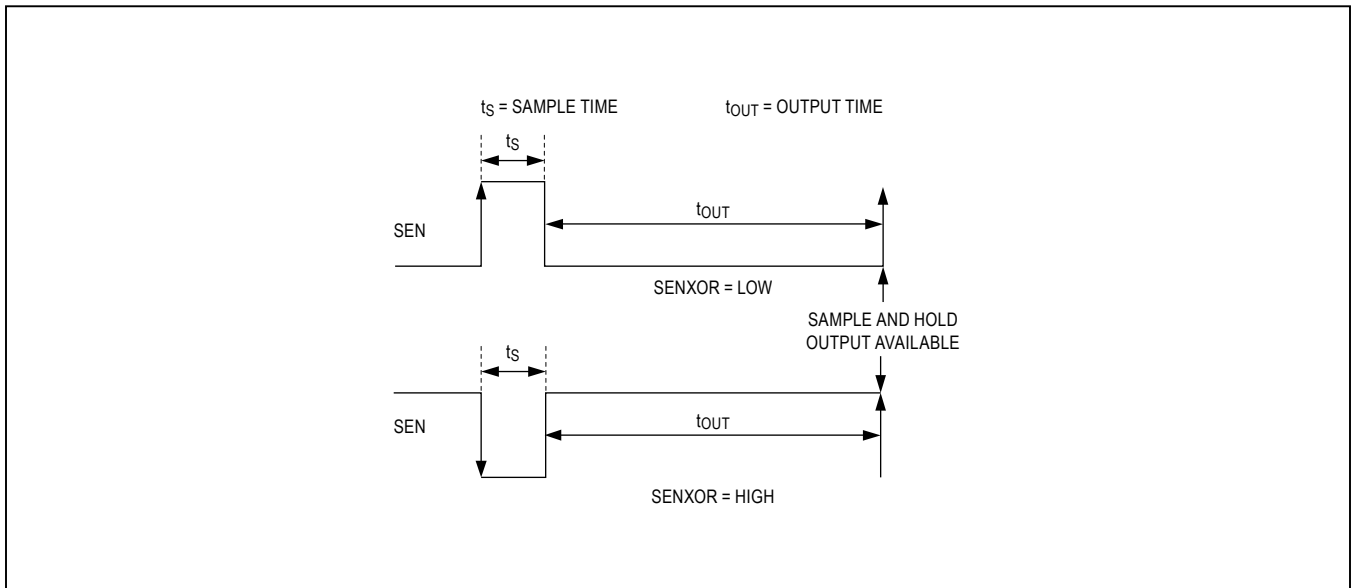


Figure 3. SEN Pulse and Sample/Hold Output Timing Diagram

**Table 1. Sample/Hold Output Voltage vs. Input**

| INPUT SELECTED (AUTO OR FORCED) | SAMPLE/HOLD OUTPUT VOLTAGE   |
|---------------------------------|--|
| VIP1                            | $4 \times \text{VIP1} = 4 \times 0.8 \times I1 \times R4$<br>$= 3.2 \times I1 \times R4$ |
| VIP2                            | $4 \times \text{VIP2} = 4 \times 0.2 \times I1 \times R5$<br>$= 0.8 \times I1 \times R5$ |

In addition to VIP1 or VIP2 auto selection, the DS3923 allows VIP1 or VIP2 forced selection using the GAIN pin. The sample/hold amplifier output is shown in [Table 1](#).

**Sampling Capacitors**

Each sample/hold input voltage is sampled using an internal capacitor. As shown in the [Block Diagram](#), when SENXOR is low, the capacitors are connected to the input during the high time of the SEN pulse. When SENXOR is high, the capacitors are connected to the input during the low time of the SEN pulse. These capacitors must be fully charged before SEN becomes inactive in order to ensure accurate sampling. An RC time constant is created by the

resistance of the voltage source connected to the sample/hold's input and the DS3923's sampling capacitors. An external capacitor may be used on the sample/hold's inputs. This external capacitance will be in parallel with the pin's ESD capacitance (~7pF). These capacitors can be discharged when the DS3923 is not sampling the input by setting the DISCHARGE pin to high.

**Discharge**

When the DISCHARGE pin is set to logic-high, the DS3923 pulls down current mirror outputs VIP1 and VIP2 to low. The discharge strength is about 50Ω. During the sample time  $t_s$ , the pin discharge is internally disabled by the DS3923 as shown in [Figure 4](#) and [Figure 5](#). When the DISCHARGE pin is set to logic-low, the pin discharge function is disabled.

**Note:** The discharge function should not be used if SENXOR is a logic high.

**Gain Selection**

The sample/hold circuit has a native gain of 4 applied to the input presented. Depending on the level of VIP1, a selection is made to present either VIP1 or VIP2 to the sample/hold circuit when SEN pulse is applied. The sample circuit applied to this buffer is chosen by a reference voltage (400mV) and a comparator to avoid outputting a clipped value. [Table 2](#) lists the conditions that make the choice. The choice made is indicated on the GAIN pin.

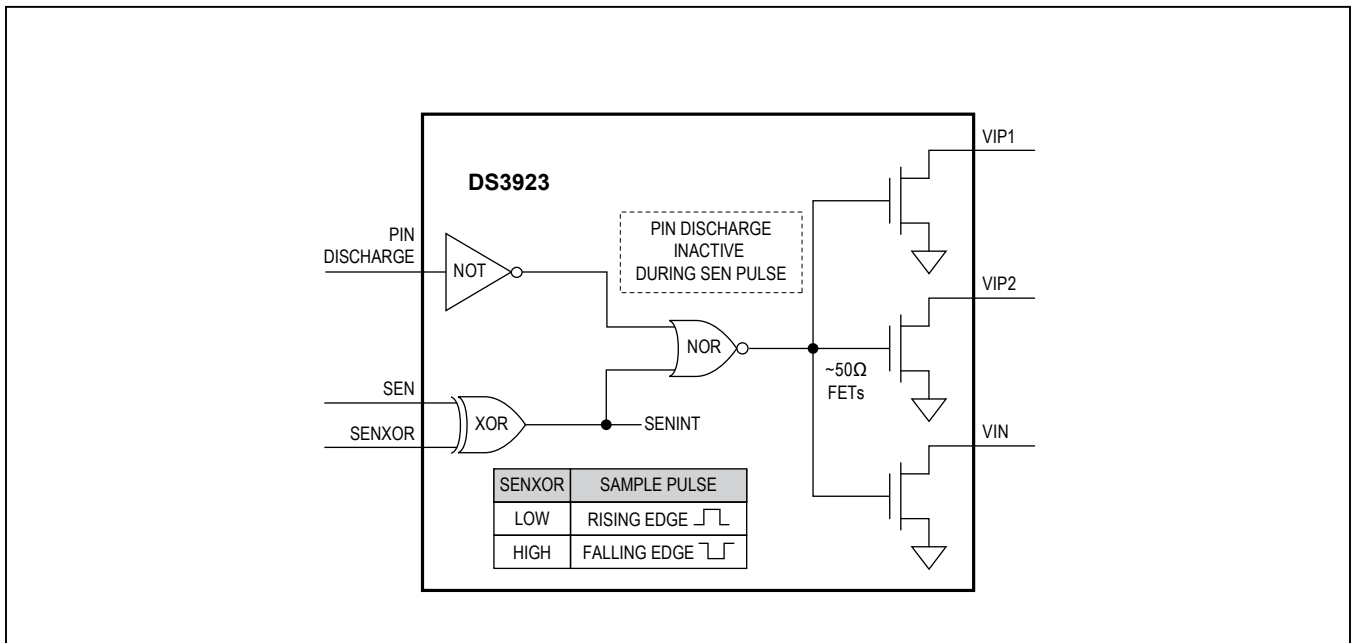


Figure 4. Discharge Logic Diagram

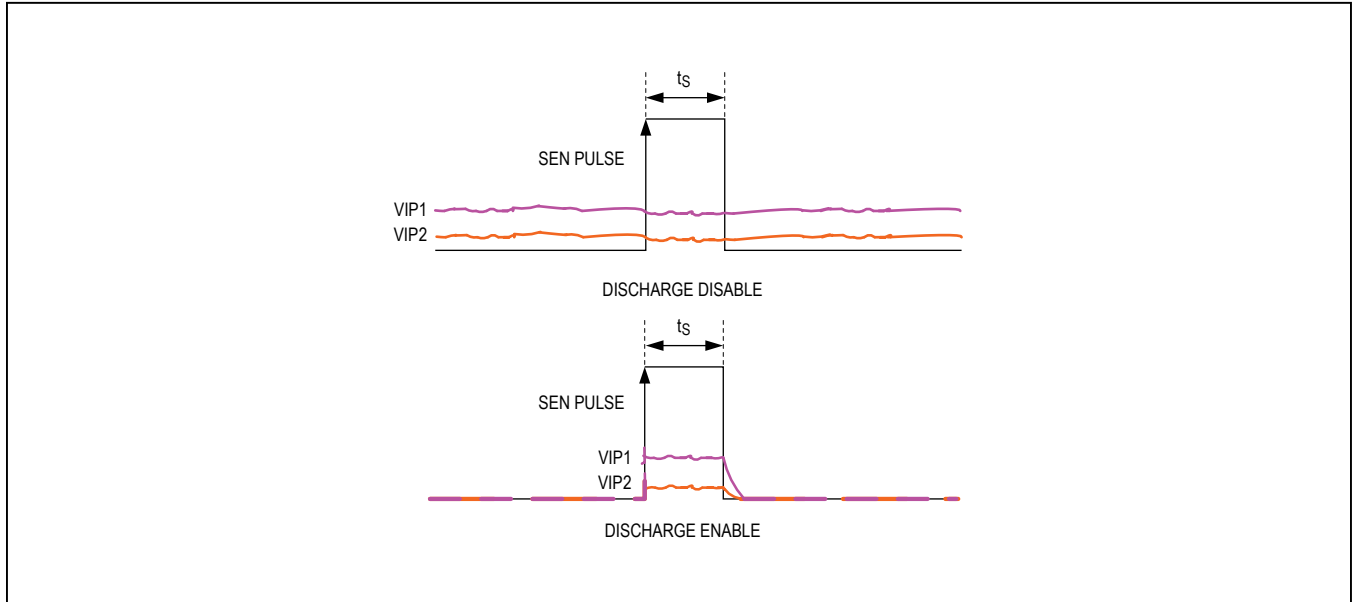


Figure 5. Discharge, Current Mirror, and SEN Pulse Timing Diagram

Table 2. Sample/Hold Input Selection

| VIP1   | INPUT SELECTED | OUTPUT VOLTAGE | GAIN OUTPUT     |
|--------|----------------|----------------|-----------------|
| < 0.4V | VIP1           | 4 × VIP1       | 0               |
| ≥ 0.4V | VIP2           | 4 × VIP2       | V <sub>CC</sub> |

Alternatively, forcing GAIN = 0 always chooses VIP1 and forcing GAIN = V<sub>CC</sub> chooses VIP2. By default, GAIN pin is pulled high.

The logical circuit is shown in [Figure 6](#).

**Output Buffer**

After sampling is complete, the sampling capacitor is switched to the output buffer. This buffer requires a small amount of time to settle, t<sub>OUT</sub> (see the [Electrical Characteristics](#) table) as shown in [Figure 3](#). When an ADC is used to measure the DS3923’s output, a step will occur at the ADC’s input caused by its sampling capacitor. The DS3923’s t<sub>REC</sub> is dependent on the size of this sampling capacitor and the voltage applied across it. To maximize accuracy, the ADC’s sampling speed (ADC clock frequency) should be slowed down until the ADC’s acquisition window is larger than the DS3923’s recovery time.

**Sampling Time and Output Error**

As sampling time (t<sub>S</sub>) decreases, V<sub>ERR</sub> increases. V<sub>ERR</sub> is largely dependent on the settling time of the sampling capacitor, and to a lesser degree to the buffer’s gain error and offset voltage. Settling time can be reduced by reducing the resistor connected between the sample/hold amplifier’s input and ground. However, a smaller resistor will decrease the amplitude of the sampled signal, and cause the relative offset errors to become more significant.

**High-Voltage (HV) Switch FET**

A high-voltage (HV) switching FET is included to optionally be used to quickly turn off the bias voltage to the APD. The strong HV FET can quickly discharge the capacitance on the MIRIN pin.

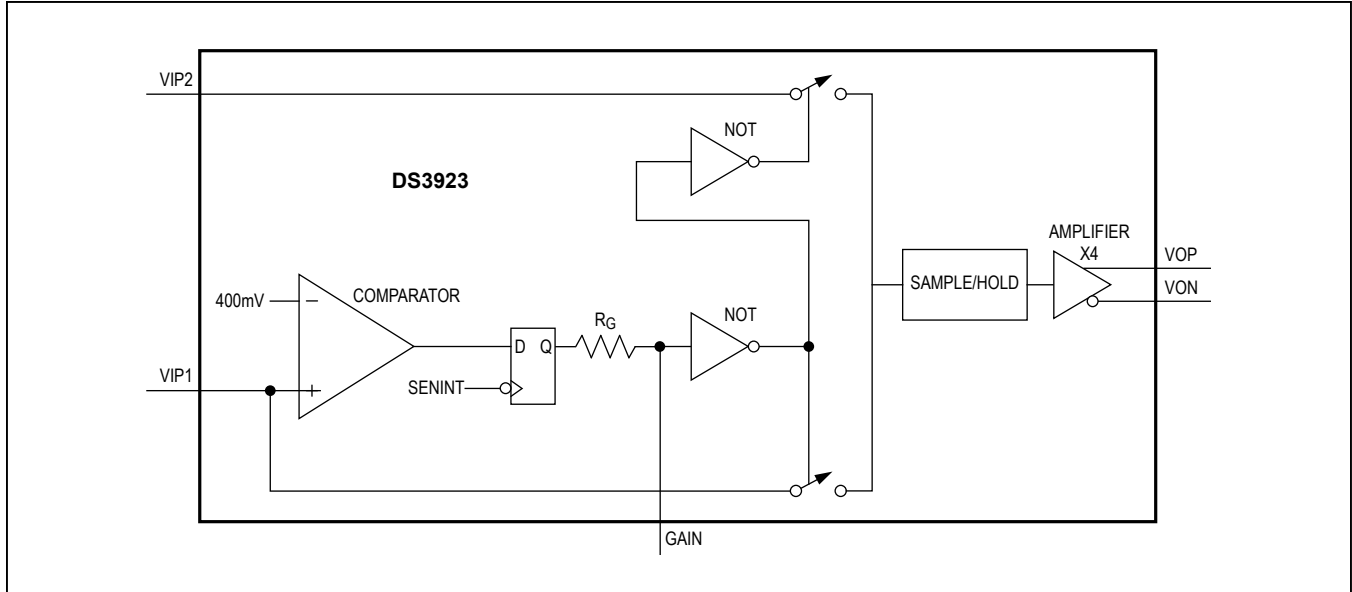


Figure 6. GAIN Selection Logic Diagram

Applications Information

Layout Considerations

Keeping all PCB traces as short as possible reduces radiated noise, stray capacitance, and trace resistance.

Ordering Information

| PART       | TEMP TANGE     | PIN-PACKAGE  |
|------------|----------------|--------------|
| DS3923T+   | -40°C to +95°C | 24-TQFN-EP** |
| DS3923T+T* | -40°C to +95°C | 24-TQFN-EP** |

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*First T denotes package type. Second T denotes Tape and reel.

\*\*EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 24 TQFN-EP   | T243A3+1     | <a href="#">21-0188</a> | <a href="#">90-0122</a> |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION   | PAGES CHANGED    |
|-----------------|---------------|---|------------------|
| 0               | 12/13         | Initial release   | —                |
| 1               | 8/14          | Notes added to <i>Pin Description</i> and <i>Discharge</i> section stating SENXOR should not be a logic-high if the discharge feature is being used.  | 8, 9, 12         |
| 2               | 3/15          | Revised recommended usage of HV FET. Revised <i>General Description</i> , <i>Features</i> , <i>Applications</i> , <i>Pin Description</i> , <i>Detailed Description</i> , and <i>Typical Application Circuit</i> . Updated the <i>Benefits and Features</i> section. | 1, 9, 10, 13, 14 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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#### Как с нами связаться

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