

128K x 24 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

JUNE 2005

FEATURES

- High-speed access time: 8, 10 ns
- CMOS low power operation
 - 756 mW (max.) operating @ 8 ns
 - 36 mW (max.) standby @ 8 ns
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Available in 119-pin Plastic Ball Grid Array (PBGA) and 100-pin TQFP packages.
- Industrial temperature available
- Lead-free available

DESCRIPTION

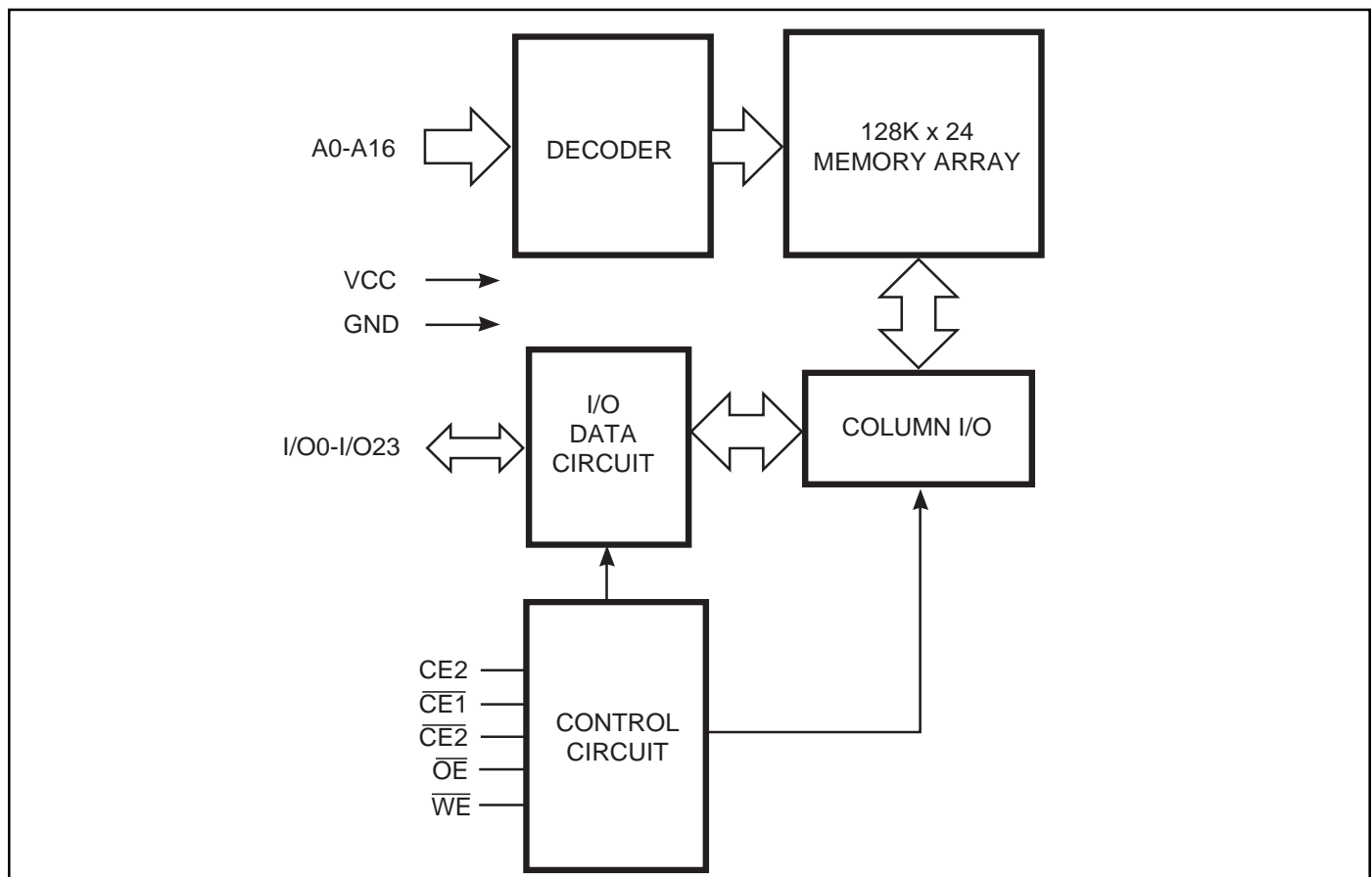
The *ISSI* IS61LV12824 is a high-speed, static RAM organized as 131,072 words by 24 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When $\overline{CE1}$, $\overline{CE2}$ are HIGH and CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE1}$, CE2, $\overline{CE2}$ and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS61LV12824 is packaged in the JEDEC standard 119-pin PBGA and 100-pin TQFP.

FUNCTIONAL BLOCK DIAGRAM



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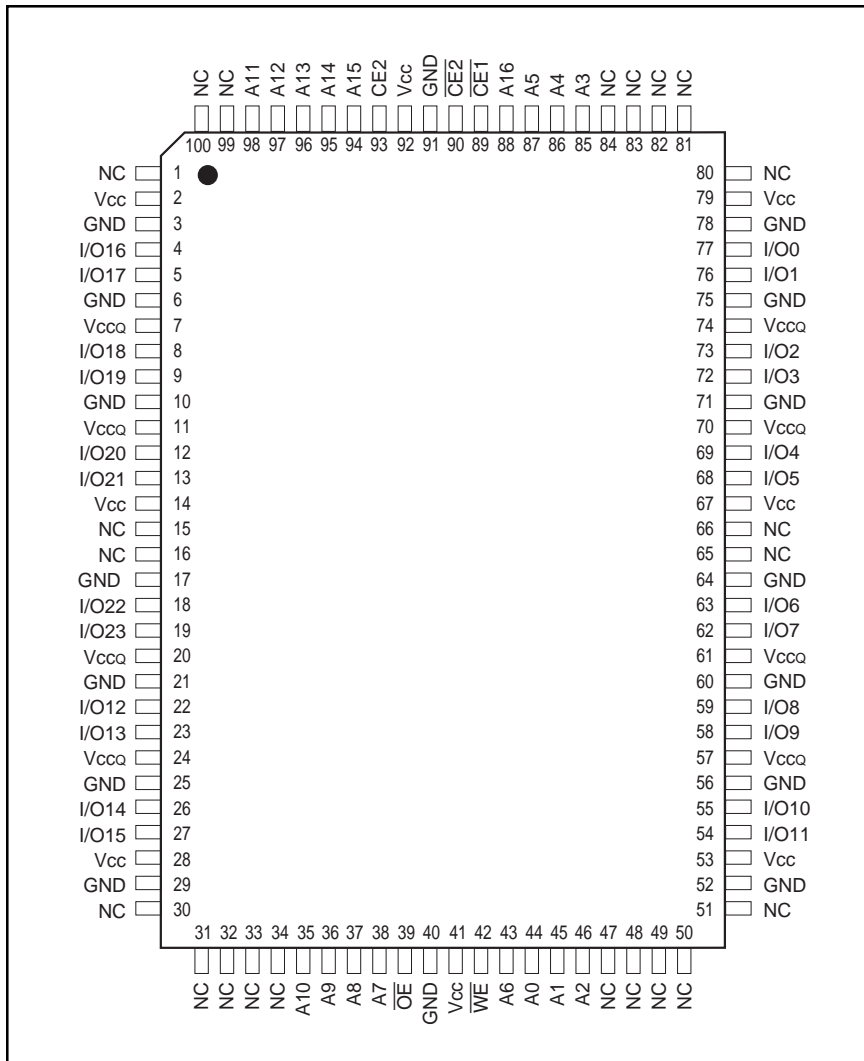
PIN CONFIGURATION - 119-pin PBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|------------------|-----------------|-------------------------|-------------------------|------------------|------------------|
| A | NC | A11 | A14 | A15 | A16 | A4 | NC |
| B | NC | A12 | A13 | $\overline{\text{CE1}}$ | A5 | A3 | NC |
| C | I/O16 | NC | CE2 | NC | $\overline{\text{CE2}}$ | NC | I/O0 |
| D | I/O17 | V _{ccq} | GND | GND | GND | V _{ccq} | I/O1 |
| E | I/O18 | GND | V _{cc} | GND | V _{cc} | GND | I/O2 |
| F | I/O19 | V _{ccq} | GND | GND | GND | V _{ccq} | I/O3 |
| G | I/O20 | GND | V _{cc} | GND | V _{cc} | GND | I/O4 |
| H | I/O21 | V _{ccq} | GND | GND | GND | V _{ccq} | I/O5 |
| J | V _{ccq} | GND | V _{cc} | GND | V _{cc} | GND | V _{ccq} |
| K | I/O22 | V _{ccq} | GND | GND | GND | V _{ccq} | I/O6 |
| L | I/O23 | GND | V _{cc} | GND | V _{cc} | GND | I/O7 |
| M | I/O12 | V _{ccq} | GND | GND | GND | V _{ccq} | I/O8 |
| N | I/O13 | GND | V _{cc} | GND | V _{cc} | GND | I/O9 |
| P | I/O14 | V _{ccq} | GND | GND | GND | V _{ccq} | I/O10 |
| R | I/O15 | NC | NC | NC | NC | NC | I/O11 |
| T | NC | A10 | A8 | $\overline{\text{WE}}$ | A0 | A1 | NC |
| U | NC | A9 | A7 | $\overline{\text{OE}}$ | A6 | A2 | NC |

PIN DESCRIPTIONS

| | |
|--|------------------------|
| A0-A16 | Address Inputs |
| I/O0-I/O23 | Data Inputs/Outputs |
| $\overline{\text{CE1}}, \overline{\text{CE2}}$ | Chip Enable Input LOW |
| CE2 | Chip Enable Input HIGH |
| $\overline{\text{OE}}$ | Output Enable Input |
| $\overline{\text{WE}}$ | Write Enable Input |
| NC | No Connection |
| V _{cc} | Power |
| V _{ccq} | I/O Power |
| GND | Ground |

PIN CONFIGURATION
100-Pin TQFP



PIN DESCRIPTIONS

| | |
|----------------------------------|------------------------|
| A0-A16 | Address Inputs |
| I/O0-I/O23 | Data Inputs/Outputs |
| $\overline{CE1}, \overline{CE2}$ | Chip Enable Input LOW |
| CE2 | Chip Enable Input HIGH |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| NC | No Connection |
| Vcc | Power |
| Vccq | I/O Power |
| GND | Ground |

TRUTH TABLE

| Mode | \overline{WE} | $\overline{CE1}$ | CE2 | $\overline{CE2}$ | \overline{OE} | I/O0-I/O23 | Vcc Current |
|-----------------|-----------------|------------------|-----|------------------|-----------------|------------|-------------|
| Not Selected | X | H | X | X | X | High-Z | ISB1, ISB2 |
| | X | X | L | X | X | | |
| | X | X | X | H | X | | |
| Output Disabled | H | L | H | L | H | High-Z | Icc |
| Read | H | L | H | L | L | DOUT | Icc |
| Write | L | L | H | L | X | DIN | Icc |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit | |
|--------|--------------------------------------|-------------------|-------------|----|
| VCC | Power Supply Voltage Relative to GND | -0.5 to 5.0 | V | |
| VTERM | Terminal Voltage with Respect to GND | -0.5 to Vcc + 0.5 | V | |
| TSTG | Storage Temperature | -65 to + 150 | °C | |
| TBIAS | Temperature Under Bias: | Com. | -10 to + 85 | °C |
| | | Ind. | -45 to + 90 | °C |
| PT | Power Dissipation | 2.0 | W | |
| IOUT | DC Output Current | ±20 | mA | |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

| Range | Ambient Temperature | Vcc (8 ns) | Vcc (10 ns) |
|------------|---------------------|------------------|-------------|
| Commercial | 0°C to +70°C | 3.3V + 10%, - 5% | 3.3V ± 10% |
| Industrial | -40°C to +85°C | 3.3V + 10%, - 5% | 3.3V ± 10% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|--------|----------------------------------|------------------------------------|------|-----------|------|
| VOH | Output HIGH Voltage | Vcc = Min., IOH = -4.0 mA | 2.4 | — | V |
| VOL | Output LOW Voltage | Vcc = Min., IOL = 8.0 mA | — | 0.4 | V |
| VIH | Input HIGH Voltage | | 2.2 | Vcc + 0.3 | V |
| VIL | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| ILI | Input Leakage | GND ≤ VIN ≤ Vcc | -1 | 1 | µA |
| ILO | Output Leakage | GND ≤ VOUT ≤ Vcc, Outputs Disabled | -1 | 1 | µA |

Note:

1. VIL (min.) = -0.3V DC; VIL (min.) = -2.0V AC (pulse width ≤ 2.0 ns).
VIH (max.) = Vcc + 0.3V DC; VIH (max.) = Vcc + 2.0V AC (pulse width ≤ 2.0 ns).

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | -8 ns | | -10 ns | | Unit |
|------------------|--|--|--------------|-----------------|-----------------|-----------------|------|
| | | | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{CC} Dynamic Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. Ind. | — 210 240 | — 180 210 | — 180 210 | mA |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , f = max. CE1, CE2, ≥ V _{IH} , CE2 ≤ V _{IL} | Com. Ind. | — 70 80 | — 50 55 | — 50 55 | mA |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{CC} = Max., CE1, CE2 ≥ V _{CC} - 0.2V, CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. Ind. | — 10 20 | — 10 20 | — 10 20 | mA |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 2 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

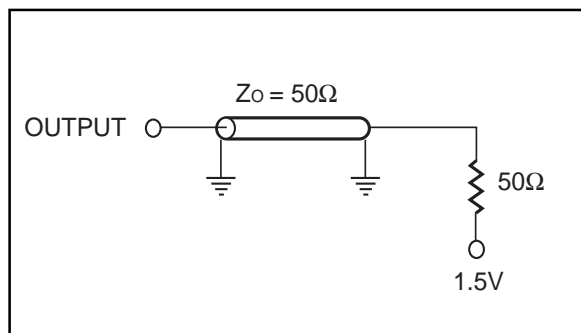
AC TEST LOADS

Figure 1

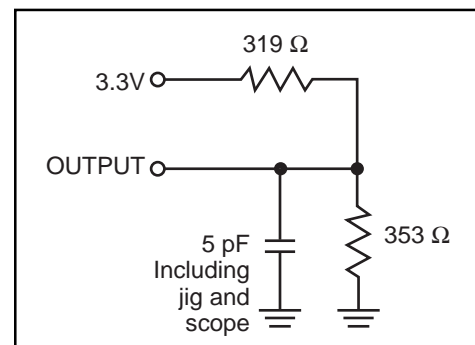


Figure 2

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

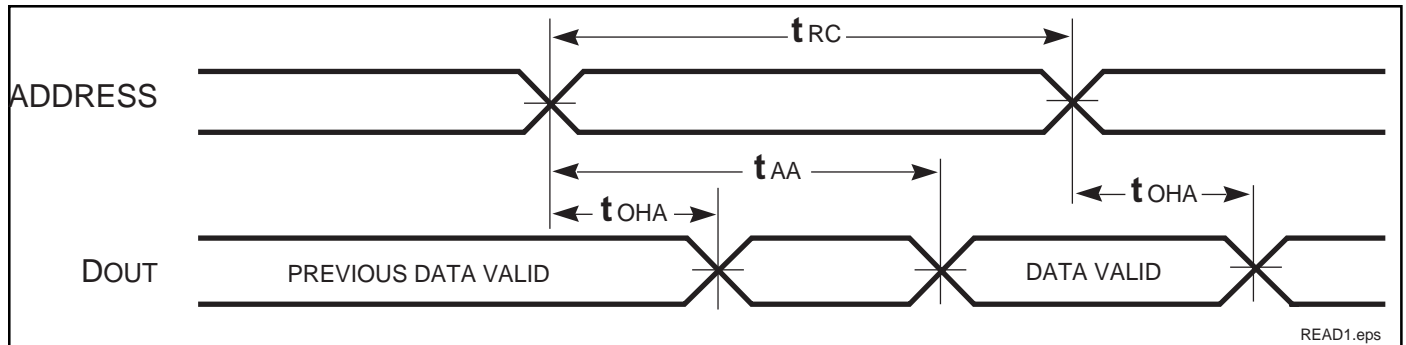
| Symbol | Parameter | -8 | | -10 | | Unit |
|----------------------------------|--|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | ns |
| t _{OH} | Output Hold Time | 3 | — | 3 | — | ns |
| t _{ACE} | $\overline{CE1}$, $\overline{CE2}$ Access Time | 8 | — | — | 10 | ns |
| t _{ACE2} | CE2 Access Time | | | | | |
| t _{DOE} | \overline{OE} Access Time | — | 4 | — | 4 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | 0 | 3 | 0 | 3 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | 0 | — | ns |
| t _{HZCE⁽²⁾} | $\overline{CE1}$, $\overline{CE2}$ to High-Z Output | 0 | 4 | 0 | 5 | ns |
| t _{HZCE2⁽²⁾} | CE2 to High-Z Output | | | | | |
| t _{LZCE⁽²⁾} | \overline{CE} , $\overline{CE2}$ to Low-Z Output | 3 | — | 3 | — | ns |
| t _{LZCE2⁽²⁾} | CE2 to Low-Z Output | | | | | |

Notes:

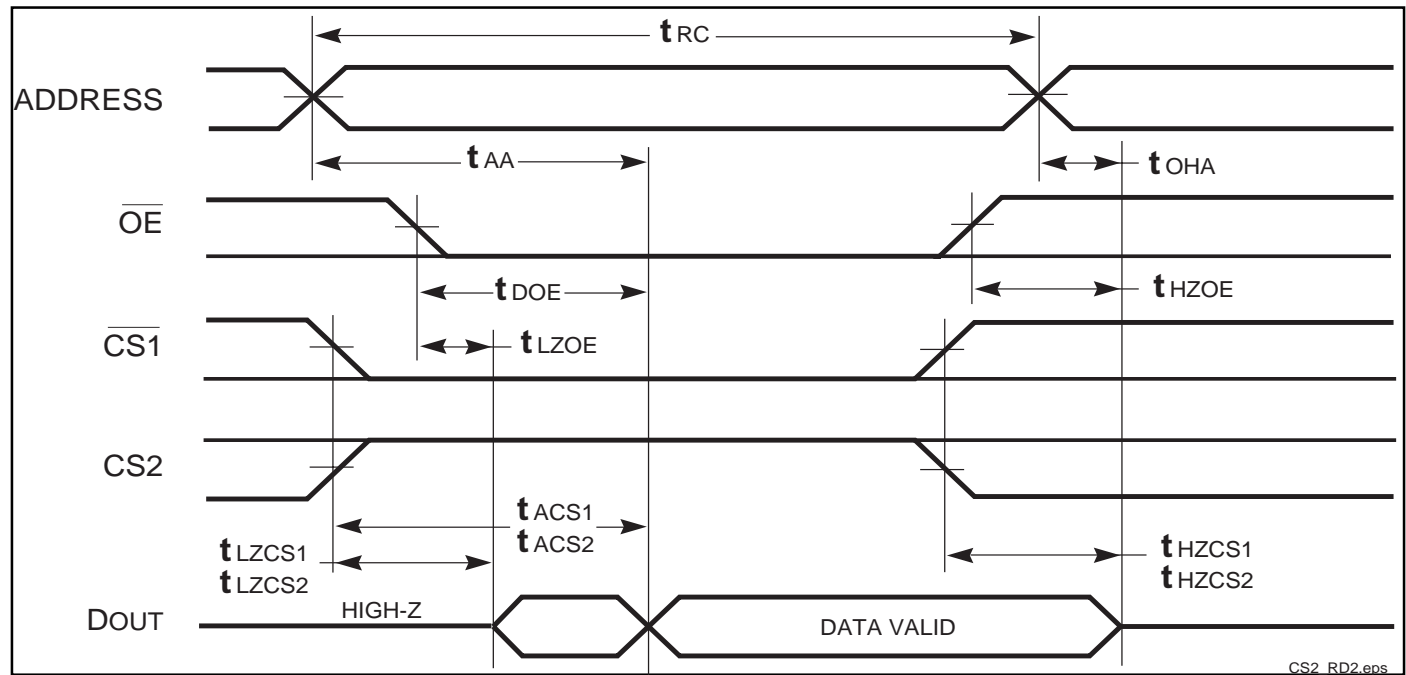
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 200 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE1} = \overline{CE2} = \overline{OE} = V_{IL}$; $CE2 = V_{IH}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE1}$, $\overline{CE2} = V_{IL}$. $CE2 = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CE1}$, $\overline{CE2}$ LOW and $CE2$ HIGH transition.

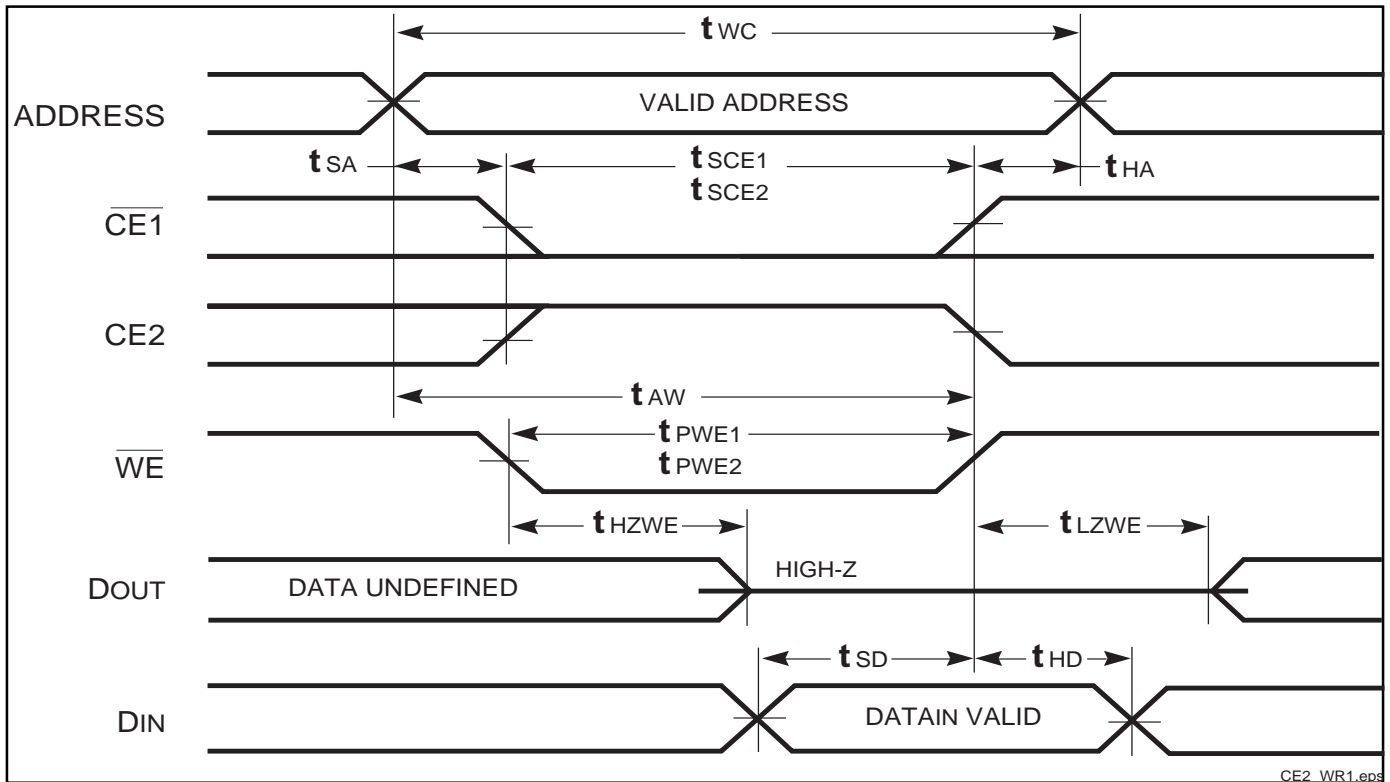
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|----------------------------------|---|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | ns |
| t _{SCE} | $\overline{CE1}$, $\overline{CE2}$ to Write End | 7 | — | 8 | — | ns |
| t _{SCE2} | CE2 to Write End | 7 | — | 8 | — | ns |
| t _{AW} | Address Setup Time to Write End | 7 | — | 8 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 6 | — | 8 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 6 | — | 9 | — | ns |
| t _{SD} | Data Setup to Write End | 4.5 | — | 5 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| t _{HZWE} ⁽²⁾ | \overline{WE} LOW to High-Z Output | — | 3.5 | — | 3.5 | ns |
| t _{LZWE} ⁽²⁾ | \overline{WE} HIGH to Low-Z Output | 3 | — | 3 | — | ns |

Notes:

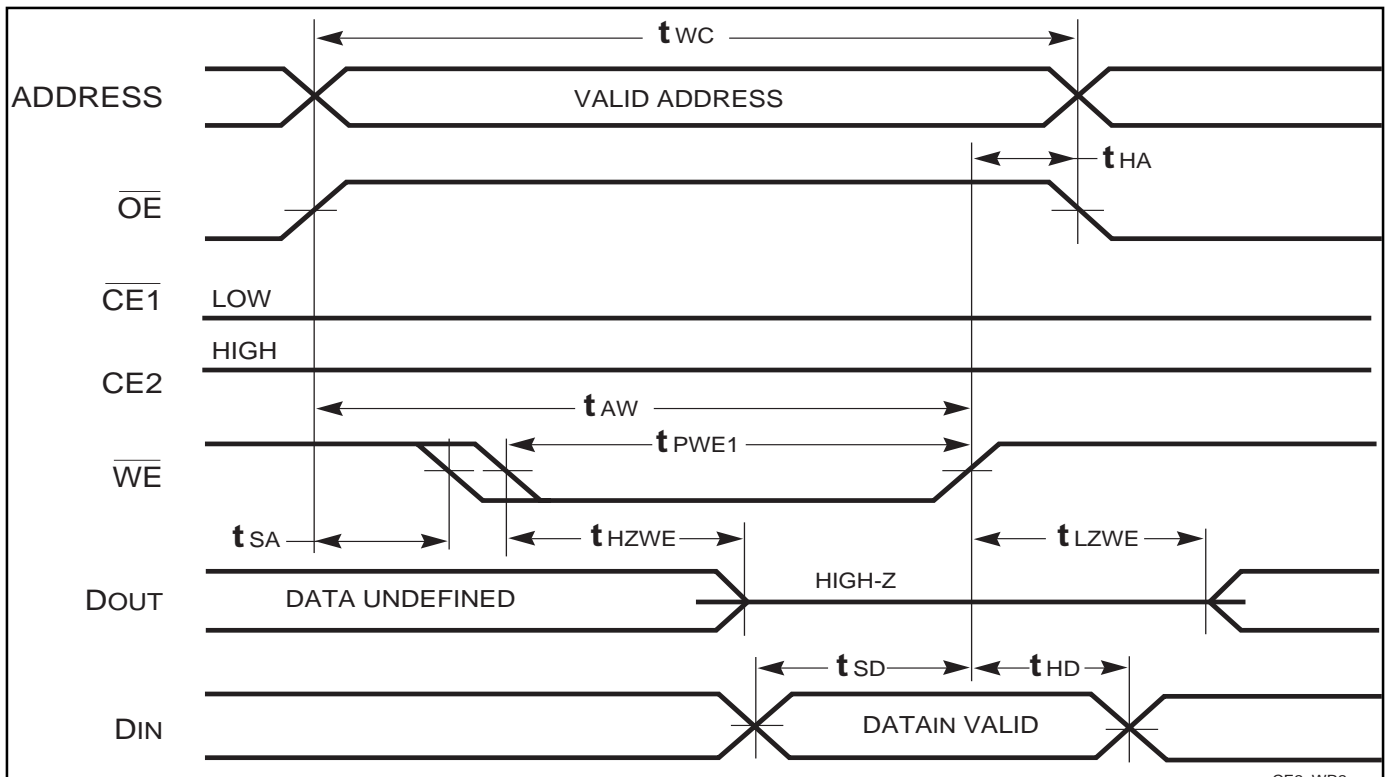
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 200 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$, $\overline{CE2}$ LOW, CE2 HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

WRITE CYCLE NO. 1 (\overline{CE} Controlled, $\overline{OE} = \text{HIGH or LOW}$)

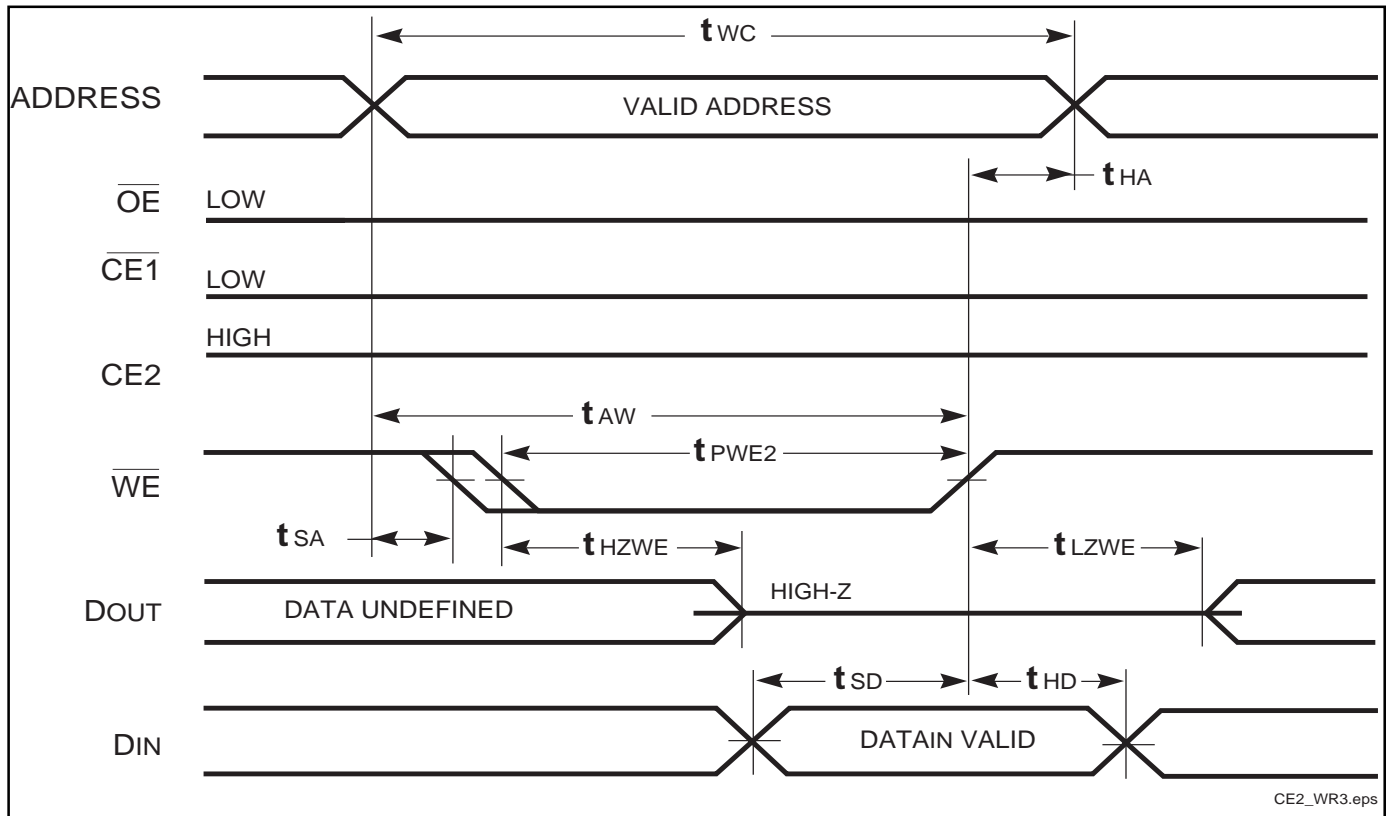


CE2_WR1.eps

WRITE CYCLE NO. 2⁽¹⁾ (\overline{WE} Controlled: $\overline{OE} = \text{HIGH during Write Cycle}$)



CE2_WR2.eps

WRITE CYCLE NO. 3⁽¹⁾ (\overline{WE} Controlled: \overline{OE} is LOW DURING WRITE CYCLE)**Note:**

1. The internal Write time is defined by the overlap of $\overline{CE1}$ and $\overline{CE2} = \text{LOW}$, $\overline{CE2} = \text{HIGH}$ and $\overline{WE} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

| Speed (ns) | Order Part No. | Package |
|------------|------------------|------------------------------------|
| 8 | IS61LV12824-8B | Plastic Ball Grid Array |
| | IS61LV12824-8BL | Plastic Ball Grid Array, Lead-free |
| | IS61LV12824-8TQ | TQFP |
| 10 | IS61LV12824-10B | Plastic Ball Grid Array |
| | IS61LV12824-10BL | Plastic Ball Grid Array, Lead-free |
| | IS61LV12824-10TQ | TQFP |

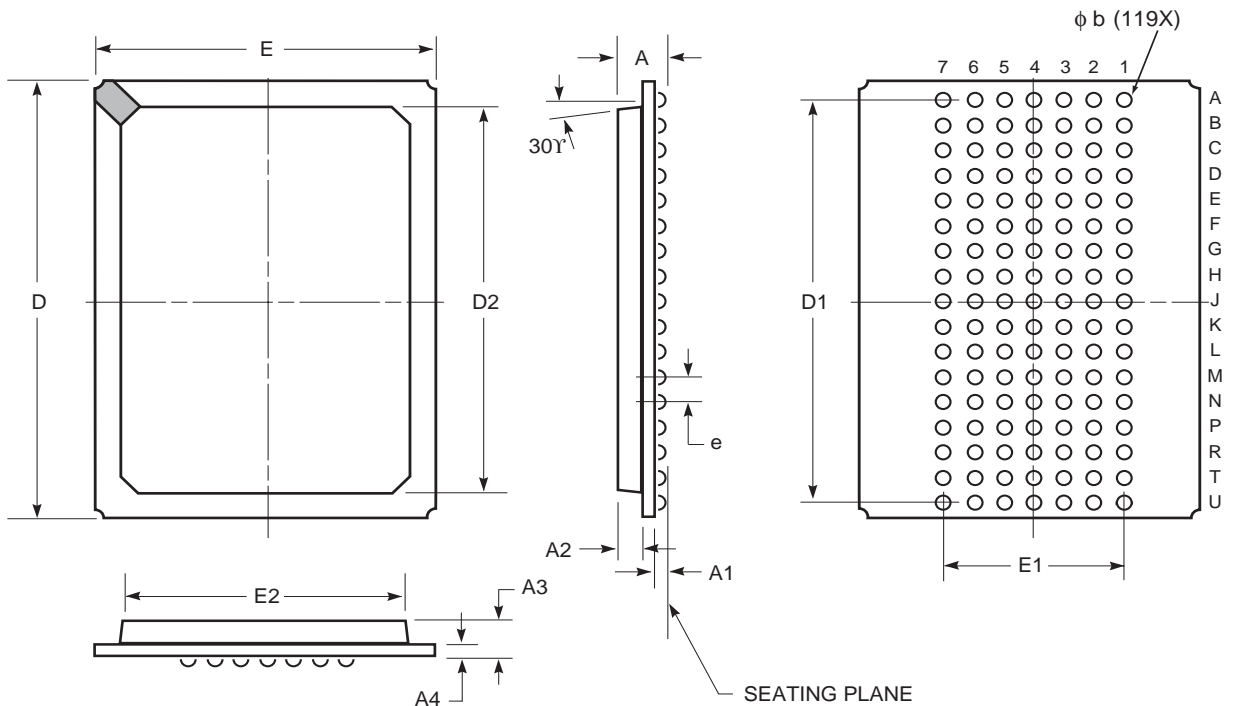
Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|--------------------|-------------------------|
| 8 | IS61LV12824-8BI | Plastic Ball Grid Array |
| 10 | IS61LV12824-10BI | Plastic Ball Grid Array |
| | IS61LV12824-10TQI | TQFP |
| | IS61LV12824-10TQLI | TQFP, Lead-free |

PACKAGING INFORMATION



Plastic Ball Grid Array Package Code: B (119-pin)



| | MILLIMETERS | | INCHES | |
|--------------|-------------|-------|-----------|-------|
| Sym. | Min. | Max. | Min. | Max. |
| N0. Leads | 119 | | | |
| A | — | 2.41 | — | 0.095 |
| A1 | 0.50 | 0.70 | 0.020 | 0.028 |
| A2 | 0.80 | 1.00 | 0.032 | 0.039 |
| A3 | 1.30 | 1.70 | 0.051 | 0.067 |
| A4 | 0.56 BSC | | 0.022 BSC | |
| b | 0.60 | 0.90 | 0.024 | 0.035 |
| D | 21.80 | 22.20 | 0.858 | 0.874 |
| D1 | 20.32 BSC | | 0.800 BSC | |
| D2 | 19.40 | 19.60 | 0.764 | 0.772 |
| E | 13.80 | 14.20 | 0.543 | 0.559 |
| E1 | 7.62 BSC | | 0.300 BSC | |
| E2 | 11.90 | 12.10 | 0.469 | 0.476 |
| e | 1.27 BSC | | 0.050 BSC | |

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC=Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

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Rev. B
02/12/03

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



| Thin Quad Flat Pack (TQ) | | | | | | | | | |
|--------------------------|-------------|-------|------------|-------|-----------|-------------|------------|--------|-----|
| Symbol | Millimeters | | Inches | | Symbol | Millimeters | | Inches | |
| | Min | Max | Min | Max | | Min | Max | Min | Max |
| Ref. Std. | | | | | | | | | |
| No. Leads (N) | 100 | | | | 128 | | | | |
| A | — | 1.60 | — | 0.063 | — | 1.60 | — | 0.063 | |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | |
| A2 | 1.35 | 1.45 | 0.053 | 0.057 | 1.35 | 1.45 | 0.053 | 0.057 | |
| b | 0.22 | 0.38 | 0.009 | 0.015 | 0.17 | 0.27 | 0.007 | 0.011 | |
| D | 21.90 | 22.10 | 0.862 | 0.870 | 21.80 | 22.20 | 0.858 | 0.874 | |
| D1 | 19.90 | 20.10 | 0.783 | 0.791 | 19.90 | 20.10 | 0.783 | 0.791 | |
| E | 15.90 | 16.10 | 0.626 | 0.634 | 15.80 | 16.20 | 0.622 | 0.638 | |
| E1 | 13.90 | 14.10 | 0.547 | 0.555 | 13.90 | 14.10 | 0.547 | 0.555 | |
| e | 0.65 BSC | | 0.026 BSC | | 0.50 BSC | | 0.020 BSC | | |
| L | 0.45 | 0.75 | 0.018 | 0.030 | 0.45 | 0.75 | 0.018 | 0.030 | |
| L1 | 1.00 REF. | | 0.039 REF. | | 1.00 REF. | | 0.039 REF. | | |
| C | 0° | 7° | 0° | 7° | 0° | 7° | 0° | 7° | |

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.

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[IS61LV12824-10TQ](#) [IS61LV12824-10TQI](#) [IS61LV12824-10TQI-TR](#) [IS61LV12824-10TQLI](#) [IS61LV12824-10TQ-TR](#)
[IS61LV12824-8TQ](#) [IS61LV12824-8TQ-TR](#) [IS61LV12824-8BL](#) [IS61LV12824-8BL-TR](#)



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