



FSDM0465RS

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged SenseFET
- Advanced Burst-Mode operation consumes under 1 W at 240V_{AC} & 0.5W load
- Precision Fixed Operating Frequency (66kHz)
- Internal Start-up Circuit
- Improved Pulse-by-Pulse Current Limiting
- Over-Voltage Protection (OVP)
- Overload Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Abnormal Over-Current Protection (AOCP)
- Auto-Restart Mode
- Under-Voltage Lock Out (UVLO) with hysteresis
- Low Operating Current (2.5mA)
- Built-in Soft-Start

Applications

- SMPS for LCD monitor and STB
- Adaptor

Description

The FSDM0465RS is an integrated Pulse Width Modulator (PWM) and SenseFET specifically designed for high-performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage power-switching regulator that combines an avalanche rugged SenseFET with a current mode PWM control block. The PWM controller includes integrated fixed frequency oscillator, under-voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise-current sources for a loop compensation and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight; while simultaneously increasing efficiency, productivity and system reliability. This device is a basic platform well suited for cost effective designs of flyback converters.

Ordering Information

| Product Number | Package | Marking Code | BV _{DSS} | R _{DS(ON)} Max. |
|-------------------------------|------------------------------------|--------------|-------------------|--------------------------|
| FSDM0465RSWDTU ⁽¹⁾ | TO-220F-6L(Forming) ⁽²⁾ | DM0465RS | 650V | 2.6 Ω |

Note:

1. WDTU: Forming Type.
2. Pb-free package per JEDEC J-STD-020B.

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Internal Block Diagram

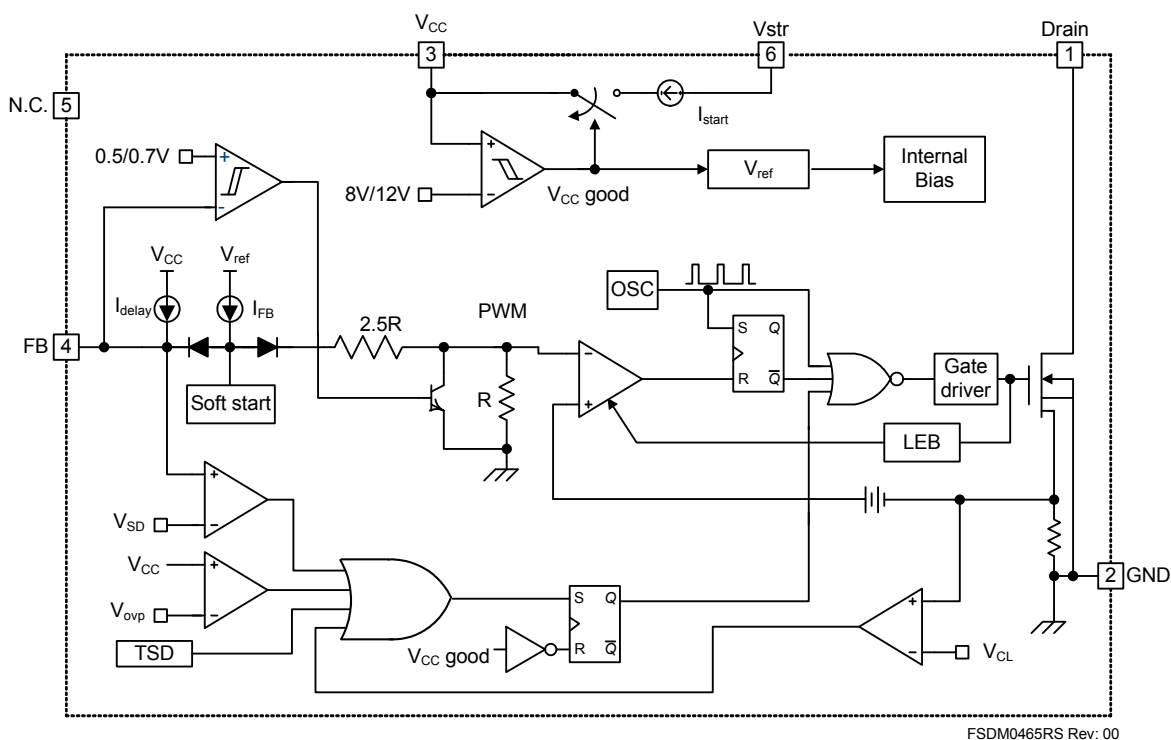


Figure 2. Functional Block Diagram of FSDM0465RS

Pin Configuration

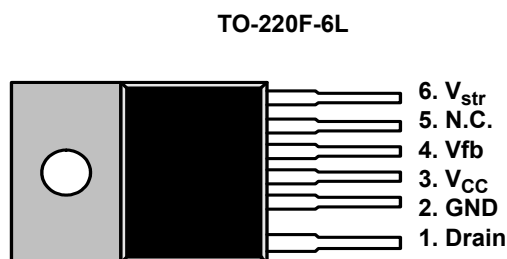


Figure 3. Pin Configuration (Top View)

Pin Definitions

| Pin # | Name | Description |
|-------|-----------|--|
| 1 | Drain | SenseFET drain. High-voltage power SenseFET drain connection. |
| 2 | GND | Ground. This pin is the control ground and the SenseFET source. |
| 3 | V_{CC} | Power Supply. This pin is the positive supply input, providing internal operating current for both start-up and steady-state operation. |
| 4 | V_{fb} | Feedback. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the FPS. |
| 5 | N.C. | No Connection. |
| 6 | V_{str} | Start-up. This pin is connected directly, or through a resistor, to the high-voltage DC link. At start-up, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source is disabled. It is not recommended to connect V_{str} and Drain together. |

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

$T_A = 25^\circ\text{C}$, unless otherwise specified.

| Symbol | Parameter | Value | Unit |
|------------------------|--|--------------------------------|------------------|
| BV_{DSS} | Drain Source Breakdown Voltage | 650 | V |
| V_{STR} | Vstr Max. Voltage | 650 | V |
| I_{DM} | Drain Current Pulsed ⁽⁷⁾ | $T_c=25^\circ\text{C}$ 9.6 | A_{DC} |
| I_D | Continuous Drain Current ⁽⁸⁾ | $T_c=25^\circ\text{C}$ 2.2 | A_{RMS} |
| | | $T_c=100^\circ\text{C}$ 1.4 | A_{RMS} |
| E_{AS} | Single Pulsed Avalanche Energy ⁽⁹⁾ | 120 | mJ |
| V_{CC} | Supply Voltage | 20 | V |
| V_{FB} | Input Voltage Range | -0.3 to 12 | V |
| $P_D(\text{Watt H/S})$ | Total Power Dissipation ($T_c=25^\circ\text{C}$) | 45 | W |
| T_j | Operating Junction Temperature | Internally limited | $^\circ\text{C}$ |
| T_A | Operating Ambient Temperature | -25 to +85 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | -55 to +150 | $^\circ\text{C}$ |
| ESD | ESD Capability, HBM Model (All pins excepts for Vstr and Vfb) | 2.0 (GND-Vstr/Vfb=1.5kV) | kV |
| | ESD Capability, Charged Device Model | 1.0 | kV |

Notes:

7. Repetitive rating: Pulse width limited by maximum junction temperature.
8. This value is RMS current rating which should not be confused by the switching current.
9. $L=14\text{mH}$, starting $T_j=25^\circ\text{C}$.

Thermal Impedance

$T_A=25^\circ\text{C}$, unless otherwise specified.

| Symbol | Parameter | Value | Unit |
|----------------------|-----------------------------|-------|--------------------|
| $\theta_{JA}^{(10)}$ | Junction-to-Ambient Thermal | 50 | $^\circ\text{C/W}$ |
| $\theta_{JC}^{(11)}$ | Junction-to-Case Thermal | 2.78 | $^\circ\text{C/W}$ |

Notes:

10. Free standing with no heat-sink under natural convection.
11. Infinite cooling condition - Refer to the SEMI G30-88.

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------------------|---|--|------|------|------|------|
| SenseFET SECTION | | | | | | |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 650V, V _{GS} = 0V | | | 250 | μA |
| | | V _{DS} = 520V, V _{GS} = 0V, T _C = 125°C | | | 250 | μA |
| R _{DS(ON)} | Static Drain Source on Resistance ⁽¹²⁾ | V _{GS} = 10V, I _D = 2.5A | | 2.2 | 2.6 | Ω |
| C _{OSS} | Output Capacitance | V _{GS} = 0V, V _{DS} = 25V, f = 1MHz | | 60 | | pF |
| t _{d(on)} | Turn-on Delay Time | V _{DD} = 325V, I _D = 5A | | 23 | | ns |
| t _r | Rise Time | | | 20 | | |
| t _{d(off)} | Turn-off Delay Time | | | 65 | | |
| t _f | Fall Time | | | 27 | | |
| CONTROL SECTION | | | | | | |
| f _{OSC} | Switching Frequency | V _{FB} = 3V | 60 | 66 | 72 | kHz |
| Δf _{STABLE} | Switching Frequency Stability | 13V ≤ V _{CC} ≤ 18V | 0 | 1 | 3 | % |
| Δf _{OSC} | Switching Frequency Variation ⁽¹³⁾ | -25°C ≤ T _A ≤ 85°C | 0 | ±5 | ±10 | % |
| I _{FB} | Feedback Source Current | V _{FB} = GND | 0.7 | 0.9 | 1.1 | mA |
| D _{MAX} | Maximum Duty Cycle | | 77 | 82 | 87 | % |
| D _{MIN} | Minimum Duty Cycle | | | | 0 | % |
| V _{START} | UVLO Threshold Voltage | V _{FB} = GND | 11 | 12 | 13 | V |
| V _{STOP} | | V _{FB} = GND | 7 | 8 | 9 | V |
| t _{S/S} | Internal Soft-start Time | V _{fb} = 3V | | 10 | 15 | ms |
| BURST MODE SECTION | | | | | | |
| V _{BURH} | Burst Mode Voltages | V _{CC} = 14V | | 0.7 | | V |
| V _{BURL} | | V _{CC} = 14V | | 0.5 | | V |
| PROTECTION SECTION | | | | | | |
| V _{SD} | Shutdown Feedback Voltage | V _{FB} ≥ 5.5V | 5.5 | 6.0 | 6.5 | V |
| I _{DELAY} | Shutdown Delay Current | V _{FB} = 5V | 2.8 | 3.5 | 4.2 | μA |
| t _{LEB} | Leading Edge Blanking Time ⁽¹³⁾ | | | 250 | | ns |
| I _{LIMIT} | Peak Current Limit ⁽¹⁴⁾ | V _{FB} = 5V, V _{CC} = 14V | 1.6 | 1.8 | 2.0 | A |
| V _{OVP} | Over-Voltage Protection | | 18 | 19 | 20 | V |
| T _{SD} | Thermal Shutdown Temperature ⁽¹³⁾ | | 130 | 145 | 160 | °C |
| TOTAL DEVICE SECTION | | | | | | |
| I _{START} | Operating Supply Current ⁽¹⁵⁾ | V _{FB} = GND, V _{CC} = 11V | | 1 | 1.3 | mA |
| I _{OP} | Operating Supply Current ⁽¹⁵⁾ | V _{FB} = GND, V _{CC} = 14V | | 2.5 | 5 | mA |
| I _{OP(MIN)} | | V _{FB} = GND, V _{CC} = 10V | | | | |
| I _{OP(MAX)} | | V _{FB} = GND, V _{CC} = 18V | | | | |

Notes:

12. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty $\leq 2\%$
13. These parameters, although guaranteed at the design, are not tested in mass production.
14. These parameters indicate the inductor current.
15. This parameter is the current flowing into the control IC.

Comparison Between FS6M07652RTC and FSDM0465RS

| Function | FS6M07652RTC | FSDM0465RS | FSDM0465RS Advantages |
|----------------------|--|---|---|
| Soft-Start | Adjustable soft-start time using an external capacitor | Internal soft-start with typically 10ms (fixed) | <ul style="list-style-type: none"> ■ Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses ■ Eliminates external components used for soft-start in most applications ■ Reduces or eliminates output overshoot |
| Burst Mode Operation | <ul style="list-style-type: none"> ■ Built into controller ■ Output voltage drops to around half | <ul style="list-style-type: none"> ■ Built into controller ■ Output voltage fixed | <ul style="list-style-type: none"> ■ Improve light load efficiency ■ Reduces no-load consumption |

Typical Performance Characteristics

(These Characteristic Graphs are Normalized at $T_A = 25^\circ\text{C}$.)

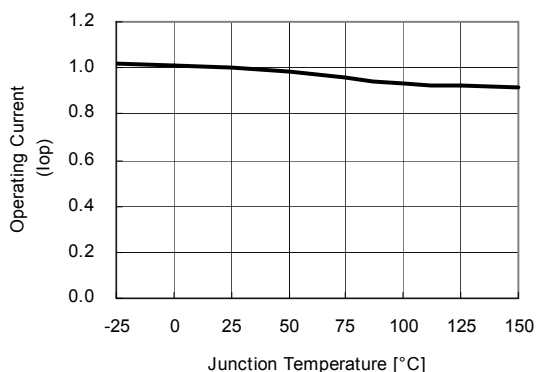


Figure 4. Operating Current vs. Temp.

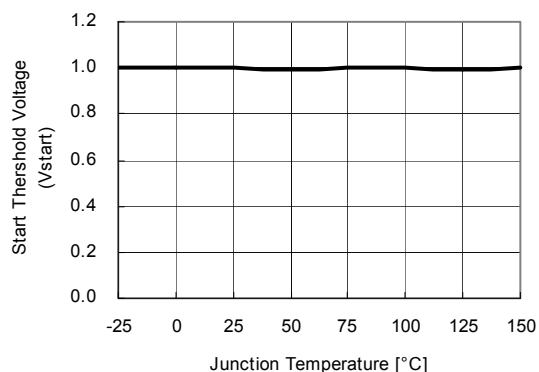


Figure 5. Start Threshold Voltage vs. Temp.

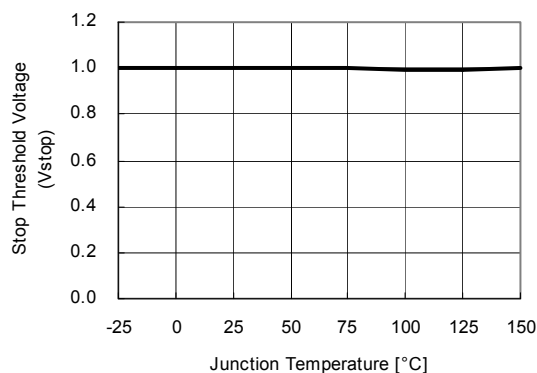


Figure 6. Stop Threshold Voltage vs. Temp.

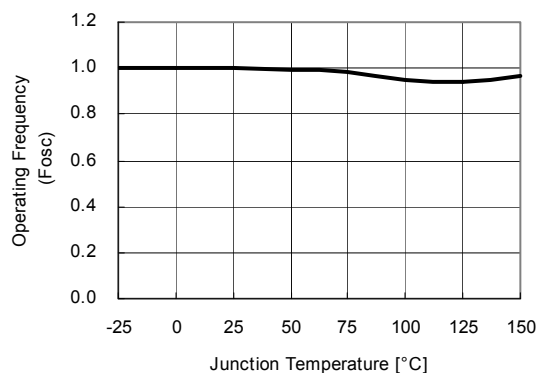


Figure 7. Operating Frequency vs. Temp.

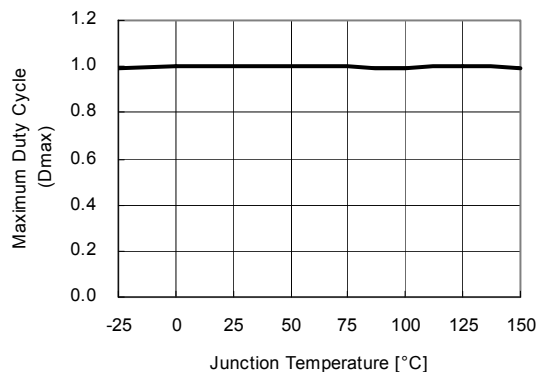


Figure 8. Maximum Duty vs. Temp.

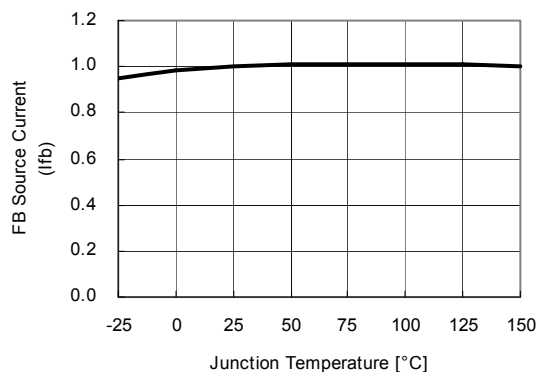


Figure 9. Feedback Source Current vs. Temp.

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at $T_A = 25^\circ\text{C}$.)

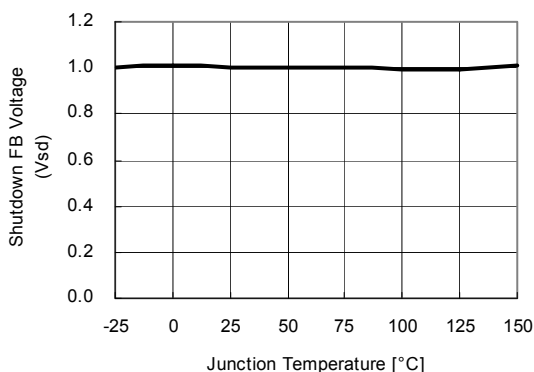


Figure 10. Shutdown Feedback Voltage vs. Temp.

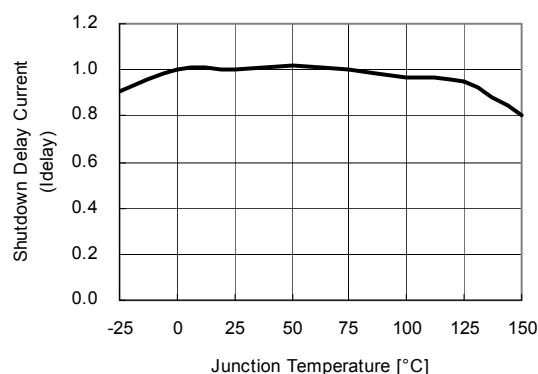


Figure 11. Shutdown Delay Current vs. Temp.

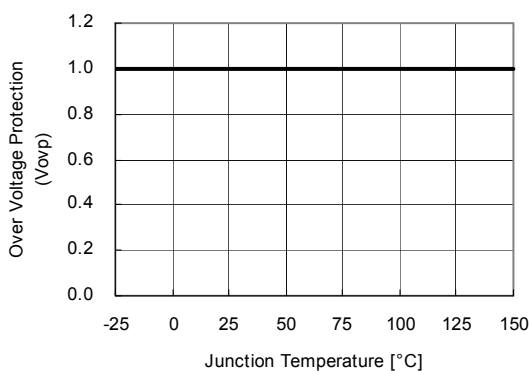


Figure 12. Over-Voltage Protection vs. Temp.

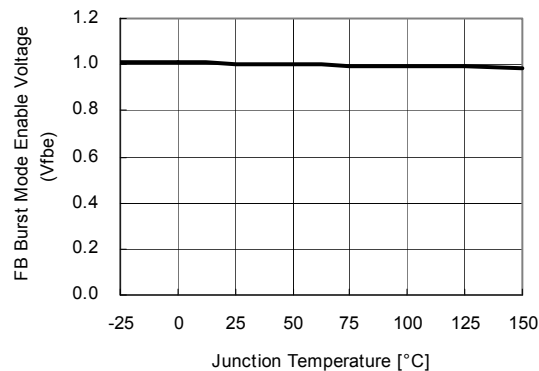


Figure 13. Burst Mode Enable Voltage vs. Temp.

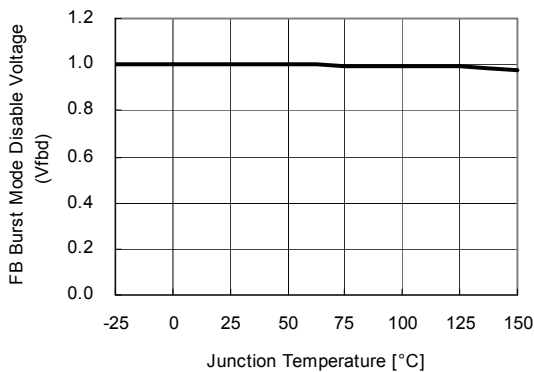


Figure 14. Burst Mode Disable Voltage vs. Temp.

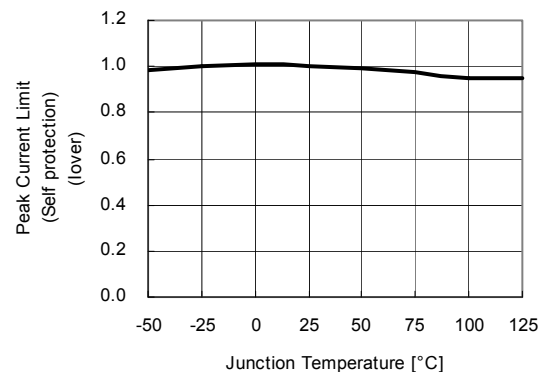
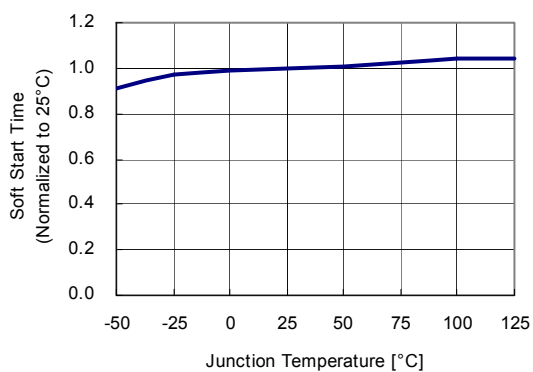


Figure 15. Current Limit vs. Temp.

Typical Performance Characteristics (Continued)(These Characteristic Graphs are Normalized at $T_A = 25^\circ\text{C}$.)**Figure 16. Soft-Start Time vs. Temp.**

Functional Description

1. Startup: In previous generations of Fairchild Power Switches (FPS™) the V_{CC} pin had an external start-up resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high-voltage current source. At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_{VCC}) that is connected to the V_{CC} pin as illustrated in Figure 17. When V_{CC} reaches 12V, the FSDM0465RS begins switching and the internal high-voltage current source is disabled. Then, the FSDM0465RS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

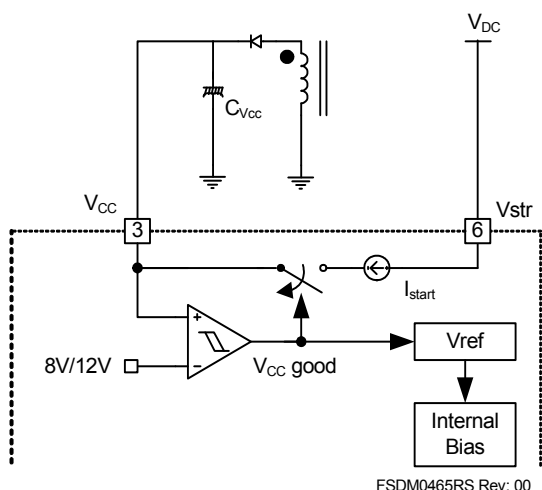


Figure 17. Internal startup circuit

2. Feedback Control: FSDM0465RS employs current mode control, as shown in Figure 18. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor plus an offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

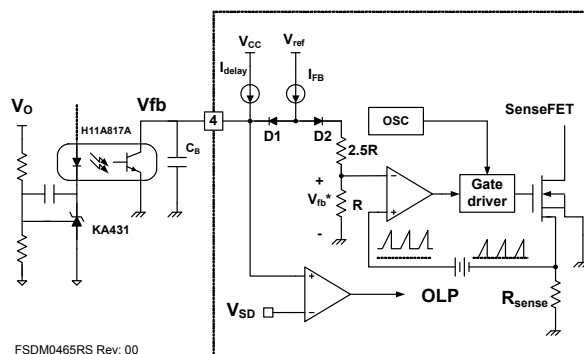


Figure 18. Pulse width modulation (PWM) circuit

2.1 Pulse-by-Pulse Current Limit: Because current mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{fb}^*) as shown in Figure 18. Assuming that the 0.9mA current source flows only through the internal resistor ($2.5R + R = 2.8k\Omega$), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (V_{fb}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping V_{fb}^* . Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, there usually exists a high-current spike through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSDM0465RS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

3. Protection Circuit: The FSDM0465RS has several self protective functions such as overload protection (OLP), over-voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost. Once the fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage, 8V, the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the Vstr pin. When V_{CC} reaches the UVLO start voltage, 12V, the FSDM0465RS resumes its normal operation. In this manner, the auto-restart can alternately enable and

disable the switching of the power SenseFET until the fault condition is eliminated (see Figure 19).

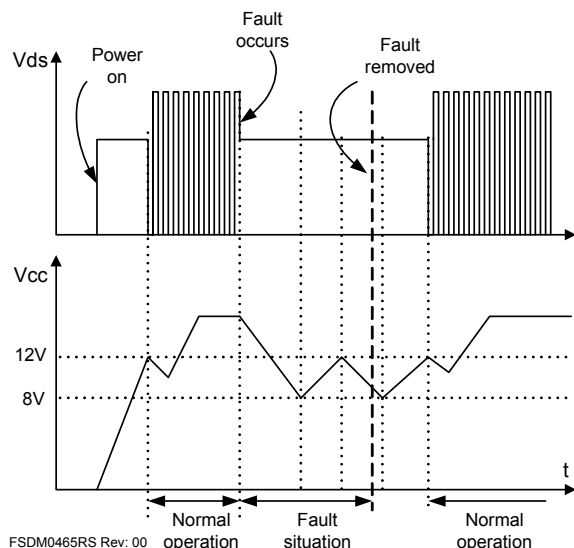


Figure 19. Auto restart operation

3.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be activated during the load transition. To avoid this undesired operation, the overload protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{fb}). If V_{fb} exceeds 2.5V, D1 is blocked and the 3.5 μ A current source starts to charge C_B slowly up to V_{CC} . In this condition, V_{fb} continues increasing until it reaches 6V, when the switching operation is terminated as shown in Figure 20. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 3.5 μ A. In general, a 10 ~ 50 ms delay time is typical for most applications.

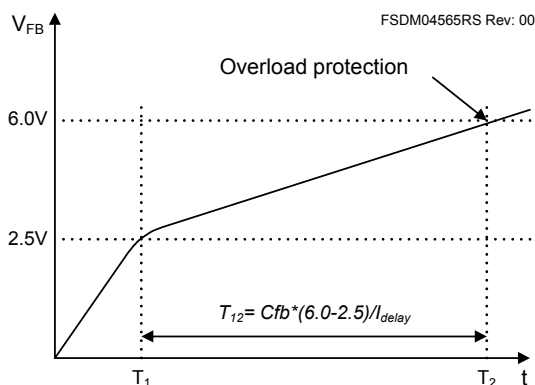


Figure 20. Overload protection

3.2 Over-voltage Protection (OVP): If the secondary side feedback circuit were to malfunction or a solder defect caused an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, V_{fb} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an over-voltage protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FSDM0465RS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 19V.

3.3 Thermal Shutdown (TSD): The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the SenseFET. When the temperature exceeds approximately 150°C, the thermal shutdown is activated.

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FPS has overload protection, it is not enough to protect the FPS in those abnormal cases, since severe current stress is imposed on the SenseFET until OLP triggers. This IC has an internal AOCP circuit shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is

greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

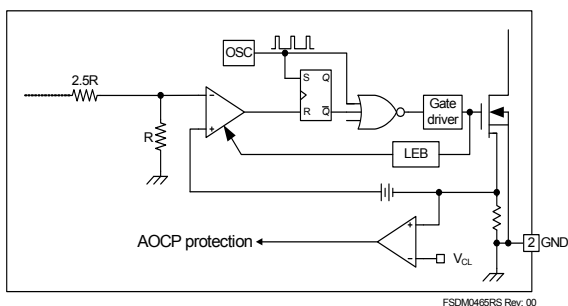


Figure 21. Abnormal Over-Current Protection

4. Soft-Start: The FSDM0465RS has an internal soft-start circuit that increases PWM comparator inverting input voltage together with the SenseFET current slowly after it starts up. The typical soft-start time is 10msec, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

5. Burst operation: To minimize power dissipation in standby mode, the FSDM0465RS enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 22, the device automatically enters burst mode when the feedback voltage drops below $V_{BURL}(500mV)$. At this point switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes $V_{BURH}(700mV)$ switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power SenseFET thereby reducing switching loss in Standby mode.

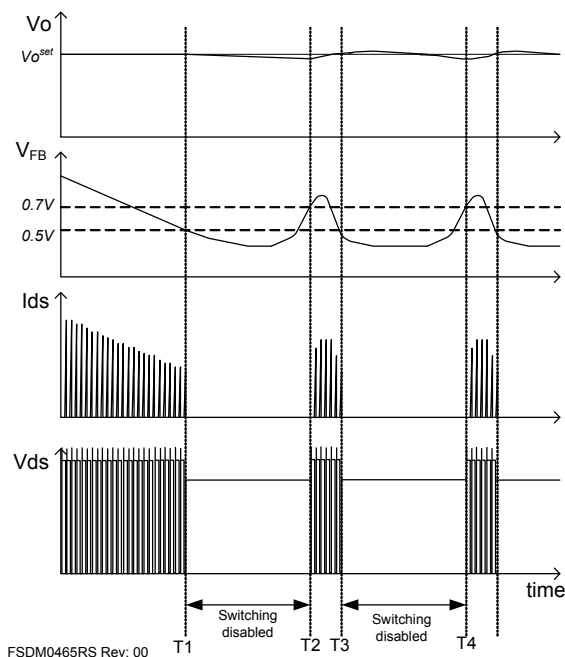


Figure 22. Waveforms of Burst Operation

2. Transformer

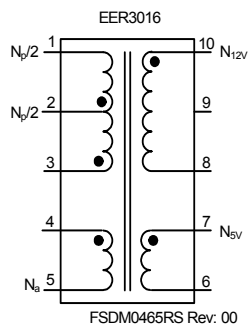


Figure 24. Transformer Schematic Diagram

3.Winding Specification

| No | Pin (s→f) | Wire | Turns | Winding Method |
|--|-----------|---------------------|-------|------------------|
| Na | 4 → 5 | $0.2^\phi \times 1$ | 8 | Center Winding |
| Insulation: Polyester Tape t = 0.050mm, 2 Layers | | | | |
| $N_{p/2}$ | 2 → 1 | $0.4^\phi \times 1$ | 18 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.050mm, 2 Layers | | | | |
| N_{12V} | 10 → 8 | $0.3^\phi \times 3$ | 7 | Center Winding |
| Insulation: Polyester Tape t = 0.050mm, 2 Layers | | | | |
| N_{5V} | 7 → 6 | $0.3^\phi \times 3$ | 3 | Center Winding |
| Insulation: Polyester Tape t = 0.050mm, 2 Layers | | | | |
| $N_{p/2}$ | 3 → 2 | $0.4^\phi \times 1$ | 18 | Solenoid Winding |
| Outer Insulation: Polyester Tape t = 0.050mm, 2 Layers | | | | |

4.Electrical Characteristics

| | Pin | Specification | Remarks |
|--------------------|-------|---------------------|---------------------------|
| Inductance | 1 - 3 | $650\mu H \pm 10\%$ | 100kHz, 1V |
| Leakage Inductance | 1 - 3 | 10 μH Max | 2 nd all short |

5. Core & Bobbin

- Core: EER 3016
- Bobbin: EER3016
- Ae(mm²): 96

6. Demo Circuit Part List

| Part | Value | Note | Part | Value | Note |
|------------------|--------------|------------------------|---------------------|---------------|-------------------|
| Fuse | | | Inductor | | |
| F101 | 2A/250V | | L201 | 5μH | Wire 1.2mm |
| NTC | | | L202 | 5μH | Wire 1.2mm |
| RT101 | 5D-9 | | Diode | | |
| Resistor | | | D101 | UF4007 | |
| R101 | 560kΩ | 1W | D102 | UF4004 | |
| R102 | 30kΩ | 1/4W | D201 | MBRF1045 | |
| R103 | 56kΩ | 2W | D202 | MBRF10100 | |
| R104 | 5Ω | 1/4W | ZD101 | Zener Diode | 22V |
| R105 | 40kΩ | 1/4W | ZD102 | Zener Diode | 10V |
| R201 | 1kΩ | 1/4W | Bridge Diode | | |
| R202 | 1.2kΩ | 1/4W | BD101 | 2KBP06M 3N257 | Bridge Diode |
| R203 | 12kΩ | 1/4W | | | |
| R204 | 5.6kΩ | 1/4W | Line Filter | | |
| R205 | 5.6kΩ | 1/4W | LF101 | 23mH | Wire 0.4mm |
| | | | IC | | |
| Capacitor | | | IC101 | FSDM0465RS | FPS™ |
| C101 | 220nF/275VAC | Box Capacitor | IC201 | KA431 (TL431) | Voltage reference |
| C102 | 220nF/275VAC | Box Capacitor | IC301 | H11A817A | Opto-coupler |
| C103 | 100μF/400V | Electrolytic Capacitor | | | |
| C104 | 2.2nF/1kV | Ceramic Capacitor | | | |
| C105 | 22μF/50V | Electrolytic Capacitor | | | |
| C106 | 47nF/50V | Ceramic Capacitor | | | |
| C201 | 1000μF/25V | Electrolytic Capacitor | | | |
| C202 | 1000μF/25V | Electrolytic Capacitor | | | |
| C203 | 1000μF/10V | Electrolytic Capacitor | | | |
| C204 | 1000μF/10V | Electrolytic Capacitor | | | |
| C205 | 47nF/50V | Ceramic Capacitor | | | |
| C301 | 4.7nF | Polyester Film Cap. | | | |

7. Layout

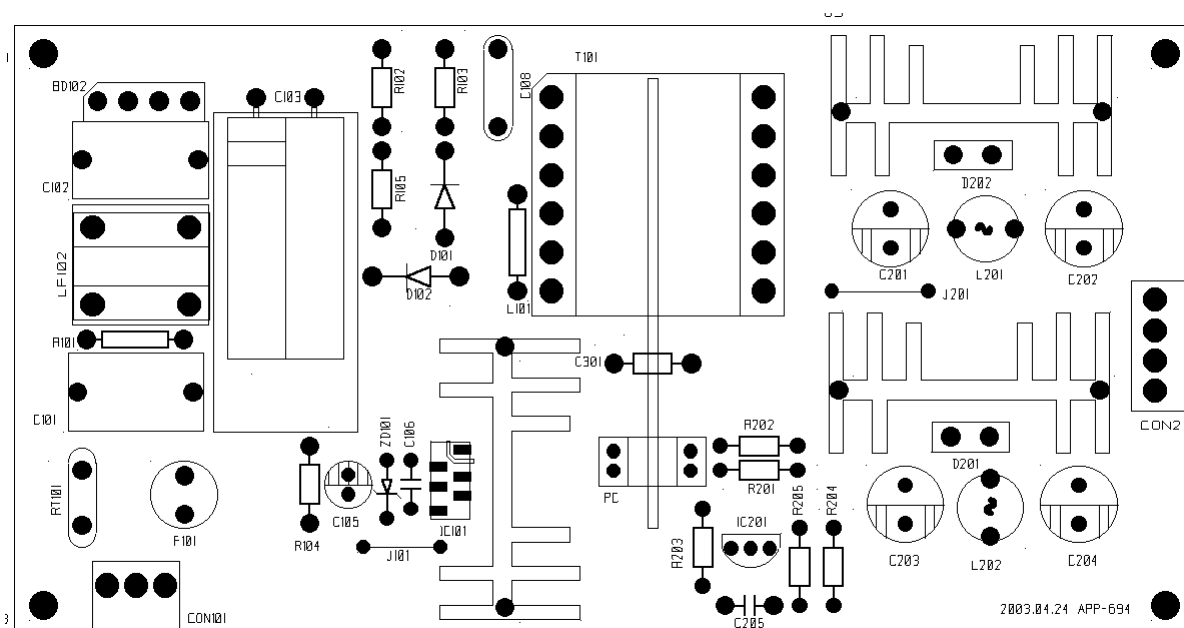


Figure 25. Layout Considerations for FSDM0465RS

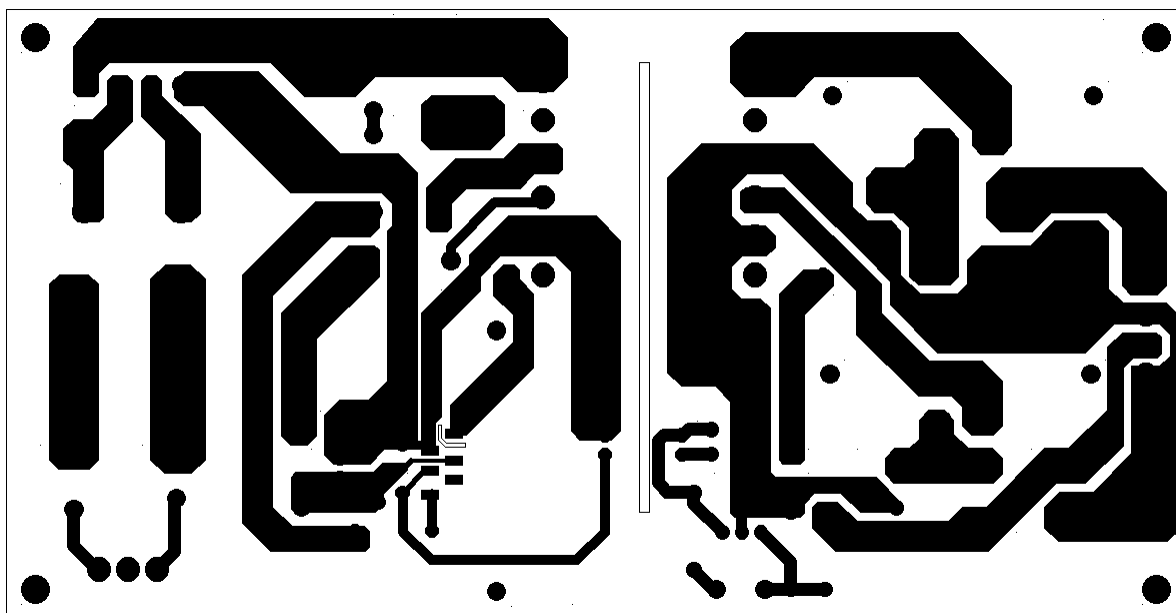
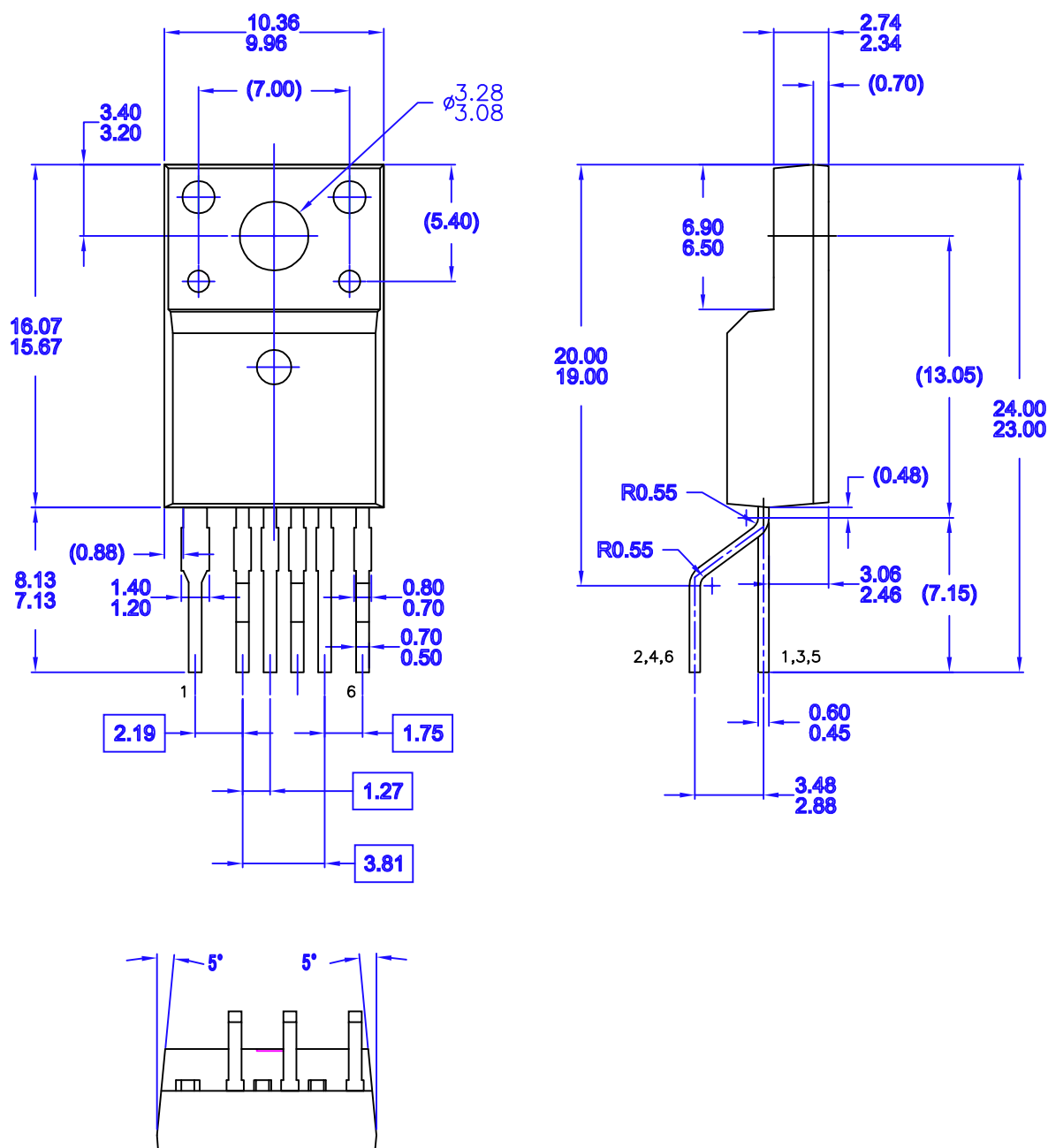


Figure 26. Layout Considerations for FSDM0465RS

Package Dimensions

TO-220F-6L (Forming)

Dimensions in millimeters



MKT-TO220A06revB

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
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Rev. I20



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