PCF8583

Clock and calendar with 240 x 8-bit RAM

Rev. 06 — 6 October 2010 Product data sheet

1. General description

The PCF8583 is a clock and calendar chip, based on a 2048 bit static CMOS[1] RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I^{2}C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock, calendar, and counter functions. The next 8 bytes can be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

2. Features and benefits

- I^{2}C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage 1.0 V to 6.0 V at 0 °C to +70 °C
- 240 × 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6.0 V
- Operating current (at f_{SCL} = 0 Hz): max 50 μA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 hour or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input and output bus (I^{2}C-bus)
- Automatic word address incrementing
- Programmable alarm, timer, and interrupt function
- Slave addresses: A1h or A3h for reading, A0h or A2h for writing

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 14.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8583P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8583T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1
PCF8583BS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm	SOT662-1

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF8583P	PCF8583P
PCF8583T	8583T
PCF8583BS	8583S

5. Block diagram

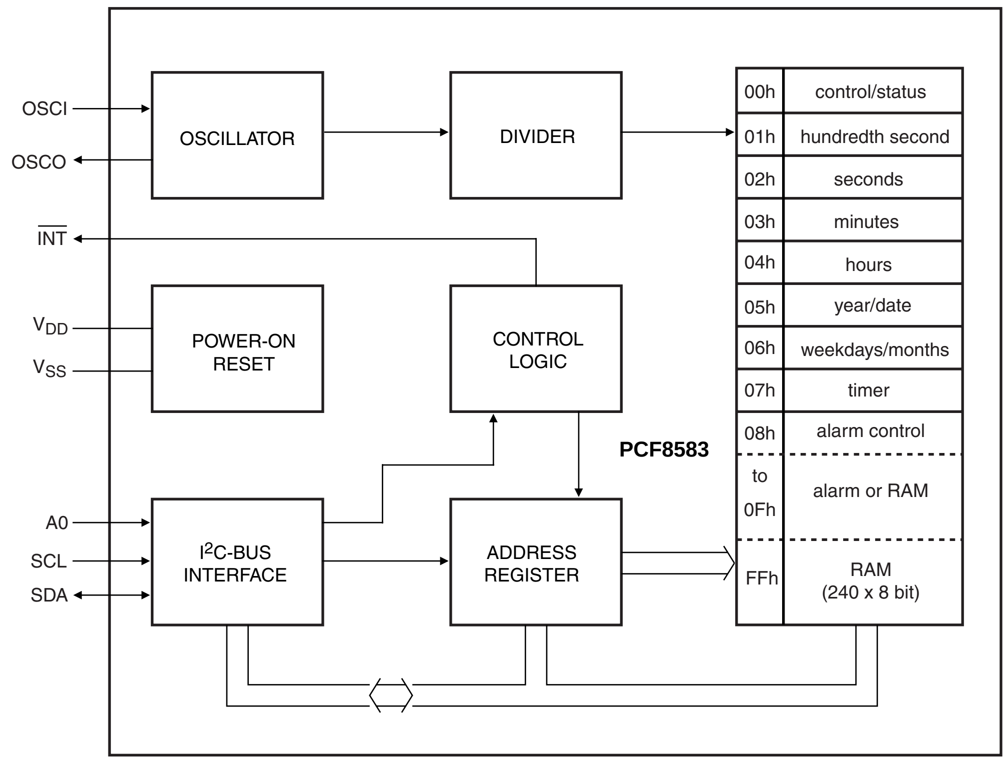
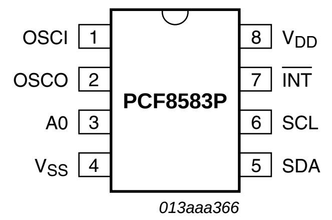


Fig 1. Block diagram of PCF8583

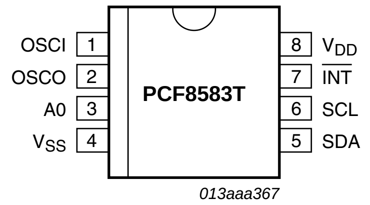
6. Pinning information

6.1 Pinning



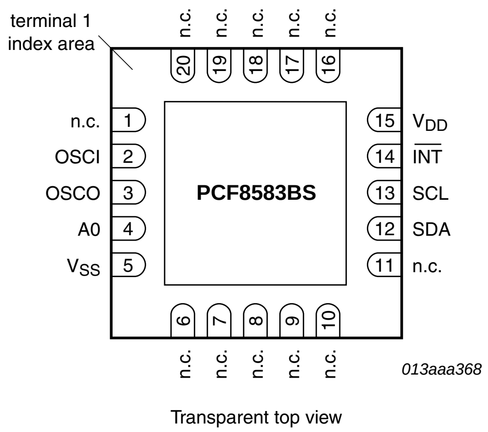
Top view. For mechanical details, see Figure 24.

Fig 2. Pin configuration for DIP8 (PCF8583P)



Top view. For mechanical details, see Figure 25.

Fig 3. Pin configuration for SO8 (PCF8583T)



For mechanical details, see Figure 26.

Fig 4. Pin configuration for HVQFN20 (PCF8583BS)

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Type	Description
	DIP8 (PCF8583P)	SO8 (PCF8583T)	HVQFN20 (PCF8583BS)		
OSCI	1	1	2	input	oscillator input, 50 Hz or event-pulse input
OSCO	2	2	3	output	oscillator output
A0	3	3	4	input	address input
V_{SS}	4	4	5[1]	supply	ground supply voltage
SDA	5	5	12	input/output	serial data line
SCL	6	6	13	input	serial clock line
$\overline{INT}$	7	7	14	output	open-drain interrupt output (active LOW)
V_{DD}	8	8	15	supply	supply voltage
n.c.	-	-	1, 6 to 11, 16 to 20	-	not connected; do not connect and do not use as feed through

[1] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

7. Functional description

The PCF8583 contains a 256 by 8 bit RAM with an 8 bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C-bus interface, and a Power-On Reset (POR) circuit.

The first 16 bytes of the RAM (memory addresses 00h to 0Fh) are designed as addressable 8 bit parallel special function registers. The first register (memory address 00h) is used as a control and status register. The memory addresses 01h to 07h are used as counters for the clock function. The memory addresses 08h to 0Fh may be programmed as alarm registers or used as free RAM locations, when the alarm is disabled.

7.1 Counter function modes

When the control and status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a Binary Coded Decimal (BCD) format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01h to 07h), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the counter during a carry condition is prevented.

When a counter is written, other counters are not affected.

7.2 Alarm function modes

By setting the alarm enable bit of the control and status register the alarm control register (address 08h) is activated.

By setting the alarm control register, a dated alarm, a daily alarm, a weekday alarm, or a timer alarm may be programmed. In the clock modes, the timer register (address 07h) may be programmed to count hundredths of a second, seconds, minutes, hours, or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control and status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (bit 2 of control and status register set logic 0) the alarm registers at addresses 08h to 0Fh may be used as free RAM.

7.3 Control and status register

The control and status register is defined as the memory location 00h with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control and status register (see Figure 5).

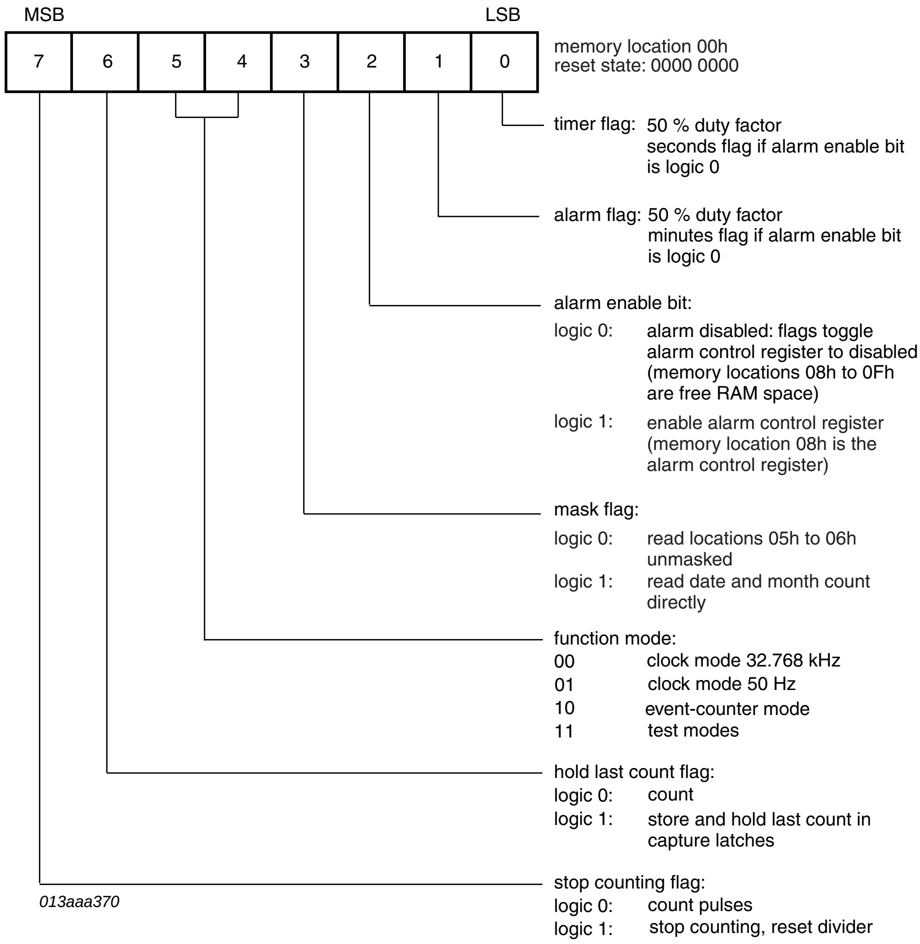


Fig 5. Control and status register

7.4 Counter registers

The format for 24 hour or 12 hour clock modes can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Figure 6.

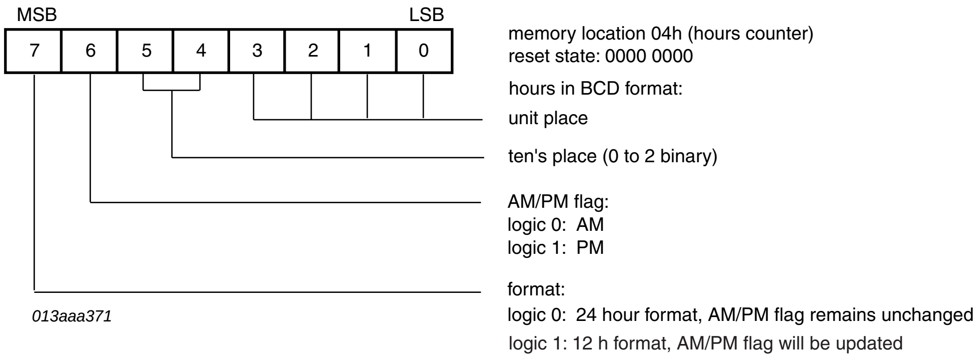


Fig 6. Format of the hours counter

The year and date are stored in memory location 05h (see Figure 7). The weekdays and months are in memory location 06h (see Figure 8).

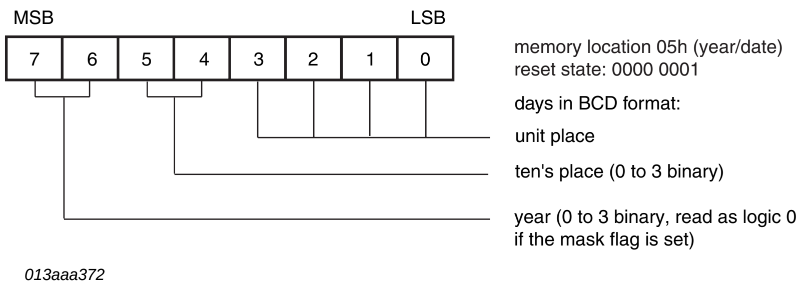


Fig 7. Format of the year and date counter

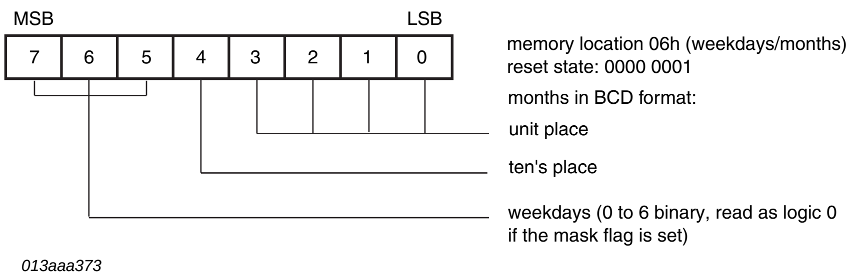


Fig 8. Format of the weekdays and month counter

When reading these memory locations the year and weekdays are masked out when the mask flag of the control and status register is set. This allows the user to read the date and month count directly. In the event-counter mode, events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Figure 9. Counter cycles are listed in Table 4.

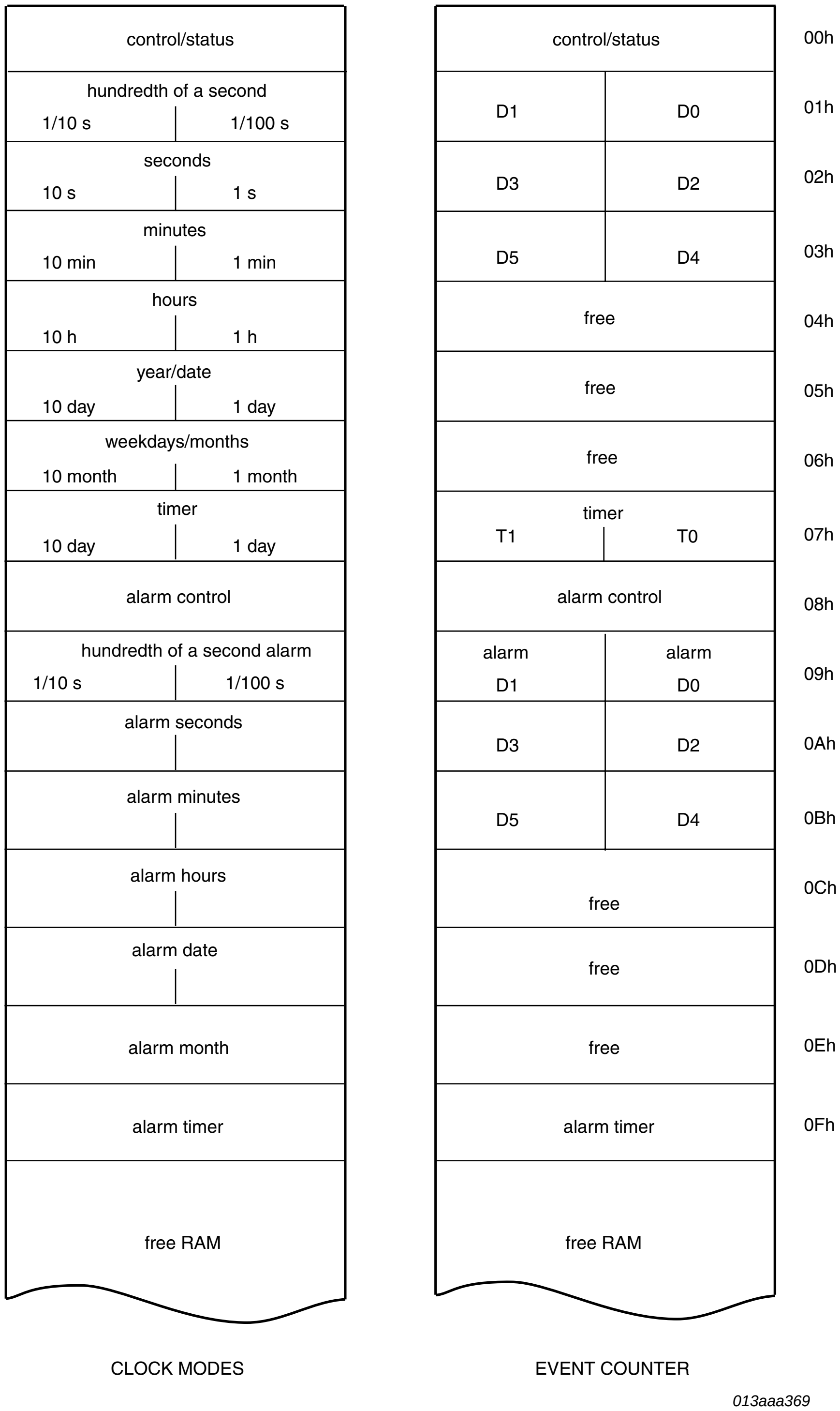


Fig 9. Register arrangement

Table 4. Cycle length of the time counters, clock modes

Unit	Counting cycle	Carry to next unit	Contents of month calendar
hundredths of a second	00 to 99	99 to 00	-
seconds	00 to 59	59 to 00	-
minutes	00 to 59	59 to 00	-
hours (24)	00 to 23	23 to 00	-
hours (12)	12 am	-	-
	01 am to 11 am	-	-
	12 pm	-	-
	01 pm to 11 pm	11 pm to 12 am	-
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, and 12
	01 to 30	30 to 01	4, 6, 9, and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, and 3
months	01 to 12	12 to 01	-
year	0 to 3	-	-
weekdays	0 to 6	6 to 0	-
timer	00 to 99	no carry	-

7.5 Alarm control register

When the alarm enable bit of the control and status register is set (address 00h, bit 2) the alarm control register (address 08h) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Figure 10).

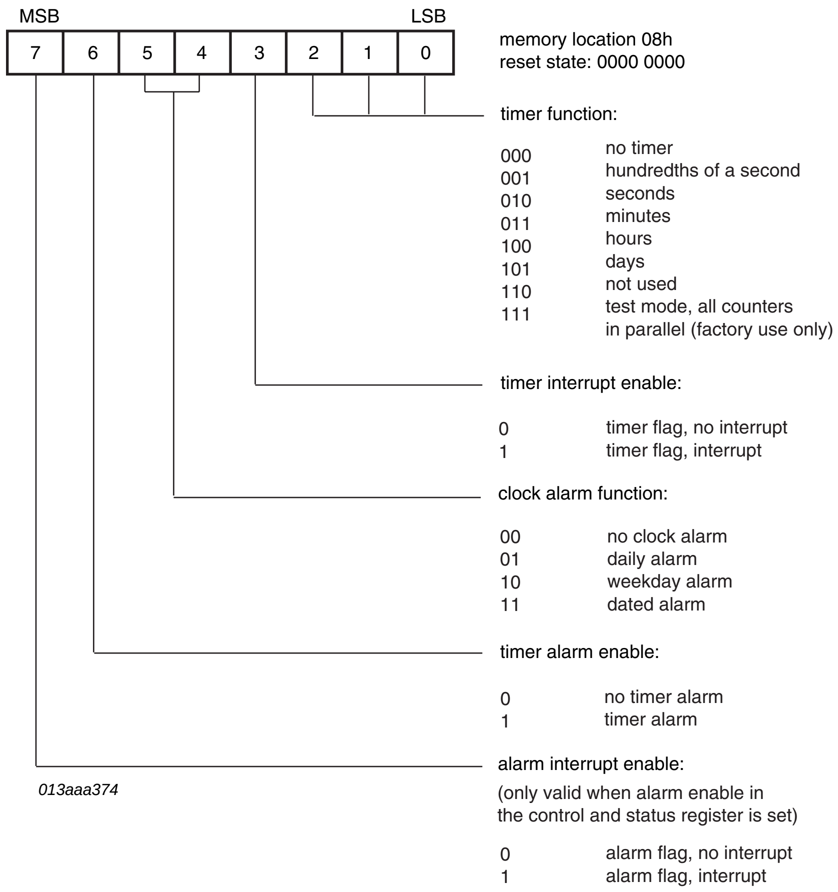


Fig 10. Alarm control registers, clock mode

7.6 Alarm registers

All alarm registers are allocated with a constant address offset of 08h to the corresponding counter registers (see Figure 9).

An alarm signal is generated when the contents of the alarm registers match bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday and month register selects the weekdays on which an alarm is activated (see Figure 11).

Remark: In the 12 hour mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

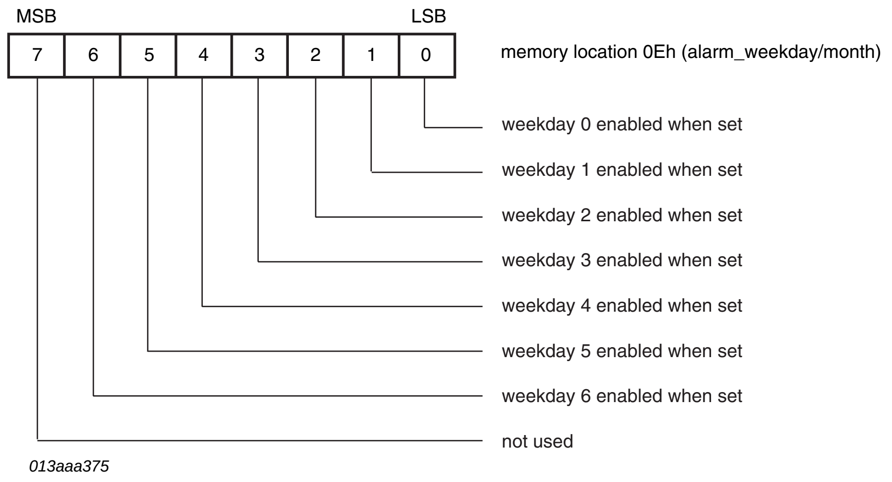


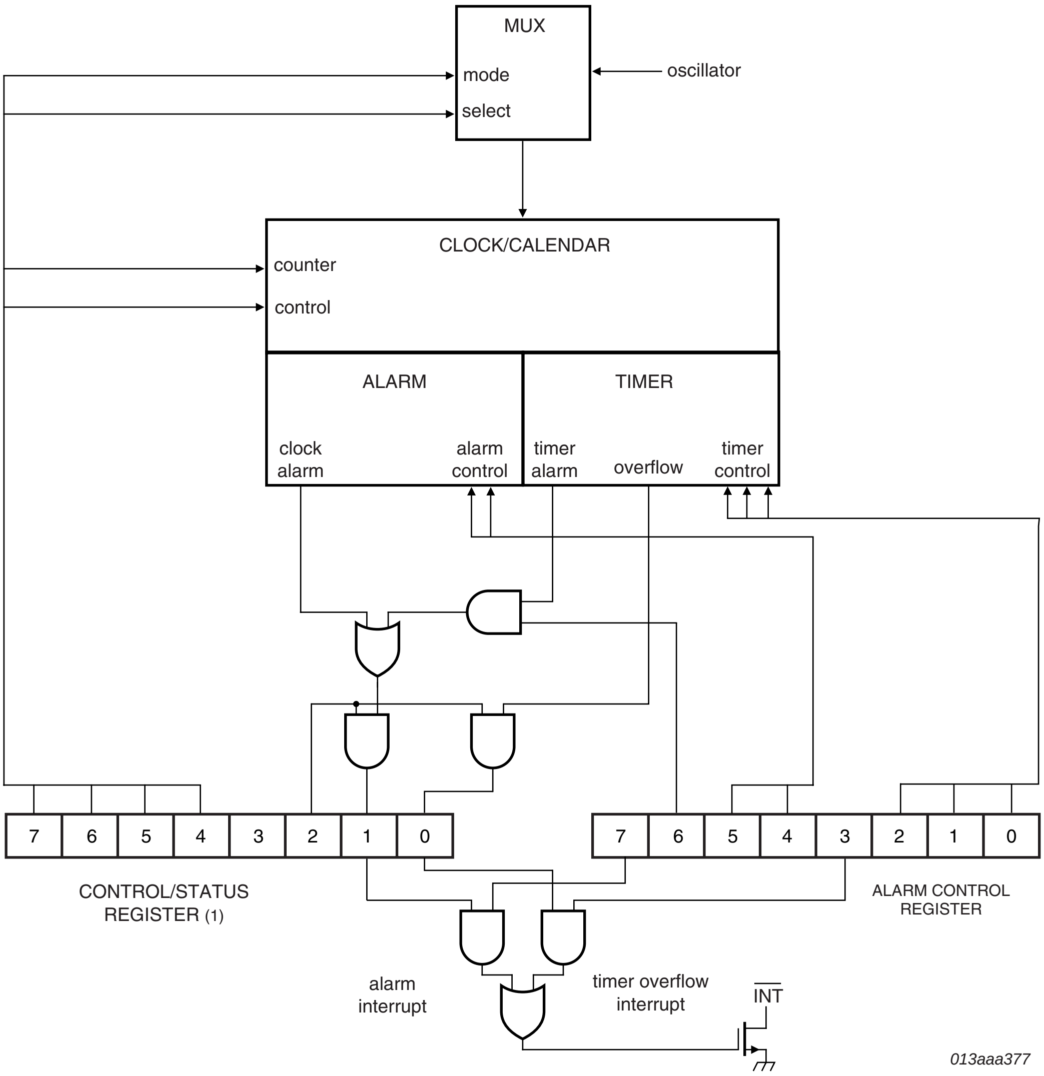
Fig 11. Selection of alarm weekdays

7.7 Timer

The timer (location 07h) is enabled by setting the control and status register to XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control and status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0Fh), the alarm flag is set (bit 1 of the control and status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Figure 12).



(1) If the alarm enable bit of the control and status register is reset (logic 0), a 1 Hz signal is observed on the interrupt pin $\overline{\text{INT}}$.

Fig 12. Alarm and timer interrupt logic diagram

7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 10 in the control and status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit).

The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in the registers 1h, 2h, and 3h. Therefore, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in the registers 9h, Ah, and Bh, and the event alarm is enabled (bits 4 and 5 which are logic 01 in the alarm control register). In this event, the alarm flag (bit 1 of the control and status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07h) increments once for every one, one hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0, 1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

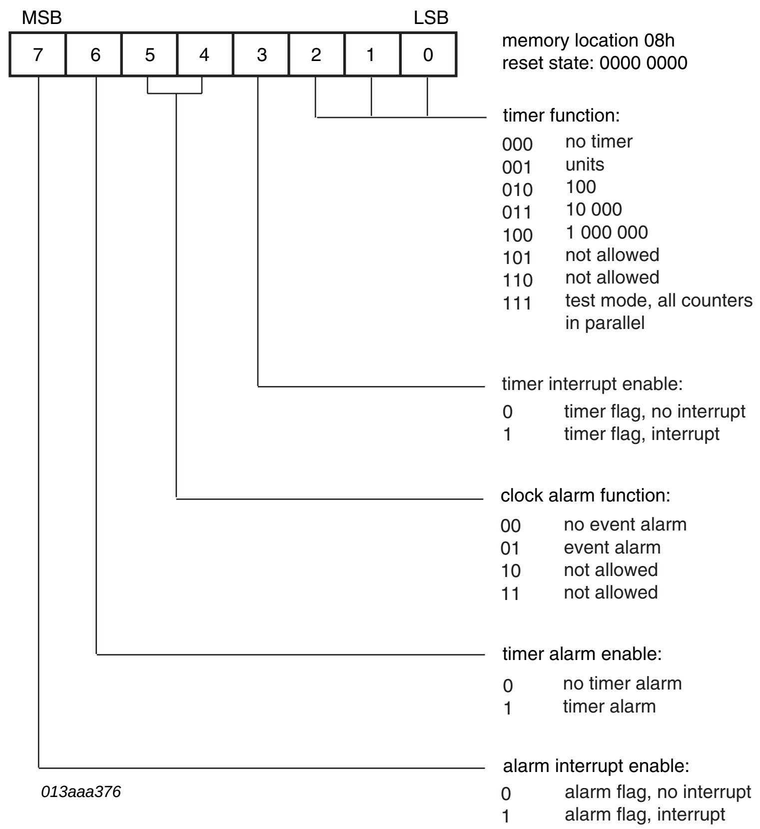


Fig 13. Alarm control register, event counter mode

7.9 Interrupt output

The conditions for activating the output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of the control and status register is logic 0), the interrupt output toggles at 1 Hz with a 50 % duty cycle (may be used for calibration). This is the default power-on state of the device. The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Figure 12.

7.10 Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI and OSCO. A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Section 11.1). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

7.11 Initialization

When power-on occurs the I^2C-bus interface, the control and status register and all clock counters are reset. The device starts time-keeping in the 32.768 kHz clock mode with the 24 hour format on the first of January at 0.00.00:00. A 1 Hz square wave with 50 % duty cycle appears at the interrupt output pin (starts HIGH).

The stop counting flag of the control and status register must be set before loading the actual time into the counters. Loading of illegal states leads to a temporary clock malfunction.

8. Characteristics of the I²C-bus

8.1 Characteristics

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

8.1.1 Bit transfer

One data bit is transferred during each clock pulse (see Figure 14). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal.

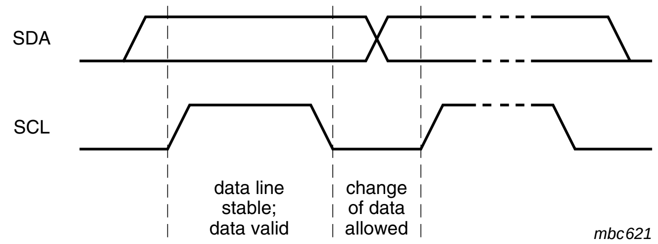


Fig 14. Bit transfer

8.1.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 15).

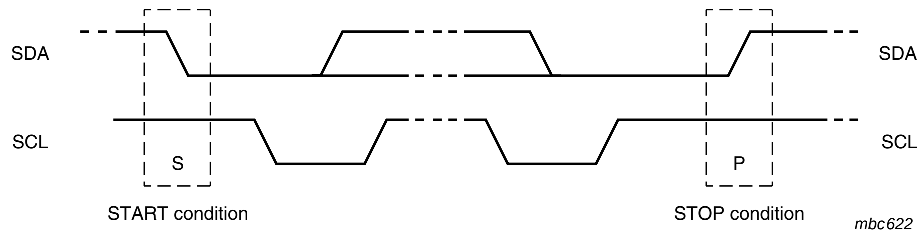


Fig 15. Definition of start and stop conditions

8.1.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver (see Figure 16). The device that controls the message is the master; and the devices which are controlled by the master are the slaves.

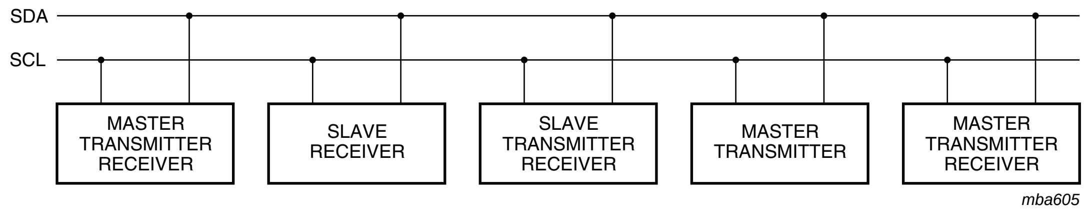


Fig 16. System configuration

8.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is illustrated in Figure 17.

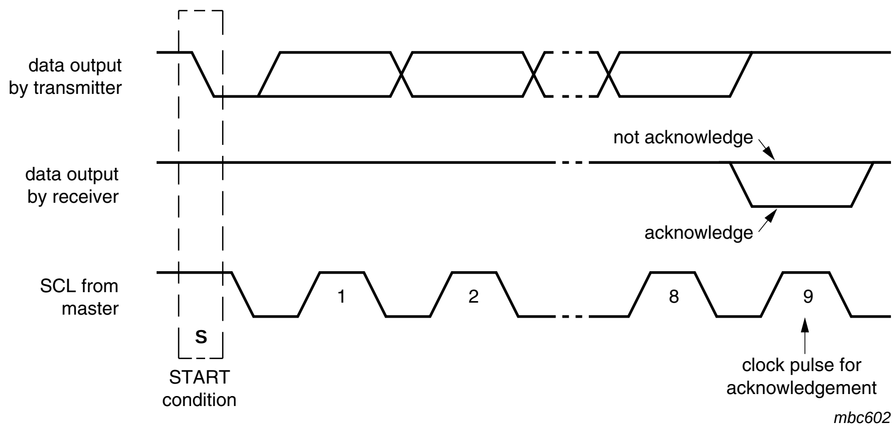


Fig 17. Acknowledgement on the I^{2}C-bus

8.2 I²C-bus protocol

8.2.1 Addressing

Before any data is transmitted on the I²C-bus, the device which must respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock and calendar acts as a slave receiver or slave transmitter. The clock signal SCL is only an input signal but the data signal SDA is a bidirectional line.

The clock and calendar slave address is shown in Table 5. Bit A0 corresponds to hardware address pin A0. Connecting this pin to V_{DD} or V_{SS} allows the device to have one of two different addresses.

Table 5. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
	1	0	1	0	0	0	A0	R/$\overline{W}$

8.2.2 Clock and calendar READ or WRITE cycles

The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figure 18, Figure 19 and Figure 20.

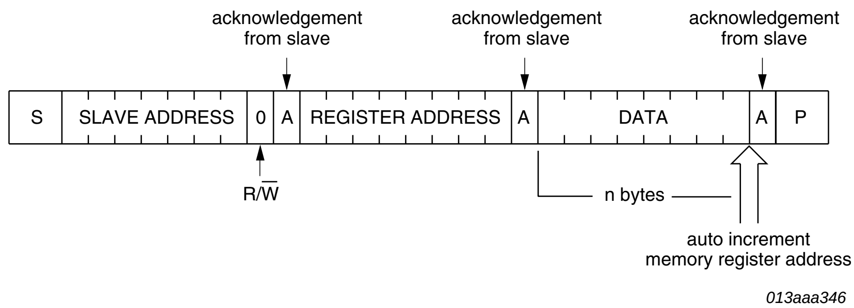
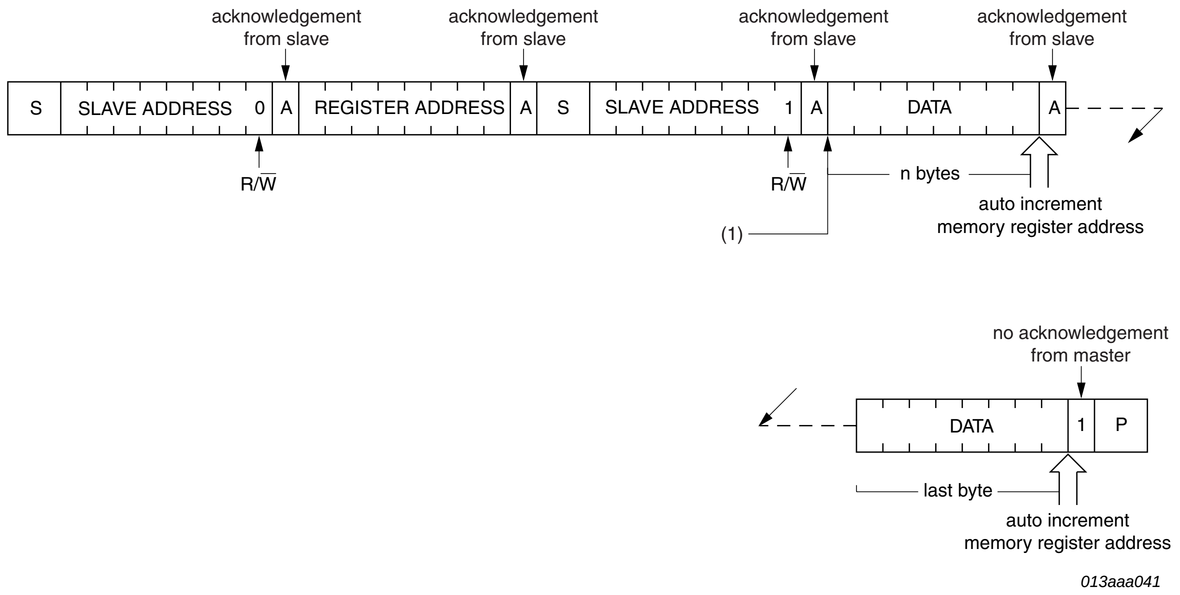


Fig 18. Master transmits to slave receiver (WRITE mode)



(1) At this moment master transmitter becomes master receiver and PCF8583 slave receiver becomes slave transmitter.

Fig 19. Master reads after setting word address (write word address; READ data)

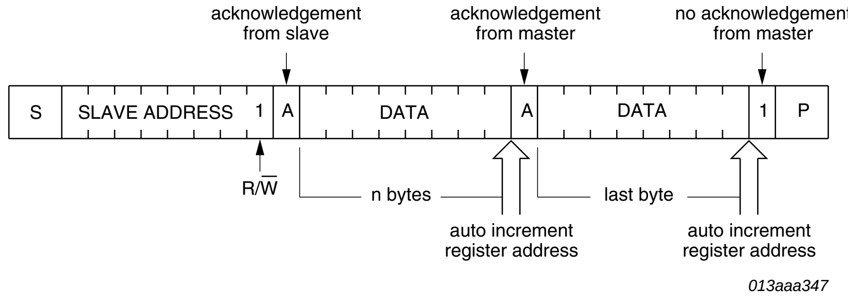


Fig 20. Master reads slave immediately after first byte (READ mode)

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.8	+7.0	V
I_{DD}	supply current			-	50	mA
I_{SS}	ground supply current			-	50	mA
V_I	input voltage			–0.8	V_{DD} + 0.8	V
I_I	input current			-	10	mA
I_O	output current			-	10	mA
P_{tot}	total power dissipation			-	300	mW
P_o	output power			-	50	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3000	V
		MM	[2]	-	±200	V
I_{lu}	latch-up current		[3]	-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 5 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”.

[3] Pass level; latch-up testing according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport requirements (see Ref. 9 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

10. Characteristics

10.1 Static characteristics

Table 7. Static characteristics

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage	operating mode					
		I^2C-bus active		2.5	-	6.0	V
		I^2C-bus inactive		1.0	-	6.0	V
		quartz oscillator					
		T_{amb} = 0 °C to +70 °C	[2]	1.0	-	6.0	V
I_{DD}	supply current	operating mode					
		f_{SCL} = 100 kHz clock mode	[3]	-	-	200	µA
		clock mode; f_{SCL} = 0 Hz					
		V_{DD} = 5.0 V	[4]	-	10	50	µA
		V_{DD} = 1.0 V	[4]	-	2	10	µA
		data retention; f_{OSCI} = 0 Hz; V_{DD} = 1.0 V					
		T_{amb} = −40 °C to +85 °C		-	-	5	µA
		T_{amb} = −25 °C to +70 °C		-	-	2	µA
V_{en}	enable voltage	I^2C-bus enable level	[5]	1.5	1.9	2.3	V
Pin SDA							
V_{IL}	LOW-level input voltage		[6]	−0.8	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		[6]	$0.7V_{DD}$	-	V_{DD} + 0.8	V
I_{OL}	LOW-level output current			3.0	-	-	mA
I_{LI}	input leakage current			−1	-	+1	µA
C_I	input capacitance		[7]	-	-	7	pF
Pins A0 and OSCI							
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−250	-	+250	nA
Pin $\overline{INT}$							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
Pin SCL							
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_I	input capacitance		[7]	-	-	7	pF

[1] Typical values measured at T_{amb} = 25 °C.

[2] When the device is powered on, V_{DD} must exceed 1.5 V until the stable operation of the oscillator is established.

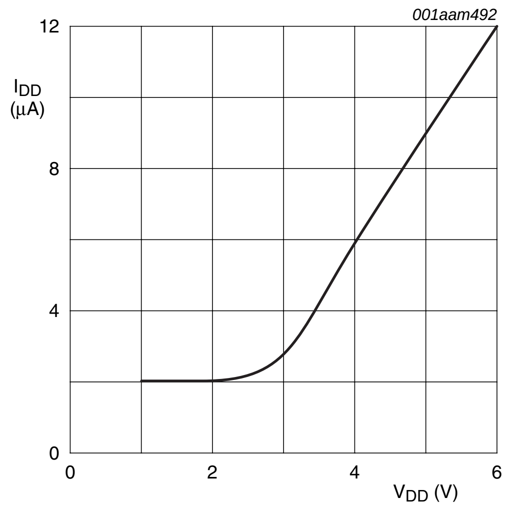
[3] Event counter mode: supply current dependant upon input frequency.

[4] See Figure 21.

[5] The I^2C-bus logic is disabled if V_{DD} < V_{en}.

[6] When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current will flow; this current must not exceed ±0.5 mA.

[7] Tested on a sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C

Fig 21. Typical supply current in clock mode as a function of supply voltage

10.2 Dynamic characteristics

Table 8. Dynamic characteristics

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
C_{OSCO}	capacitance on pin OSCO		-	40	-	pF
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	-	0.2	-	ppm
$f_{clk(ext)}$	external clock frequency	on pin OSCI [1]	-	-	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_S	series resistance		-	-	40	kΩ
C_L	parallel load capacitance		-	10	-	pF
C_{trim}	trimmer capacitance		5	-	25	pF
I²C-bus timing (see Figure 21)[2]						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	100	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	-	µs
t_r	rise time of both SDA and SCL signals		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;DAT}$	data valid time		-	-	3.4	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	-	µs

[1] Event counter mode only.

[2] All timing values are valid within the operating supply voltage, ambient temperature range, reference to V_{IL} and V_{IH} and with an input voltage swing of V_{SS} to V_{DD}.

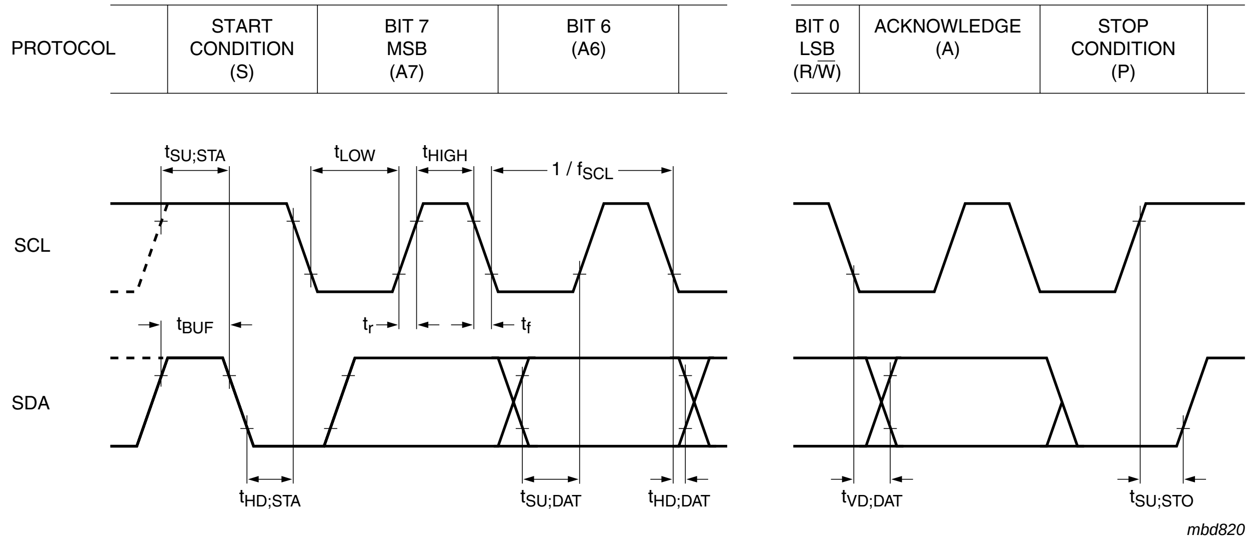


Fig 22. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

11. Application information

11.1 Quartz frequency adjustment

11.1.1 Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout, a fixed capacitor can be used. The frequency is measured using the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance. Average deviations of ±5 minutes per year are possible.

11.1.2 Method 2: OSCI trimmer

Using the alarm function (via the I^2C-bus) a signal faster than the 1 Hz is generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power the device on
- Initialize the device (alarm functions).

Routine:

- Set clock to time t and set alarm to time t + Δt
- at time t + Δt (interrupt) repeat routine.

11.1.3 Method 3: Direct measurement

Direct measurement of oscillator output (allowing for test probe capacitance).

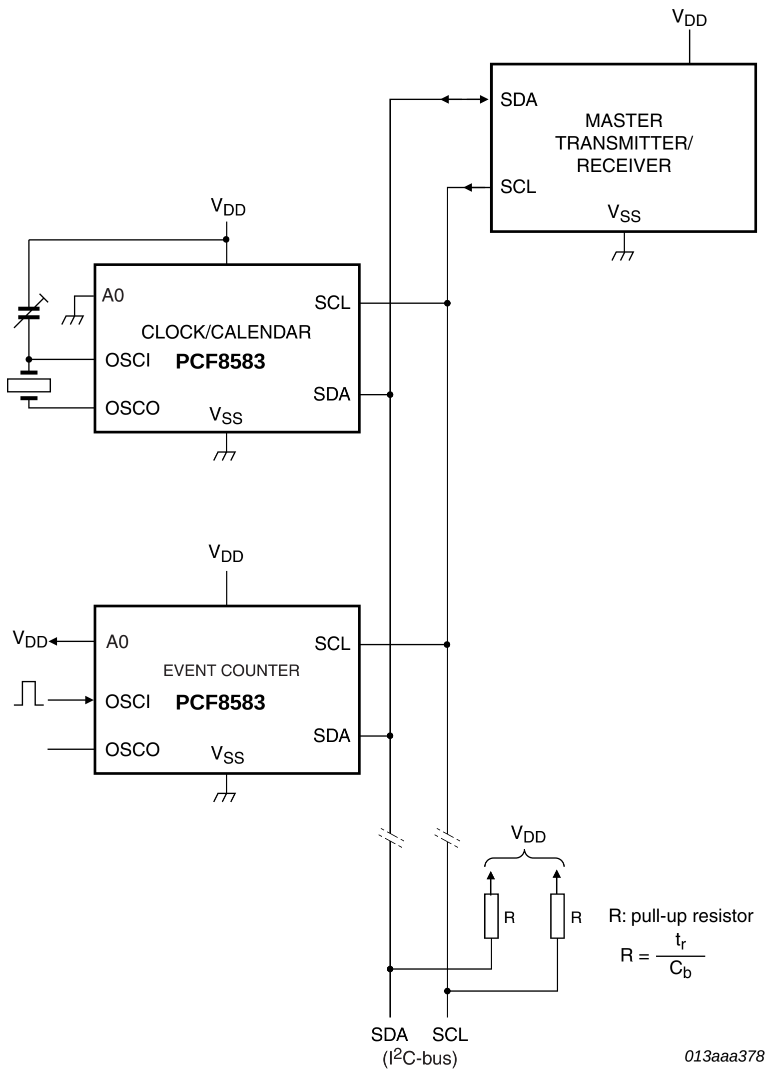
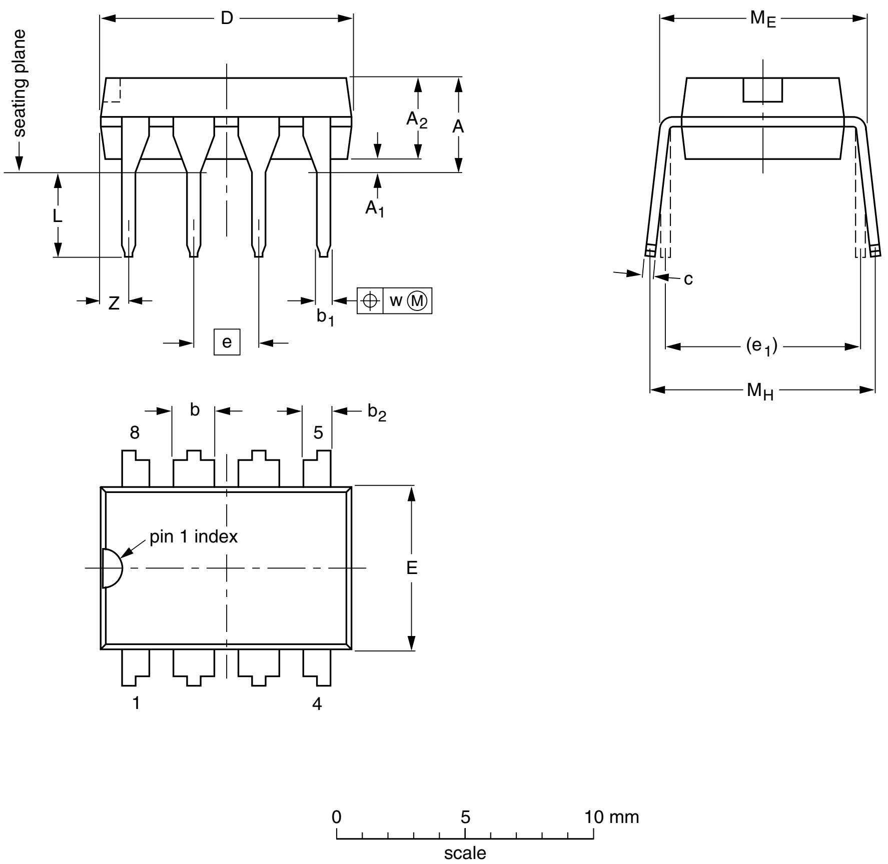


Fig 23. Application example

12. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

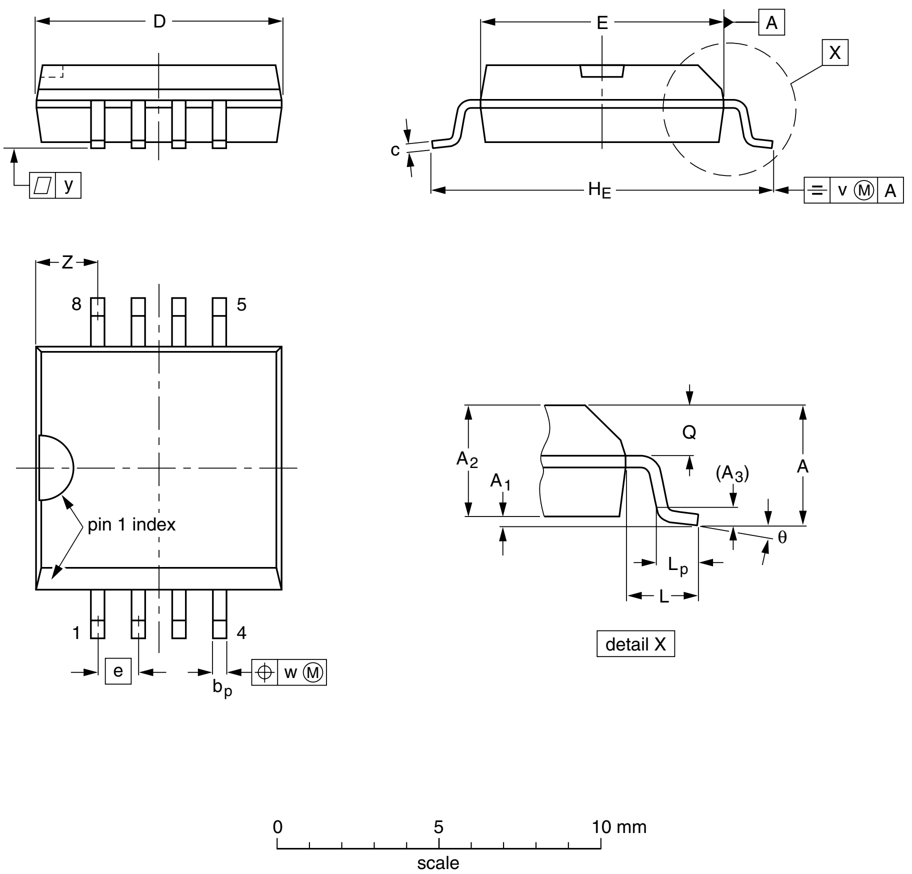
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 24. Package outline SOT97-1 (DIP8) of PCF8583P

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.05	0.419 0.394	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

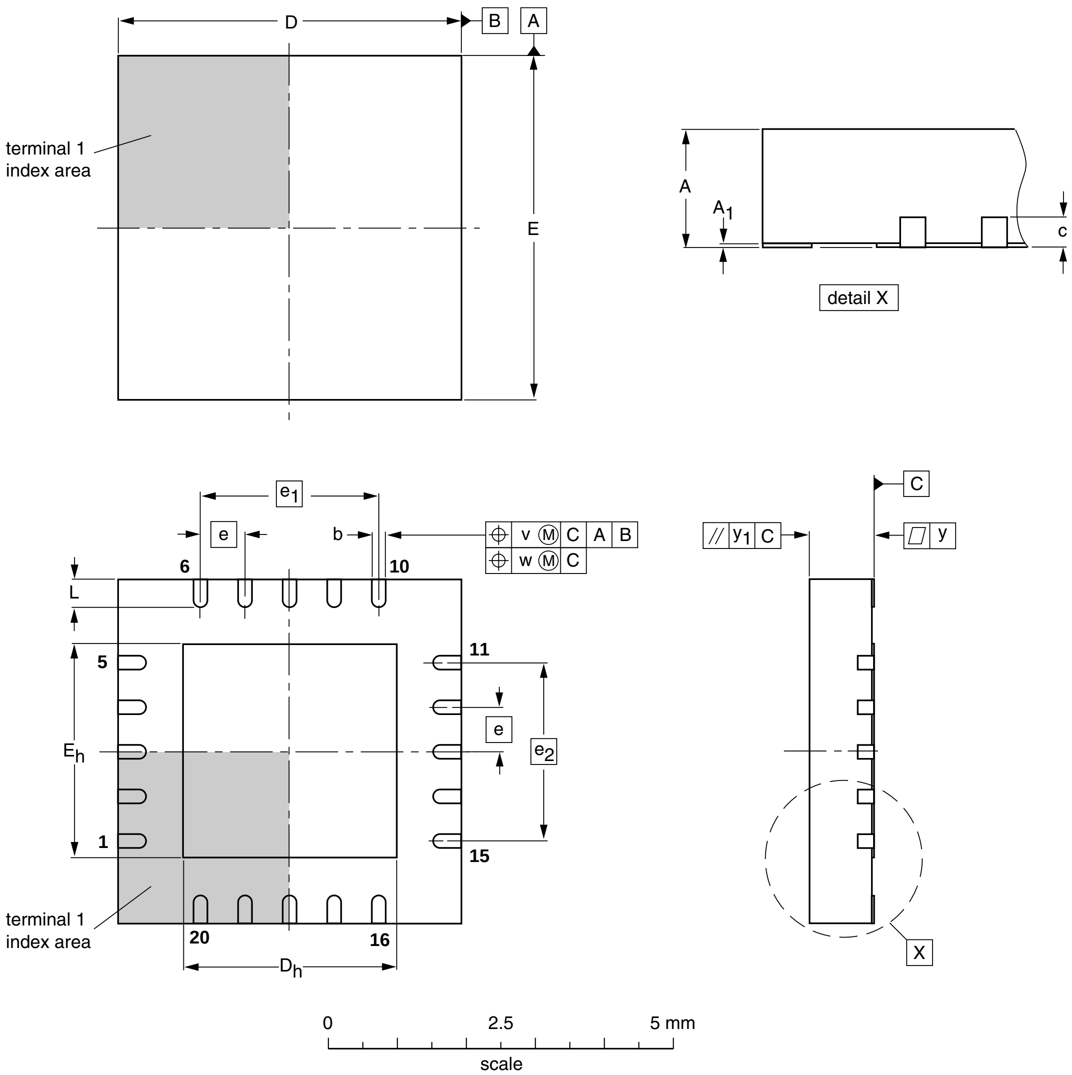
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT176-1						~~97-05-22~~ 03-02-19

Fig 25. Package outline SOT176-1 (SO8) of PCF8583T

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm **SOT662-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 26. Package outline SOT662-1 (HVQFN20) of PCF8583BS

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 27) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

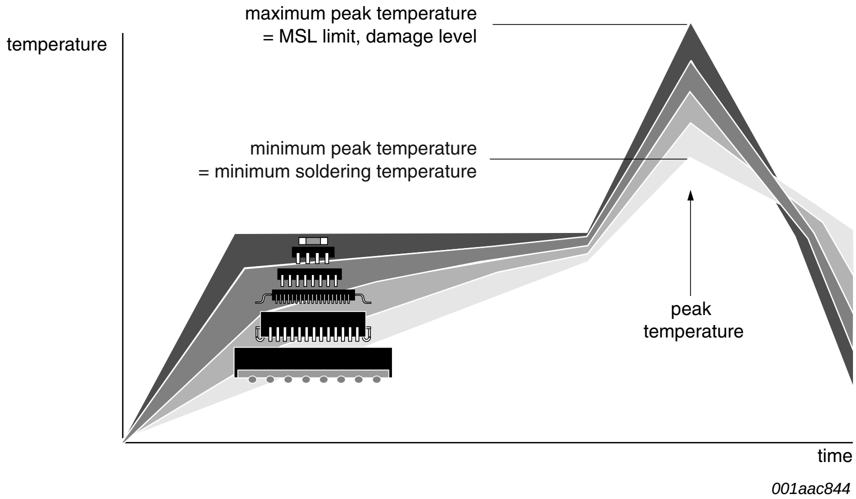
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 27.



MSL: Moisture Sensitivity Level

Fig 27. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
PCB	Printed-Circuit Board
PM	Post Meridiem
POR	Power-On Reset
PPM	Parts Per Million
RF	Radio Frequency
RAM	Random Access Memory
SCL	Serial Clock Line
SDA	Serial DAta line
SMD	Surface-Mount Device

15. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **IPC/JEDEC J-STD-020 —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **NX3-00092 —** NXP store and transport requirements

[10] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[11] **UM10204 —** I^2C-bus specification and user manual

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8583 v.6	20101006	Product data sheet	-	PCF8583_5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Add HVQFN20 package			
PCF8583_5	19970715	Product Specification	-	PCF8583_4
PCF8583_4	19970328	Product Specification	-	PCF8583_CNV_3
PCF8583_CNV_3	19961003	Product Specification	-	PCF8583_2

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^{2}C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Contents

1 General description . . . 1
2 Features and benefits . . . 1
3 Ordering information . . . 2
4 Marking . . . 2
5 Block diagram . . . 2
6 Pinning information . . . 3
6.1 Pinning . . . 3
6.2 Pin description . . . 4
7 Functional description . . . 5
7.1 Counter function modes . . . 5
7.2 Alarm function modes . . . 5
7.3 Control and status register . . . 6
7.4 Counter registers . . . 7
7.5 Alarm control register . . . 9
7.6 Alarm registers . . . 10
7.7 Timer . . . 11
7.8 Event counter mode . . . 12
7.9 Interrupt output . . . 13
7.10 Oscillator and divider . . . 13
7.11 Initialization . . . 14
8 Characteristics of the I²C-bus . . . 15
8.1 Characteristics . . . 15
8.1.1 Bit transfer . . . 15
8.1.2 Start and stop conditions . . . 15
8.1.3 System configuration . . . 15
8.1.4 Acknowledge . . . 16
8.2 I²C-bus protocol . . . 17
8.2.1 Addressing . . . 17
8.2.2 Clock and calendar READ or WRITE cycles . 17
9 Limiting values . . . 19
10 Characteristics . . . 20
10.1 Static characteristics . . . 20
10.2 Dynamic characteristics . . . 22
11 Application information . . . 24
11.1 Quartz frequency adjustment . . . 24
11.1.1 Method 1: Fixed OSCI capacitor . . . 24
11.1.2 Method 2: OSCI trimmer . . . 24
11.1.3 Method 3: Direct measurement . . . 24
12 Package outline . . . 26
13 Soldering of SMD packages . . . 29
13.1 Introduction to soldering . . . 29
13.2 Wave and reflow soldering . . . 29
13.3 Wave soldering . . . 29
13.4 Reflow soldering . . . 30
14 Abbreviations . . . 32
15 References . . . 33
16 Revision history . . . 34
17 Legal information . . . 35
17.1 Data sheet status . . . 35
17.2 Definitions . . . 35
17.3 Disclaimers . . . 35
17.4 Trademarks . . . 36
18 Contact information . . . 36
19 Contents . . . 37

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 6 October 2010

Document identifier: PCF8583

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.