Title	***Reference Design Report for a 8.4 W Open Frame Power Supply Using LinkSwitch™-3 LNK6407D***
Specification	90 VAC – 265 VAC Input; 12 V, 0.7 A Output
Application	Open Frame Power Supply for Appliances
Author	Applications Engineering Department
Document Number	RDR-734
Date	January 31, 2019
Revision	1.2

Summary and Features

- Primary-side control eliminates secondary-side control and optocoupler
- >83% efficiency at full load
- Easily meet ErP regulation with >70% efficiency at 500 mW output
- Provides ±5% constant voltage (CV) and ±10% constant current
- Max power output guarantee <15 W to easily meet UL simplified qualification requirement
- Accurate over-temperature protection with hysteretic recovery
- Auto-restart output short-circuit and open loop protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 12 V, 0.7 A adapter utilizing a device from the LinkSwitch-3 family of ICs. This design is intended to show the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

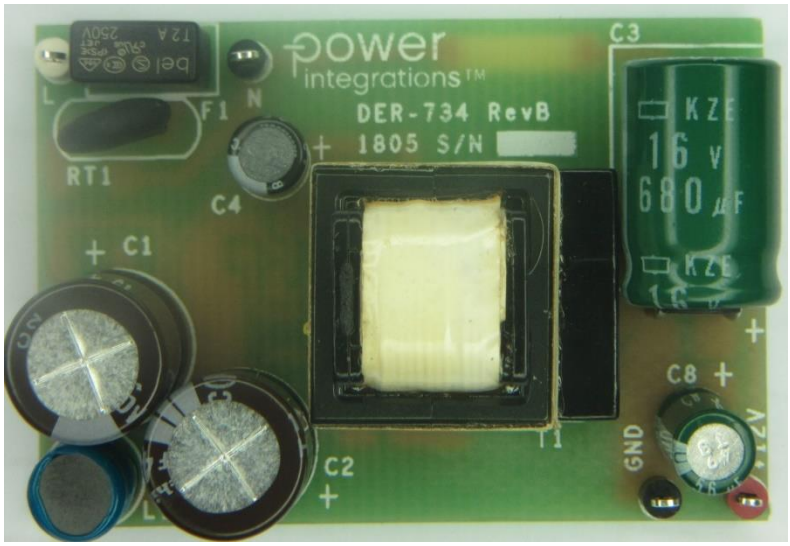

Figure 1 – Populated Circuit Board Photograph, Top.

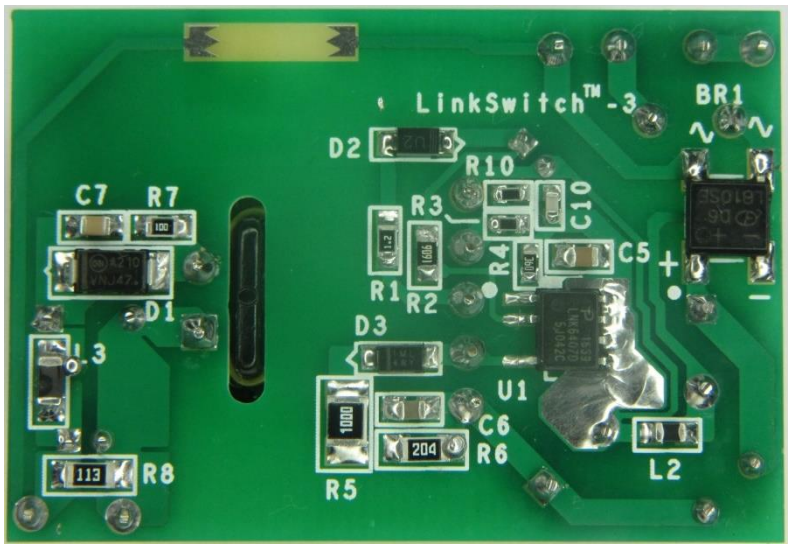

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				75	mW	265 VAC Input
Output						
Output Voltage	V_{OUT}		12.00		V	±5% PCB connector side
Output Ripple Voltage	V_{RIPPLE}			200	mVpp	Measured at the PCB connector
Output Current	I_{OUT}	0.7			A	
Continuous Output Power	P_{OUT}		8.4		W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	80.93			%	DoE Level VI, Basic Voltage
Environmental						
Conducted EMI		CISPR22B / EN55022B Load floating or grounded via artificial hand				Resistive Load, 6 dB Margin.
Safety		IEC950 / UL1950 Class II				Designed to Meet.
Differential Line Surge		1			kV	
Common Mode Surge (L1/L2-PE)		2			kV	Ring Wave, Common Mode: 12 Ω.
ESD		±16			kV	Air Discharge
		±8			kV	Contact Discharge
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic Diagram

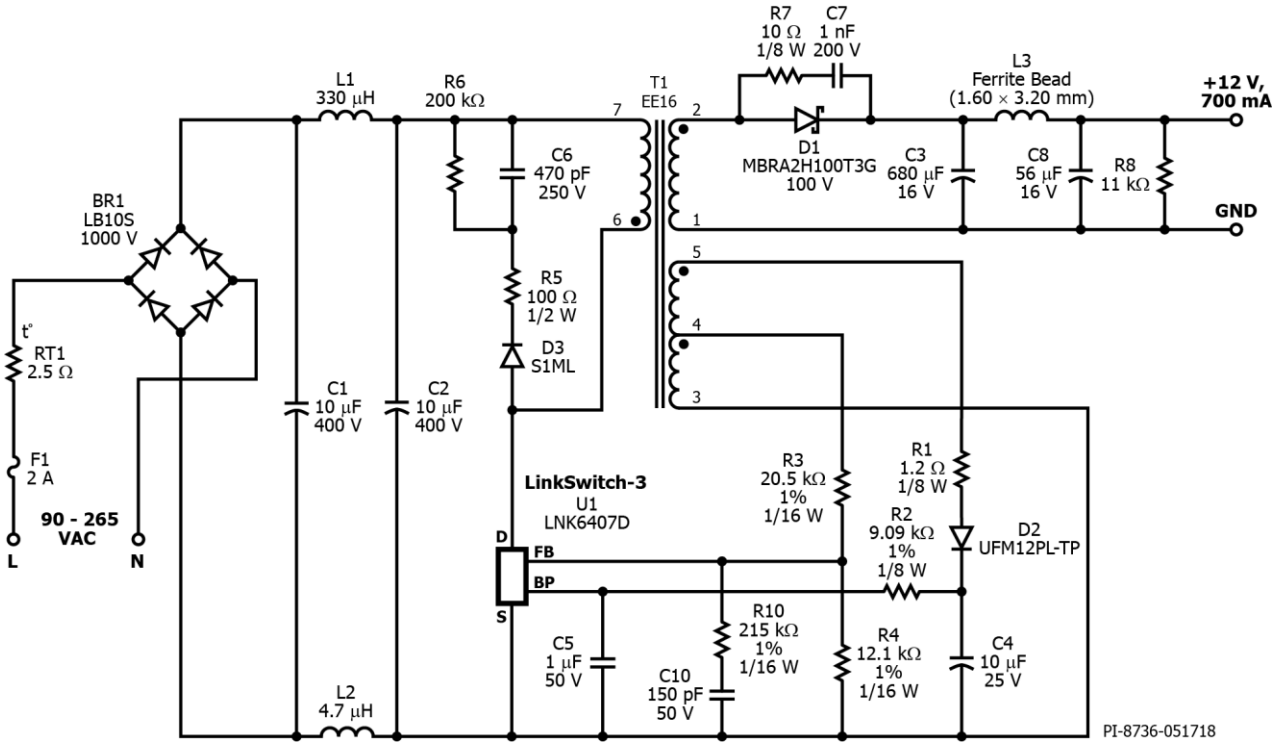

Figure 3 – Schematic Diagram.

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4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 provides protection against catastrophic failure of components on the primary-side.

Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply due to the low impedance of the input capacitor C1 and C2.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors, C1 and C2.

Capacitors C1 and C2 provide filtering of the rectified AC Input and together with L1 and L2 form a π (pi) filter to attenuate differential mode EMI.

4.2 *LNK6407D Primary*

The LNK6407D device (U1) incorporates the power switching device, oscillator, CV/CC control engine, and start-up and protection function on a single IC. The integrated 725 V power MOSFET allows sufficient voltage margins across universal AC input applications. The device is powered from the BYPASS pin with the decoupling capacitor C5 via the bias circuit R1, R2, D2, C4, with bias winding of transformer T1. The resistor R1 helps dampen the ringing on the bias winding voltage. The resistor R2 limits the BYPASS pin current.

The rectified and filtered input voltage is applied to one end of the transformer T1 primary winding. The other side of the T1 primary winding is driven by the internal MOSFET of U1. A low cost RCD clamp formed by D3, R5, R6 and C6 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

4.3 *Output Rectification and Filtering*

Transformer T1 secondary voltage is rectified by a Schottky barrier-type diode D1 and filtered by the low ESR output capacitor C3. A post-filter using L3 and C8 were added to improve the voltage peak-to-peak ripple at the output connector.

4.4 *Output Regulation*

The LNK6407D regulates the output using ON/OFF control for CV regulation and frequency control for CC regulation. The output voltage is sensed by a feedback winding on transformer T1. The feedback resistors R3 and R4 were selected using standard 1% tolerance resistor values to center both the nominal output voltage and constant current regulation thresholds. Resistor R10 and capacitor C10 across the feedback pin improve transient response and output voltage ripple measurements. Resistor R8 provides a

minimum load to maintain the output regulation when no-load is connected across the output.

4.5 *Design Key Points*

The design targets to meet the standard basic voltage DoE Level VI and COC5 Tier 2 regulatory requirements. Efficiency was optimized with the transformer design, active devices, primary clamp and filter components, and bias voltage. For the transformer design, maximizing the wire gauge of the primary and secondary windings to fit the bobbin width helps decrease copper loss with the increased conducted effective area.

To minimize power losses, the primary clamp or RCD snubber circuit were selected such that the peak MOSFET drain voltage is maintained to <680 V while still meeting efficiency and thermal performance of these components. Also, since LinkSwitch-3 uses primary side regulation (PSR), the resulting peak MOSFET drain voltage will affect the feedback voltage sensing and should settle at 1% within 1.2 µs from the turn-off of the primary MOSFET for best output regulation. The use of slow recovery type (typical t_{rr} >1 µs) reduces the feedback voltage ringing and further improve regulation.

An external bias supply through the bias winding of the transformer also increases efficiency, especially at light load, and lowers the no-load input power consumption by disabling the internal high-voltage supply for LNK6407D.

Proper selection of the secondary side components (output diode, output filter capacitor, and preload) likewise helps meet efficiency specifications. A low forward voltage and low leakage current Schottky-barrier type diode was used with a voltage rating enough to have around 20% margin from actual diode voltage stress to the peak inverse voltage (PIV) rating of the diode. Take into consideration the diode's self-heating to meet thermal and efficiency margins. For the output filter capacitor, a very-low ESR type with a high ripple current rating can be used to meet output voltage ripple specification and improves efficiency. And since the preload is a fixed loss to the power supply, it should be sized such that the output voltage at no-load is within the target regulation.

The design also aims to have a good margin for conducted EMI performance and simplify the input filter stage by eliminating the need for a common mode choke or Y-class capacitor. The transformer uses E-Shield technique to minimize the noise coupling by having a cancellation shield as the first layer of the transformer filling the bobbin width followed by the primary winding. To decrease the loss incurred by parasitic capacitance between the shield and the primary winding, the 4 layers of tape were added. Succeeding windings are for the bias, feedback and the secondary. The secondary was wound in counter-clockwise direction with respect to the other windings with the physical start connected to the GND and terminating the winding to the anode of the output diode. To further decrease noise coupling, the core was connected to B- (negative side of the input bulk capacitor).

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5 PCB Layout

PCB copper thickness is 1 oz (2.8 mils / 70 μm) unless otherwise stated.

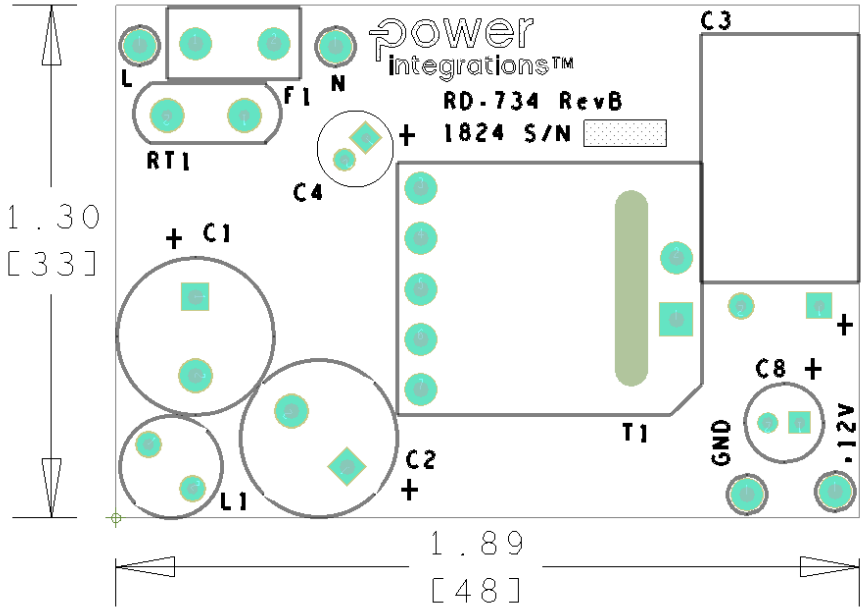

Figure 4 – Printed Circuit Layout, Top.

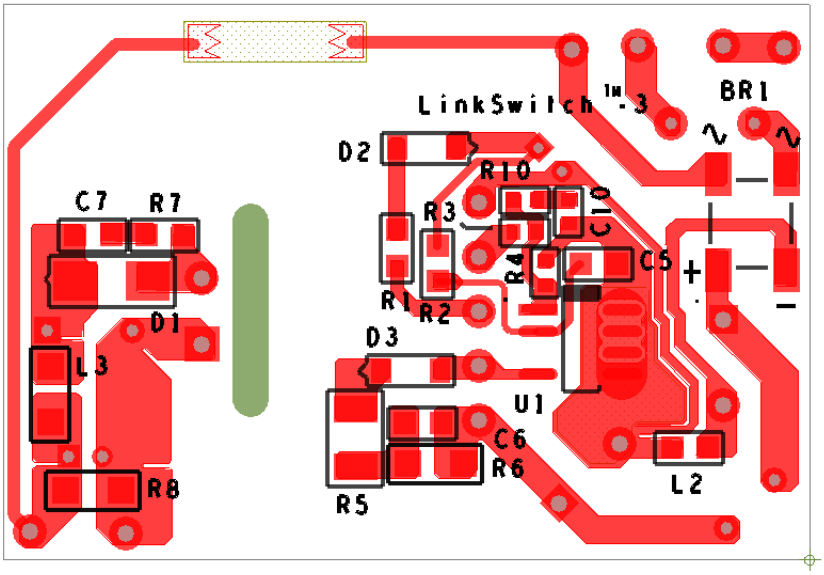

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 *Main BOM*

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, SOPA-4	LB10S	Good Ark
2	2	C1, C2	10 μF, ±20%, 400 V, Electrolytic, (10 x 14.5)	UVC2G100MPD	Nichicon
3	1	C3	680 μF, 16 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE160ELL681MJ16S	Nippon Chemi-Con
4	1	C4	10 μF, 20%, 25 V, Electrolytic,-55°C ~ 105°C, 1000 Hrs @ 105°C,Gen Purpose, (5 x 6)	UMT1E100MDD1TP	Nichicon
5	1	C5	1 μF, 16 V, Ceramic, X7R, 0805	GRM21BR71C105KA01L	Murata
6	1	C6	470 pF, 250 V, Ceramic, GCM, 0805	GCM21A7U2E471JX01D	Murata
7	1	C7	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
8	1	C8	56 μF, 16 V, Electrolytic, Very Low ESR, 22 mΩ, (10 x 25)	EKZE160ELL560ME11D	Nippon Chemi-Con
9	1	C10	CAP, CER, 150pF, ±5% ,50V,-55°C ~ 125°C, C0G/NP0, 0603 (1608 Metric)	GRM1885C1H151JA01D	Murata
10	1	D1	Diode, Schottky, 100 V, 2 A, Fast Recovery =< 500 ns, > 200 mA (Io), Tj -65°C ~ 175°C, DO-214AC, SMA	MBRA2H100T3G	ON Semi
11	1	D2	100V, 1 A, Ultrafast Recovery, SOD-123FL	UFM12PL-TP	Micro Commercial
12	1	D3	1 kV, 1 A, Standard Recovery, SMA	S1ML	Taiwan Semi
13	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
14	1	L1	330 μH, 0.34 A, 7 x 10.5 mm	SBC2-331-341	Tokin
15	1	L2	4.7 μH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
16	1	L3	Ferrite Bead, 60 Ω, 4 A, 1206 SMD	FBMJ3216HM600-T	Taiyo Yuden
17	1	R1	RES, 1.2 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ1R2V	Panasonic
18	1	R2	RES, 9.09 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9091V	Panasonic
19	1	R3	RES, 20.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2052V	Panasonic
20	1	R4	RES, 12.1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1212V	Panasonic
21	1	R5	RES, 100 Ω, 5%, 1/2 W, Thick Film, 1210	ERJ-14YJ101U	Panasonic
22	1	R6	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
23	1	R7	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
24	1	R8	RES, 11 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ113V	Panasonic
25	1	R10	RES, 215 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2153V	Panasonic
26	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
27	1	T1	Bobbin, EE16, Horizontal, 7 pins (5primary,2secondary)	RH-EE-1606-1	Shenzhen Rui Qi Danend
28	1	U1	LinkSwitch-III, LNK6407D, 1%, SO-8-D	LNK6407D	Power Integrations

6.2 *Miscellaneous Parts*

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	L	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
2	2	N, GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
3	1	+12V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone

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7 Transformer Specification

7.1 *Electrical Diagram*

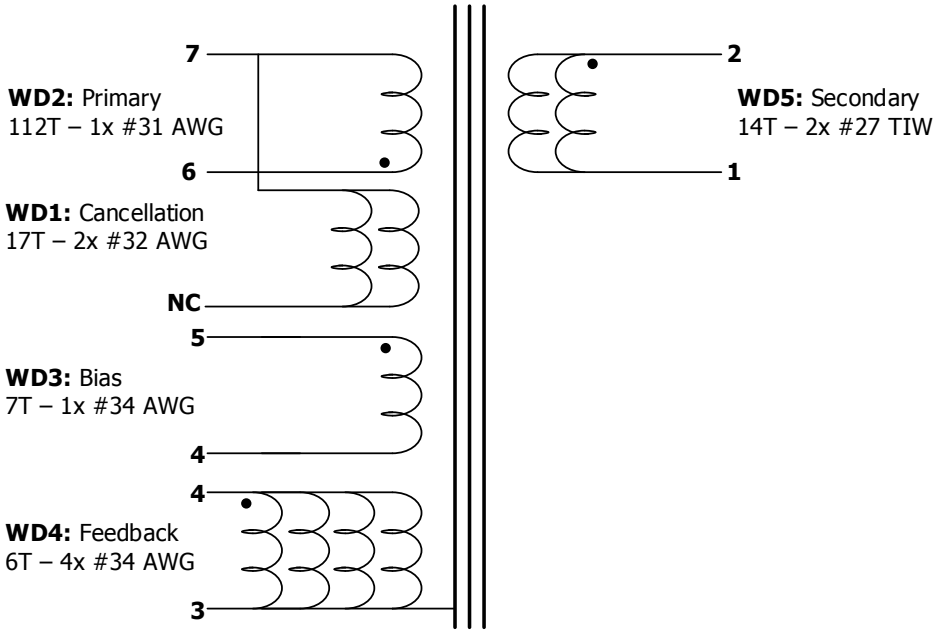

Figure 6– Transformer Electrical Diagram.

7.2 *Electrical Specification*

Electrical Strength	1 sec, 60 Hz, from pins 3-7 to pins 1-2	3000 VAC
Primary Inductance	Pins 6-7, all other windings open, measured at 100 kHz, 1 V_{RMS}.	1270 μH ±10%
Primary Leakage Inductance	Pins 6-7, with pins 1-2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	60 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EE16, Ferrite Core PC40, gapped for ALG of 101nH/T².
[2]	Bobbin: EE-1606-1 Horizontal.
[3]	Magnet Wire: #32 AWG, Double Coated.
[4]	Magnet Wire: #31 AWG, Double Coated.
[5]	Magnet Wire: #34 AWG, Double Coated.
[6]	Triple Insulated Wire: #27 AWG
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 8.43 mm Wide.
[8]	Bus Wire: #30 AWG, Belden Electronics Div; or Equivalent.
[9]	Varnish: Dolph BC-359.
[10]	Tape: 3M 1298 Polyester Film 1 mil thick, 4.5 mm Wide.

7.4 *Transformer Build Diagram*

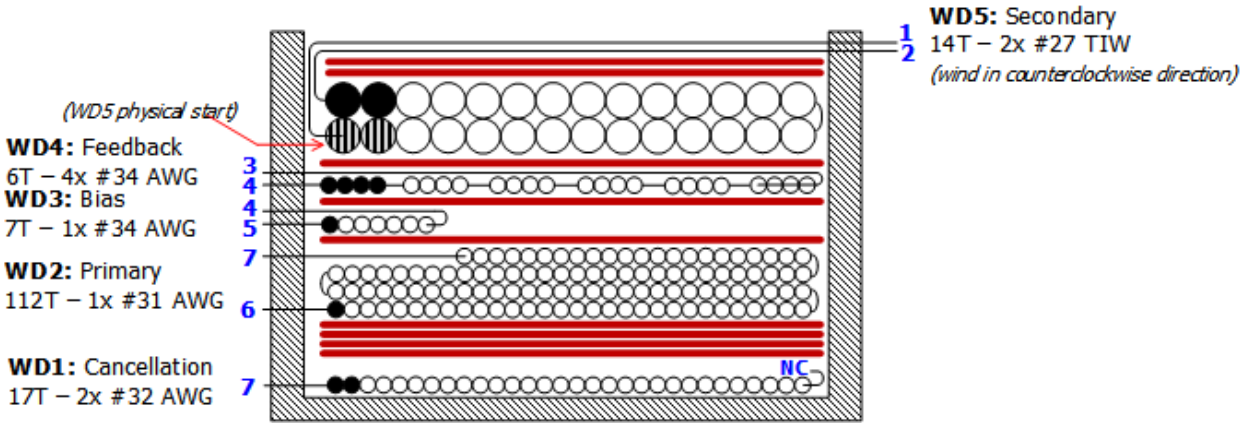

Figure 7– Transformer Build Diagram.

7.5 *Transformer Instructions*

Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that primary side (5-pin) is on the left side with pin 3 at the bottom. Winding direction is clockwise direction.
WD1 Cancellation	Start at pin 7, wind 17 turns (x2 filar) of wire Item [3] in one layer. Last turn will be left floating (not connected).
Insulation	4 layers of tape Item [7] for insulation.
WD2 Primary	Start at pin 6, wind 112 turns (x1 filar) of wire Item [4] in 4 layers with tight tension (Layer 1 –30T, Layer 2 – 30T, Layer 3 – 30T, Layer 4 – 22T). At the last turn, bring the wire back to the left and terminate at pin 7.
Insulation	1 layer of tape Item [7] for insulation.
WD3 Bias	Start at pin 5, wind 7 turns (x1 filar) of wire Item [5]. Terminate winding at pin 4.
Insulation	1 layer of tape Item [7] for insulation.
WD4 Feedback	Start at pin 4, wind 6 turns (x4 filar) of wire Item [5]. Spread the turns across the bobbin width. Terminate at pin 3.
Insulation	1 layer of tape Item [7] for insulation.
WD5 Secondary	Reverse position of the bobbin on winder such that the primary side (5-pin) is on the right side with pin 7 at the bottom. Winding in clockwise direction. Start winding at the right side of the bobbin with 14 turns (x2 filar) of wire Item [6]. Connect the start winding on pin 1 and terminate on pin 2 on the left side of the bobbin.
Insulation	2 layers of tape Item [7] to secure the windings.
Finish	Gap core halves for 1270 μH inductance. Use 2" of bus wire Item [8] solder to pin 3. Wrap core halves and bus wire above which lean along the core with tape Item [10]. Coat with Varnish Item [9].

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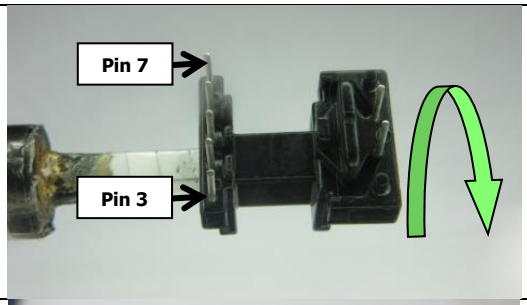
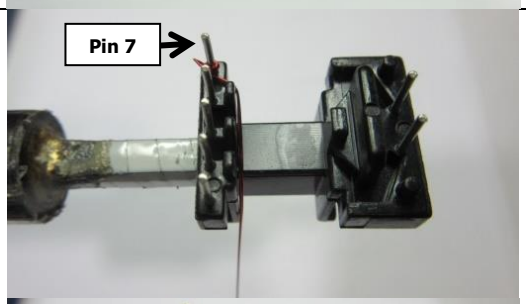
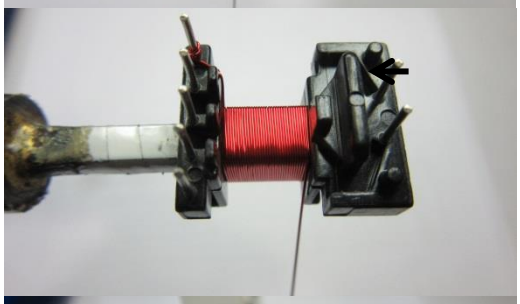
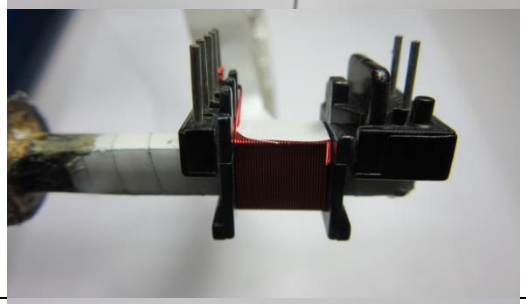
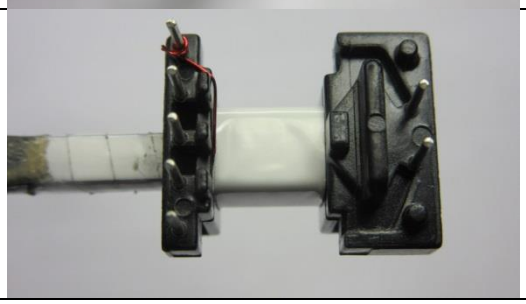
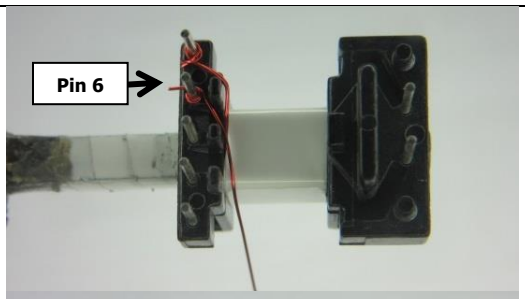
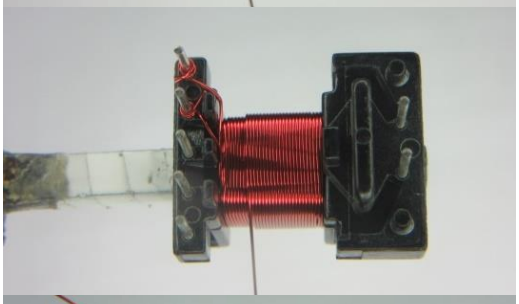
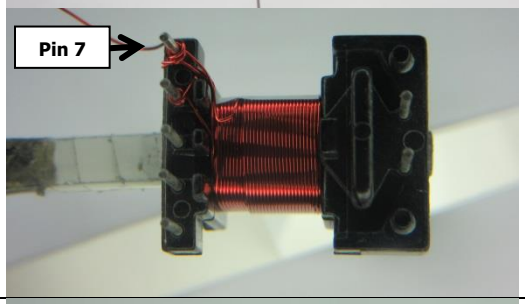
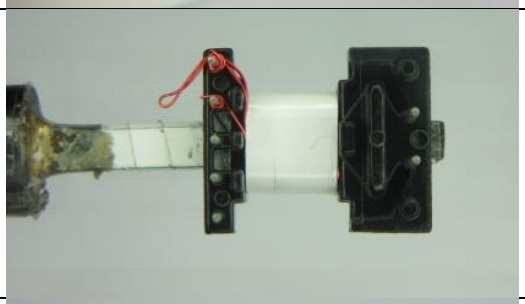
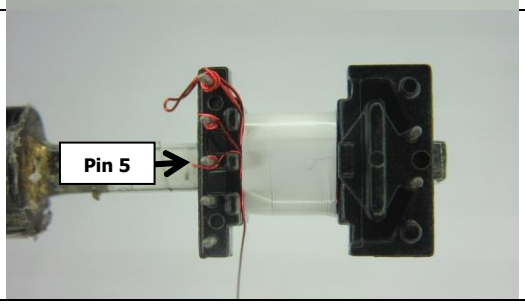
7.6 *Winding Illustrations*

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that primary side (5-pin) is on the left side with Pin 3 at the bottom. Winding direction is clockwise direction.
WD1 Cancellation	  	Start at pin 7, wind 17 turns (x2 filar) of wire Item [3] in one layer. Last turn will be left floating (not connected).
Insulation		4 layers of tape Item [7] for insulation.

WD2 Primary	  	Start at pin 6, wind 112 turns (x1 filar) of wire Item [4] in 4 layers with tight tension (Layer 1 –30T, Layer 2 – 30T, Layer 3 – 30T, Layer 4 – 22T). At the last turn, bring the wire back to the left and terminate at pin 7.
Insulation		1 layer of tape Item [7] for insulation.
WD3 Bias		Start at pin 5, wind 7 turns (x1 filar) of wire Item [5].

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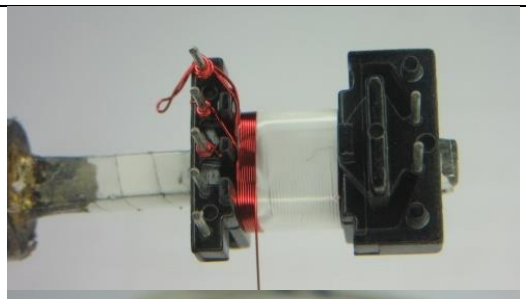
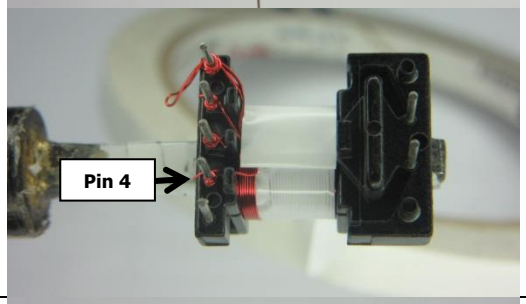
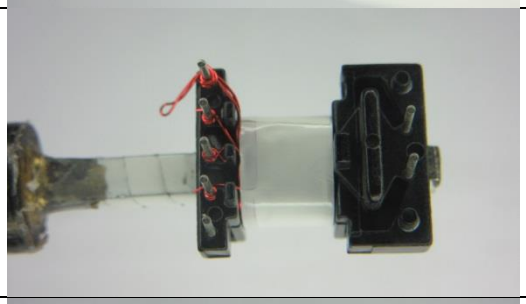
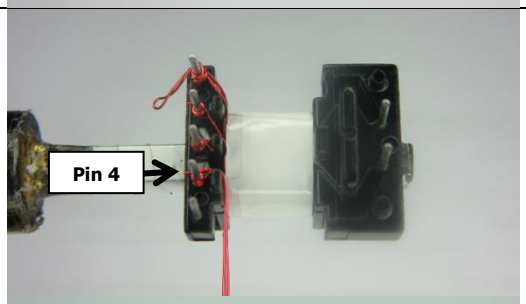
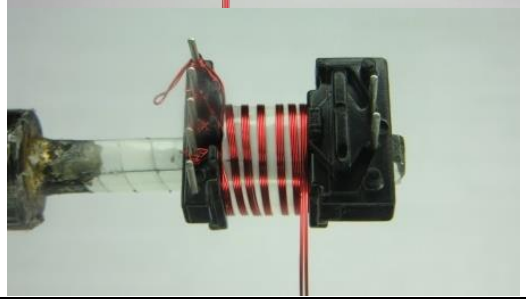
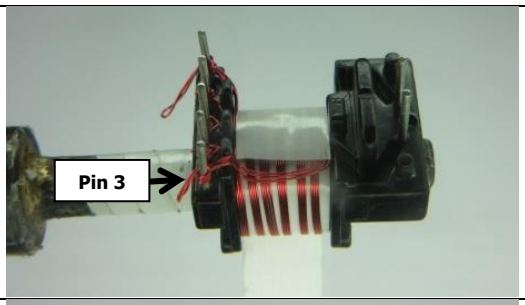
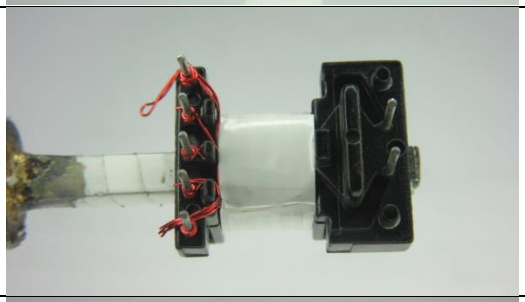
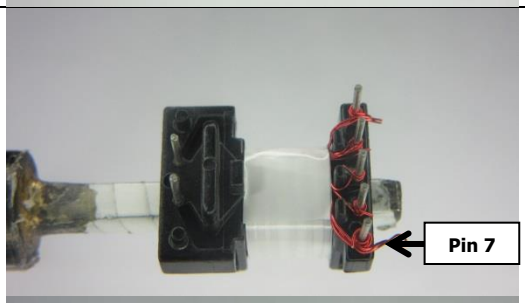
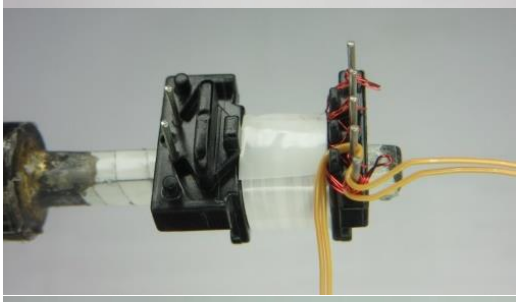
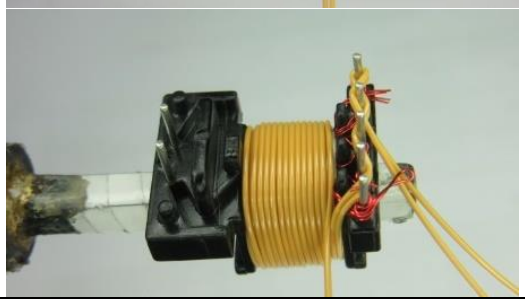
WD3 Bias	 	Terminate winding at pin 4.
Insulation		1 layer of tape Item [7] for insulation.
WD4 Feedback	 	Start at pin 4, wind 6 turns (x4 filar) of wire Item [5]. Distribute the turns across the bobbin width.

WD4 Feedback		Terminate at pin 3.
Insulation		1 layer of tape Item [7] for insulation.
WD5 Secondary	  	Reverse position of the bobbin on winder such that the primary side (5-pin) is on the right side with Pin 7 at the bottom. Winding in clockwise direction. Start winding at the right side of the bobbin with 14 turns (x2 filar) of wire Item [6].

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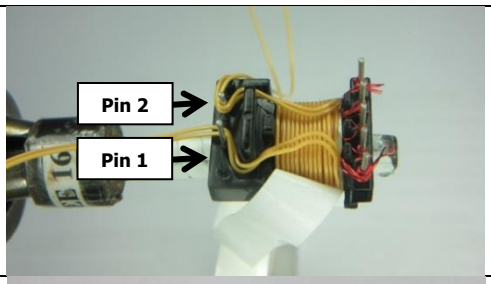
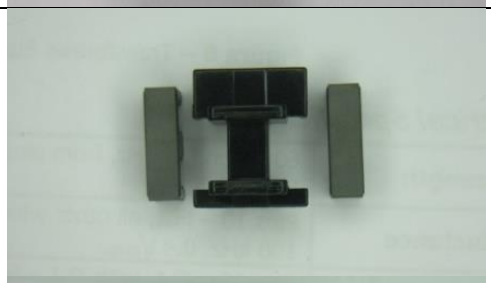
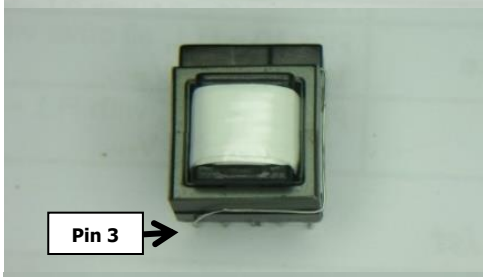
WD5 Secondary		Connect the start winding on Pin 1 and terminate on Pin 2 on the left side of the bobbin.
Insulation		2 layers of tape Item [7] to secure the windings.
Finish		Gap core halves for 1270 μH inductance.
		Use 2” of bus wire Item [8] solder to pin 3.
		Wrap core halves and bus wire above which lean along the core with tape Item [10].
		Coat with varnish Item [9].

8 Transformer Design Spreadsheet

1	ACDC_LinkSwitch-3_080516; Rev.2.3; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-3 Discontinuous Flyback Transformer Design Spreadsheet
2	**ENTER APPLICATION VARIABLES**					
3	VACMIN	90		90	V	Minimum AC Input Voltage
4	VACMAX	265		265	V	Maximum AC Input Voltage
5	fL	50		50	Hz	AC Mains Frequency
6	Application Type	Adapter		Adapter		Choose application type
7	VO	12.00		12.00	V	Output Voltage (at continuous power)
8	IO	0.70		0.70	A	Minimum required output current
9	Power	.	Info	8.40	W	!!! Continuous output power may be too high. Verify thermal performance
10	n	0.84		0.84		Efficiency Estimate at output terminals.
11	Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
12	tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
13	CIN	20.00		20.00	uF	Input Capacitance
15	**ENTER LinkSwitch-3 VARIABLES**					
16	Chosen Device	LNK64x7D		LNK64x7D		Chosen LinkSwitch-3 device and package. E.g. - LNK64x4D or LNK64x8K
17	Cable drop compensation option	1%		1%		Select level of cable drop compensation
18	Complete Part Number			LNK6407D		Full Part Number
19	ILIMITMIN			0.41	A	Minimum Current Limit
20	ILIMITTYP			0.44	A	Typical Current Limit
21	ILIMITMAX			0.47	A	Maximum Current Limit
22	FS	77.50		77.50	kHz	Typical Device Switching Frequency at maximum power
23	VOR			100.00	V	Reflected Output Voltage (VOR < 135 V Recommended)
24	VDS			10.00	V	LinkSwitch-3 on-state Drain to Source Voltage
25	VD	0.50		0.50	V	Output Winding Diode Forward Voltage Drop
26	KP			1.18		KP assuming minimum LP, VMIN, and Maximum Switching Frequency, but not including frequency jitter.
29	**FEEDBACK WINDING PARAMETERS**					
30	NFB	6.00		6.00		Feedback winding turns
31	VFLY			5.36	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
32	VFOR			5.14	V	Forward voltage - Voltage on Feedback Winding during switch on time
34	**BIAS WINDING PARAMETERS**					
35	BIAS	Ext. Bias		Ext. Bias		Select between self bias or external bias to supply the IC. Note that this will affect ILIMIT
36	VB	11.00		11.00	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
37	NB			7.00		Bias Winding number of turns
38	REXT			7.50	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
39	**DESIGN PARAMETERS**					
40	DCON			4.60	us	Desired output diode conduction time
41	DCON_FINAL			4.68	us	Final output conduction diode, assuming integer values for NP and NS, and VMIN
42	TON			4.88	us	LinkSwitch-3 On-time (calculated at LPMIN, VMIN

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						and ILIMITMIN)
43	RUPPER			19.86	k-ohm	Upper resistor in Feedback resistor divider
44	RLOWER			11.27	k-ohm	Lower resistor in resistor divider
46	**ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES**					
47	**Core Type**					
48	Core	EE16		EE16		Enter Transformer Core.
49	Custom_Core					Enter Core name if selection on drop down menu is "Custom"
50	Bobbin			BE-16-116CP		Bobbin part number
51	AE			19.20	mm^2	Core Effective Cross Sectional Area
52	LE			35.00	mm	Core Effective Path Length
53	AL			1140.00	nH/turn^2	Ungapped Core Effective Inductance
54	BW	8.00		8.00	mm	Bobbin Physical Winding Width
55	M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
56	L	4.00		3.00		Number of Primary Layers
57	NS			14.00	turns	Number of Secondary Turns. To adjust Secondary number of turns change DCON
59	**DC INPUT VOLTAGE PARAMETERS**					
60	VMIN			95.92	V	Minimum DC bus voltage
61	VMAX			374.77	V	Maximum DC bus voltage
63	**CURRENT WAVEFORM SHAPE PARAMETERS**					
64	DMAX			0.47		Maximum duty cycle measured at VMIN
65	IAVG			0.12	A	Input Average current, at VMIN
66	IP			0.41	A	Peak primary current
67	IR			0.41	A	Primary ripple current
68	IRMS			0.19	A	Primary RMS current
70	**TRANSFORMER PRIMARY DESIGN PARAMETERS**					
71	LPMIN			1142.65	uH	Minimum Primary Inductance
72	LPTYP			1269.62	uH	Typical Primary inductance
73	LP_TOLERANCE	10.00		10.00	%	Tolerance in primary inductance
74	NP			112.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
75	ALG			101.21	nH/turn^2	Gapped Core Effective Inductance
76	BM_TARGET			2600.00	Gauss	Target Flux Density
77	BM		Info	2603.70	Gauss	Maximum Operating Flux Density (calculated with LPTYP, ILIMITTYP), BM < 2600 is recommended
78	BP			3061.83	Gauss	Peak Operating Flux Density (calculated with LPMAX, ILIMITMAX), BP < 3100 is recommended
79	BAC			1301.85	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
80	ur			165.37		Relative Permeability of Ungapped Core
81	LG			0.24	mm	Gap Length (LG > 0.1 mm)
82	BWE			32.00	mm	Effective Bobbin Width
83	OD	0.28		0.28	mm	Maximum Primary Wire Diameter including insulation
84	INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
85	DIA			0.23	mm	Bare conductor diameter
86	AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
87	CM			80.63	Cmils	Bare conductor effective area in circular mils
88	CMA			432.83	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
89						
90	**TRANSFORMER SECONDARY DESIGN PARAMETERS**					
91						
92	ISP			3.28	A	Peak Secondary Current assuming Ilimitmin
93	ISRMS			1.46	A	Secondary RMS Current assuming Ilimitmax and Dmax
94	IRIPPLE			1.28	A	Output Capacitor RMS Ripple Current

95	CMS			291.93	Cmils	Secondary Bare Conductor minimum circular mils
96	AWGS			25.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
98	**VOLTAGE STRESS PARAMETERS**					
99	VDRAIN			604.77	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
100	PIVS			78.18	V	Output Rectifier Maximum Peak Inverse Voltage
102	**FINE TUNING**					
103	RUPPER_ACTUAL	20.50		20.50	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
104	RLOWER_ACTUAL	12.10		12.10	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
105	Actual (Measued) Output Voltage (VDC)			12.00	V	Measured Output voltage from first prototype
106	Actual (Measured) Output Current (ADC)			0.70	Amps	Measured Output current from first prototype
107	RUPPER_FINE			20.50	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 20.5 k-ohms
108	RLOWER_FINE			12.10	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 12.1 k-ohms

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9 Performance Data

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

9.1 *Average Efficiency*

9.1.1 Efficiency Requirements

Test	Average	Average	Average	Average	10% Load	10% Load
Model	Standard	Basic Voltage	Basic Voltage	Basic Voltage	Basic Voltage	Basic Voltage
Effective	Now	2016	Now	2016	Now	2016
Power [W]	**Energy Star 2**	**DoE Level VI**	**CoC v5 Tier 1**	**CoC v5 Tier 2**	**CoC v5 Tier 1**	**CoC v5 Tier 2**
8.4	**75.52%**	**80.93%**	**77.92%**	**81.14%**	**67.92%**	**71.14%**

9.1.2 Average Efficiency Measured (Across PCB Connector)

Load (%)	115 VAC (%)	230 VAC (%)
100	83.48	83.62
75	83.14	83.10
50	82.76	80.16
25	81.00	78.74
10	77.89	76.52
Average	**82.59**	**81.41**

9.1.3 Average Efficiency Measured (at the End of 100 mΩ Cable)

Load (%)	115 VAC (%)	230 VAC (%)
100	82.90	83.16
75	82.74	82.69
50	82.44	79.87
25	80.68	78.44
10	77.07	75.21
Average	**82.19**	**81.04**

9.2 *Efficiency vs. Line*

Soak for 20 minutes and 5 minutes for each line/step.

9.2.1 Measured at 0.7 A Full Load.

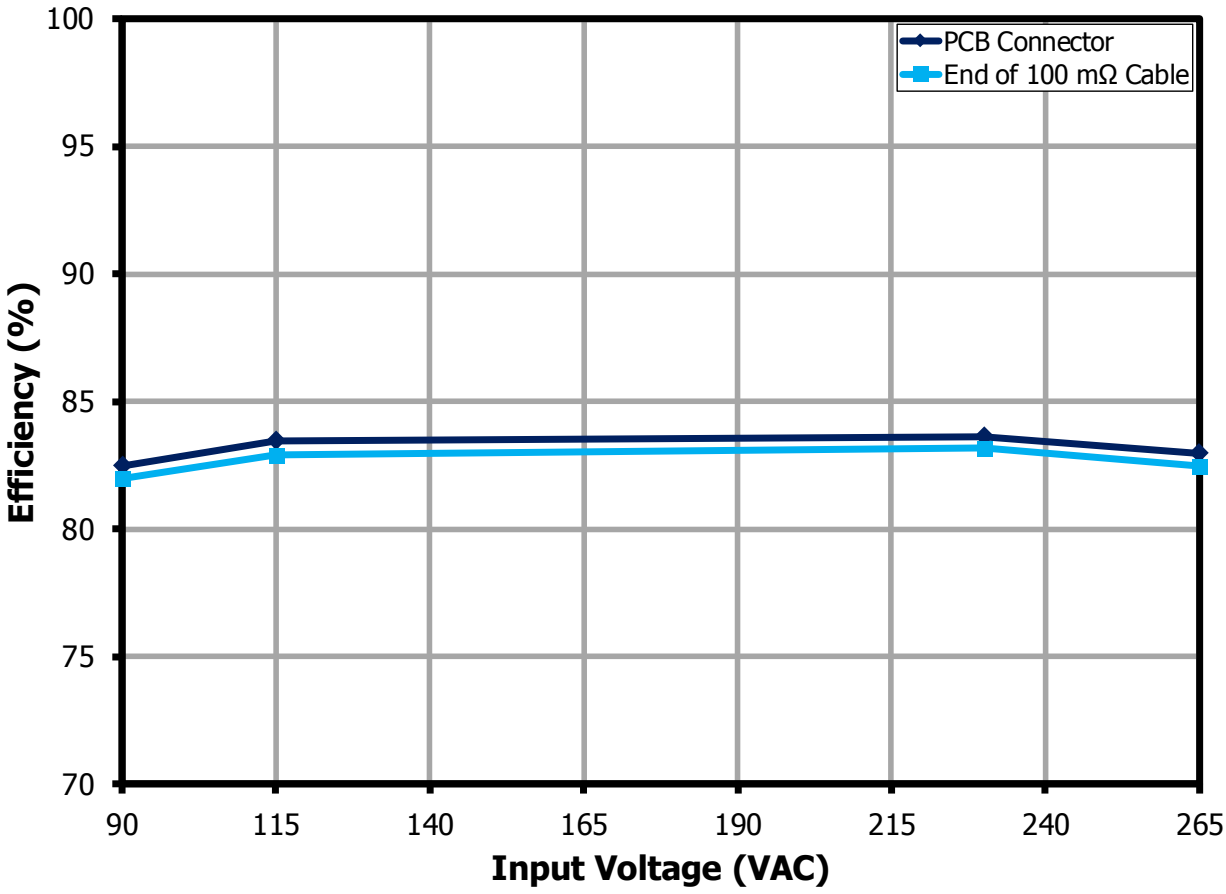

Figure 8 – Efficiency vs. Line.

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9.3 *Efficiency vs. Load*

Soak for 5 minutes and 30 seconds for each load step.

9.3.1 Measured across PCB connector

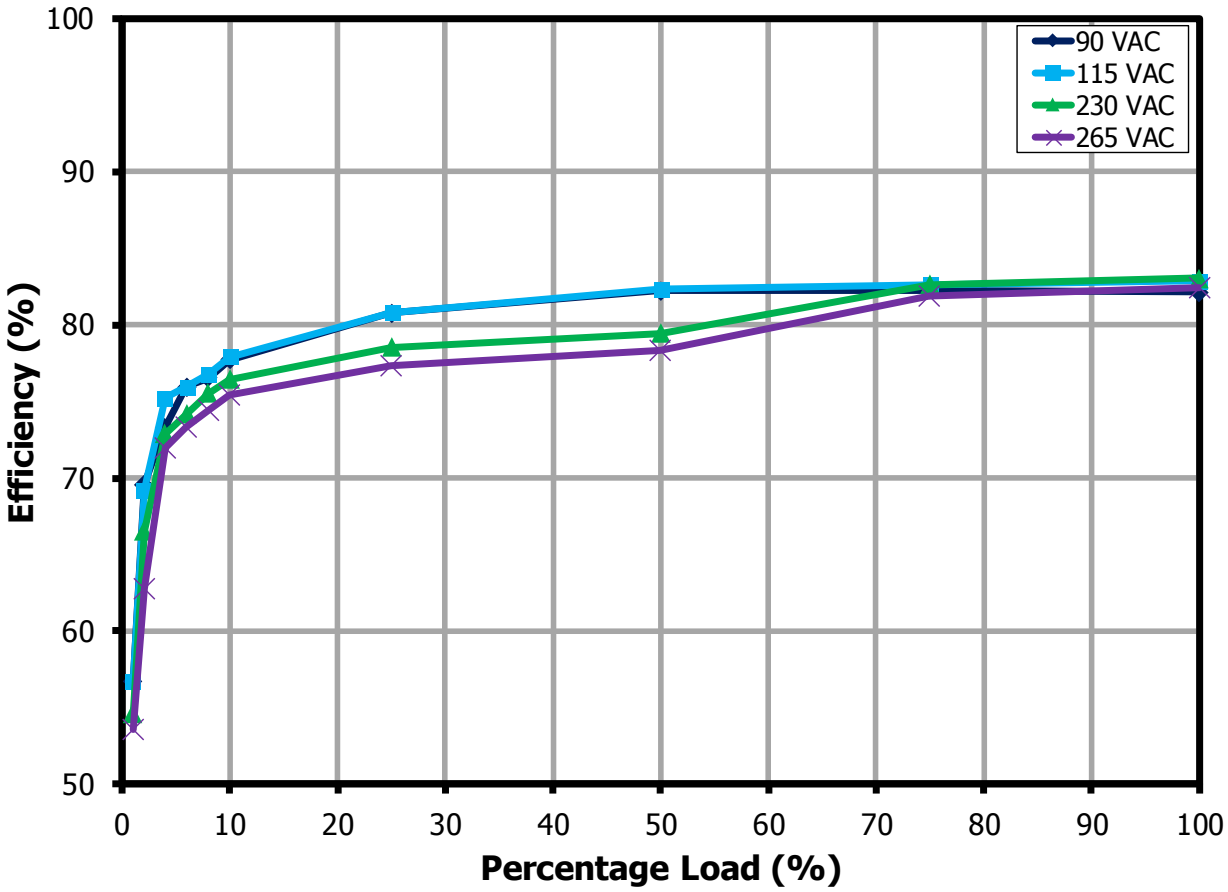

Figure 9 – Efficiency vs. Load (Measured Across PCB Connector).

9.3.2 Measured at the End 100 mΩ Cable

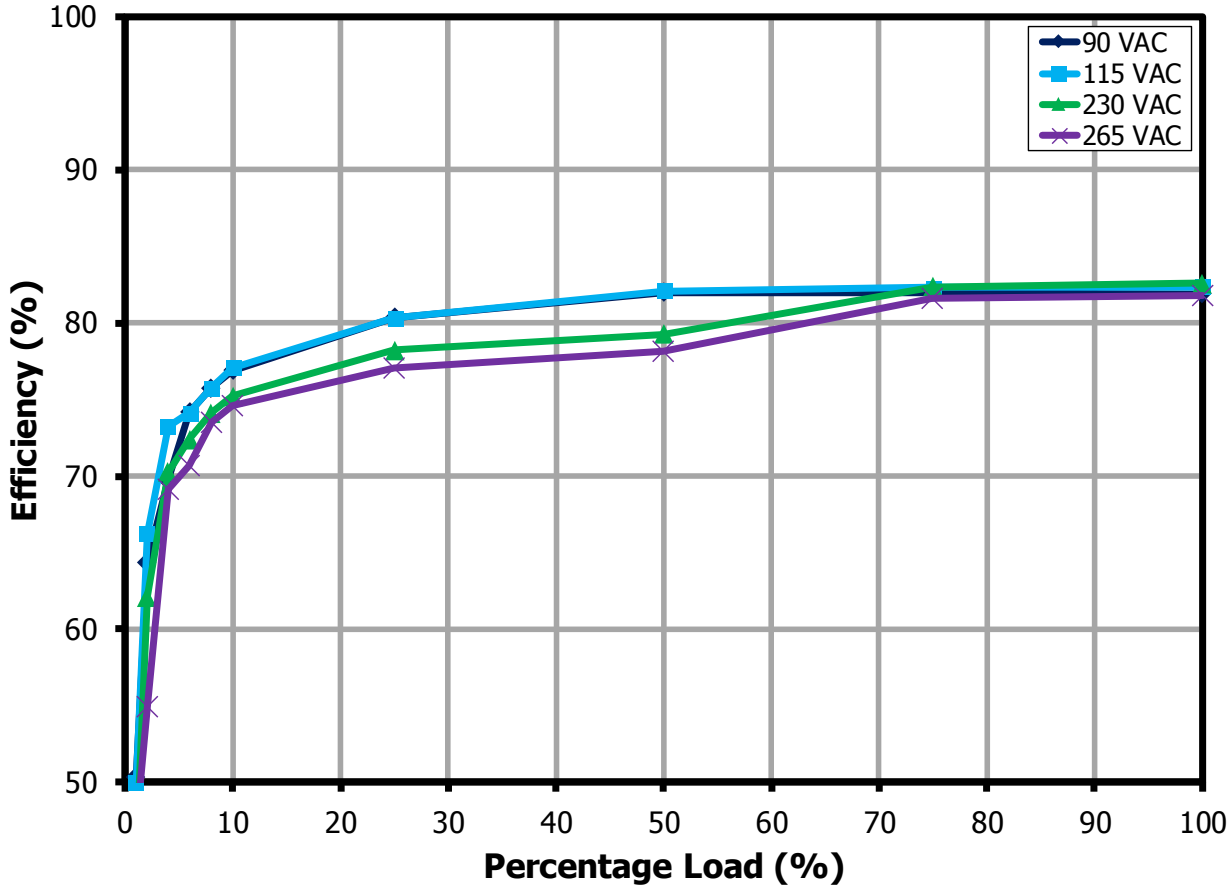

Figure 10 – Efficiency vs Load (Measured at the End of 1.2m #22 Cable).

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10 CV/CC Regulation

10.1 *CV/CC Regulation at 25 ºC Measured Across PCB Connector*

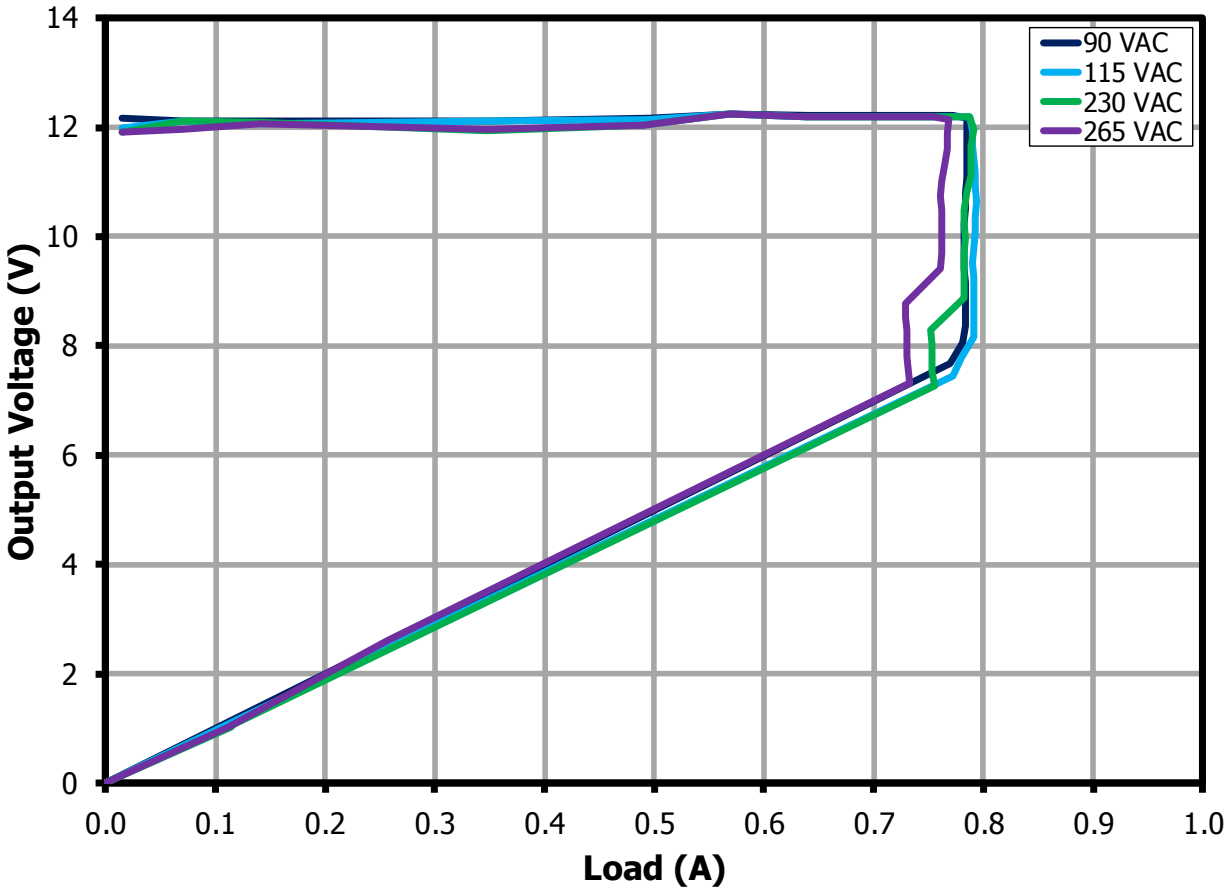

Figure 11 – CV/CC across PCB connector. Room Temperature.

10.2 *CV/CC Regulation at 25 ºC Measured on End of 100 mΩ Cable*

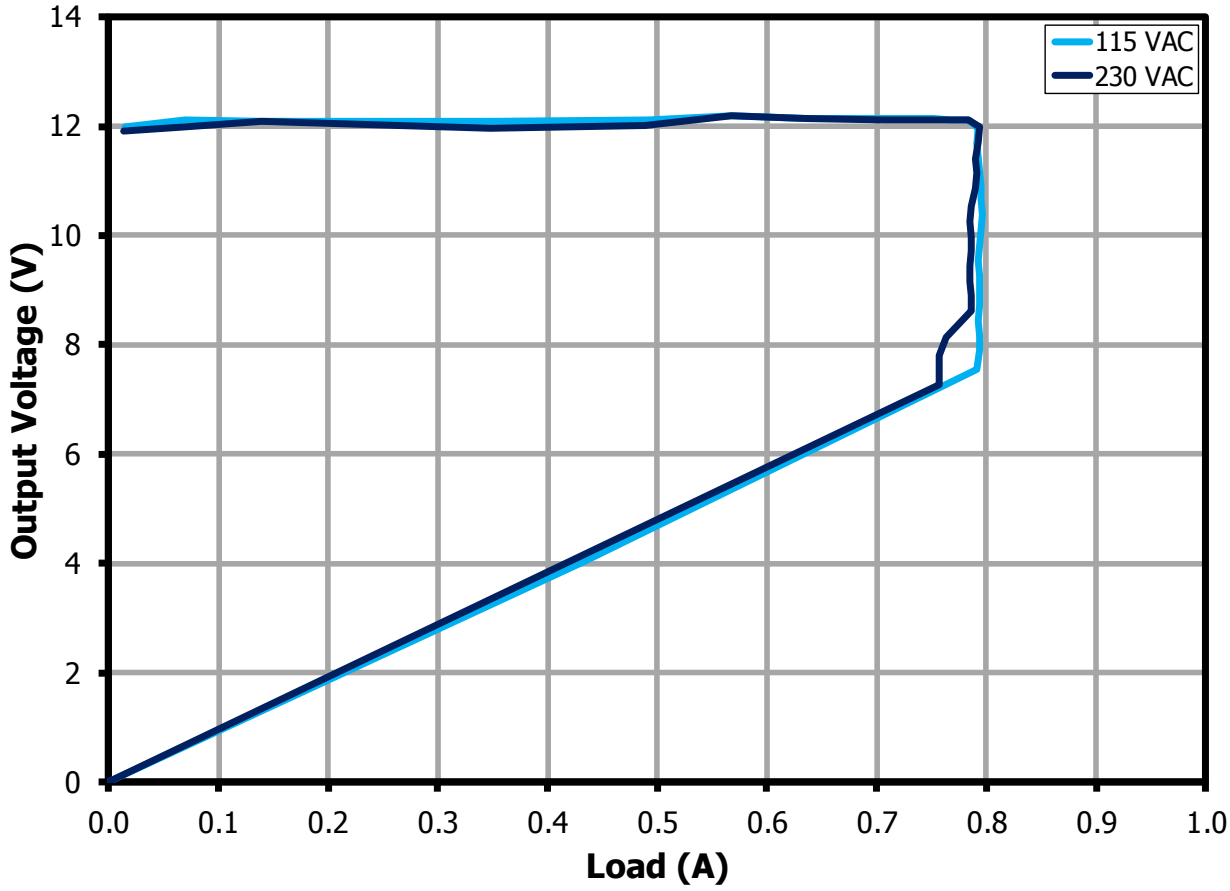

Figure 12 – CV/CC Measured at the End of 100 mΩ Cable. Room Temperature.

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10.3 ***CV/CC Regulation at Hot and Cold Temperature***

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Ambient temperature inside was measured using type T thermocouple.

Figure 13 – Test Set-up.

10.3.1 90 VAC

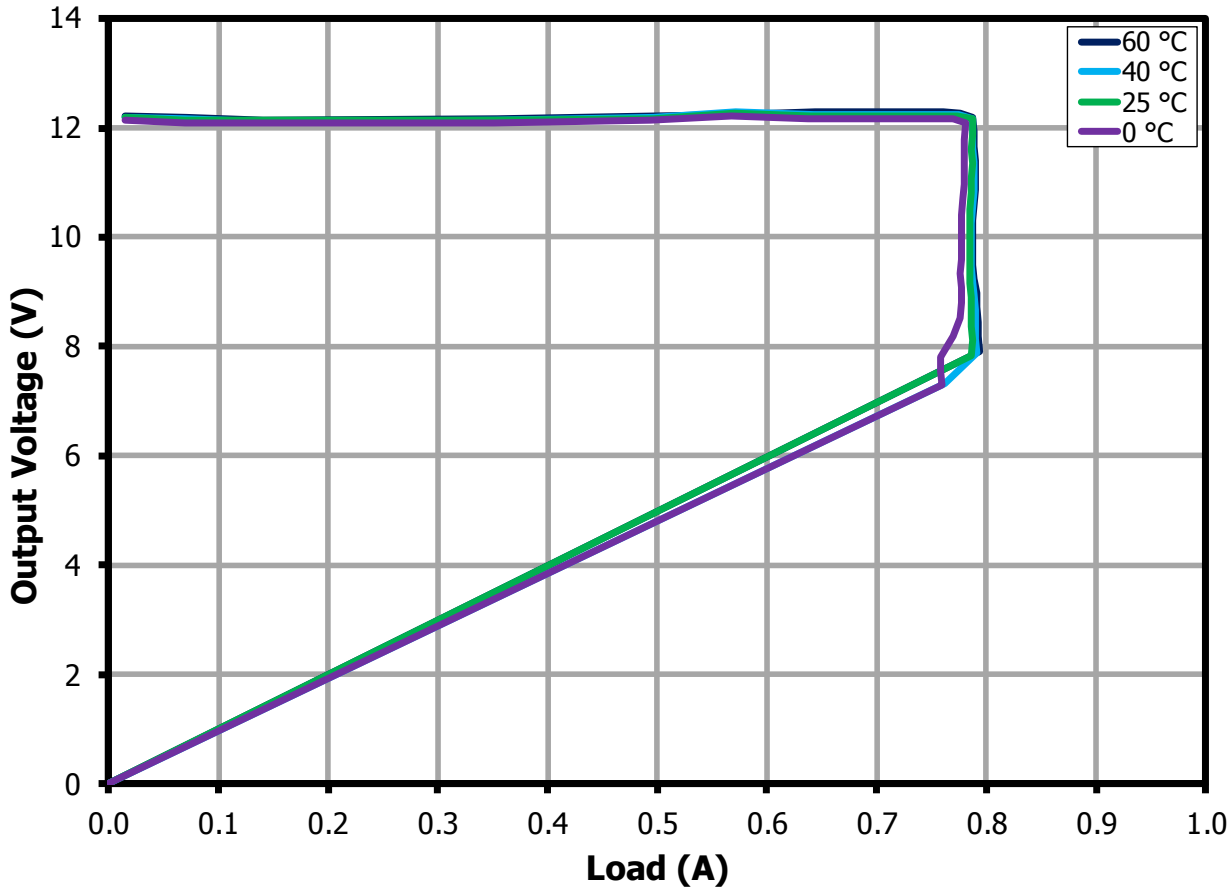

Figure 14 – 90 VAC CV/CC Measured at the End of 100 mΩ Cable.

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10.3.2 115 VAC

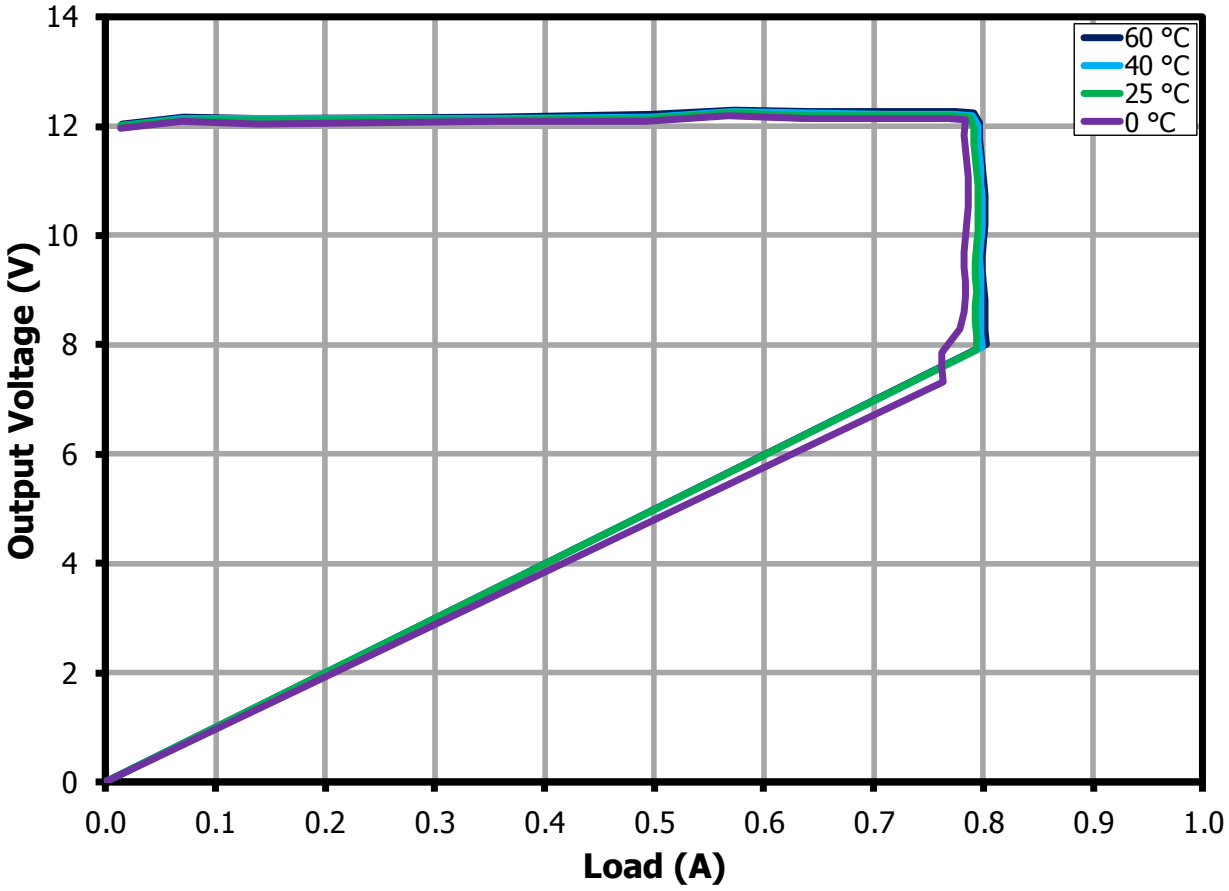

Figure 15 – 115 VAC CV/CC Measured at the End of 100 mΩ Cable.

10.3.3 230 VAC

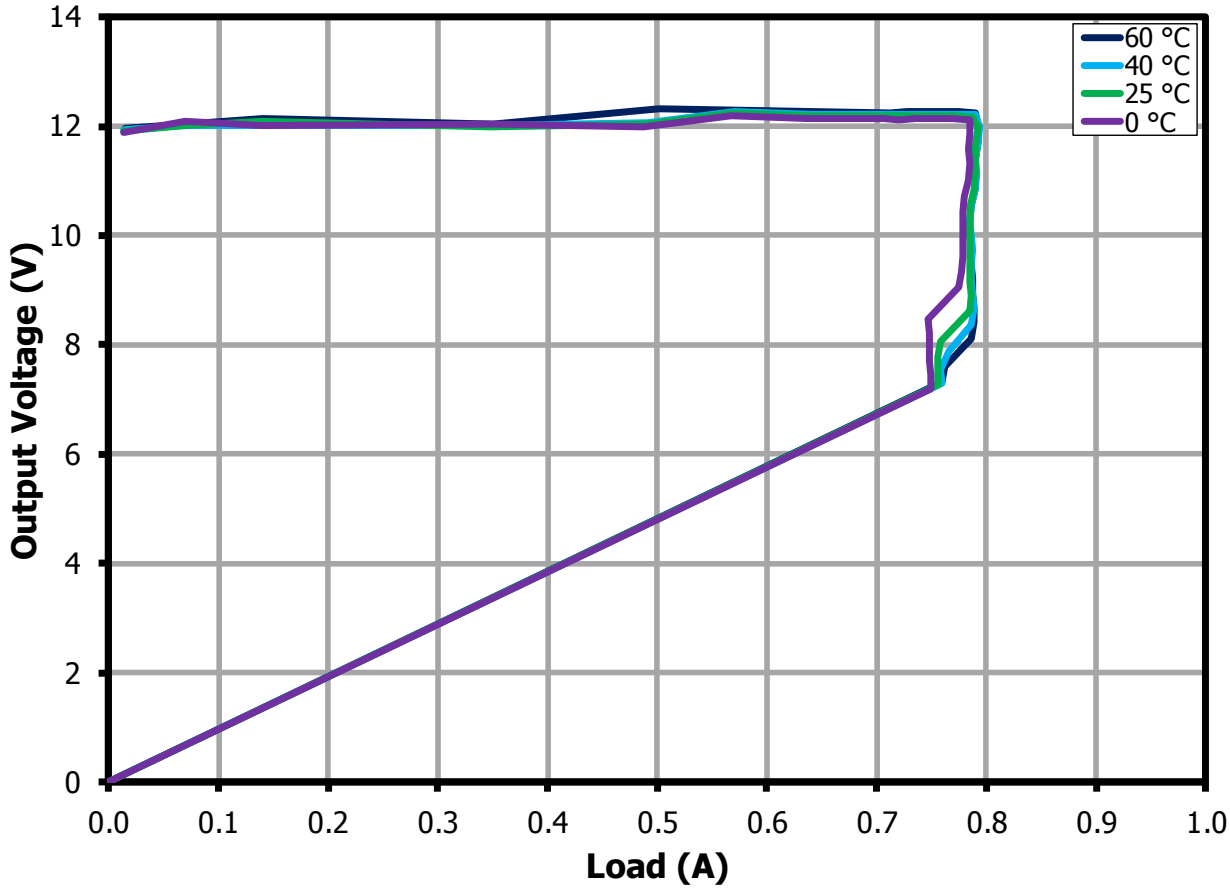

Figure 16 – 230 VAC CV/CC Measured at the End of 100 mΩ Cable.

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10.3.4 265 VAC

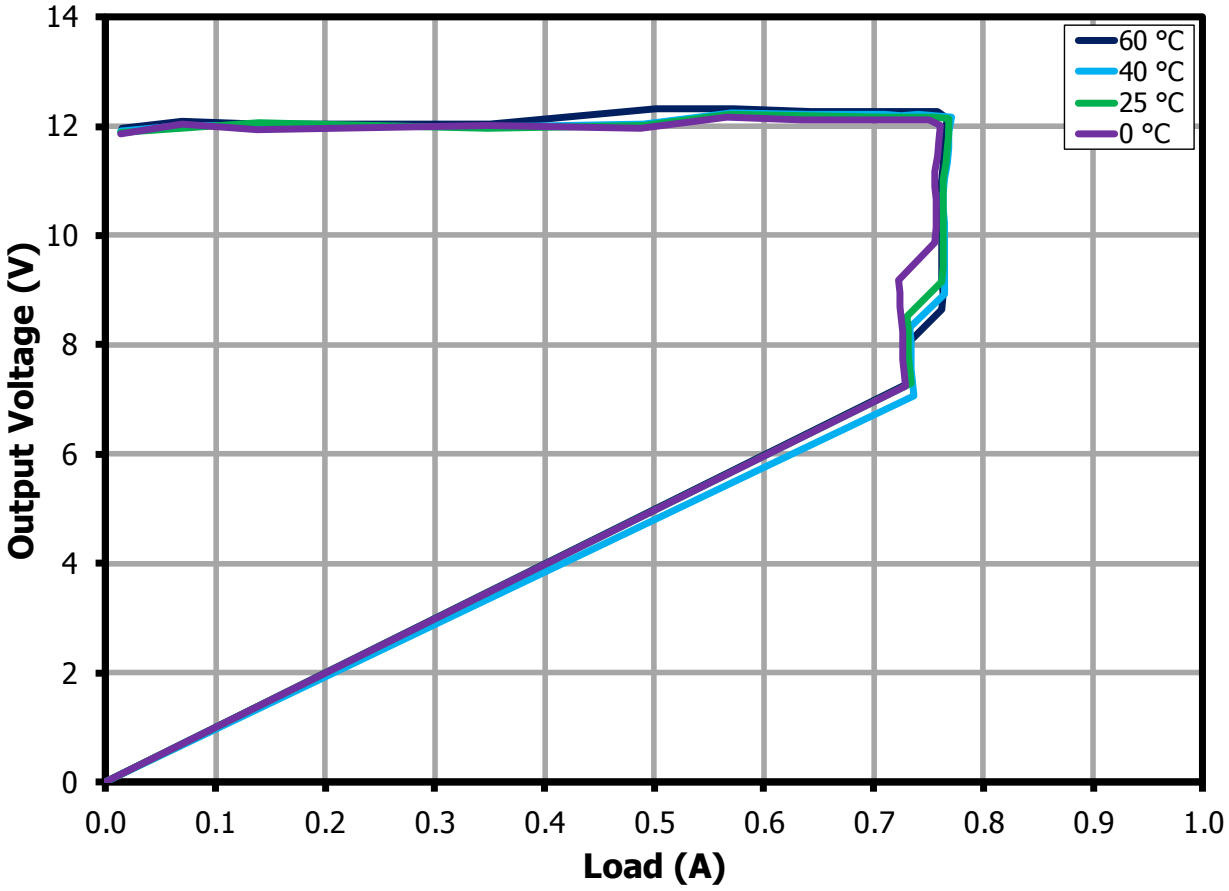

Figure 17 – 265 VAC CV/CC Measured at the End of 100 mΩ Cable.

11 No-Load Input Power

Soak for 15 minutes and 3 minutes integration time for each line/step.

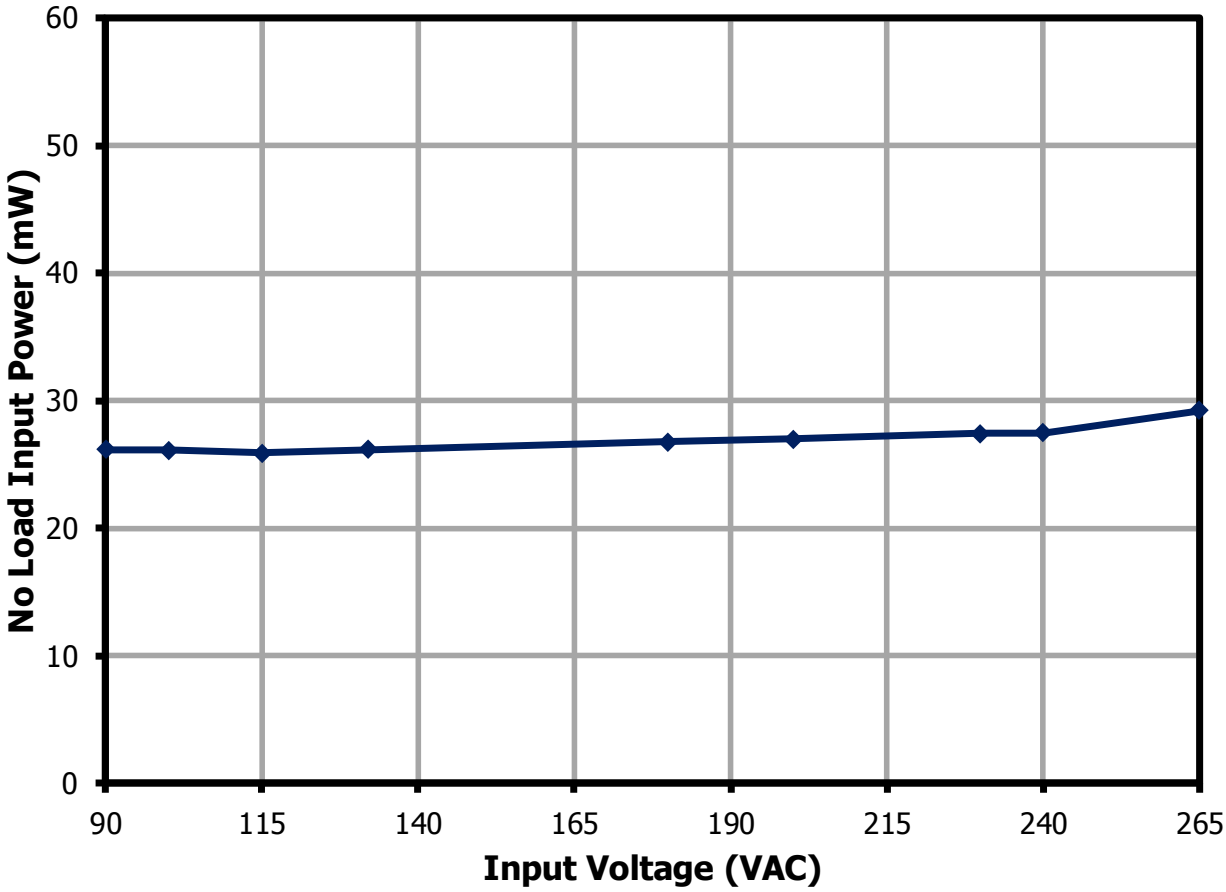

Figure 18 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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12 Line Regulation

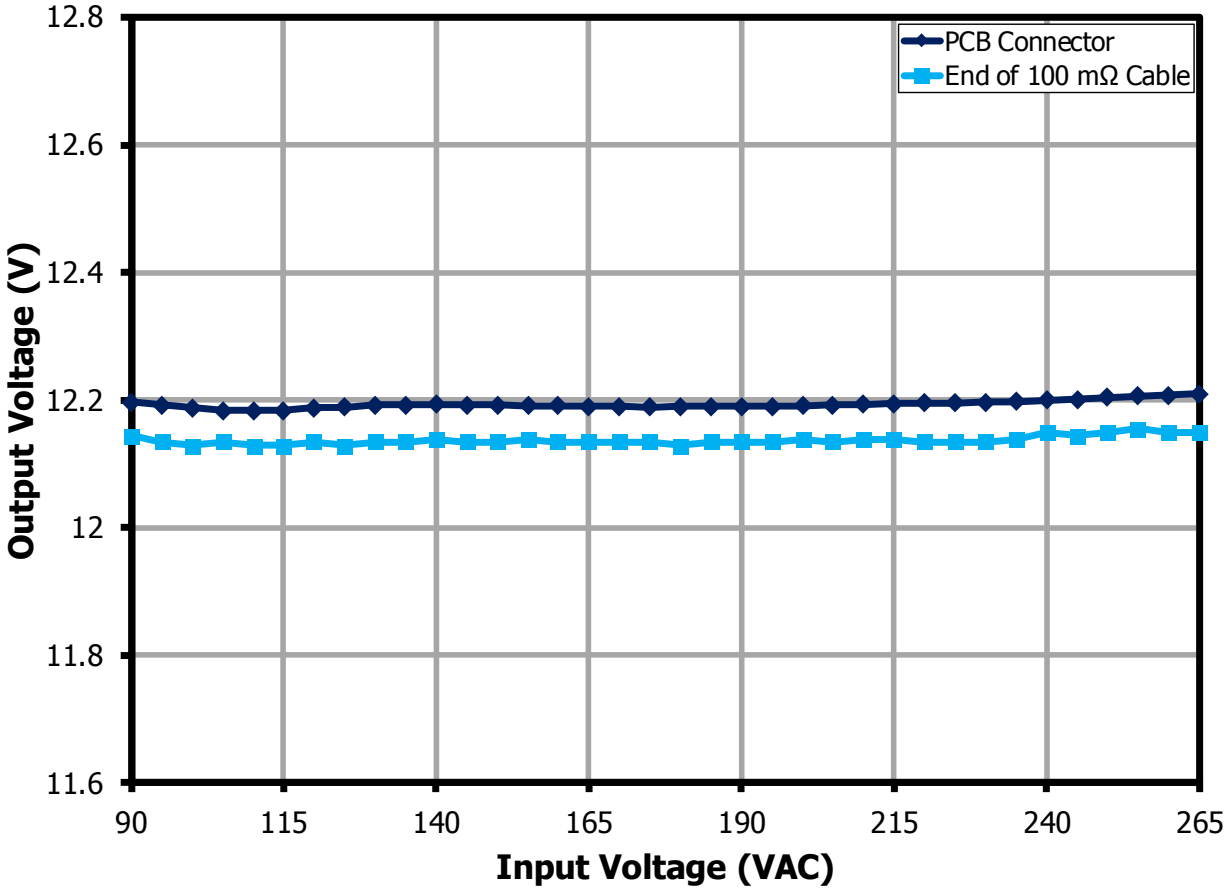

Figure 19 – Line Regulation.

13 Load Regulation

13.1.1 Measured across PCB connector

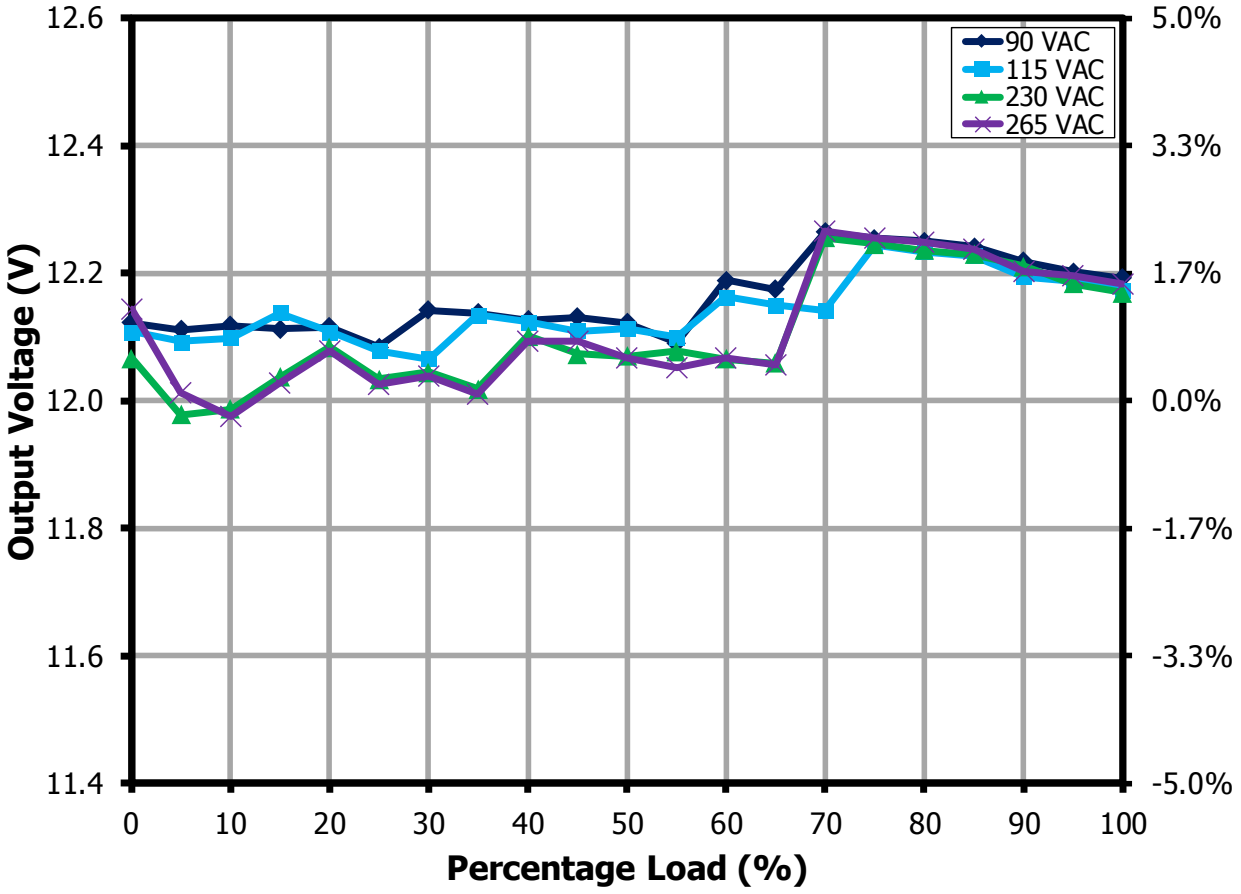

Figure 20 – Load Regulation (Across PCB Connector).

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13.1.2 Measured at the End of 100 mΩ Cable

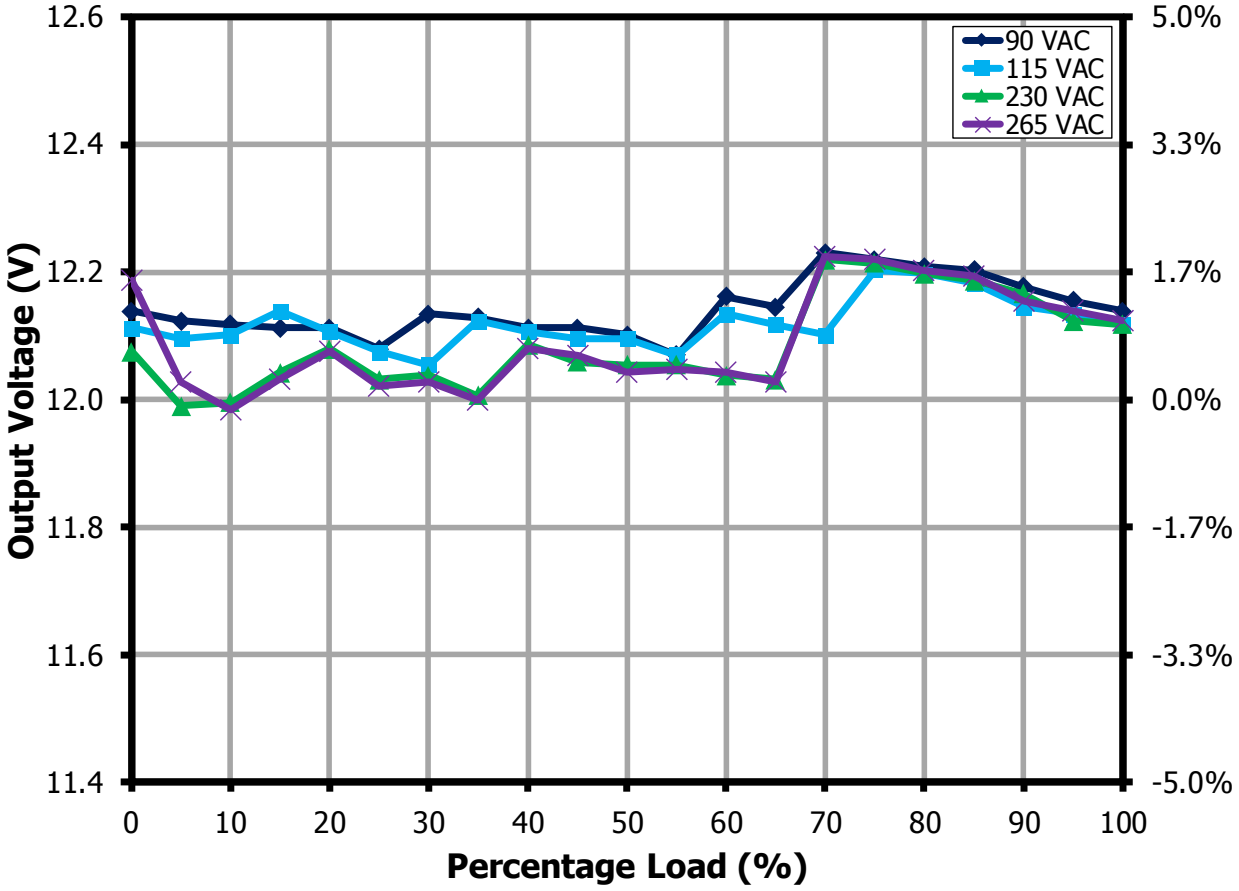

Figure 21 – Load Regulation (At End of 100 mΩ Cable).

14 Thermal Performance

14.1 *Thermal Scan at Room Temperature*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Temperature was measured using Thermal Camera. Soak time at full load is 2 hours.

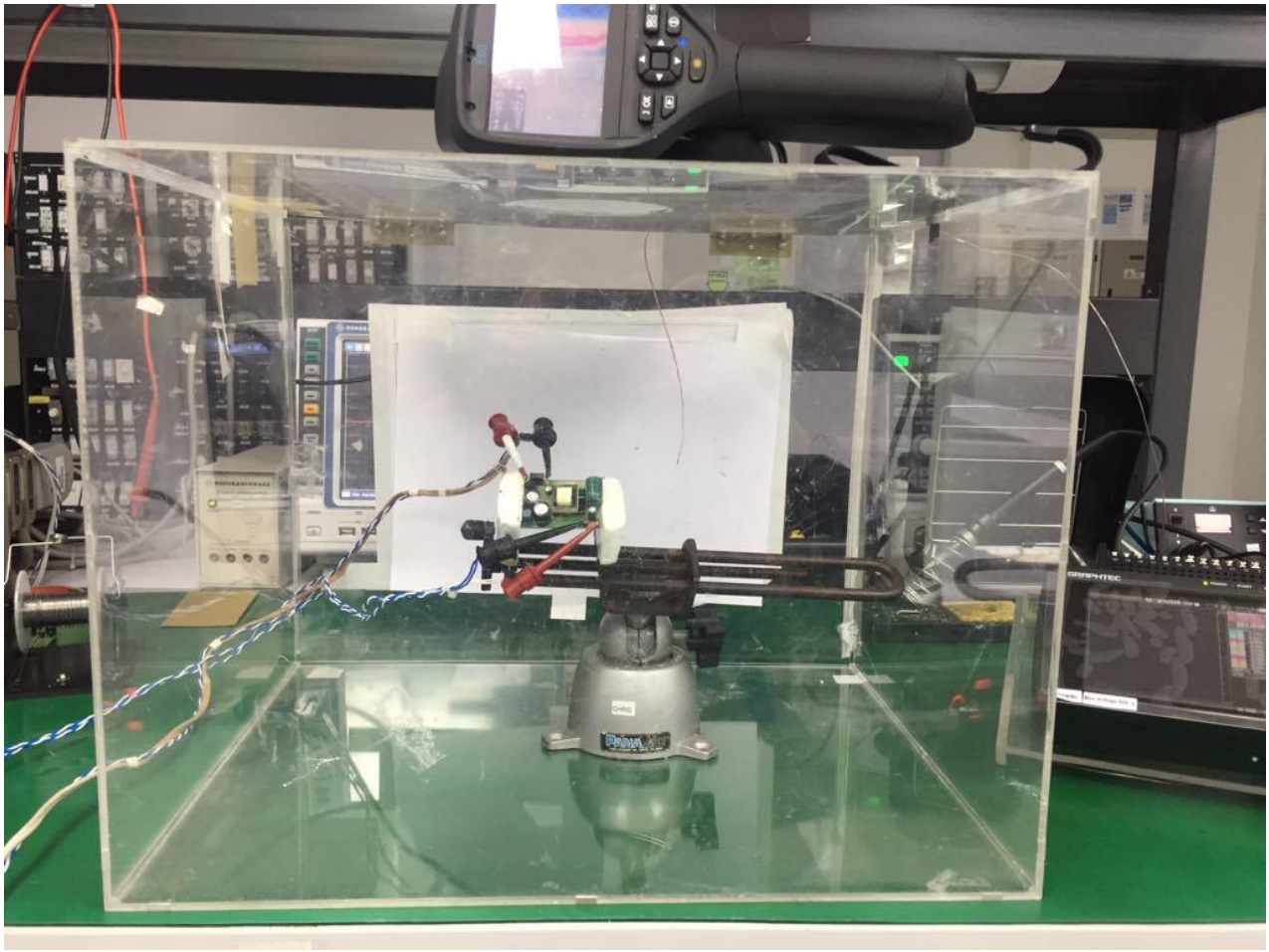

Figure 22 – Test Set-up.

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14.1.1 90 VAC

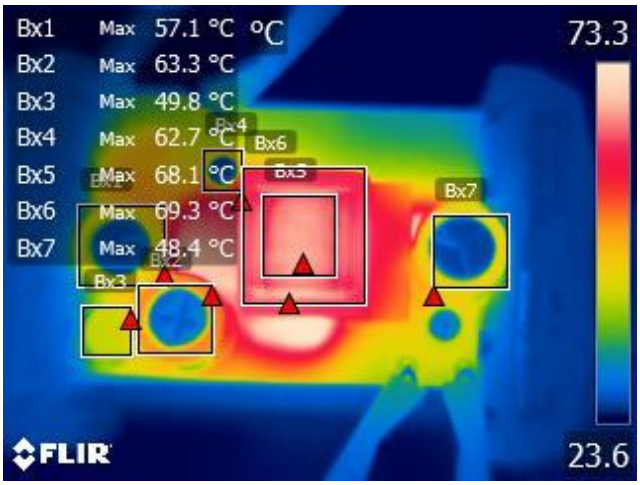

Figure 23 – 90 VAC, 0.7 A Load. Top Side. Ambient = 27.5 ºC.

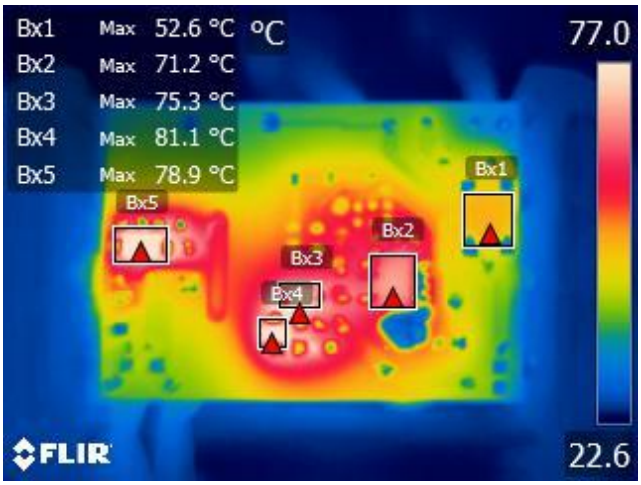

Figure 24 – 90 VAC, 0.7 A Load. Bottom Side. Ambient = 27.5 ºC.

Component	Temperature (ºC)
IC (U1)	71.2
Bridge Rectifier (BR1)	52.6
Freewheel Diode (D1)	78.9
Snubber Diode (D3)	81.1
Input Choke (L1)	49.8
Transformer-Core (T1-core)	69.3
Transformer-Winding (T1-wdg)	68.1
Input Capacitor (C1)	57.1
Input Capacitor (C2)	63.3
Output Capacitor (C3)	48.4
Bias Capacitor (C4)	62.7
Snubber Resistor (R5)	81.1

14.1.2 115 VAC

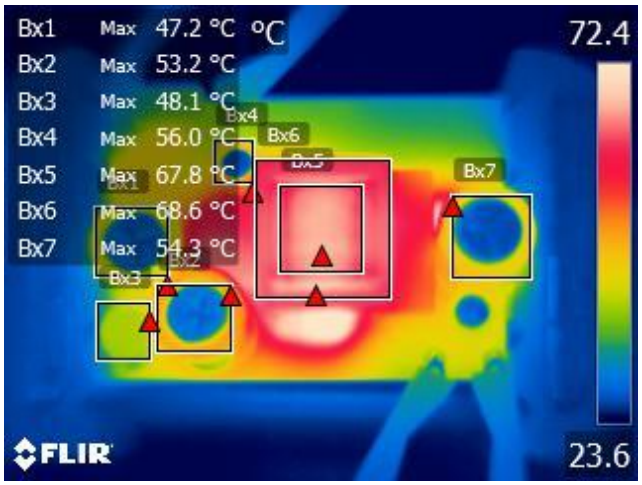

Figure 25 – 115 VAC, 0.7 A Load. Top Side. Ambient = 27.5 ºC.

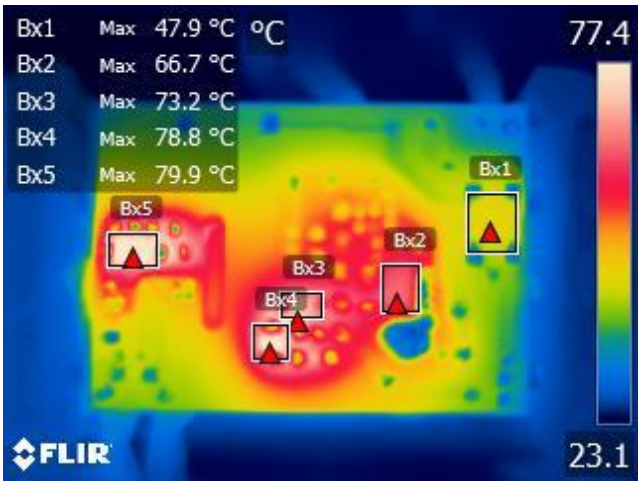

Figure 26 – 115 VAC, 0.7 A Load. Bottom Side. Ambient = 27.5 ºC.

Component	Temperature (ºC)
IC (U1)	66.7
Bridge Rectifier (BR1)	47.9
Freewheel Diode (D1)	79.9
Snubber Diode (D3)	73.2
Input Choke (L1)	48.1
Transformer-Core (T1-core)	68.6
Transformer-Winding (T1-wdg)	67.8
Input Capacitor (C1)	47.2
Input Capacitor (C2)	53.2
Output Capacitor (C3)	54.3
Bias Capacitor (C4)	56.0
Snubber Resistor (R5)	78.8

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14.1.3 230 VAC

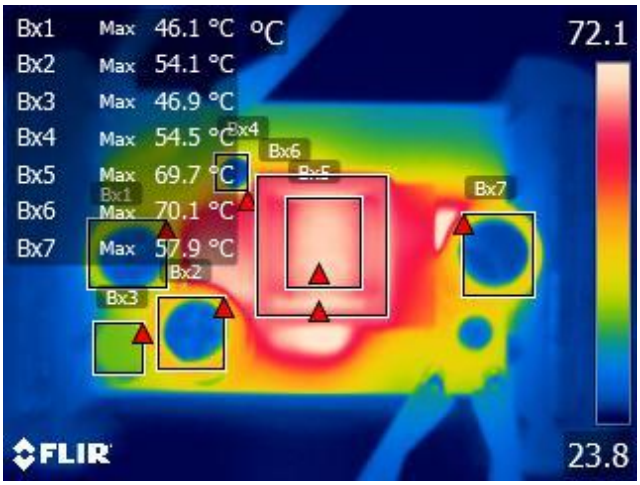

Figure 27 – 230 VAC, 0.7 A Load. Top Side. Ambient = 27.5 ºC.

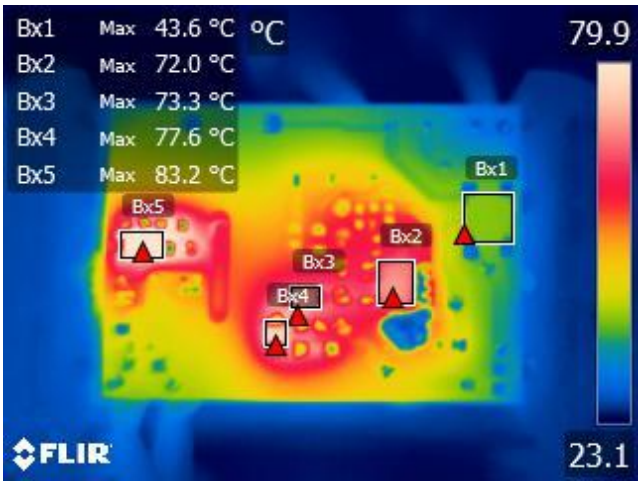

Figure 28 – 230 VAC, 0.7 A Load. Bottom Side. Ambient = 27.5 ºC.

Component	Temperature (ºC)
IC (U1)	72.0
Bridge Rectifier (BR1)	43.6
Freewheel Diode (D1)	83.2
Snubber Diode (D3)	73.3
Input Choke (L1)	46.9
Transformer-Core (T1-core)	70.1
Transformer-Winding (T1-wdg)	69.7
Input Capacitor (C1)	46.1
Input Capacitor (C2)	54.1
Output Capacitor (C3)	57.9
Bias Capacitor (C4)	54.5
Snubber Resistor (R5)	77.6

14.1.4 265 VAC

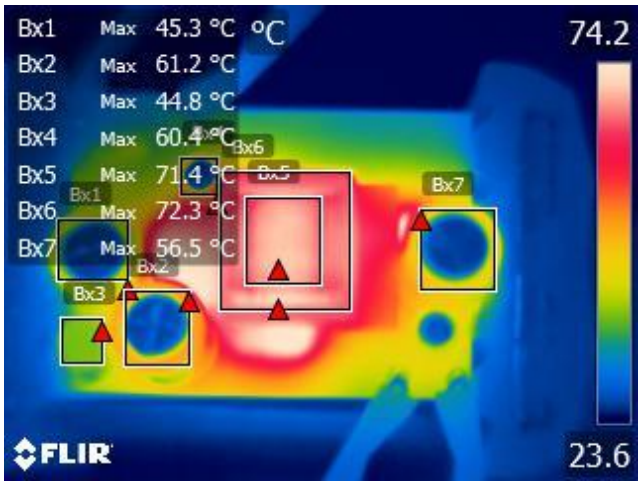

Figure 29 – 265 VAC, 0.7 A Load. Top Side. Ambient = 27.5 ºC.

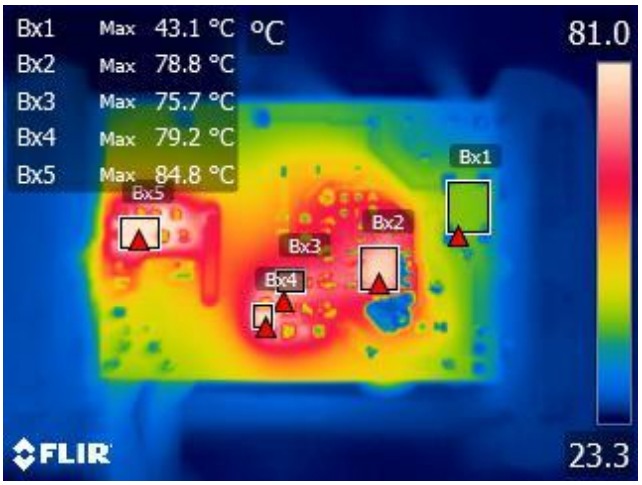

Figure 30 – 265 VAC, 0.7 A Load. Ambient = 27.5 ºC.

Component	Temperature (ºC)
IC (U1)	78.8
Bridge Rectifier (BR1)	43.1
Freewheel Diode (D1)	84.4
Snubber Diode (D3)	75.7
Input Choke (L1)	44.8
Transformer-Core (T1-core)	72.3
Transformer-Winding (T1-wdg)	71.4
Input Capacitor (C1)	45.3
Input Capacitor (C2)	61.2
Output Capacitor (C3)	56.5
Bias Capacitor (C4)	60.4
Snubber Resistor (R5)	79.2

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15 Thermal Performance at 70 °C

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Ambient temperature inside enclosure is 70 ºC. Temperature was measured using type T thermocouple. Soak time at full load is 1 hour.

Figure 31 – Test Set-up.

15.1 *90 VAC*

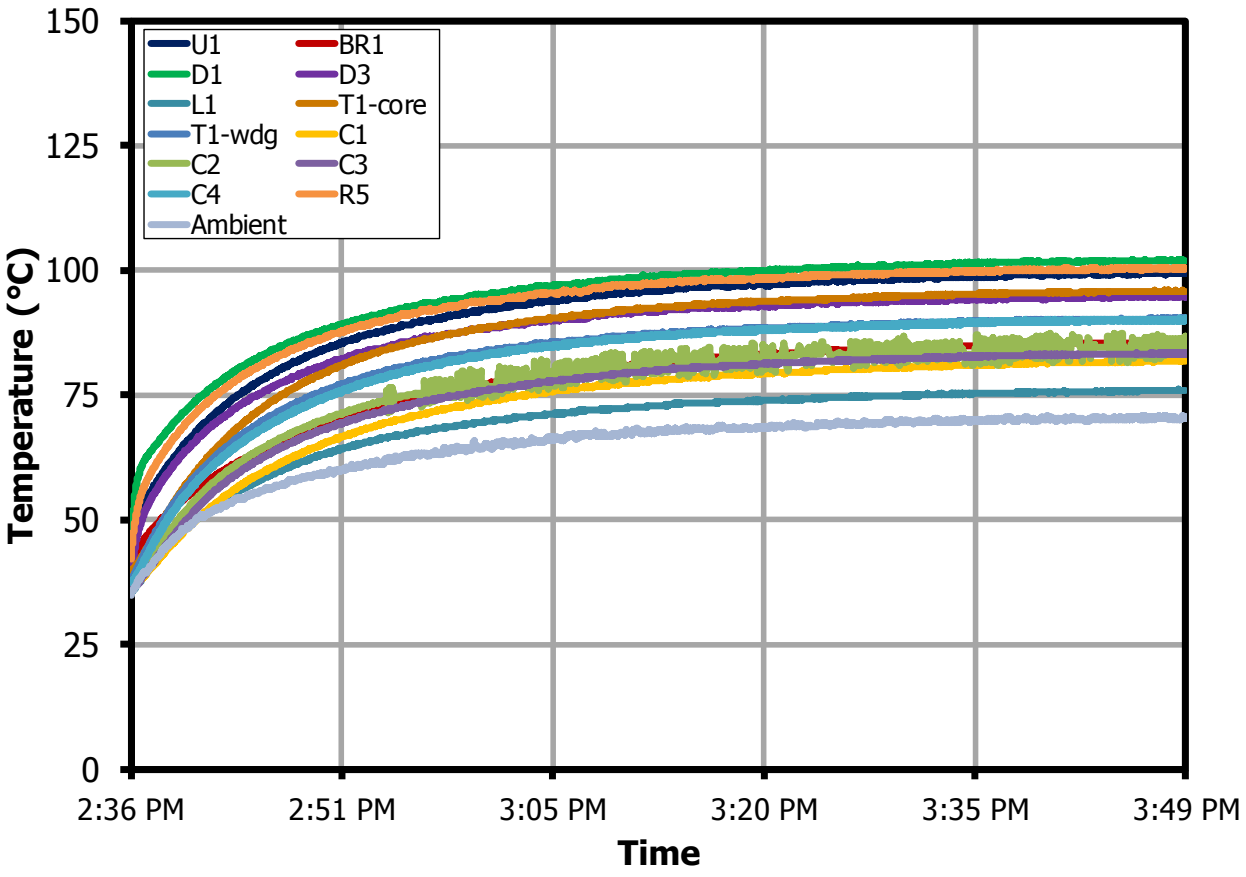

Figure 32 – Thermal Performance at 70 ºC (90 VAC).

Component	Temperature (ºC)
IC (U1)	99.3
Bridge Rectifier (BR1)	85.6
Freewheel Diode (D1)	101.9
Snubber Diode (D3)	94.7
Input Choke (L1)	75.9
Transformer-Core (T1-core)	95.9
Transformer-Winding (T1-wdg)	90.3
Input Capacitor (C1)	81.9
Input Capacitor (C2)	85.6
Output Capacitor (C3)	83.3
Bias Capacitor (C4)	90.1
Snubber Resistor (R5)	100.4
Ambient Temperature	70.4

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15.2 *265 VAC*

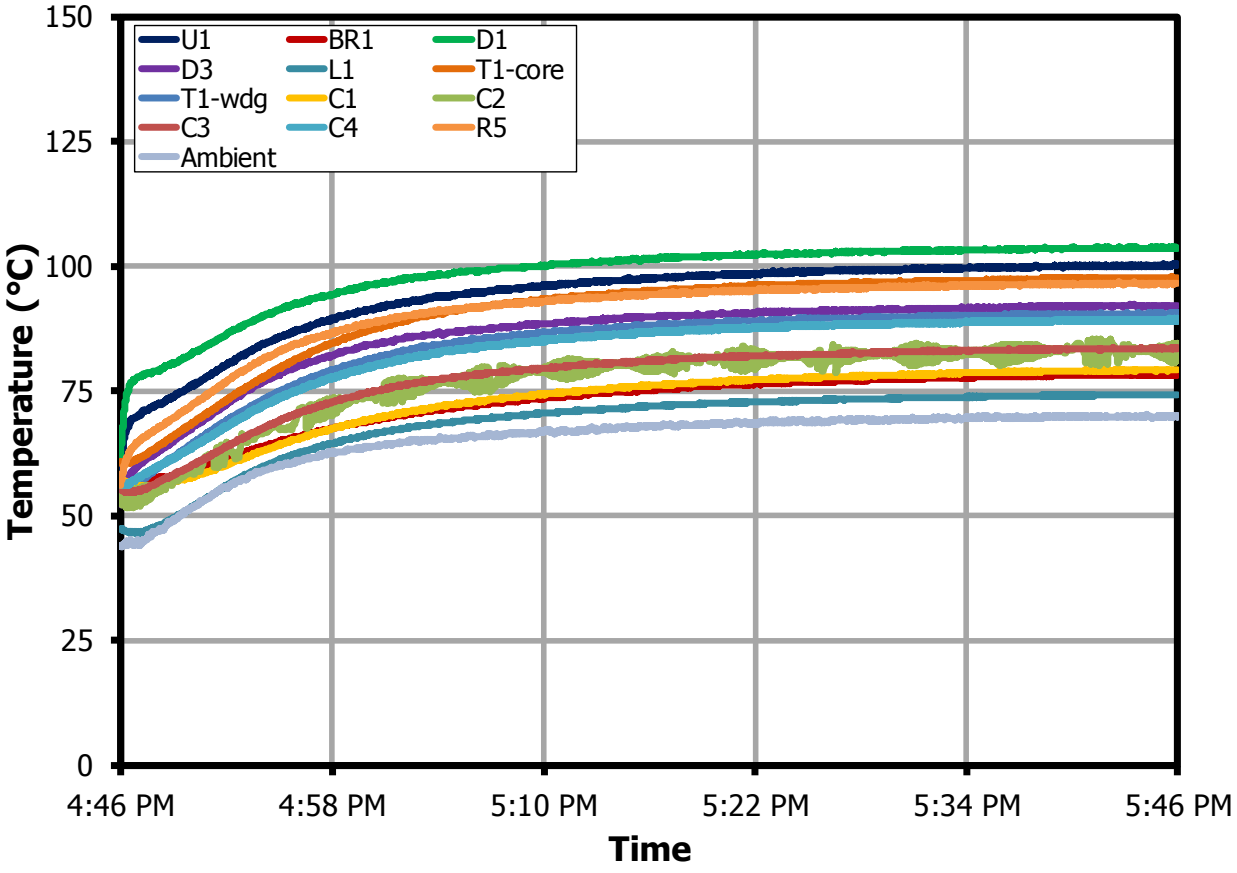

Figure 33 – Thermal Performance at 70 ºC (265 VAC).

Component	Temperature (ºC)
IC (U1)	100.4
Bridge Rectifier (BR1)	78.4
Freewheel Diode (D1)	103.7
Snubber Diode (D3)	92.2
Input Choke (L1)	74.3
Transformer-Core (T1-core)	97.8
Transformer-Winding (T1-wdg)	90.7
Input Capacitor (C1)	79.3
Input Capacitor (C2)	81.6
Output Capacitor (C3)	83.7
Bias Capacitor (C4)	89.2
Snubber Resistor (R5)	96.6
Ambient Temperature	70.0

16 Over Temperature Protection

16.1 *90 VAC*

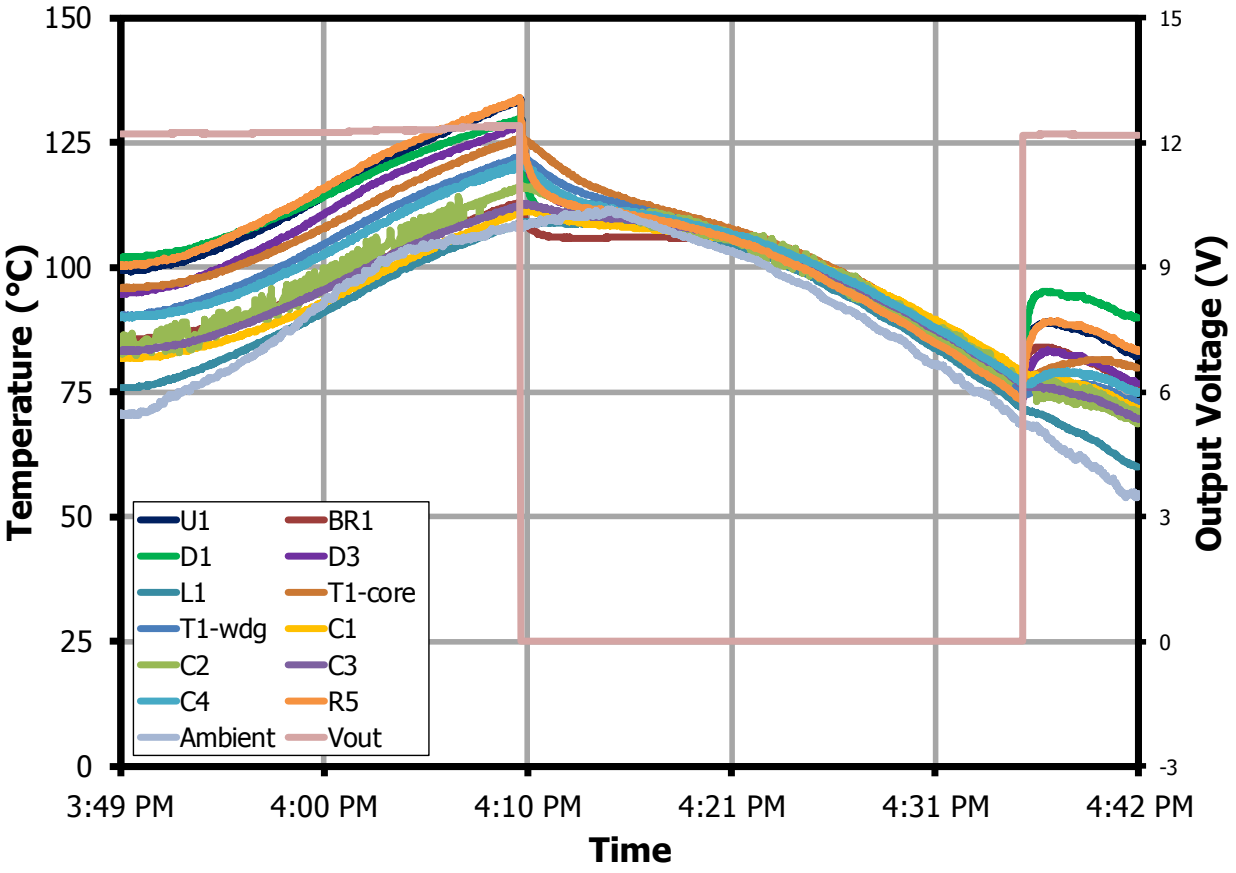

Figure 34 – 90 VAC Over Temperature Protection.

Component	At OTP Trigger Temperature (ºC)	At Recovery Temperature (ºC)
IC (U1)	133.6	76.6
Bridge Rectifier (BR1)	113.2	78.5
Freewheel Diode (D1)	129.9	76.3
Snubber Diode (D3)	128.5	72.8
Input Choke (L1)	108.8	71.9
Transformer-Core (T1-core)	125.9	78.0
Transformer-Winding (T1-wdg)	122.2	74.7
Input Capacitor (C1)	111.0	79.0
Input Capacitor (C2)	115.9	76.3
Output Capacitor (C3)	112.4	76.5
Bias Capacitor (C4)	120.7	76.8
Snubber Resistor (R5)	133.9	73.6
Ambient Temperature	108.5	68.5

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16.2 *265 VAC*

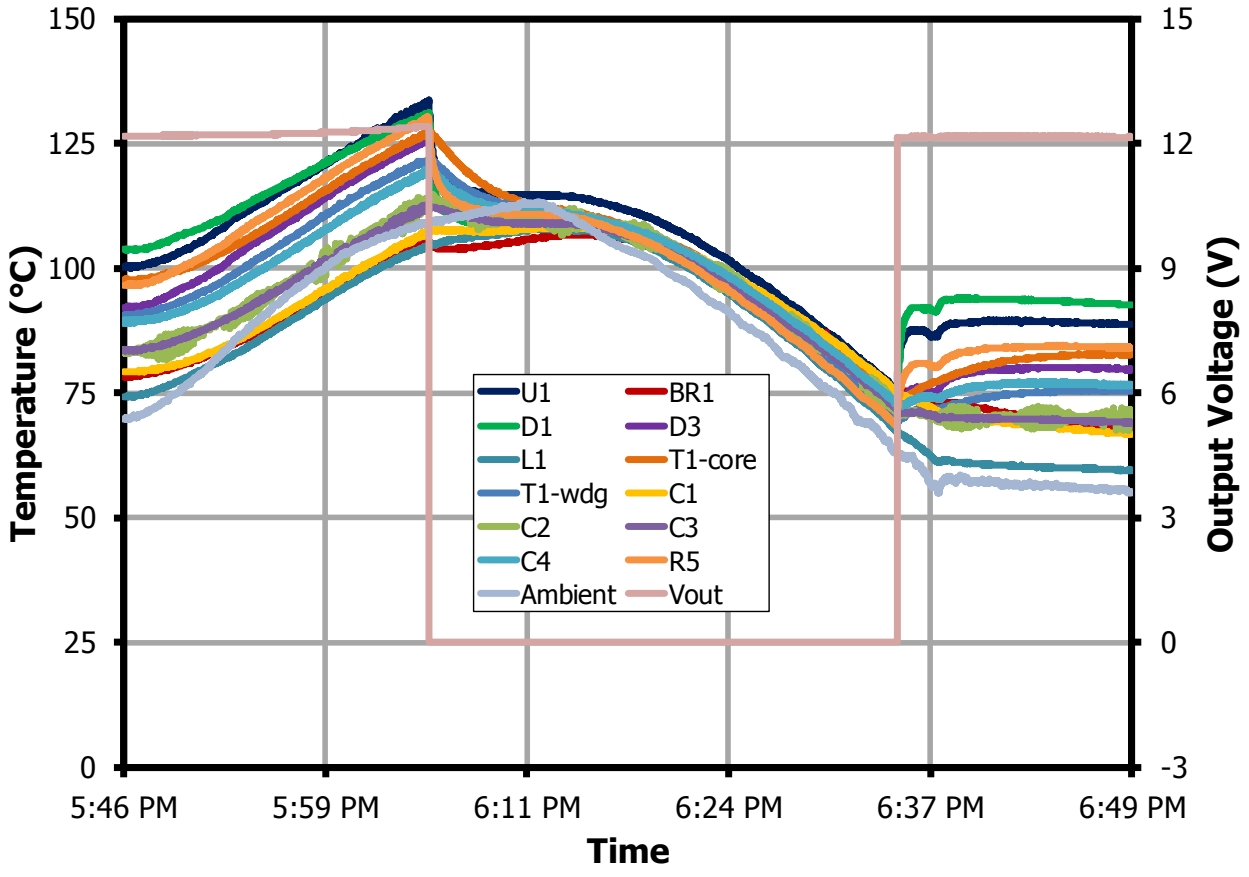

Figure 35 – 265 VAC Over Temperature Protection.

Component	At OTP Trigger Temperature (ºC)	At Recovery Temperature (ºC)
IC (U1)	133.2	75.5
Bridge Rectifier (BR1)	105.5	74.3
Freewheel Diode (D1)	130.8	71.1
Snubber Diode (D3)	125.8	67.8
Input Choke (L1)	104.5	67.3
Transformer-Core (T1-core)	127.1	73.6
Transformer-Winding (T1-wdg)	121.8	70
Input Capacitor (C1)	107.1	75.3
Input Capacitor (C2)	114.1	71.6
Output Capacitor (C3)	112	71.8
Bias Capacitor (C4)	120	72.8
Snubber Resistor (R5)	130.2	68.7
Ambient Temperature	109.1	62.7

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17 Test Waveforms

17.1 *Load Transient Response*

Measured across PCB connector.

17.1.1 0% - 100% Load Condition

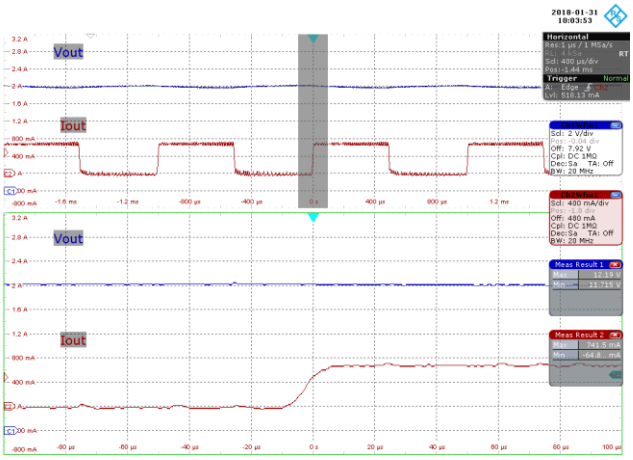

Figure 36 – 90 VAC 60 Hz, 0% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400 mA / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.19 V, V_{MIN}: 11.715 V.

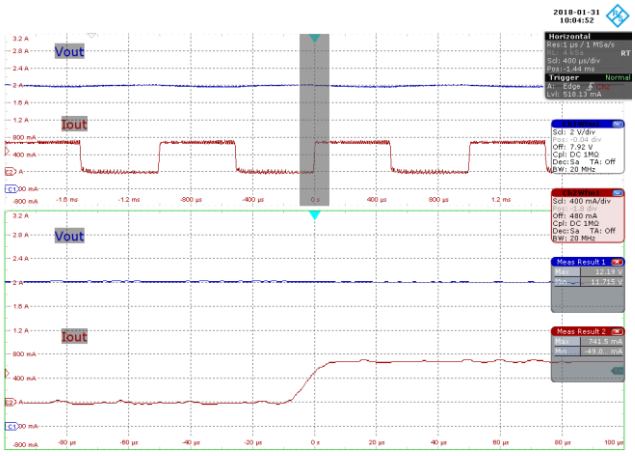

Figure 37 – 115 VAC 60 Hz, 0% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400 mA / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.19 V, V_{MIN}: 11.715 V.

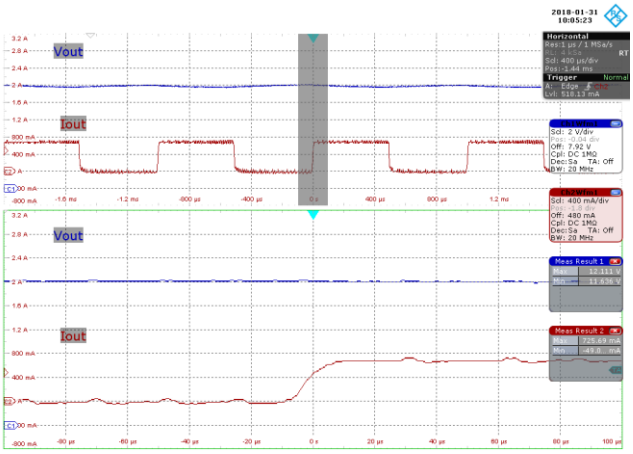

Figure 38 – 230 VAC 60 Hz, 0% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400m A / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.111 V, V_{MIN}: 11.636 V.

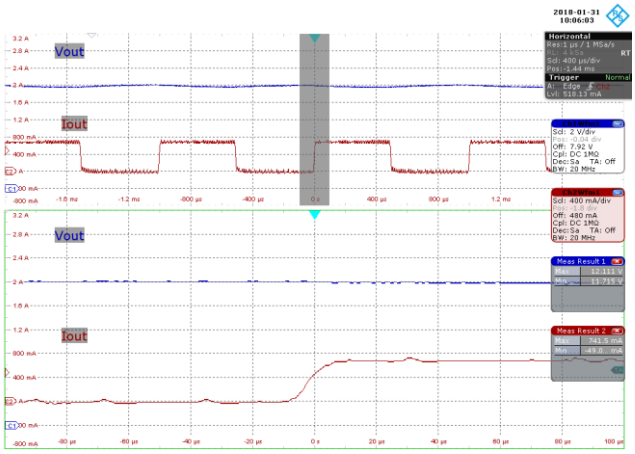

Figure 39 – 265 VAC 60 Hz, 0% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400m A / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.111 V, V_{MIN}: 11.715 V.

17.1.2 50% - 100% Load Condition

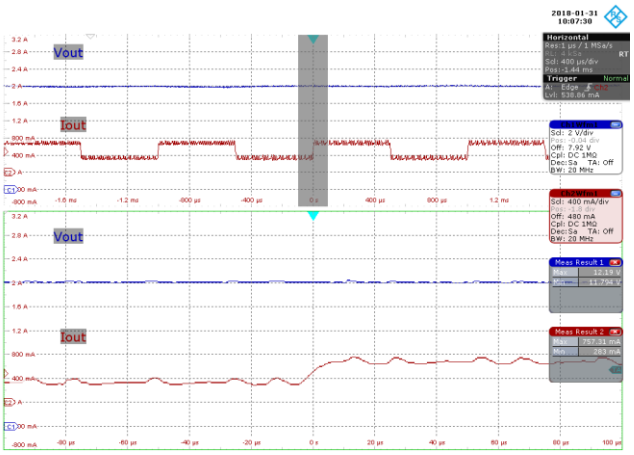

Figure 40 – 90 VAC 60 Hz, 50% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400m A / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.19 V, V_{MIN}: 11.794 V.

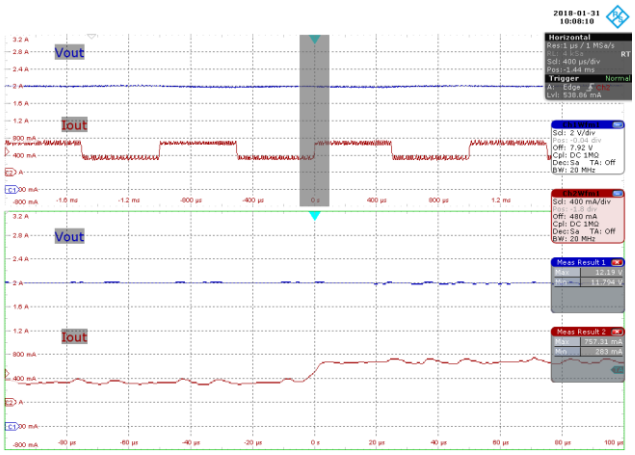

Figure 41 – 115 VAC 60 Hz, 50% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400m A / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.19 V, V_{MIN}: 11.794 V.

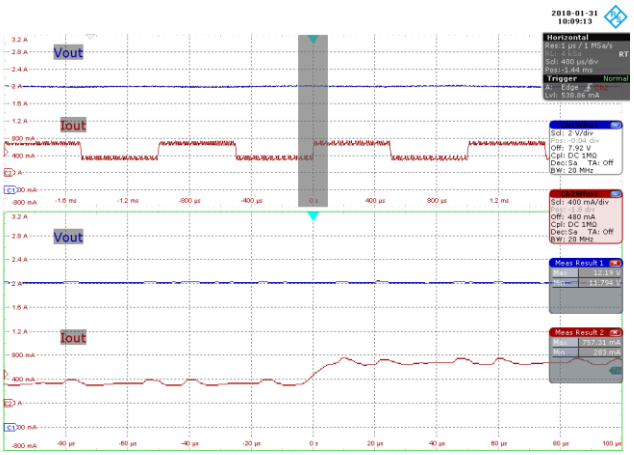

Figure 42 – 230 VAC 60 Hz, 50% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400m A / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.19 V, V_{MIN}: 11.794 V.

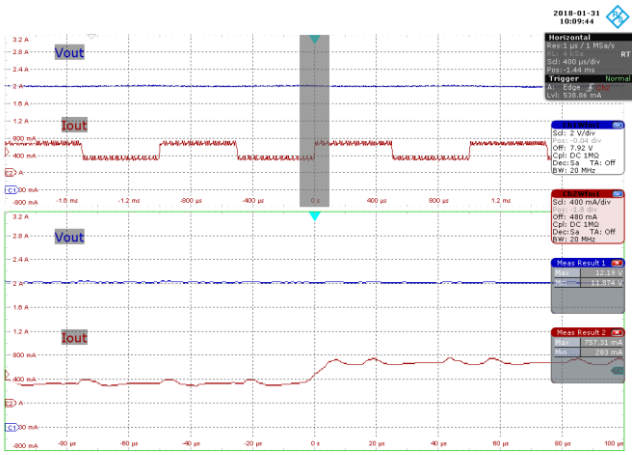

Figure 43 – 265 VAC 60 Hz, 50% - 100% Load.
CH1: V_{OUT}, 2 V / div., 400 µs / div.
CH2: I_{LOAD}, 400m A / div., 400 µs / div.
Zoom: 20 µs / div.
V_{MAX}: 12.19 V, V_{MIN}: 11.874 V.

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17.2 *Output Voltage at Start-up*

17.2.1 Measured at the End of 1.2m #22 Cable

17.2.2 CC mode

17.2.2.1 100% Load

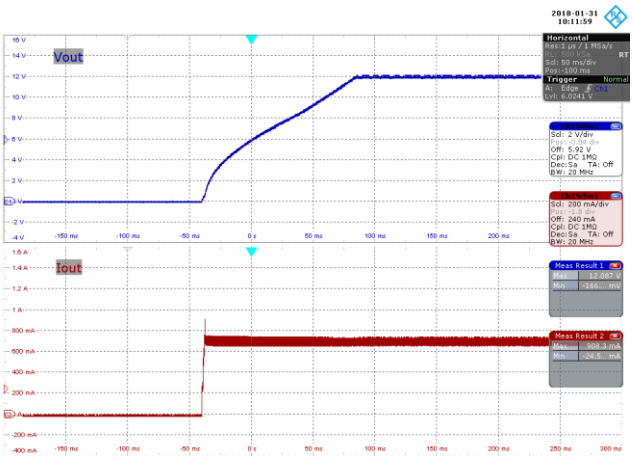

Figure 44 – 90 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

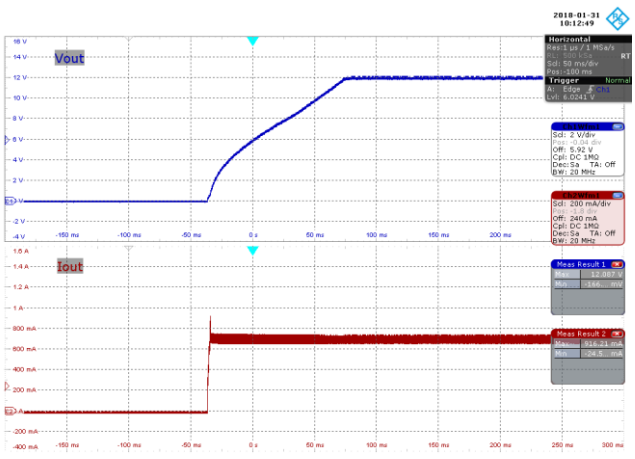

Figure 45 – 115 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

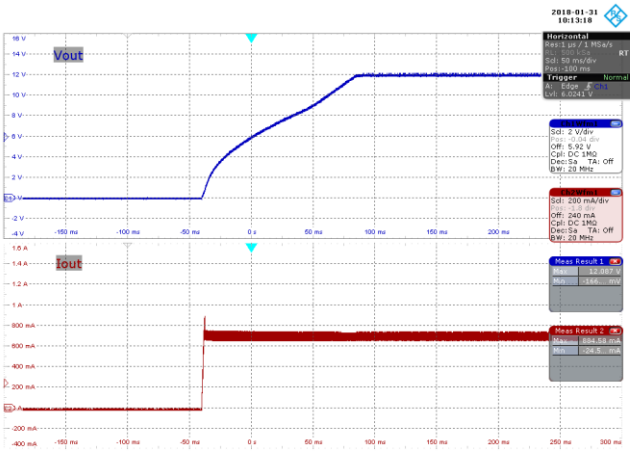

Figure 46 – 230 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

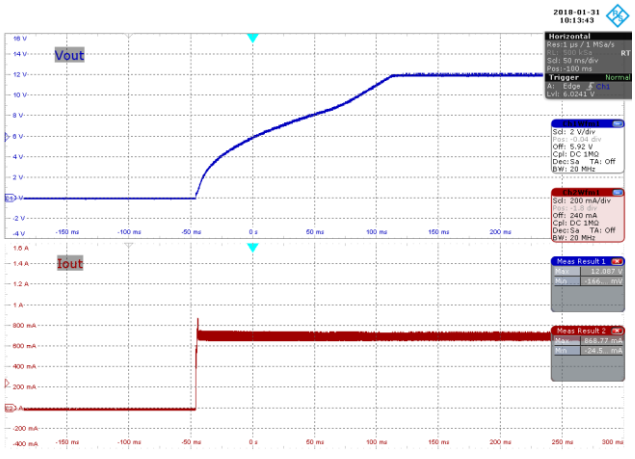

Figure 47 – 265 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

17.2.2.2 0% Load

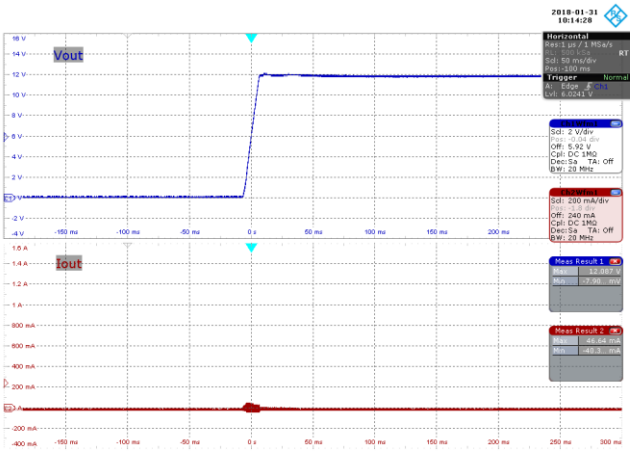

Figure 48 – 90 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

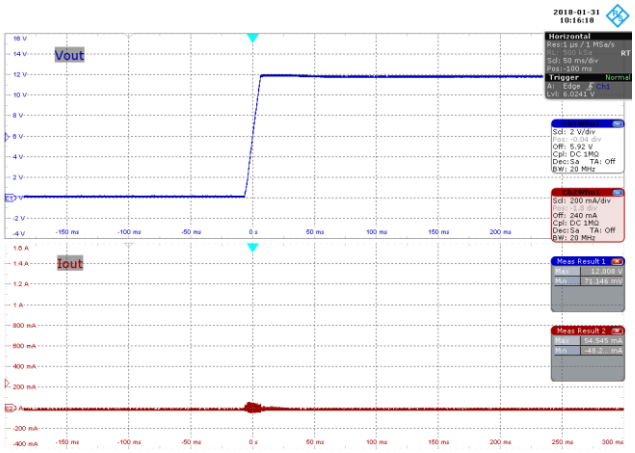

Figure 49 – 115 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

Figure 50 – 230 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

Figure 51 – 265 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

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17.2.3 CR mode

17.2.3.1 100% Load

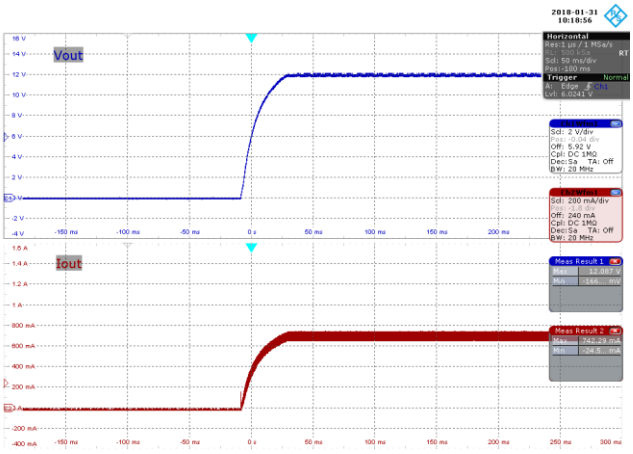

Figure 52 – 90 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

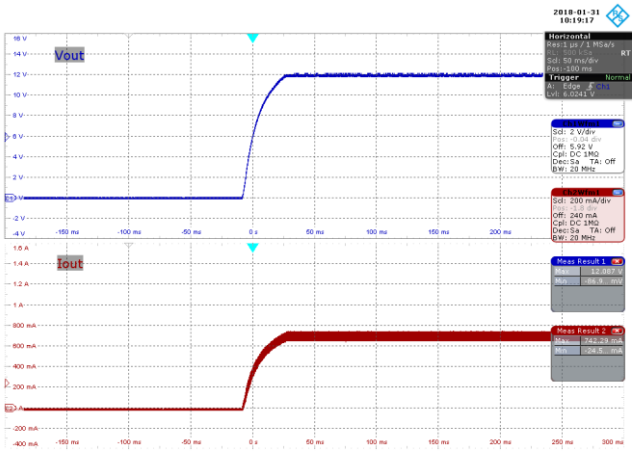

Figure 53 – 115 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

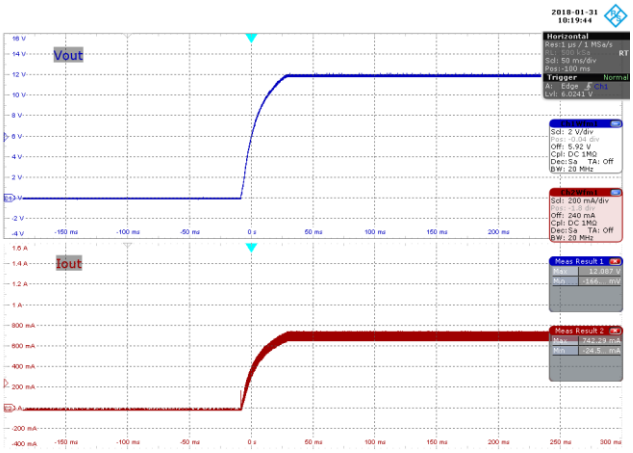

Figure 54 – 230 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

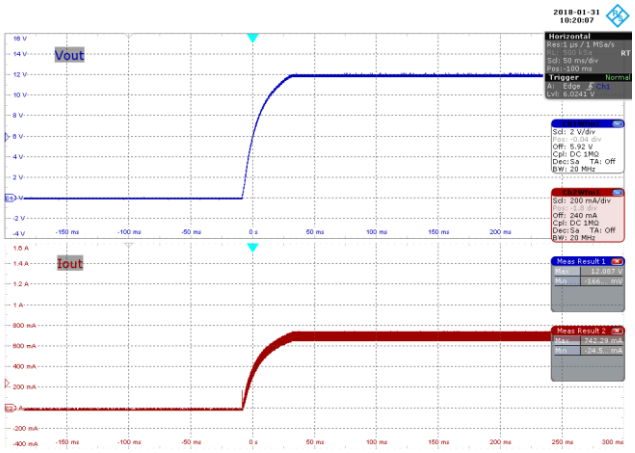

Figure 55 – 265 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

17.2.3.2 0% Load

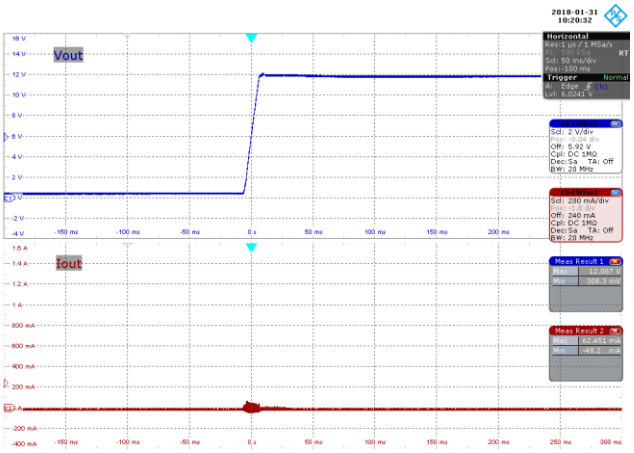

Figure 56 – 90 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

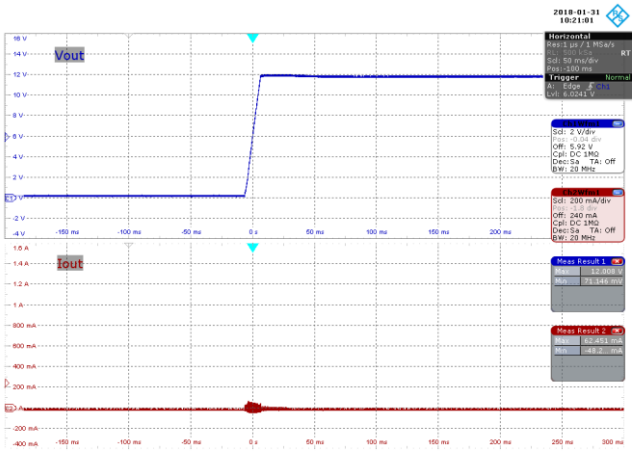

Figure 57 – 115 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

Figure 58 – 230 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

Figure 59 – 265 VAC 60 Hz, No-Load Start-up.
Upper: V_{OUT}, 2 V / div., 50 ms / div.
Lower: I_{OUT}, 200 mA / div., 50 ms / div.

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17.3 *Switching Waveforms*

17.3.1 Drain-to-Source Voltage and Current at Normal Operation

17.3.1.1 100% Load

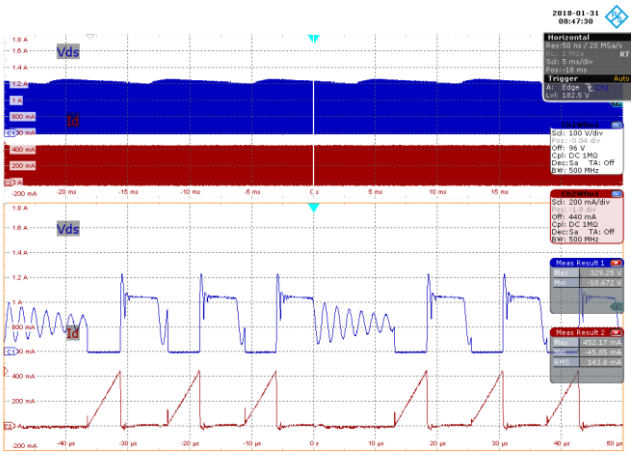

Figure 60 – 90 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms / div.
CH2: I_{DS}, 200 mA / div., 5 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 329.25 V, $I_{DS(MAX)}$ = 452.2 mA.

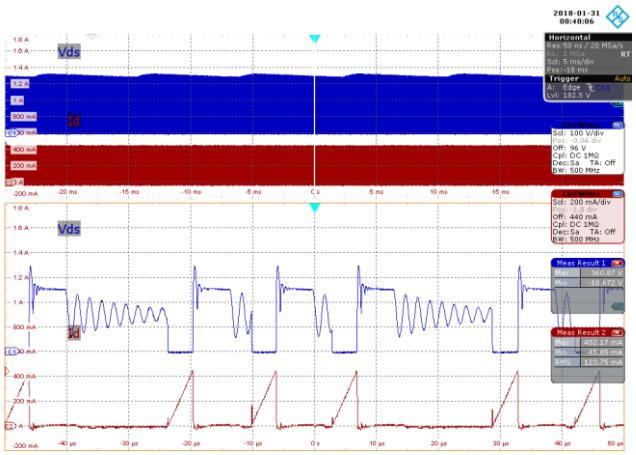

Figure 61 – 115 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms / div.
CH2: I_{DS}, 200 mA / div., 5 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 360.87 V, $I_{DS(MAX)}$ = 452.2 mA.

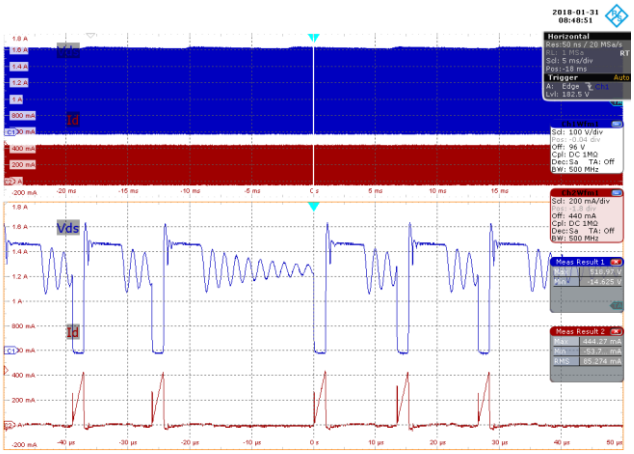

Figure 62 – 230 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms / div.
CH2: I_{DS}, 200 mA / div., 5 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 518.97 V, $I_{DS(MAX)}$ = 444.3 mA.

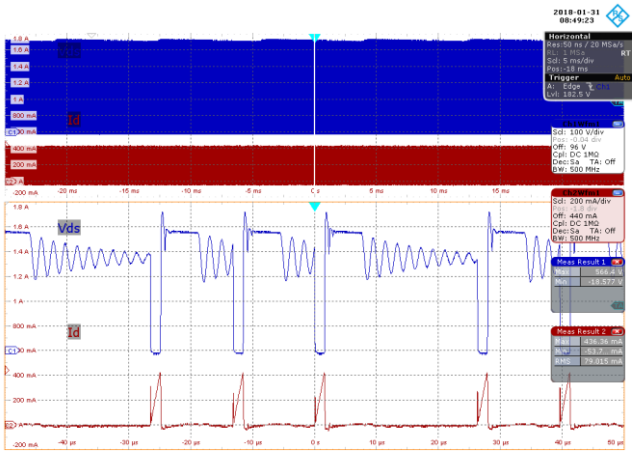

Figure 63 – 265 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 5 ms / div.
CH2: I_{DS}, 200 mA / div., 5 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 566.4 V, $I_{DS(MAX)}$ = 436.4 mA.

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17.3.1.2 0% Load

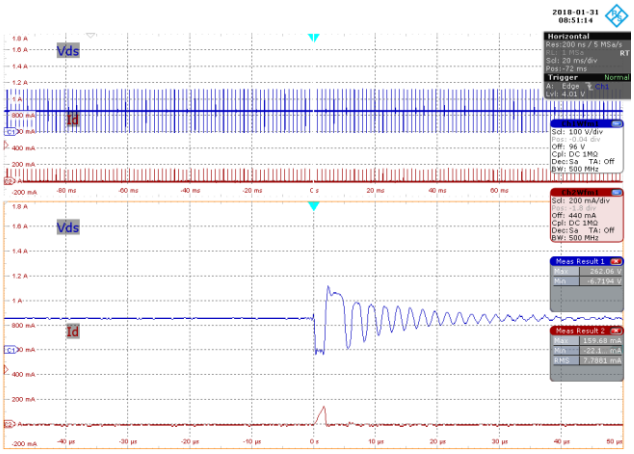

Figure 64 – 90 VAC 60 Hz, No-Load.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 262.06 V, $I_{DS(MAX)}$ = 159.7 mA.

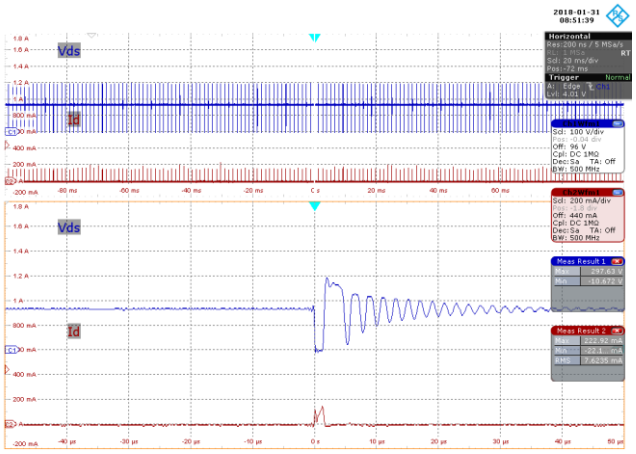

Figure 65 – 115 VAC 60 Hz, No-Load.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 297.63 V, $I_{DS(MAX)}$ = 222.9 mA.

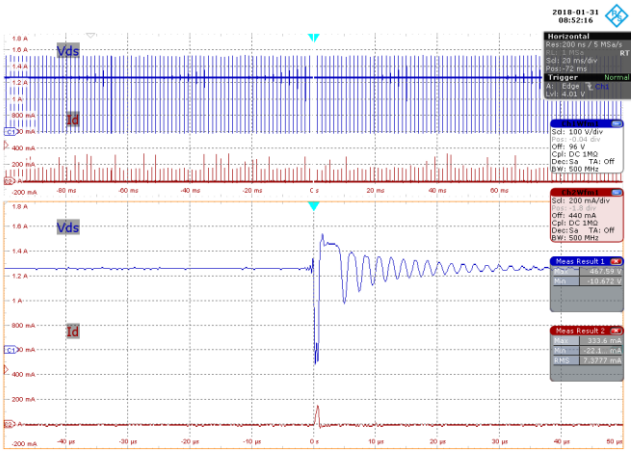

Figure 66 – 230 VAC 60 Hz, No-Load.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 467.59 V, $I_{DS(MAX)}$ = 333.6 mA

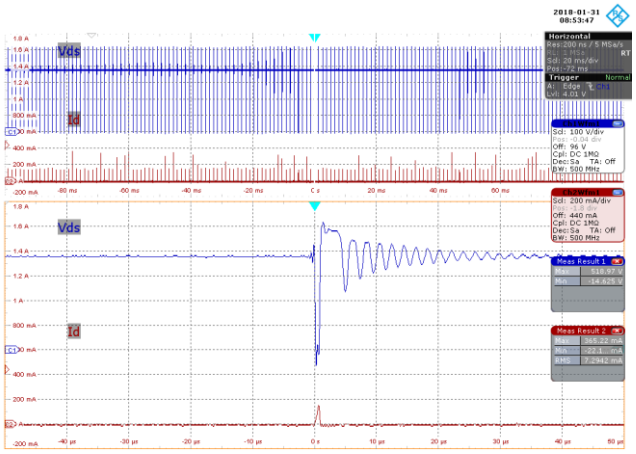

Figure 67 – 265 VAC 60 Hz, No-Load.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 518.97 V, $I_{DS(MAX)}$ = 365.22 mA.

17.3.2 Drain-to-Source Voltage and Current at Startup Operation

17.3.2.1 100% Load

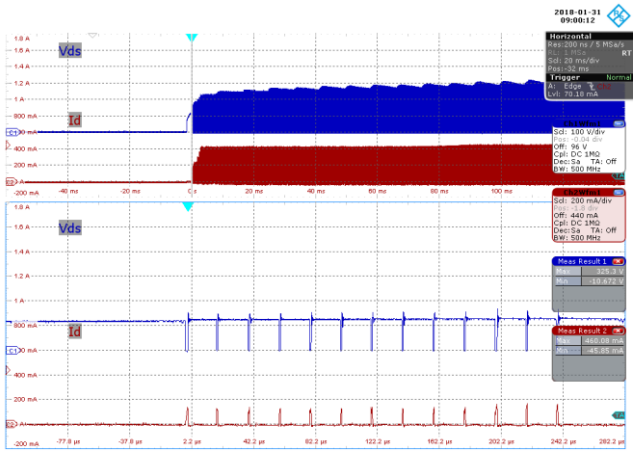

Figure 68 – 90 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 325.3 V, $I_{DS(MAX)}$ = 460.1 mA.

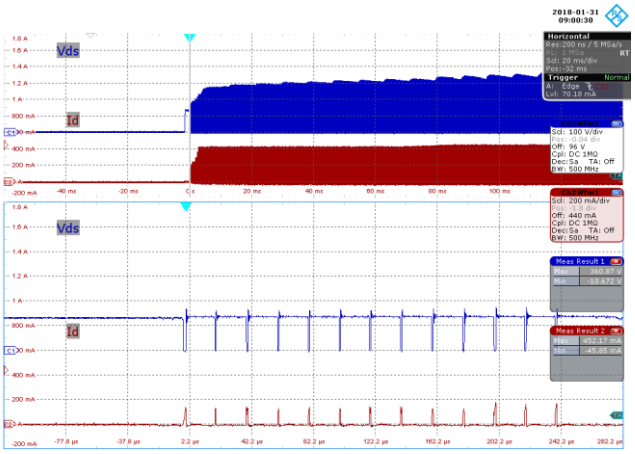

Figure 69 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 360.87 V, $I_{DS(MAX)}$ = 452.17 mA.

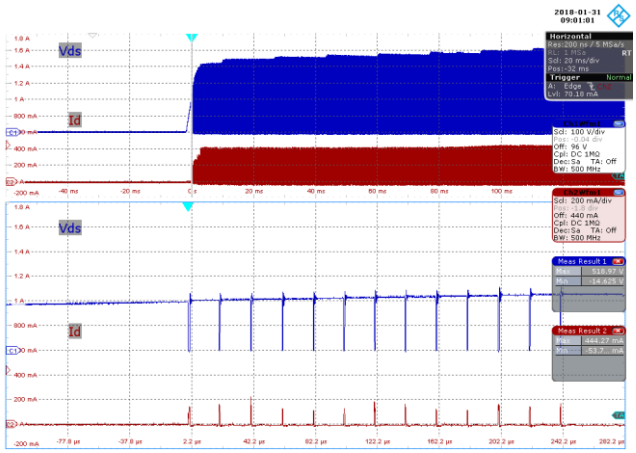

Figure 70 – 230 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 518.97 V, $I_{DS(MAX)}$ = 444.27 mA.

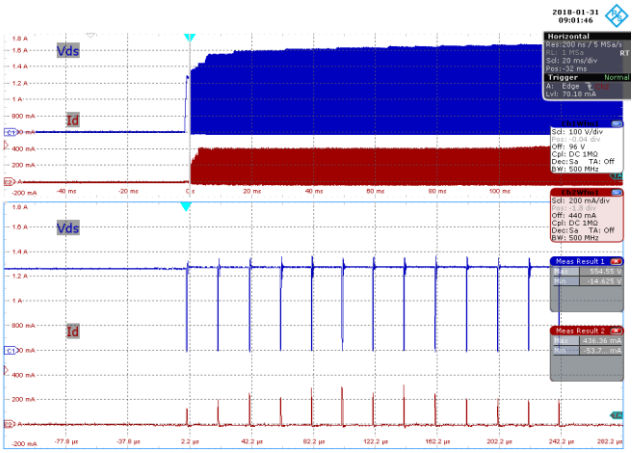

Figure 71 – 265 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 554.55 V, $I_{DS(MAX)}$ = 436.36 mA.

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17.3.2.2 0% Load

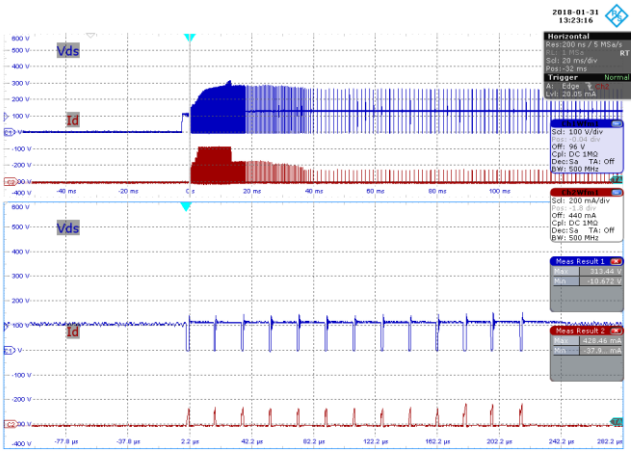

Figure 72 – 90 VAC 60 Hz, No-Load Start-up.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 313.44 V, $I_{DS(MAX)}$ = 428.46 mA.

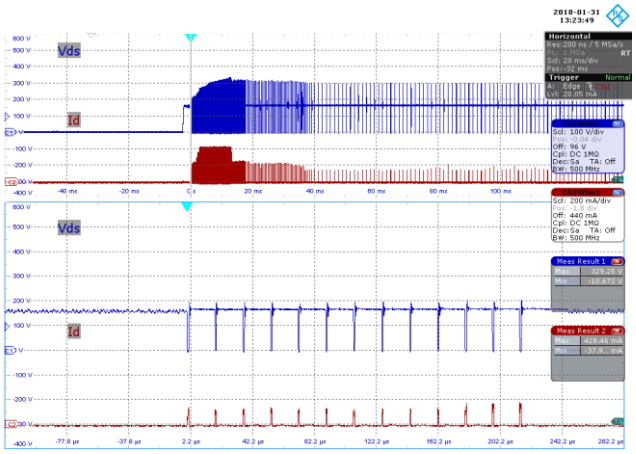

Figure 73 – 115 VAC 60 Hz, No-Load Start-up.
CH1: V_{DS}, 100 V / div., 20 ms / div.
CH2: I_{DS}, 200 mA / div., 20 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 329.25 V, $I_{DS(MAX)}$ = 428.46 mA.

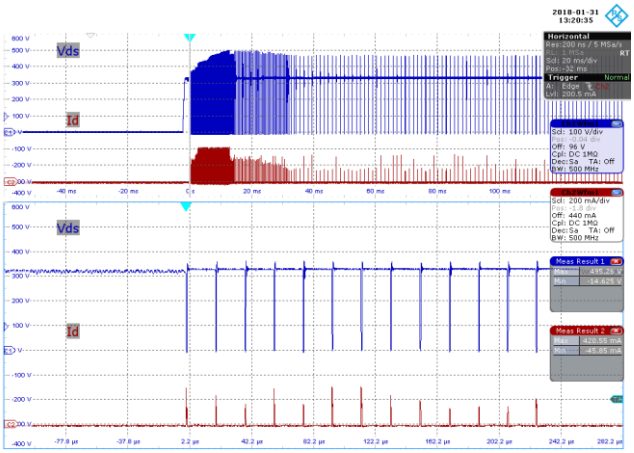

Figure 74 – 230 VAC 50 Hz, No-Load Start-up.
CH1: V_{DS}, 100 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 495.26 V, $I_{DS(MAX)}$ = 420.55 mA.

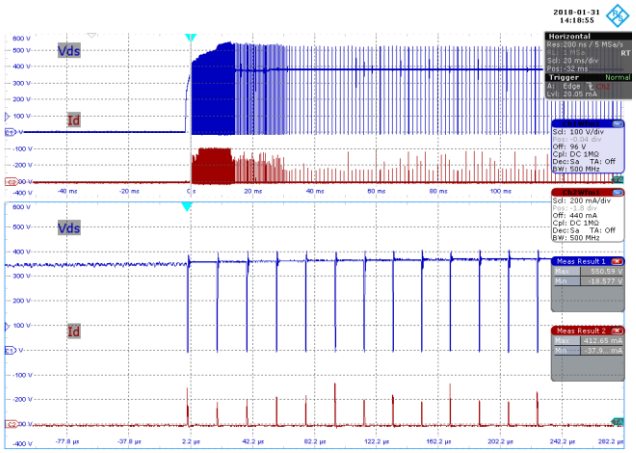

Figure 75 – 265 VAC 50 Hz, No-Load Start-up.
CH1: V_{DS}, 100 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 40 µs / div.
$V_{DS(MAX)}$ = 550.59 V, $I_{DS(MAX)}$ = 412.7 mA.

17.3.3 Output Diode Voltage at Normal Operation

17.3.3.1 100% Load

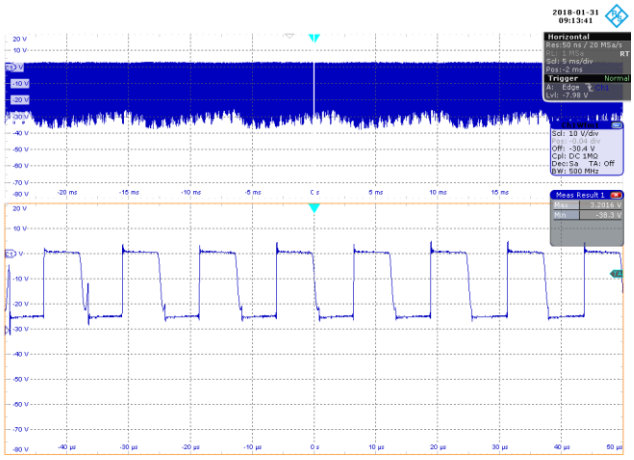

Figure 76 – 90 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 38.3 V.

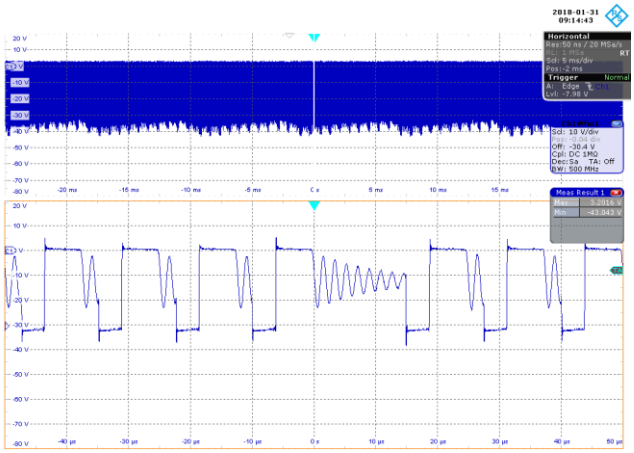

Figure 77 – 115 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div
Zoom: 10 µs / div.
PIV_{MAX} = 43.043 V.

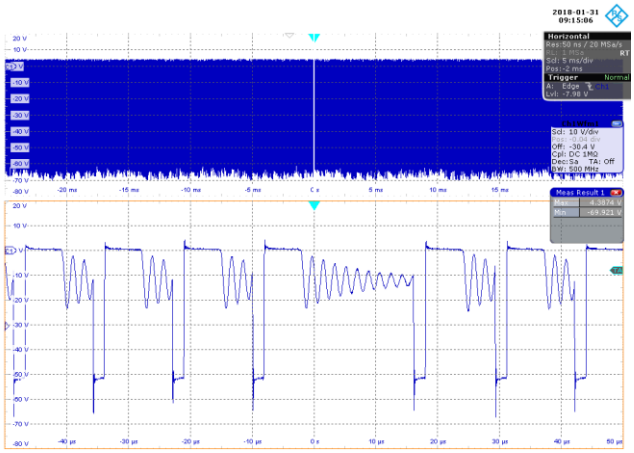

Figure 78 – 230 VAC 50 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 69.921 V.

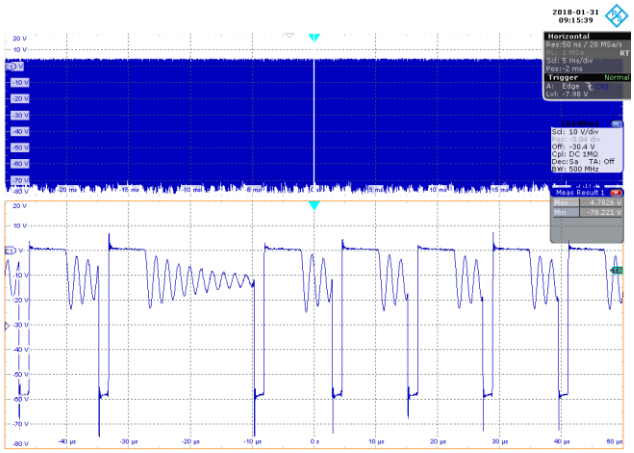

Figure 79 – 265 VAC 50 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 78.221 V.

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17.3.3.2 0% Load

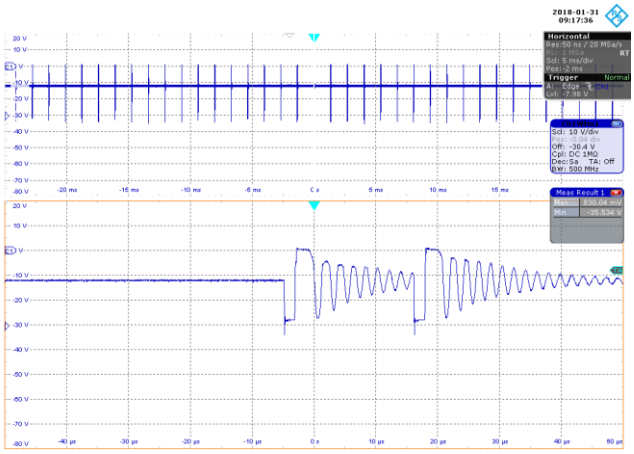

Figure 80 – 90 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 35.534 V.

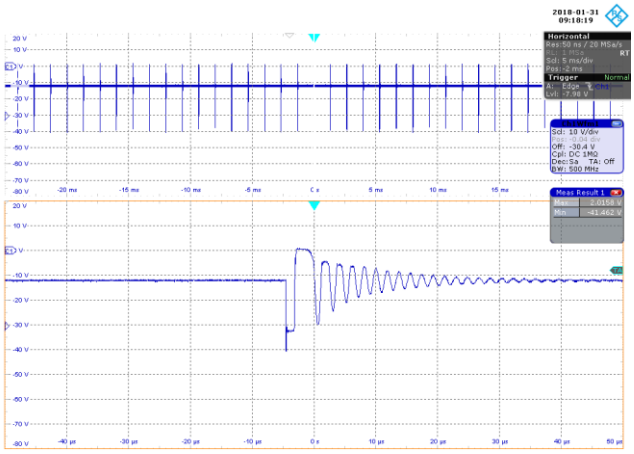

Figure 81 – 115 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 41.462 V.

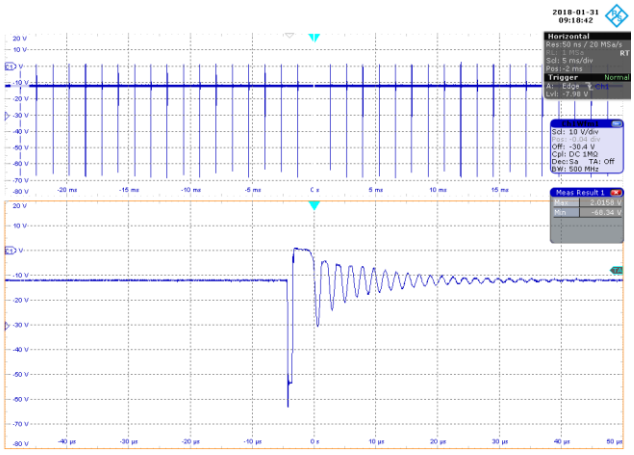

Figure 82 – 230 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 68.34 V.

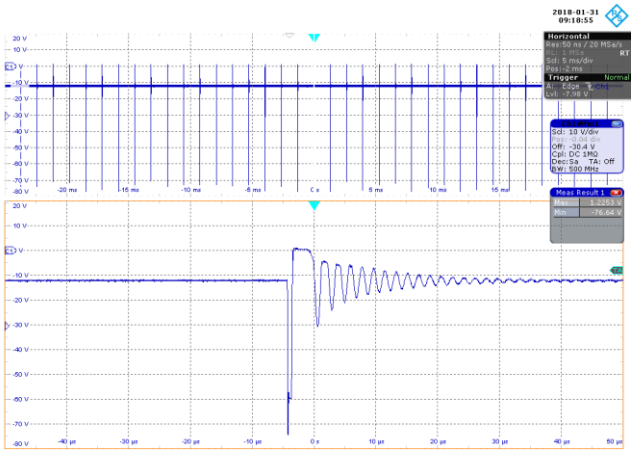

Figure 83 – 265 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 76.64 V.

17.3.4 Output Diode Voltage at Startup Operation

17.3.4.1 100% Load

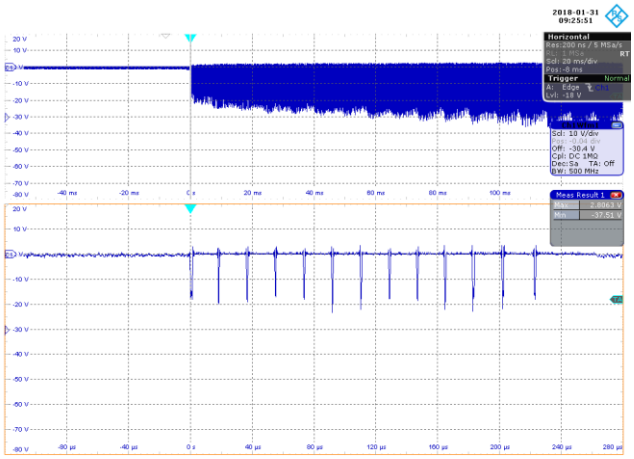

Figure 84 – 90 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 20 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 37.51 V.

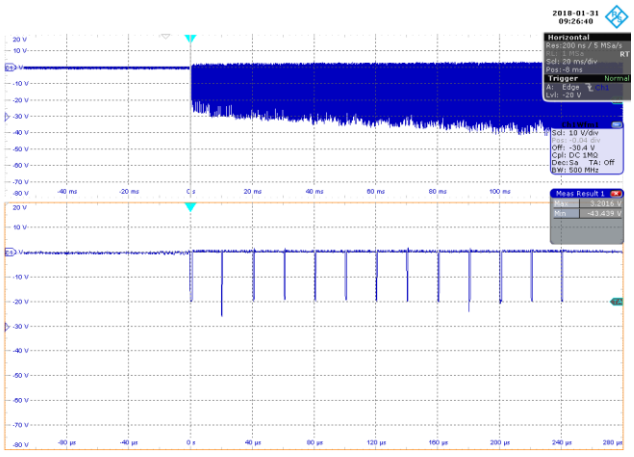

Figure 85 – 115 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 20 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 43.439 V.

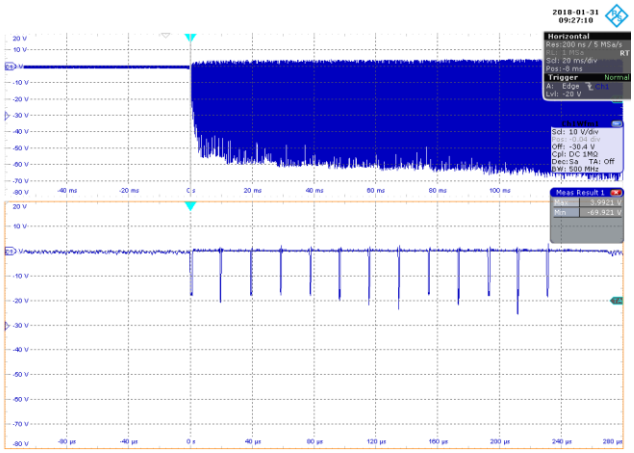

Figure 86 – 230 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 69.921 .

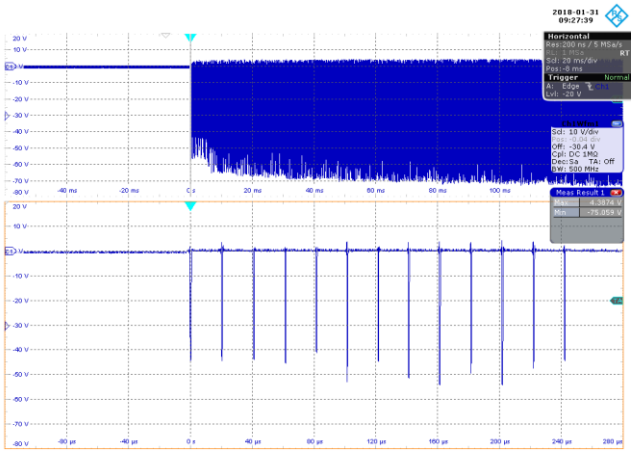

Figure 87 – 265 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 5 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 75.059 V.

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17.3.4.2 0% Load

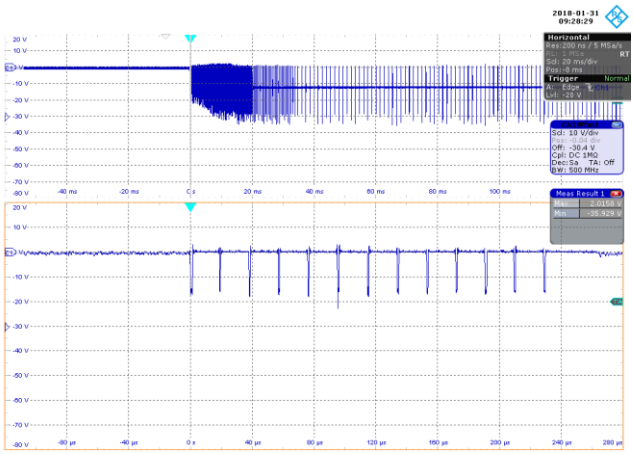

Figure 88 – 90 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 20 ms / div.
Zoom: 40 µs / div.
PIV_{MAX} = 36.929 V.

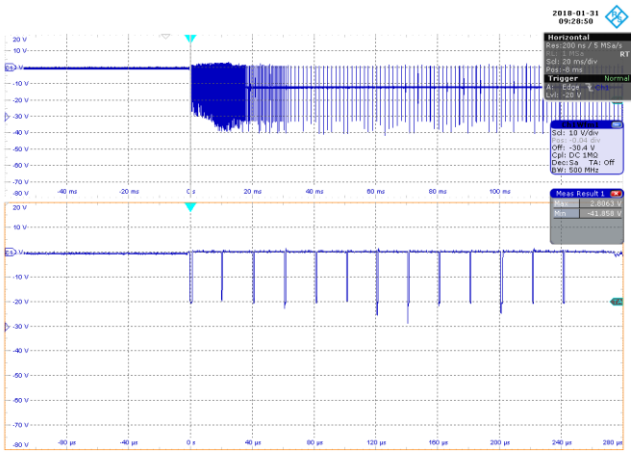

Figure 89 – 115 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 20 ms / div.
Zoom: 40 µs / div.
PIV_{MAX} = 41.858 V.

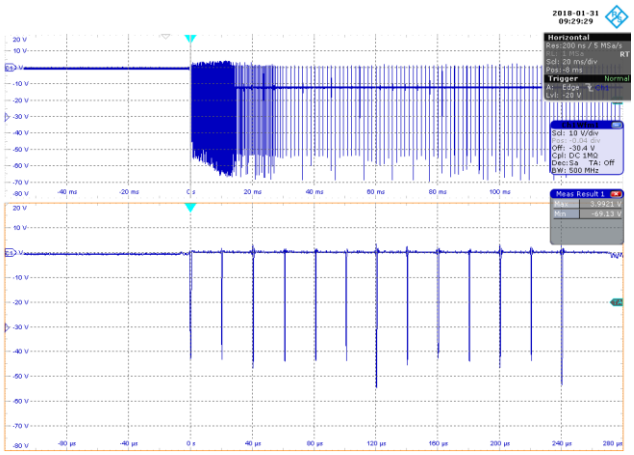

Figure 90 – 230 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 20 ms / div.
Zoom: 40 µs / div.
PIV_{MAX} = 69.13 V.

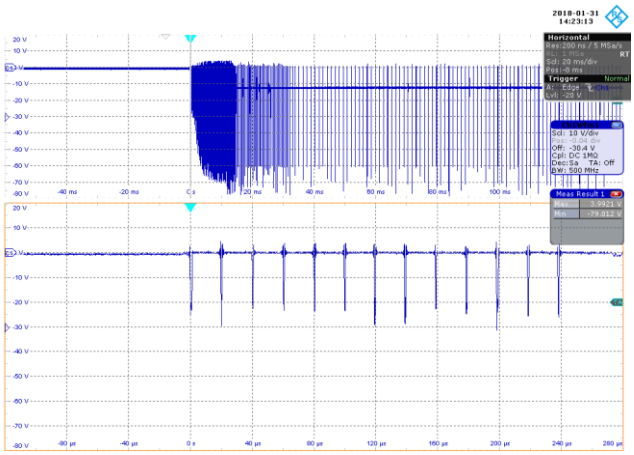

Figure 91 – 265 VAC 60 Hz, No-Load.
CH1: V_{FWL_Diode} - 10 V / div., 20 ms / div.
Zoom: 40 µs / div.
PIV_{MAX} = 79.012 V.

17.4 ***Brown-in / Brown-out Test***

No abnormal overheating nor voltage overshoot / undershoot was observed during and after 0.1 V / s brown-in and brown-out test.

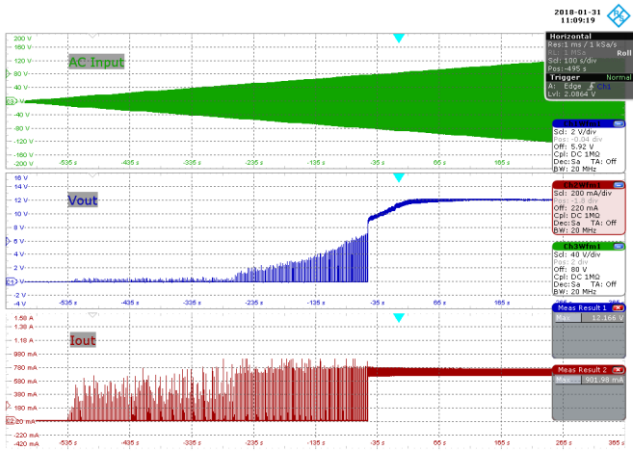

Figure 92 – Brown-in Test.
0 to 90 VAC 0.1 V / s.
CH1: V_{OUT}, 2 V / div., 100 s /div.
CH2: I_{OUT}, 200 mA / div., 100 s / div.
CH3: AC_{IN}, 40 V / div., 100 s / div.
Highest Average Input Power: 10.66 W at 64.6 VAC.

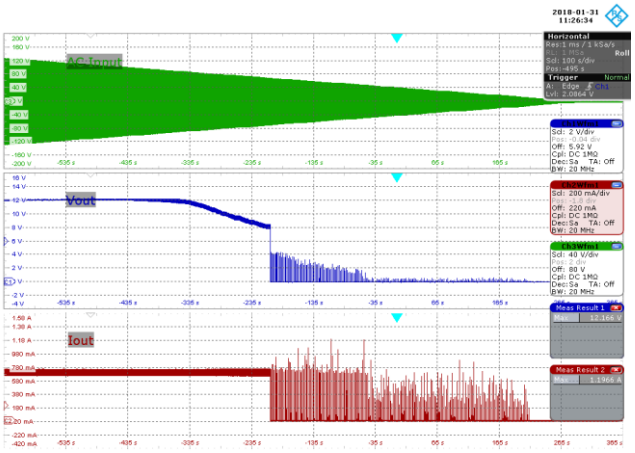

Figure 93 – Brown-out Test.
90 to 0 VAC at 0.1 V / s.
CH1: V_{OUT}, 2 V / div., 100 s /div.
CH2: I_{OUT}, 200 mA / div., 100 s / div.
CH3: AC_{IN}, 40 V / div., 100 s / div.
Highest Average Input Power: 10.575 W at 64.2 VAC.

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17.5 *Output Short Circuit Auto-restart Test*

Output is shorted at the end of the cable.

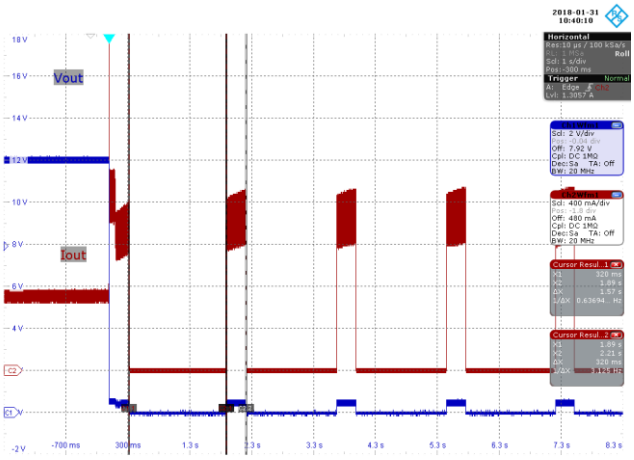

Figure 94 – 90 VAC, Normal Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 400 mA / div., 1 s / div.
$t_{AR(ON)}$: 320 ms.
$t_{AR(OFF)}$: 1.57 s.

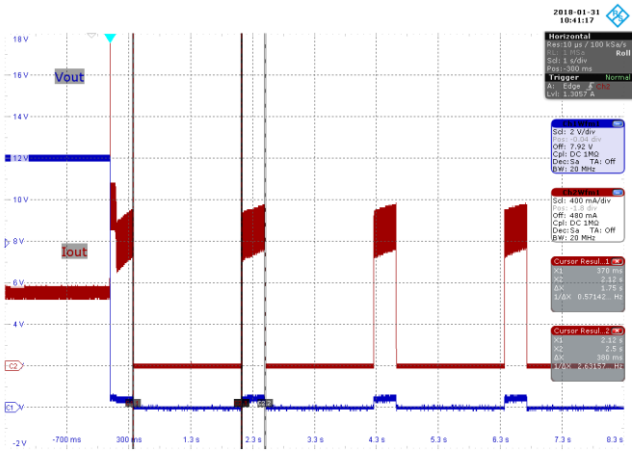

Figure 95 – 265 VAC, Normal Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 400 mA / div., 1 s / div.
$t_{AR(ON)}$: 380 ms.
$t_{AR(OFF)}$: 1.75 s.

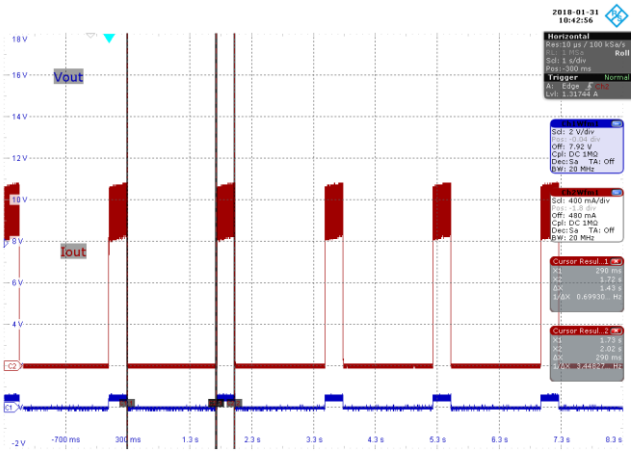

Figure 96 – 90 VAC, Startup Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 400 mA / div., 1 s / div.
$t_{AR(ON)}$: 290 ms
$t_{AR(OFF)}$: 1.43 s

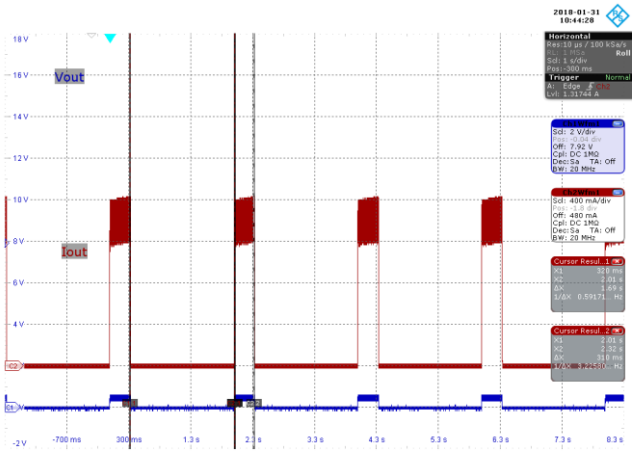

Figure 97 – 265 VAC, Startup Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 400 mA / div., 1 s / div.
$t_{AR(ON)}$: 301 ms
$t_{AR(OFF)}$: 1.69 s

17.6 *Output Ripple Measurements*

17.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

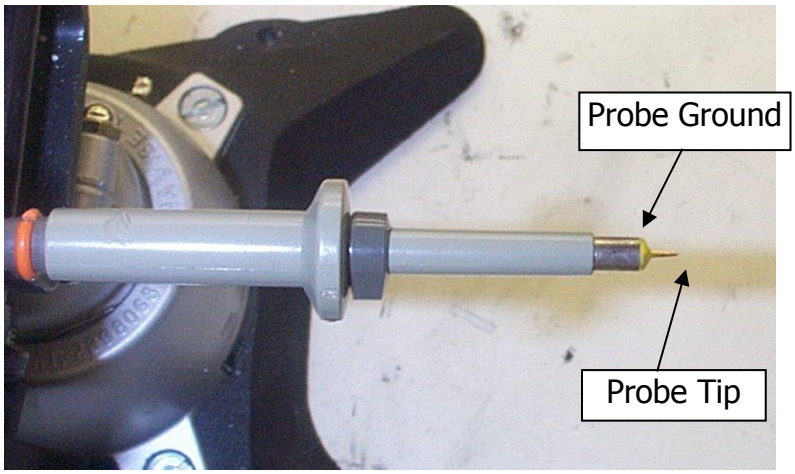

Figure 98 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

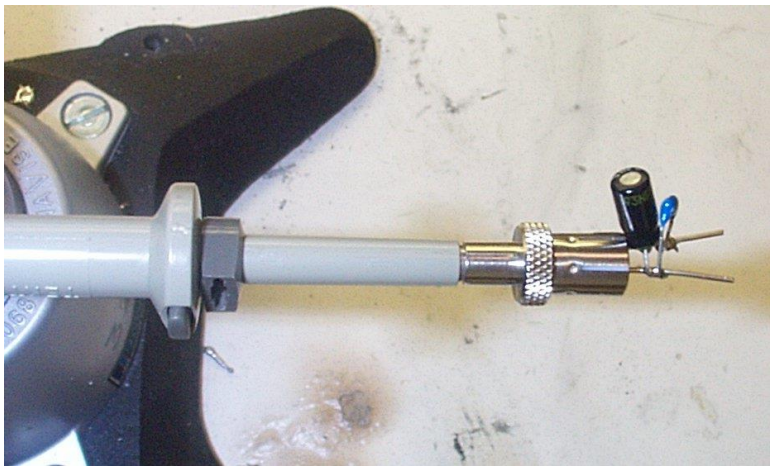

Figure 99 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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17.6.2 Measurement Results

Measured across the PCB connector

17.6.2.1 100% Load Condition

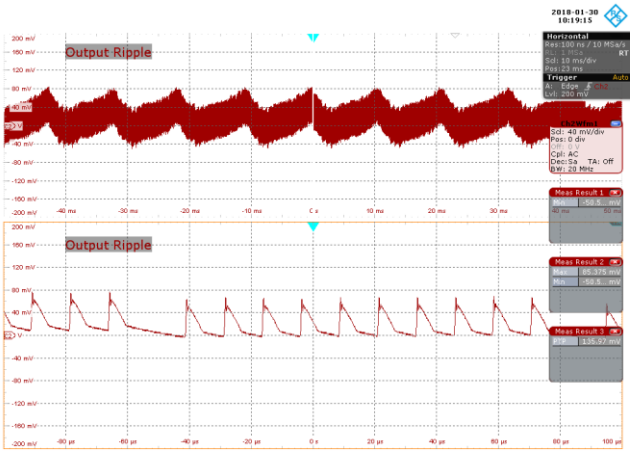

Figure 100 – 90 VAC 47 Hz, 100% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 135.9 mV).

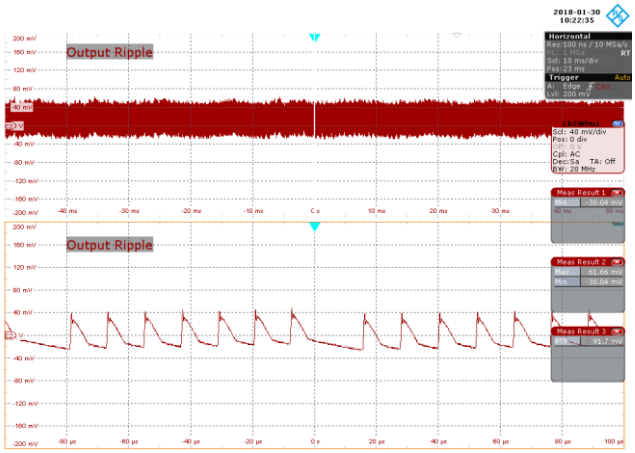

Figure 101 – 115 VAC 47 Hz, 100% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 91.6 mV).

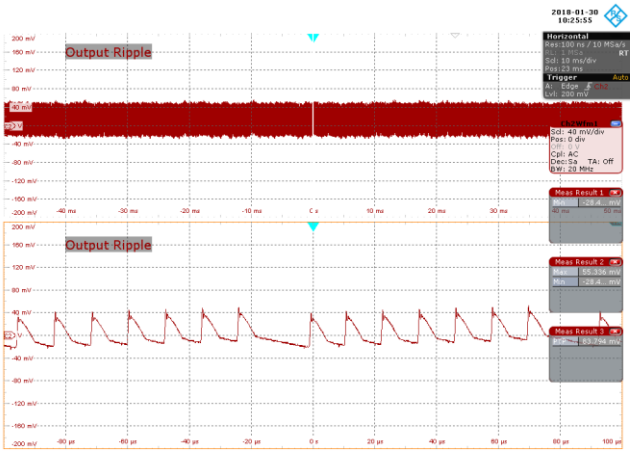

Figure 102 – 230VAC 47 Hz, 100% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 83.7 mV).

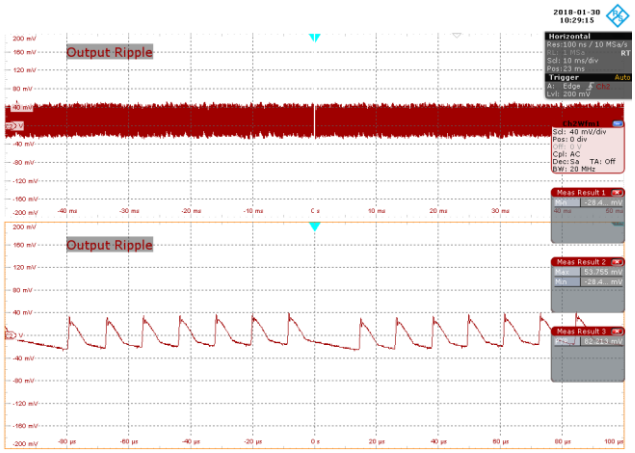

Figure 103 – 265VAC 47 Hz, 100% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 82.2 mV).

17.6.2.2 75% Load Condition

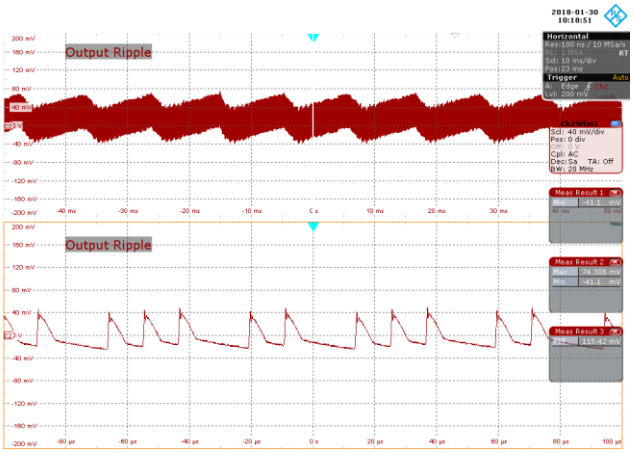

Figure 104 – 90 VAC 47 Hz, 75% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 85.3 mV).

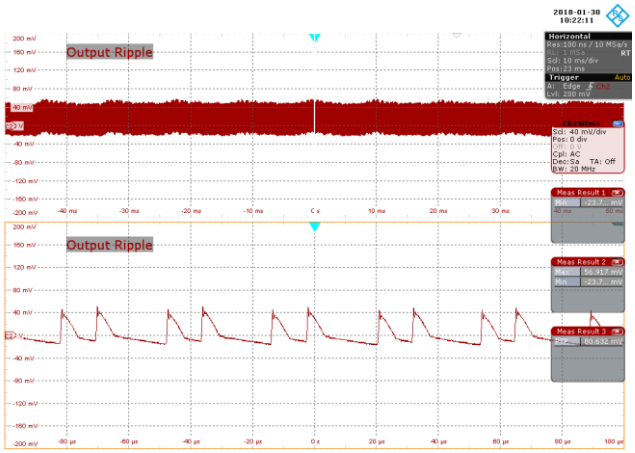

Figure 105 – 115 VAC 47 Hz, 75% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 80.6 mV).

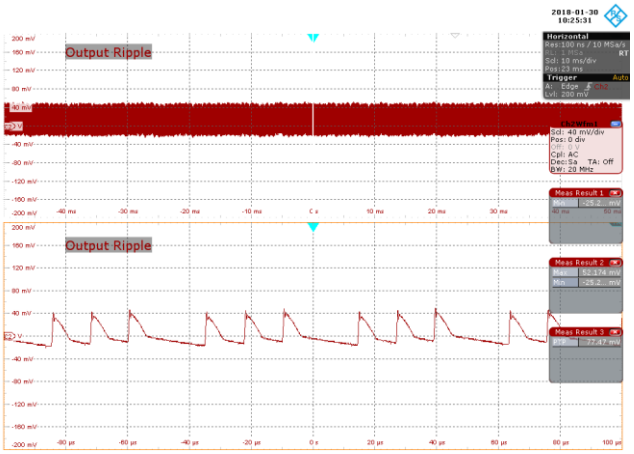

Figure 106 – 230 VAC 47 Hz, 75% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 64.8 mV).

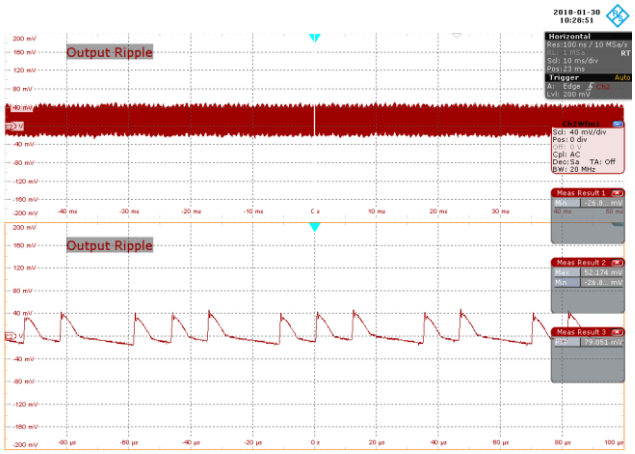

Figure 107 – 265 VAC 47 Hz, 75% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 63.2 mV).

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17.6.2.3 50% Load Condition

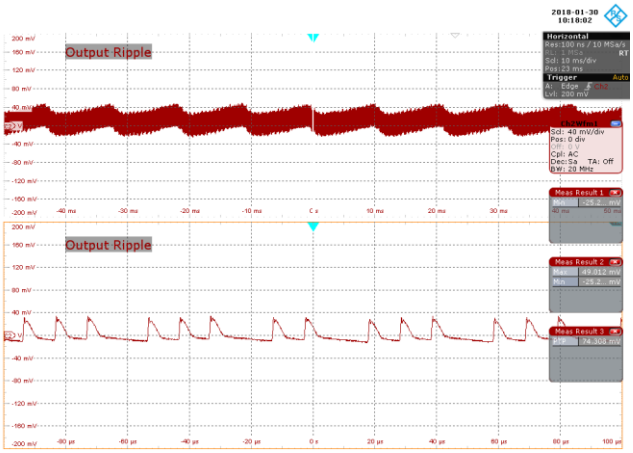

Figure 108 – 90 VAC 47 Hz, 50% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 74.3 mV).

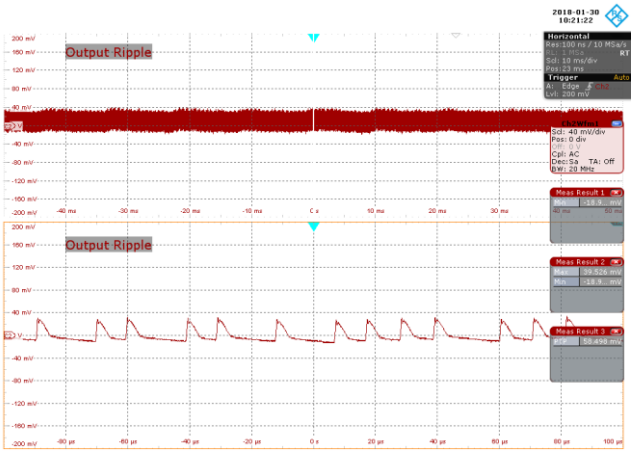

Figure 109 – 115 VAC 47 Hz, 50% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 58.4 mV).

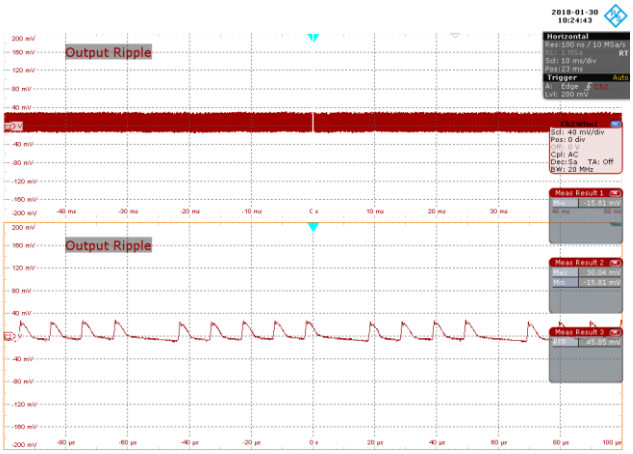

Figure 110 – 230 VAC 47 Hz, 50% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 45.8 mV).

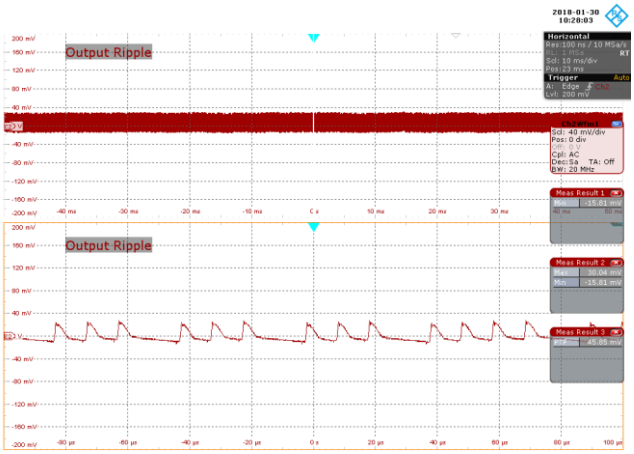

Figure 111 – 265 VAC 47 Hz, 50% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 45.8 mV).

17.6.2.4 25% Load Condition

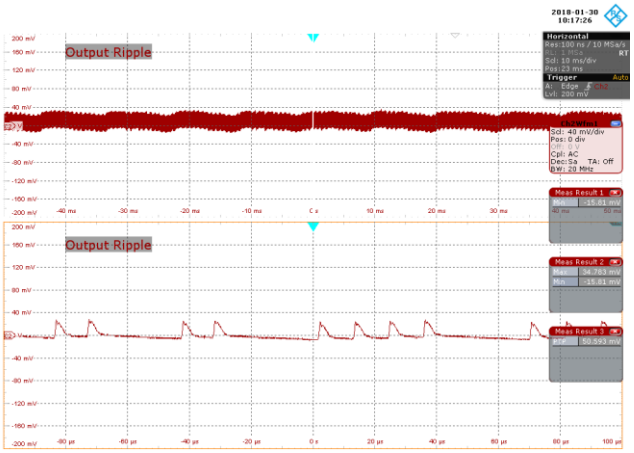

Figure 112 – 90 VAC 47 Hz, 25% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 50.5 mV).

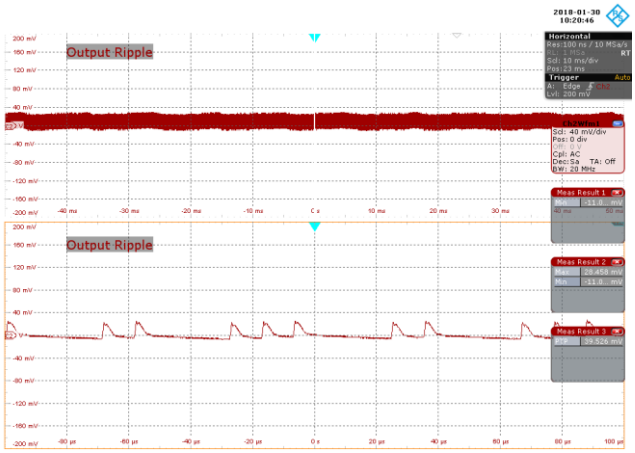

Figure 113 – 115 VAC 47 Hz, 25% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 39.5 mV).

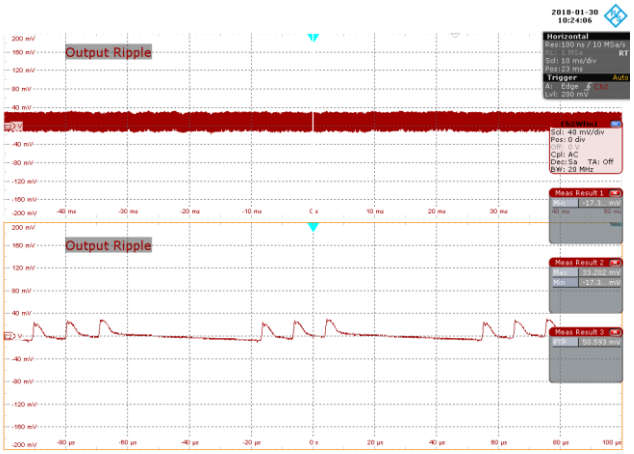

Figure 114 – 230 VAC 47 Hz, 25% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 50.5 mV).

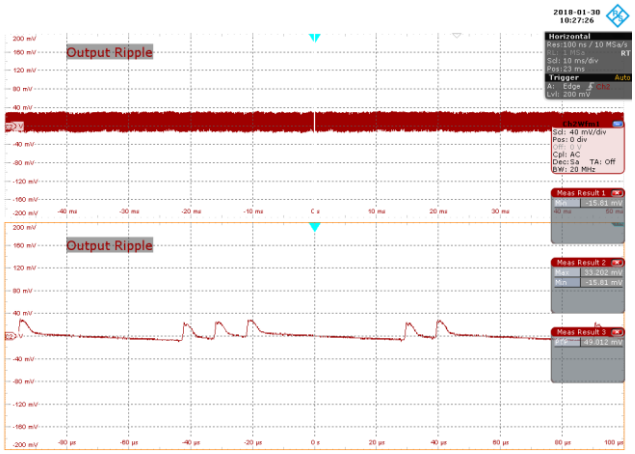

Figure 115 – 265 VAC 47 Hz, 25% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 49.0 mV).

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17.6.2.5 0% Load Condition

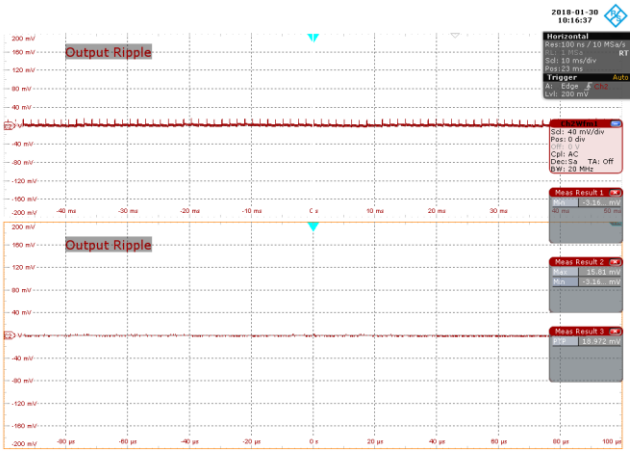

Figure 116 – 90 VAC 47 Hz, 0% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 18.9 mV).

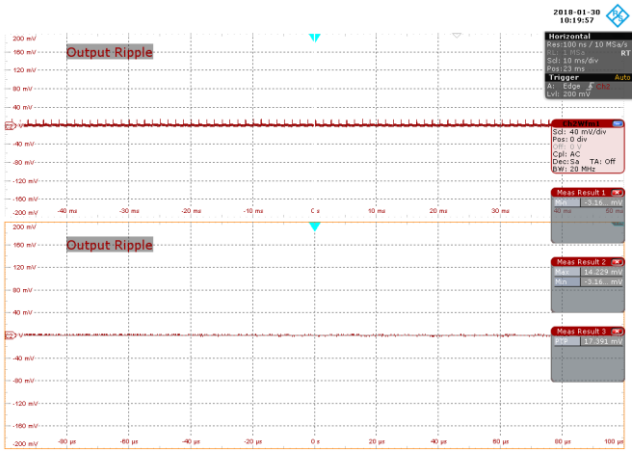

Figure 117 – 115 VAC 47 Hz, 0% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 17.3 mV).

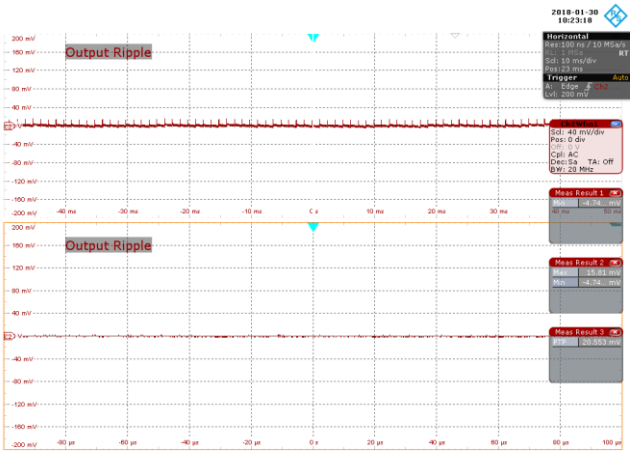

Figure 118 – 230 VAC 47 Hz, 0% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 20.5 mV).

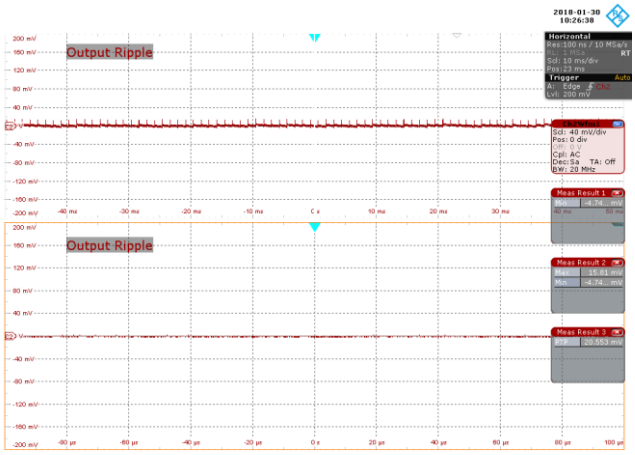

Figure 119 – 265 VAC 47 Hz, 0% Load.
CH1: V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 20.5 mV).

17.6.3 Ripple at Hot and Cold Temperatures

17.6.3.1 90 VAC

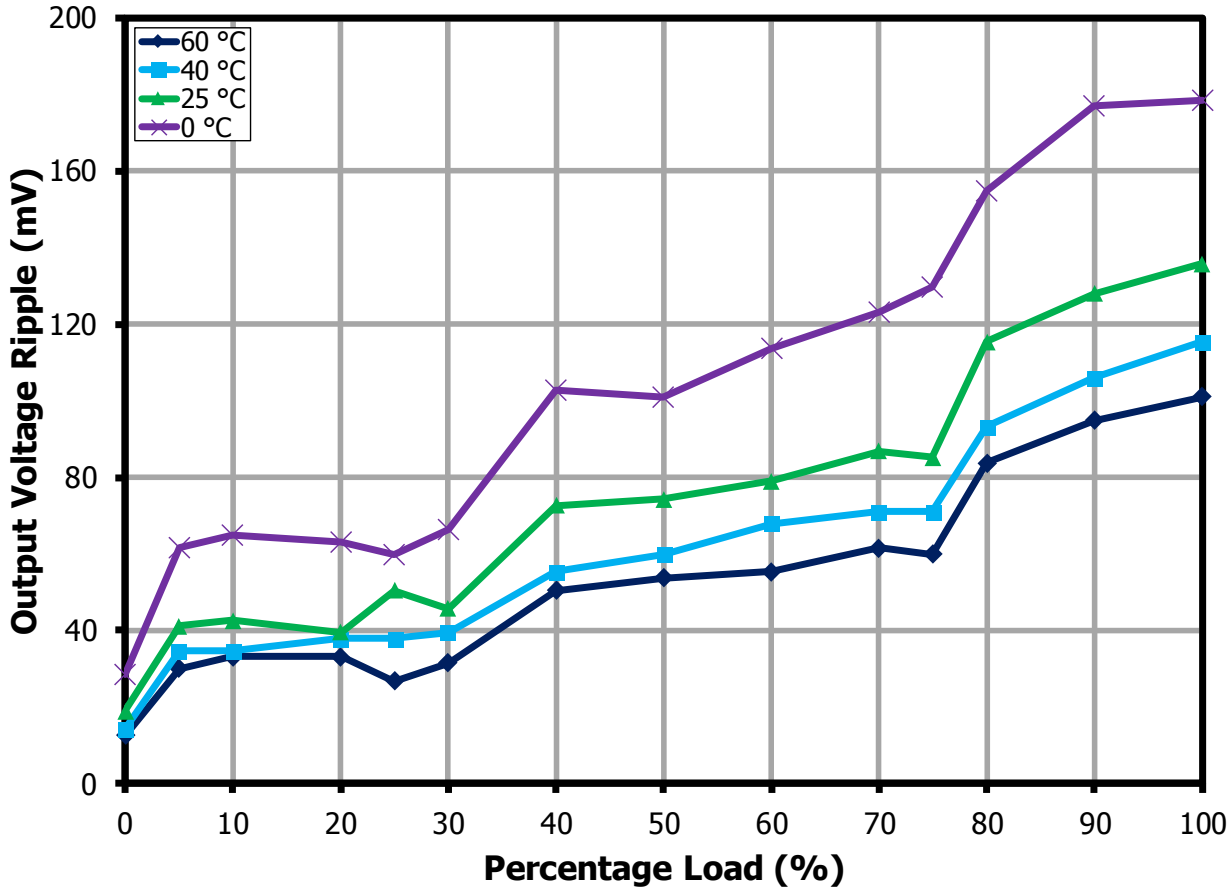

Figure 120 – 90 VAC Voltage Ripple.

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17.6.3.2 115 VAC

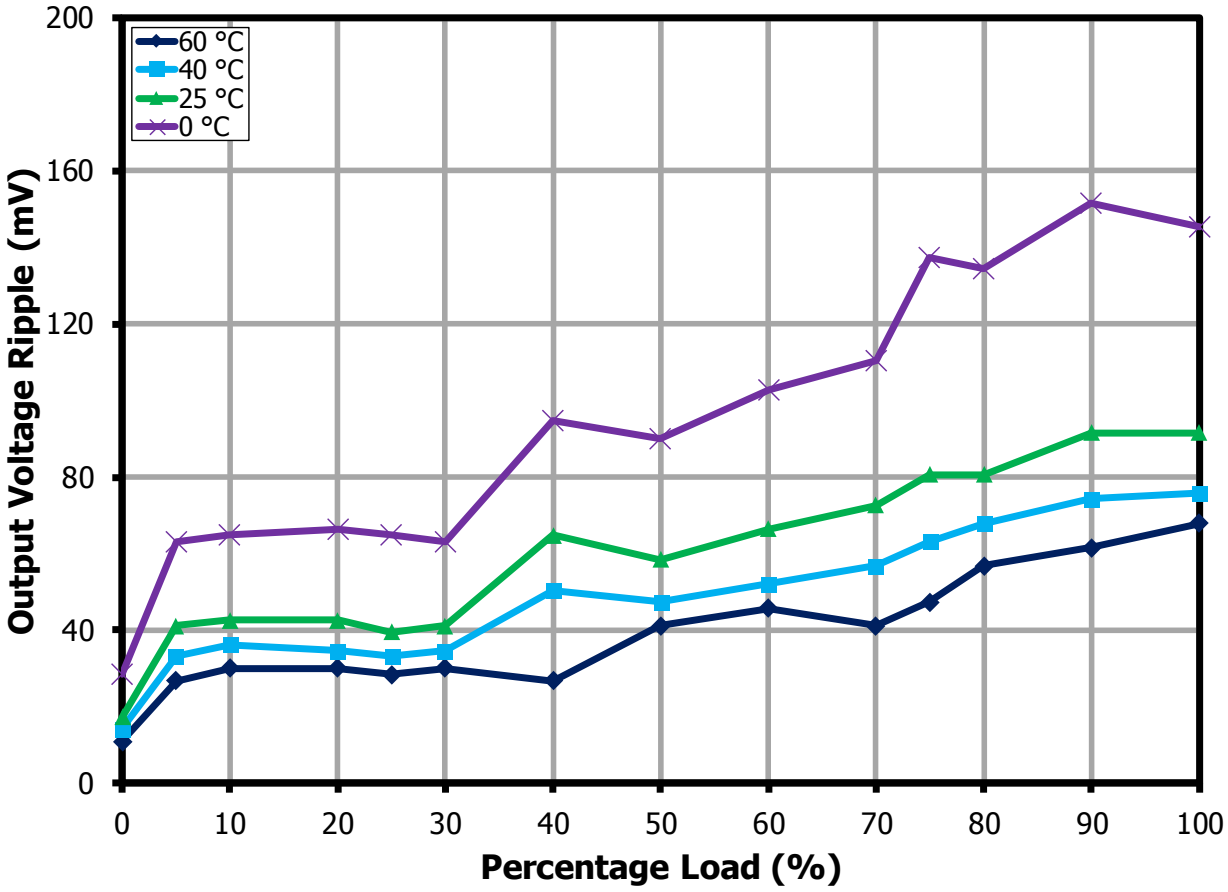

Figure 121 – 115 VAC Voltage Ripple.

17.6.3.3 230 VAC

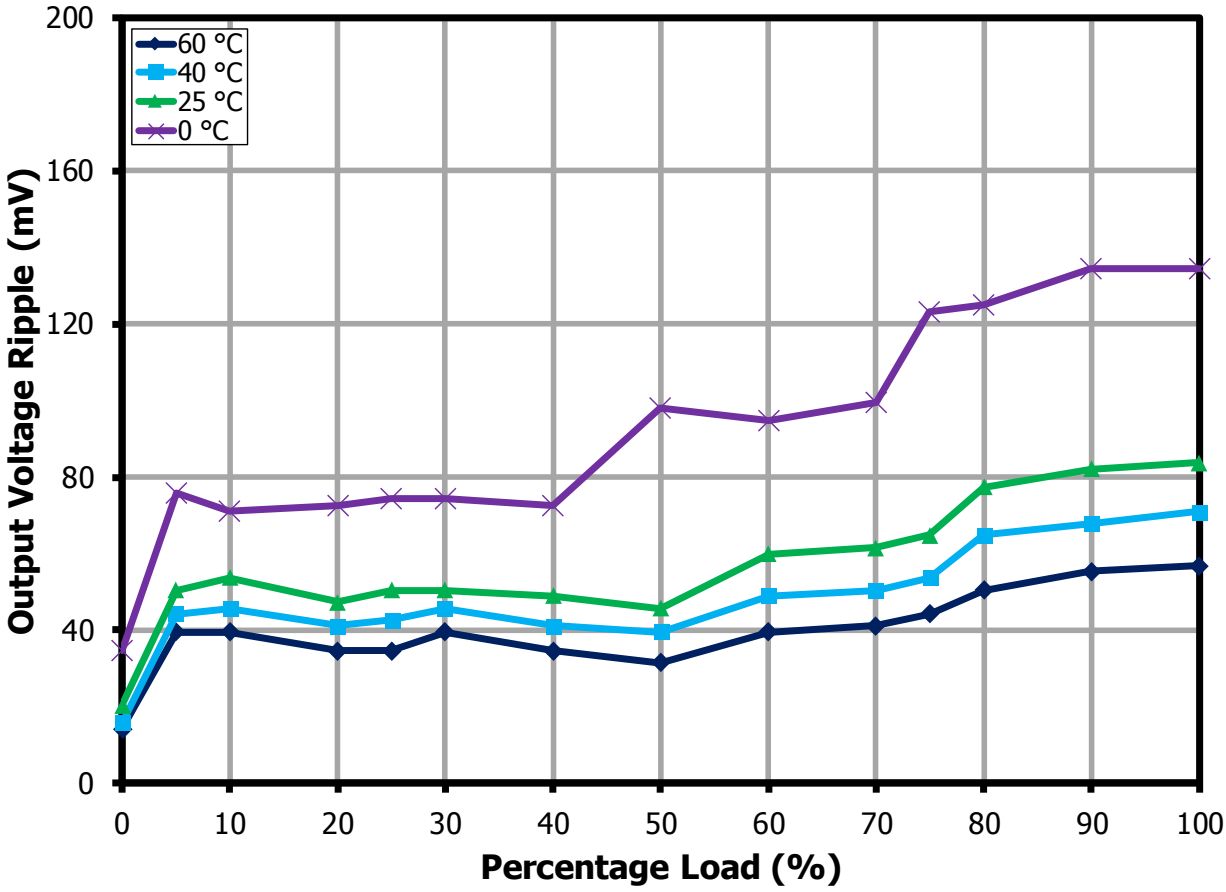

Figure 122 – 230 VAC Voltage Ripple.

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17.6.3.4 265 VAC

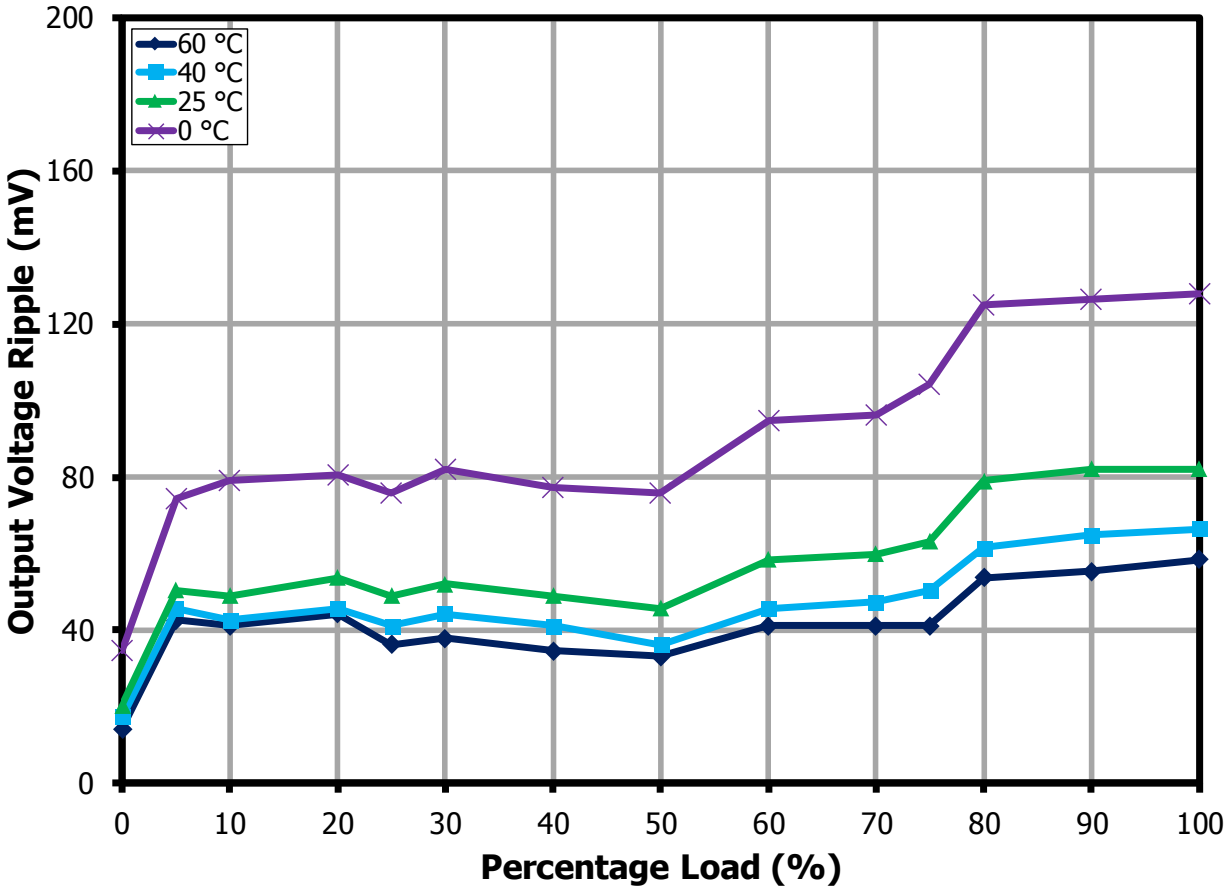

Figure 123 – 265 VAC Output Voltage Ripple.

18 Conducted EMI

18.1 *Test Set-up*

Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Full Load with input voltage set at 230 VAC and 115 VAC.

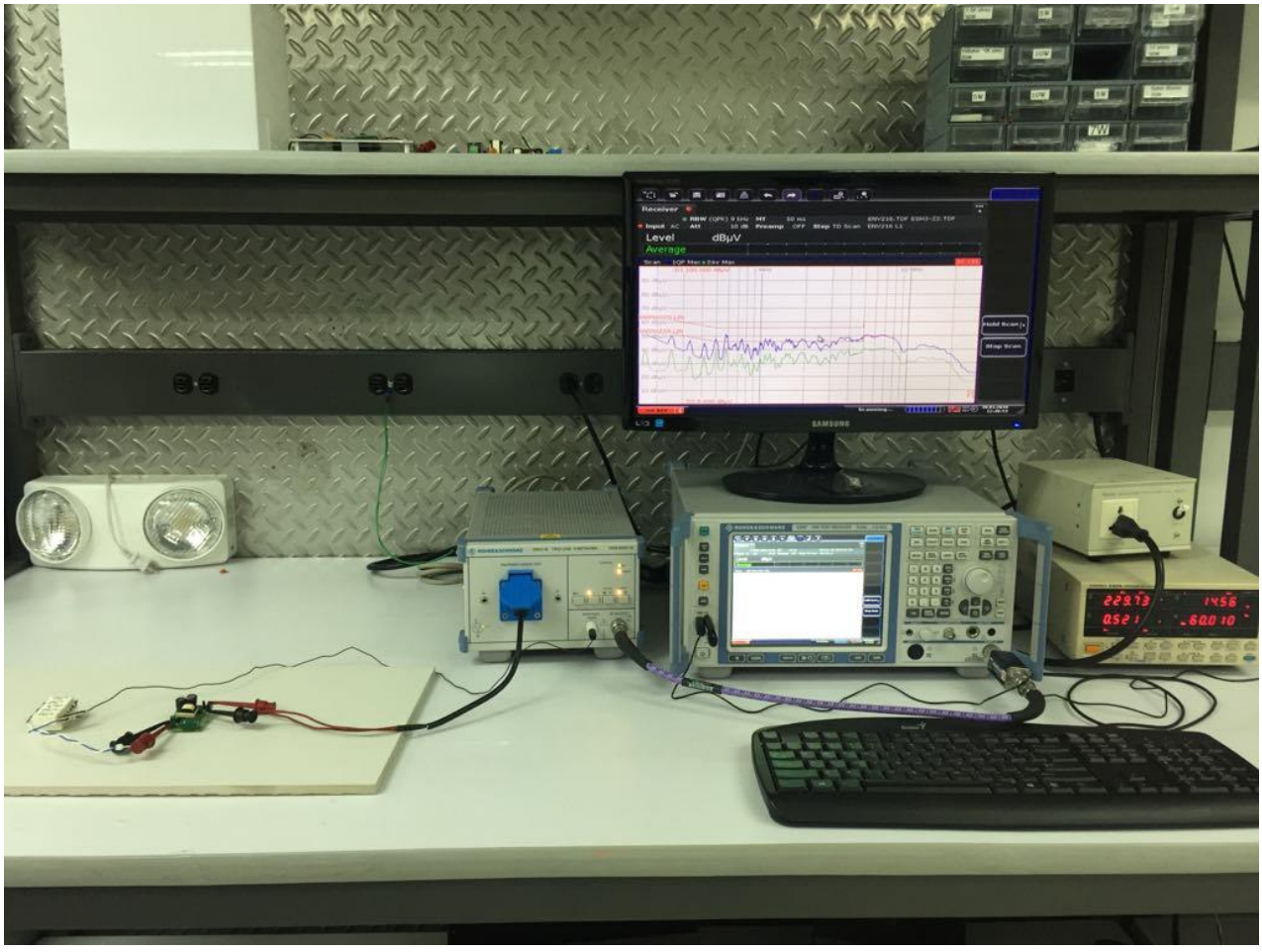

Figure 124 – Conducted EMI Test Set-up.

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18.2 *8.4 W Resistive Load, Floating Output*

18.2.1 115 VAC, Line

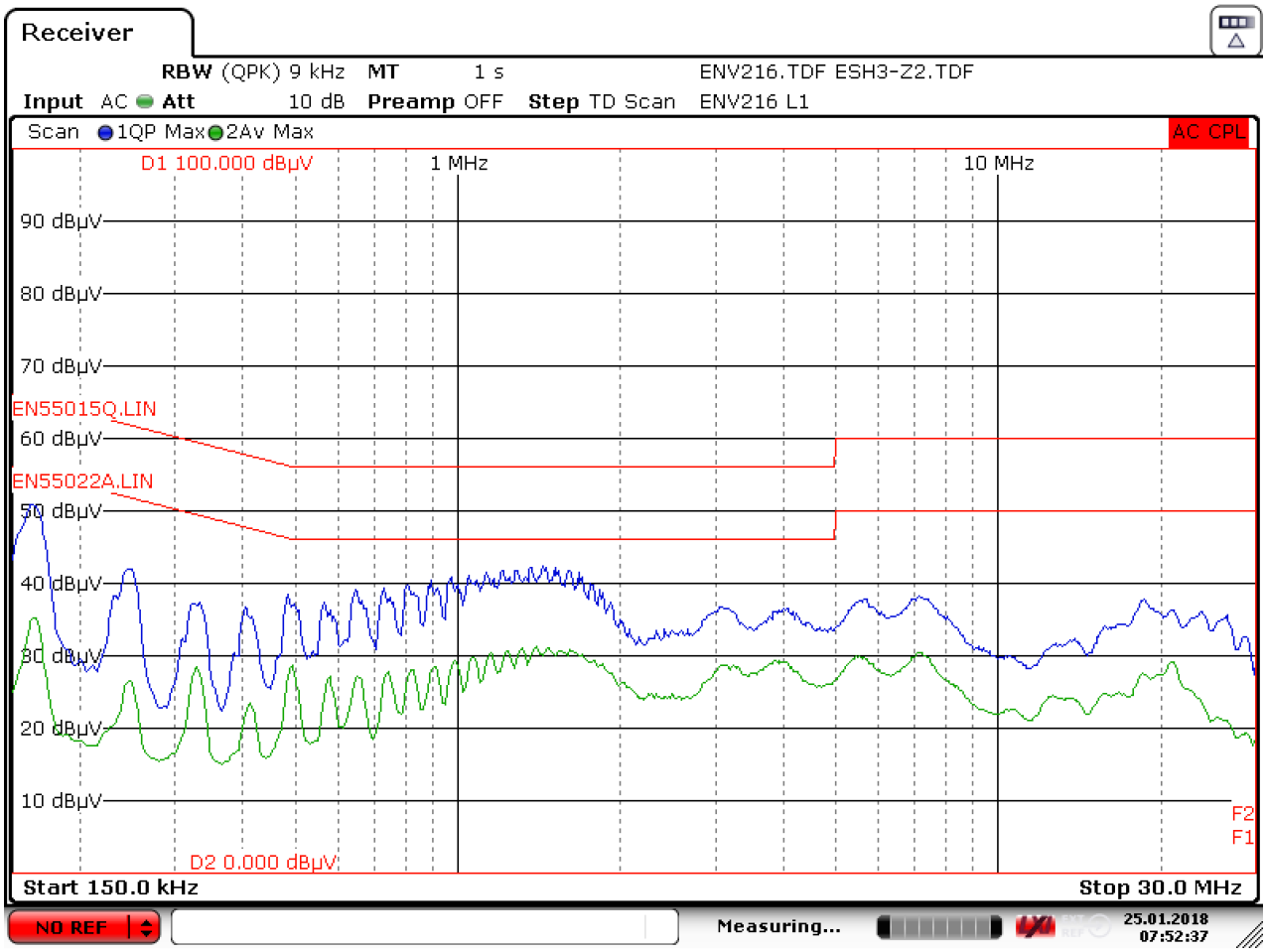
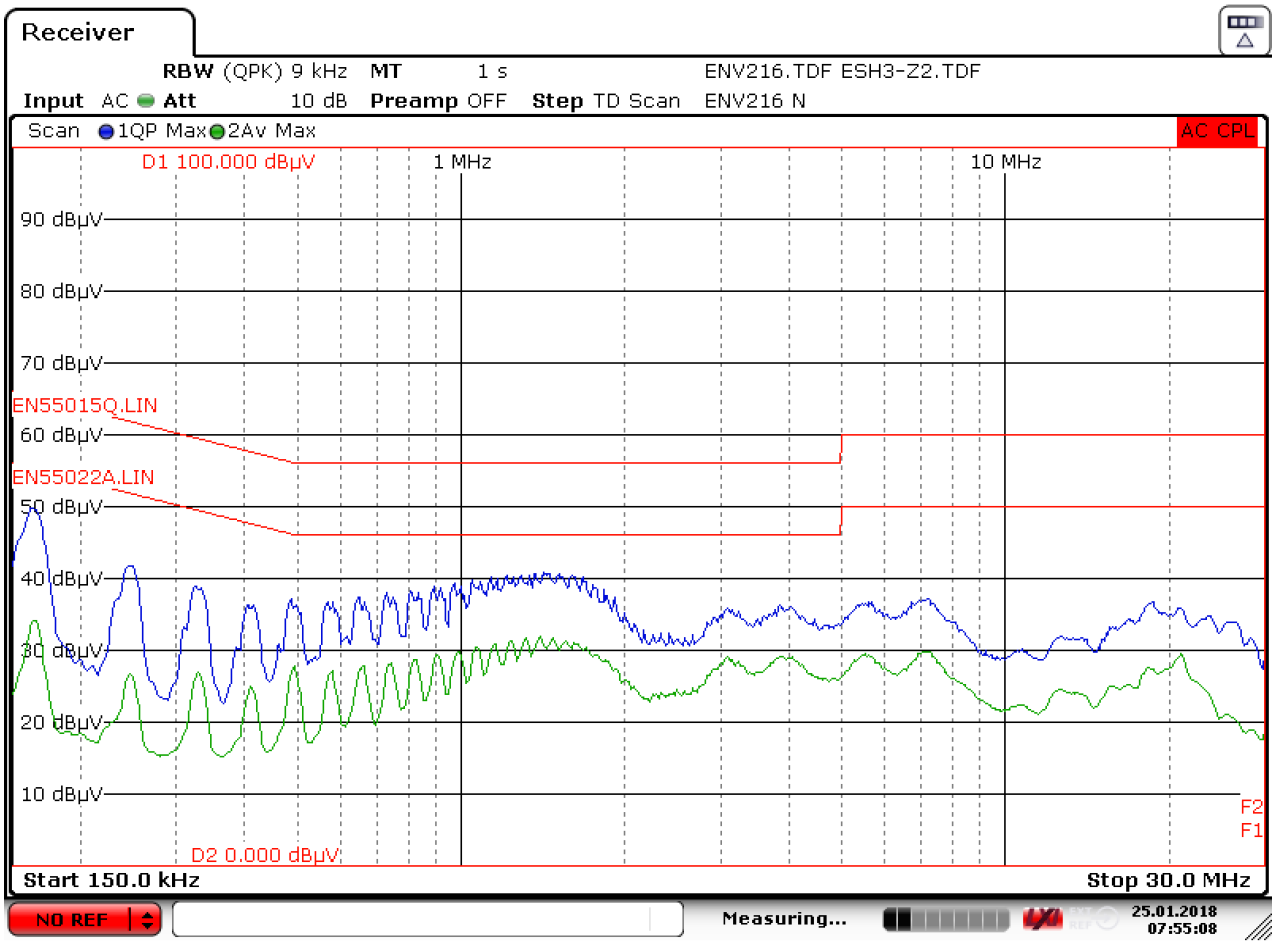


Figure 125 – Floating Ground EMI at 115 VAC, Line.

18.2.2 115 VAC, Neutral



Date: 25.JAN.2018 07:55:08

Figure 126 – Floating Ground EMI at 115 VAC, Neutral.

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18.2.3 230 VAC, Line

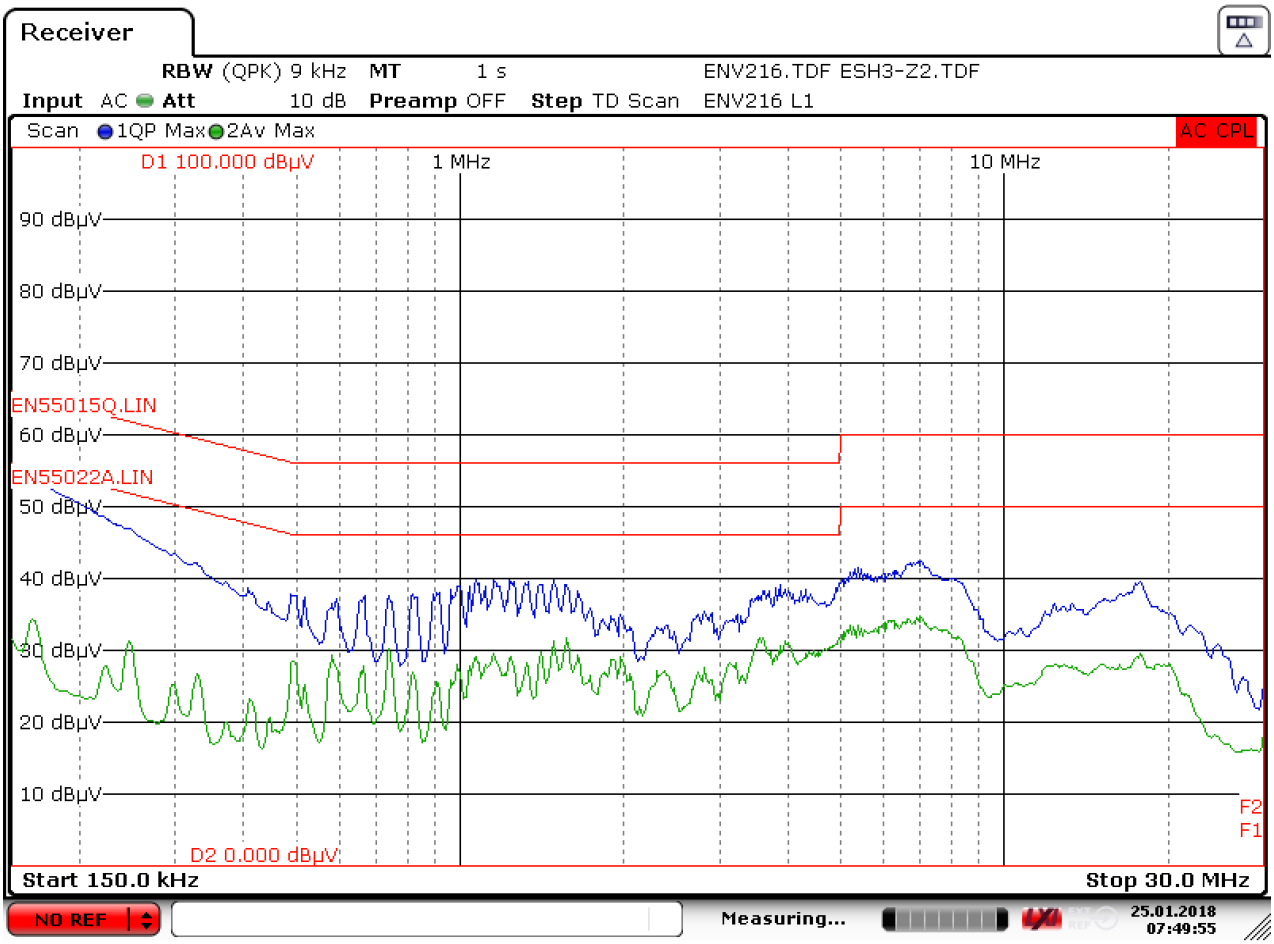

Figure 127 – Floating Ground EMI at 230 VAC, Line.

18.2.4 230 VAC, Neutral

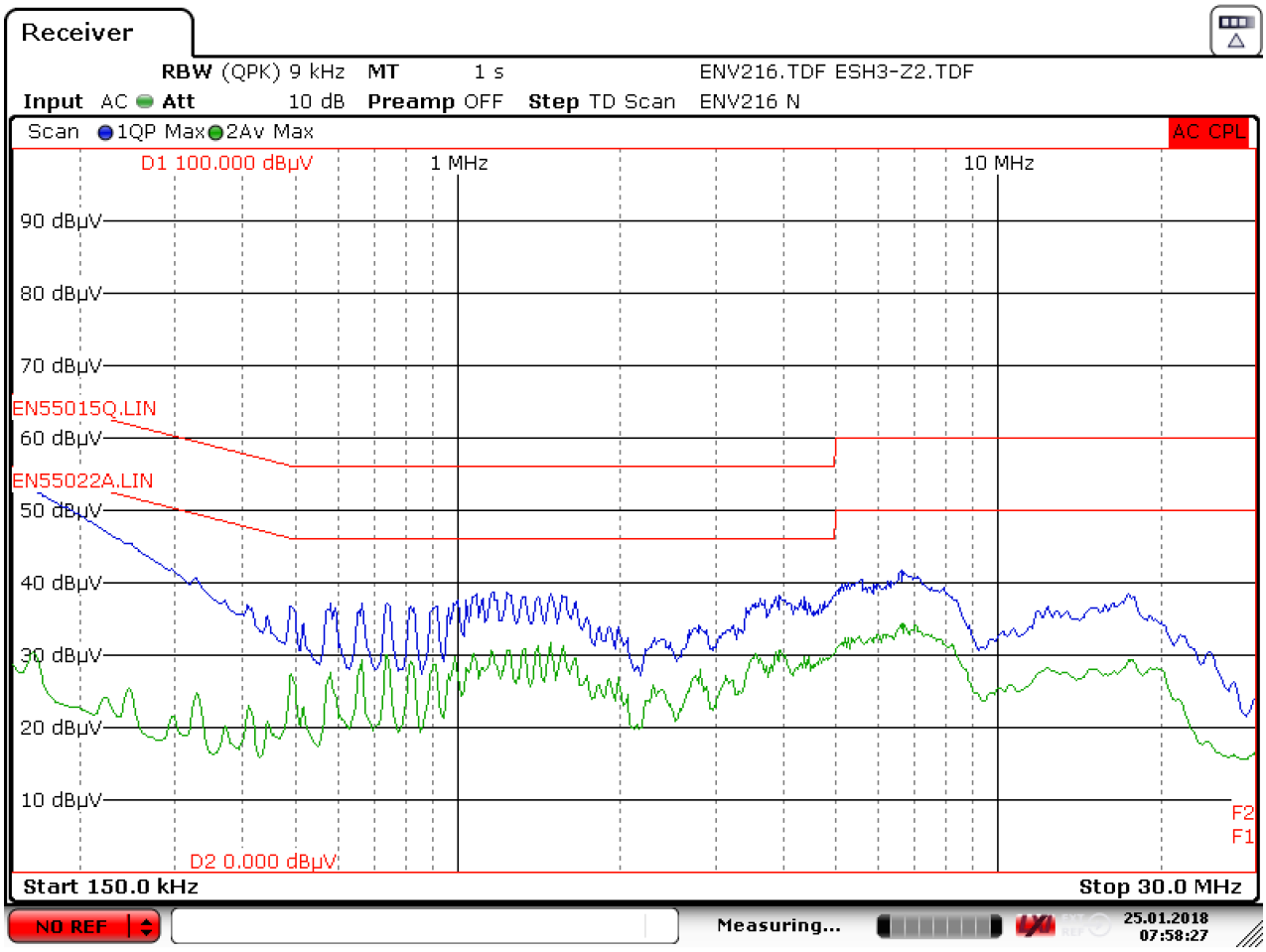

Figure 128 – Floating Ground EMI at 230 VAC, Neutral.

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18.3 *8.4 W Resistive Load, Artificial Hand*

18.3.1 115 VAC, Line

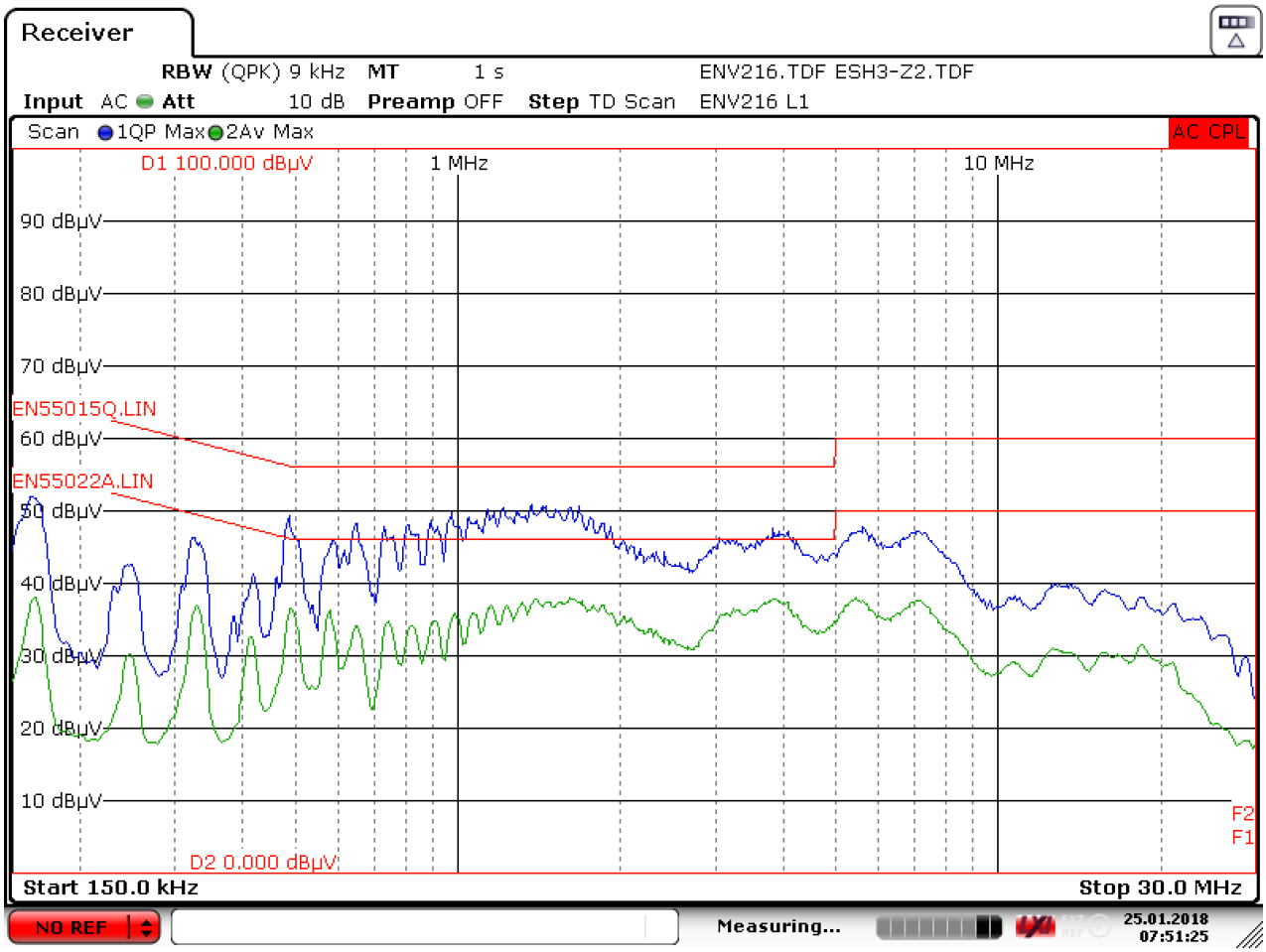

Figure 129 – Artificial Hand Ground EMI at 115 VAC, Line.

18.3.2 115 VAC, Neutral

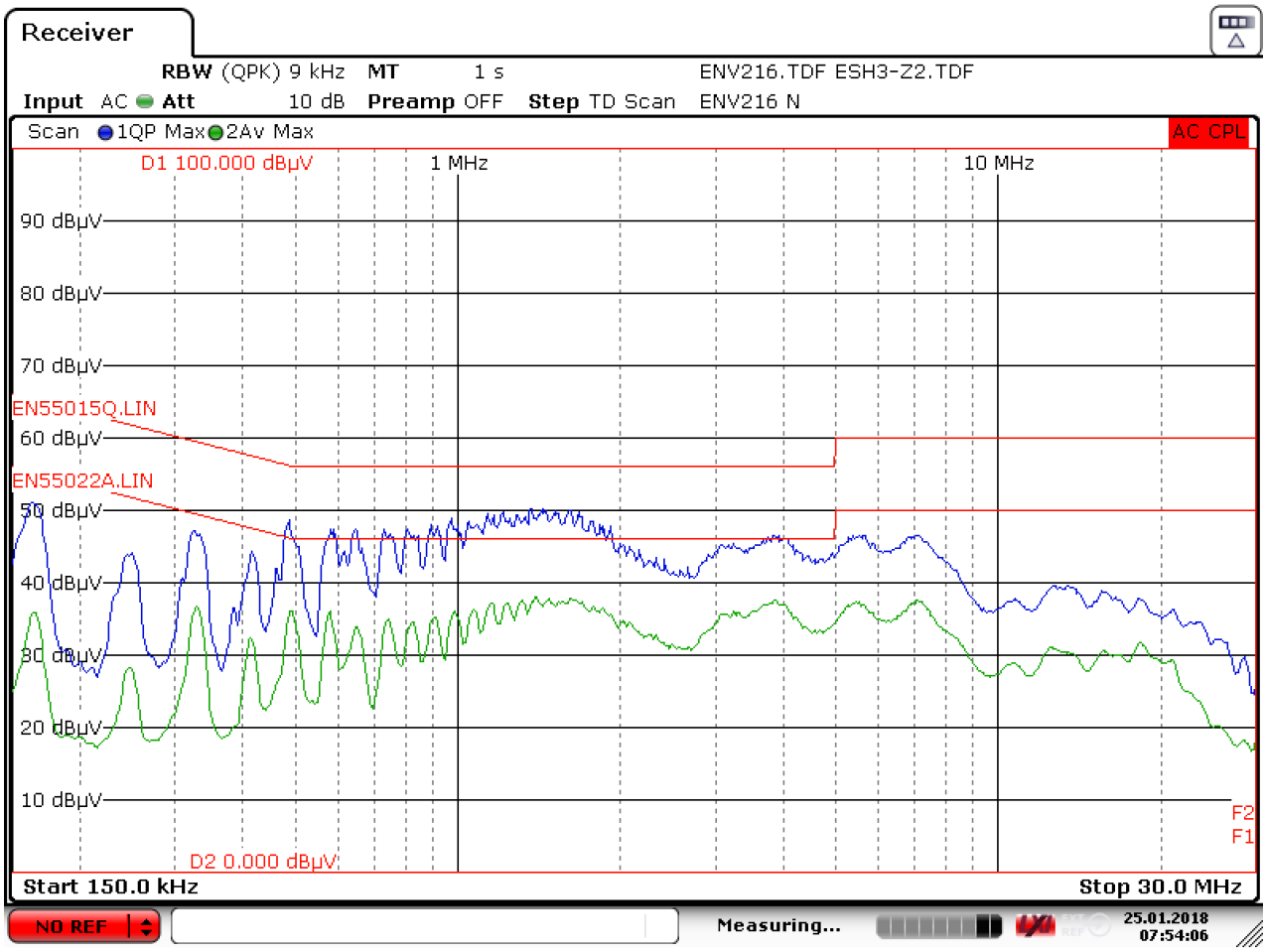

Figure 130 – Artificial Hand Ground EMI at 115 VAC, Neutral.

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18.3.3 230 VAC, Line

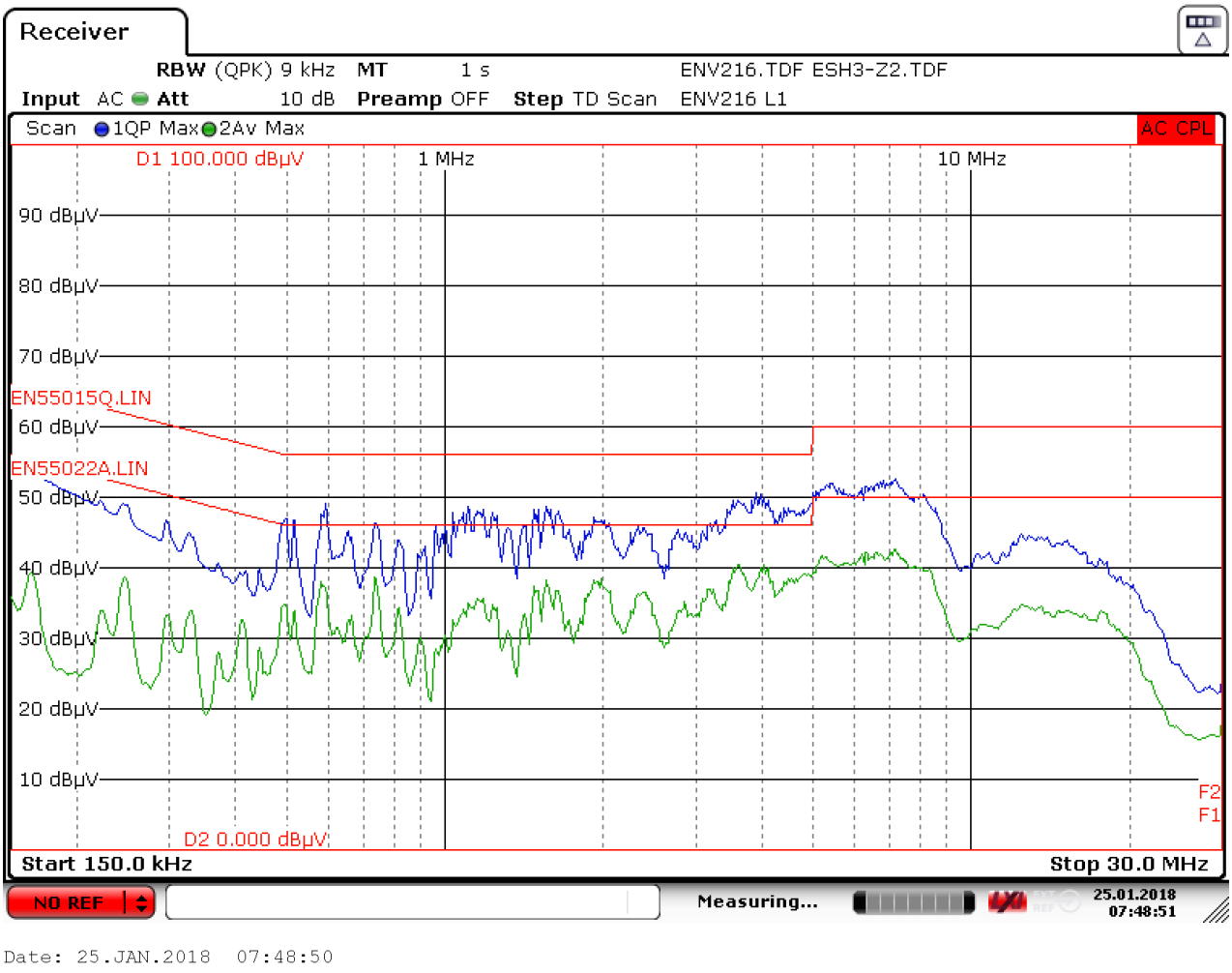

Figure 131 – Artificial Hand Ground EMI at 230 VAC, Line.

18.3.4 230 VAC, Neutral

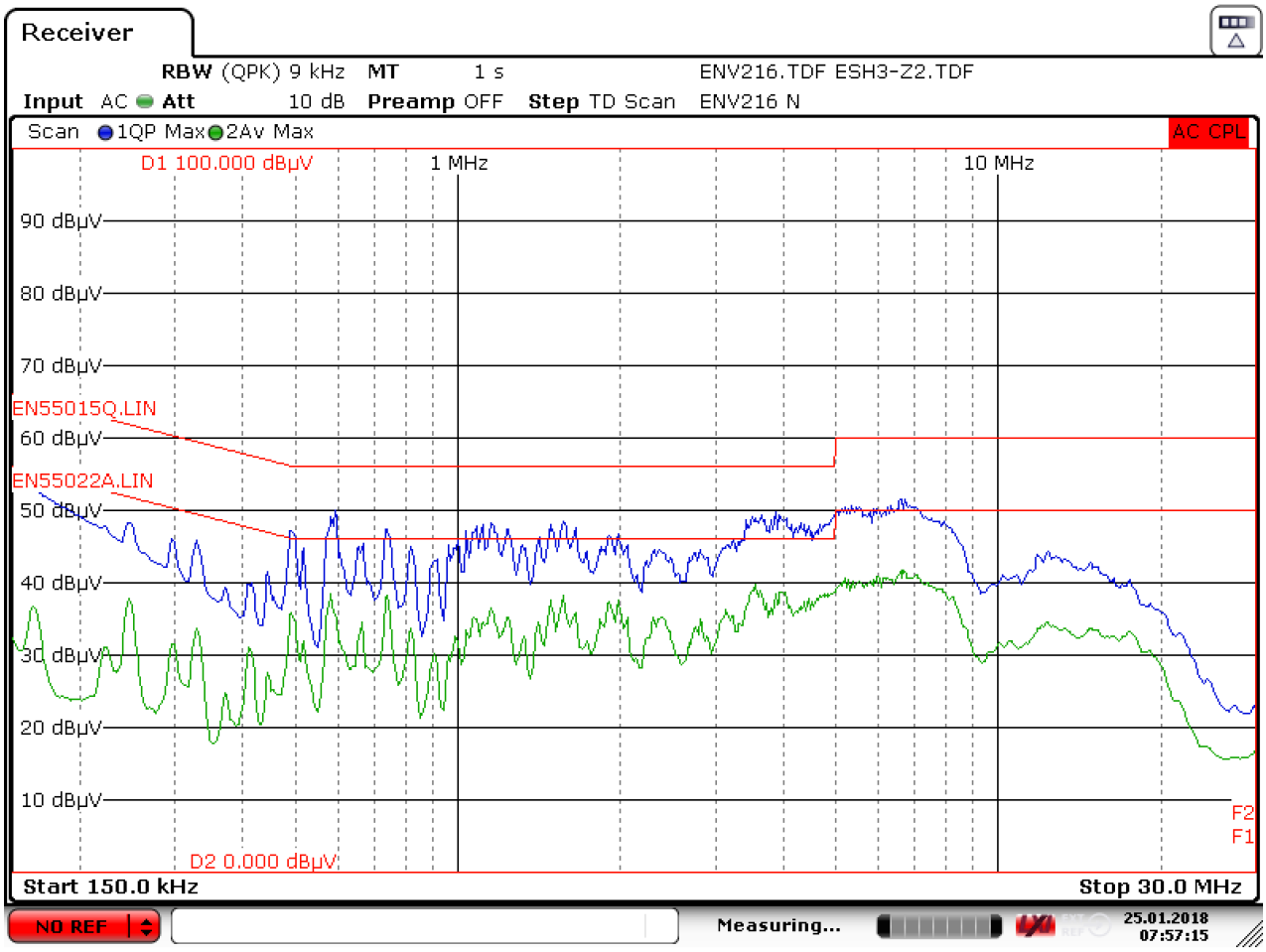

Figure 132 – Artificial Hand Ground EMI at 230 VAC, Neutral.

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19 ESD Test

19.1 *ESD Test*

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
+8000	115	Contact	10	PASS
+16000	115	Air	10	PASS
+8000	230	Contact	10	PASS
+16000	230	Air	10	PASS

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
-8000	115	Contact	10	PASS
-16000	115	Air	10	PASS
-8000	230	Contact	10	PASS
-16000	230	Air	10	PASS

20 Revision History

Date	Author	Revision	Description & Changes	Reviewed
22-May-18	CE	1.0	Initial Release	Apps & Mktg
05-Dec-18	KM	1.1	Updated Application on First Page	
31-Jan-19	KM	1.2	Updated Page 1 Summary Bullets	

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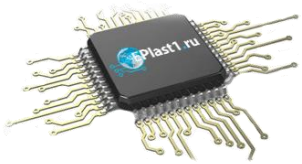
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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