CC1310 SimpleLink™ Ultralow Power Sub-1-GHz Wireless MCU

1 Device Overview

1.1 Features

- Microcontroller
  - Powerful ARM® Cortex®-M3
  - EEMBC CoreMark® Score: 142
  - EEMBC ULPBench™ Score: 158
  - Up to 48-MHz Clock Speed
  - 128KB of In-System Programmable Flash
  - 8KB of SRAM for Cache (or as General-Purpose RAM)
  - 20KB of Ultralow Leakage SRAM
  - 2-Pin cJTAG and JTAG Debugging
  - Supports Over-the-Air Upgrade (OTA)
- Ultralow Power Sensor Controller
  - Can Run Autonomous From the Rest of the System
  - 16-Bit Architecture
  - 2KB of Ultralow Leakage SRAM for Code and Data
- Efficient Code-Size Architecture, Placing TI-RTOS, Drivers and Bootloader in ROM
- RoHS-Compliant Package
  - 7-mm × 7-mm RGZ VQFN48 (30 GPIOs)
  - 5-mm × 5-mm RHB VQFN48 (15 GPIOs)
  - 4-mm × 4-mm RSM VQFN48 (10 GPIOs)
- Peripherals
  - All Digital Peripheral Pins Can Be Routed to Any GPIO
  - Four General-Purpose Timer Modules (Eight 16-Bit or Four 32-Bit Timers, PWM Each)
  - 12-Bit ADC, 200 ksamples/s, 8-Channel Analog MUX
  - Continuous Time Comparator
  - Ultralow Power Clocked Comparator
  - Programmable Current Source
  - UART
  - 2× SSI (SPI, MICROWIRE, TI)
  - I2C
  - I2S
  - Real-Time Clock (RTC)
  - AES-128 Security Module
  - True Random Number Generator (TRNG)
  - Support for Eight Capacitive Sensing Buttons
  - Integrated Temperature Sensor
- External System
  - On-Chip Internal DC-DC Converter
  - Very Few External Components
  - Seamless Integration With the SimpleLink™ CC1190 Range Extender
- Low Power
  - Wide Supply Voltage Range: 1.8 to 3.8 V
  - Active-Mode RX: 5.5 mA
  - Active-Mode TX at +10 dBm: 12.9 mA
  - Active-Mode MCU 48 MHz Running Coremark: 2.5 mA (51 µA/MHz)
  - Active-Mode MCU: 48.5 CoreMark/mA
  - Active-Mode Sensor Controller at 24 MHz: 0.4 mA + 8.2 µA/MHz
  - Sensor Controller, One Wake Up Every Second Performing One 12-Bit ADC Sampling: 0.85 µA
  - Standby: 0.6 µA (RTC Running and RAM and CPU Retention)
  - Shutdown: 185 nA (Wakeup on External Events)
- RF Section
  - Excellent Receiver Sensitivity –124 dBm Using Long-Range Mode, –110 dBm at 50 kbps
  - Excellent Selectivity: 52 dB
  - Excellent Blocking Performance: 90 dB
  - Programmable Output Power up to +14 dBm
  - Single-Ended or Differential RF Interface
  - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
    - ETSI EN 300 220, EN 303 131, EN 303 204 (Europe)
    - FCC CFR47 Part 15 (US)
    - ARIB STD-T108 (Japan)
  - Wireless M-Bus and IEEE 802.15.4g PHY
- Tools and Development Environment
  - Full-Feature and Low-Cost Development Kits
  - Multiple Reference Designs for Different RF Configurations
  - Packet Sniffer PC Software
  - Sensor Controller Studio
  - SmartRF™ Studio
  - SmartRF Flash Programmer 2
  - IAR Embedded Workbench® for ARM
  - Code Composer Studio™

1.2 Applications

- 315-, 433-, 470-, 500-, 779-, 868-, 915-, and 920-MHz ISM and SRD Systems
- Low-Power Wireless Systems With 50-kHz to 5-MHz Channel Spacing
- SmartGrid and Automatic Meter Reading
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless Healthcare Applications
- Wireless Sensor Networks
- Active RFID
- IEEE 802.15.4g, IP-Enabled Smart Objects (6LoWPAN), Wireless M-Bus, KNX Systems, Wi-SUN, ZigBee and Proprietary Systems
- Energy Harvesting Applications
- ESL (Electronic Shelf Label)
- Long-Range Sensor Applications
- Heat Cost Allocators

1.3 Description

The device is a member of the CC26xx and CC13xx family of cost-effective, ultralow power, 2.4-GHz and sub-1-GHz RF devices. Very low active RF, MCU current, and low-power mode current consumption provide excellent battery lifetime and allow operation on small coin-cell batteries and in energy-harvesting applications.

The CC1310 device is the first part in a Sub-1-GHz family of cost-effective, ultralow power wireless MCUs. The CC1310 device combines a flexible, very low power RF transceiver with a powerful 48-MHz Cortex-M3 microcontroller in a platform supporting multiple physical layers and RF standards. A dedicated Radio Controller (Cortex-M0) handles low-level RF protocol commands that are stored in ROM or RAM, thus ensuring ultralow power and flexibility. The low-power consumption of the CC1310 device does not come at the expense of RF performance; the CC1310 device has excellent sensitivity and robustness (selectivity and blocking) performance.

The CC1310 device is a highly integrated, true single-chip solution incorporating a complete RF system and an on-chip DC-DC converter.

Sensors can be handled in a very low-power manner by a dedicated autonomous ultralow power MCU that can be configured to handle analog and digital sensors; thus the main MCU (Cortex-M3) is able to maximize sleep time.

The CC1310 power and clock management and radio systems require specific configuration and handling by software to operate correctly. This has been implemented in the TI RTOS, and it is therefore recommended that this software framework is used for all application development on the device. The complete TI-RTOS and device drivers are offered in source code free of charge.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC1310F128RGZ	VQFN (48)	7.00 mm × 7.00 mm
CC1310F128RHB	VQFN (32)	5.00 mm × 5.00 mm
CC1310F128RSM	VQFN (32)	4.00 mm × 4.00 mm
CC1310F64RGZ	VQFN (48)	7.00 mm × 7.00 mm
CC1310F64RHB	VQFN (32)	5.00 mm × 5.00 mm
CC1310F64RSM	VQFN (32)	4.00 mm × 4.00 mm
CC1310F32RGZ	VQFN (48)	7.00 mm × 7.00 mm
CC1310F32RHB	VQFN (32)	5.00 mm × 5.00 mm
CC1310F32RSM	VQFN (32)	4.00 mm × 4.00 mm

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 shows a block diagram for the CC1310 device.

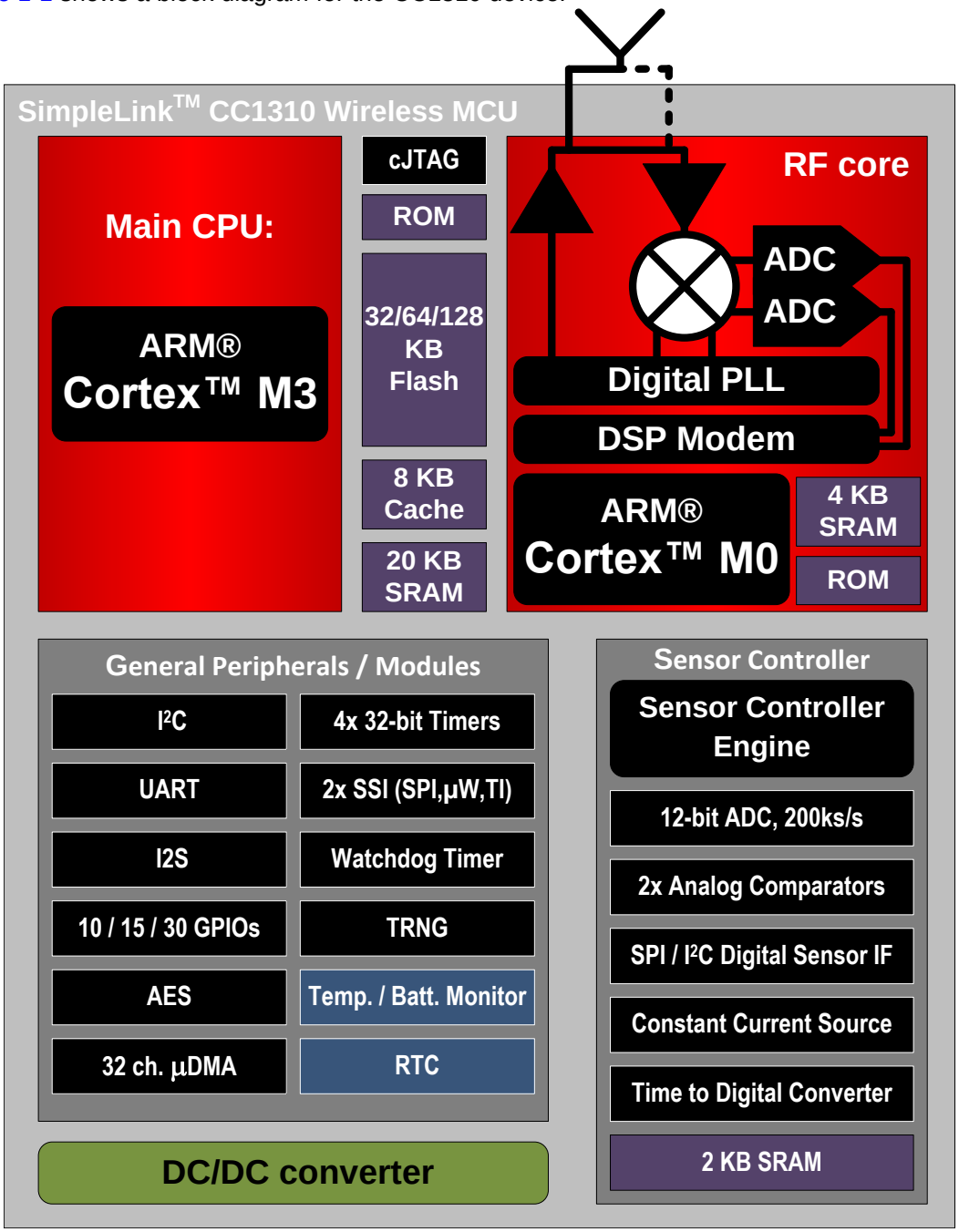

Figure 1-1. CC1310 Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 30, 2015 to October 23, 2015 **Page**

- Added the RSM and RHB packages 6

Changes from August 31, 2015 to September 30, 2015 **Page**

- Changed device status from: Product Preview to: Production Data 1
- Removed the RSM and RHB packages 6
- Changed *Typical Characteristics* section 24

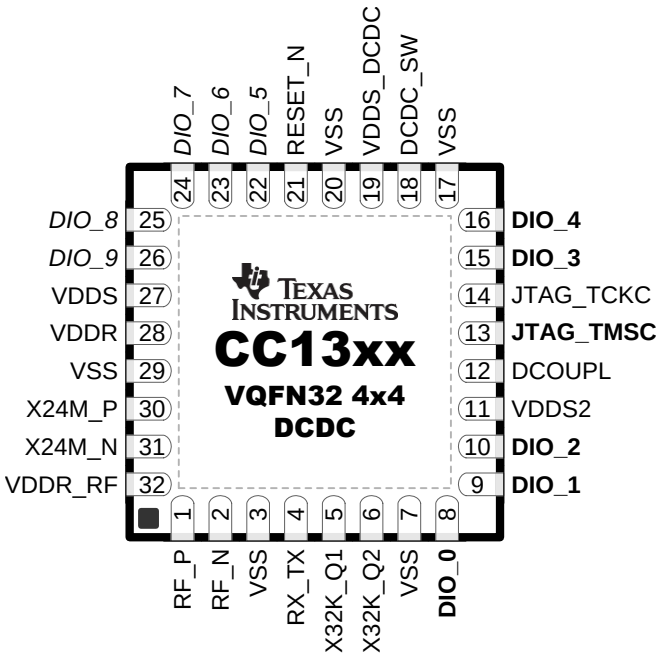
3 Device Comparison

Table 3-1. Device Family Overview

DEVICE	PHY SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE SIZE
CC1310F128RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g	128	20	30	7 mm × 7 mm
CC1310F64RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g	64	16	30	
CC1310F32RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g	32	16	30	
CC1310F128RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g	128	20	15	5 mm × 5 mm
CC1310F64RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g	64	16	15	
CC1310F32RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g	32	16	15	
CC1310F128RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g	128	20	10	4 mm × 4 mm
CC1310F64RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g	64	16	10	
CC1310F32RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g	32	16	10	

4 Terminal Configuration and Functions

4.1 Pin Diagram – RSM Package



Note: I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

Figure 4-1. RSM (4-mm × 4-mm) Pinout, 0.4-mm Pitch

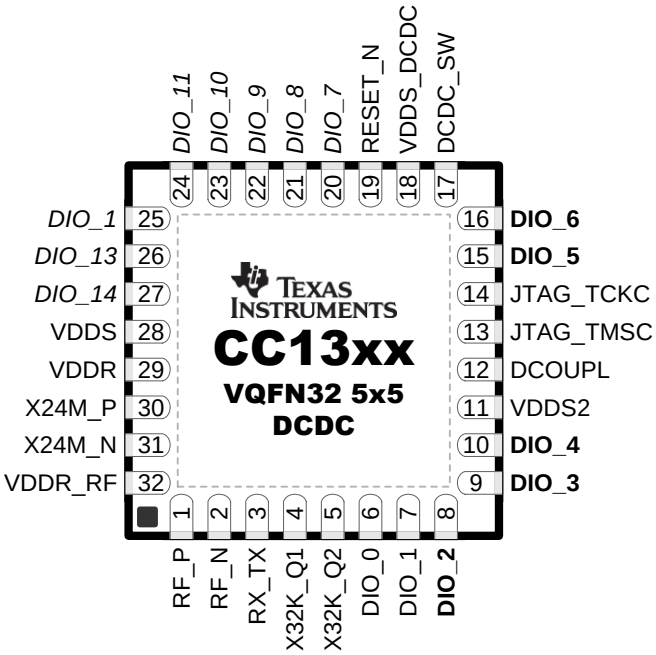
4.2 Signal Descriptions – RSM Package

Table 4-1. Signal Descriptions – RSM Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	18	Power	Output from internal DC-DC(1). Tie to ground for external regulator mode (1.7-V to 1.95-V operation)
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling capacitor(2)
DIO_0	8	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_1	9	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_2	10	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_3	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_4	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_5	22	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_6	23	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_7	24	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_8	25	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_9	26	Digital/Analog I/O	GPIO, Sensor Controller, Analog
EGP	—	Power	Ground – Exposed Ground Pad
JTAG_TMSC	13	Digital I/O	JTAG TMSC
JTAG_TCKC	14	Digital I/O	JTAG TCKC
RESET_N	21	Digital input	Reset, active low. No internal pullup
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RX_TX	4	RF I/O	Optional bias pin for the RF LNA
VDDS	27	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply(1)
VDDS_DCDC	19	Power	1.8-V to 3.8-V DC-DC supply. Tie to ground for external regulator mode (1.7-V to 1.95-V operation)
VDDR	28	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC(3)(2)
VDDR_RF	32	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC(4)(2)
VSS	3, 7, 17, 20, 29	Power	Ground
X32K_Q1	5	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	6	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2

(1) See Section 8.2, technical reference manual for more details.
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.3 Pin Diagram – RHB Package



Note: I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

Figure 4-2. RHB (5-mm × 5-mm) Pinout, 0.5-mm Pitch

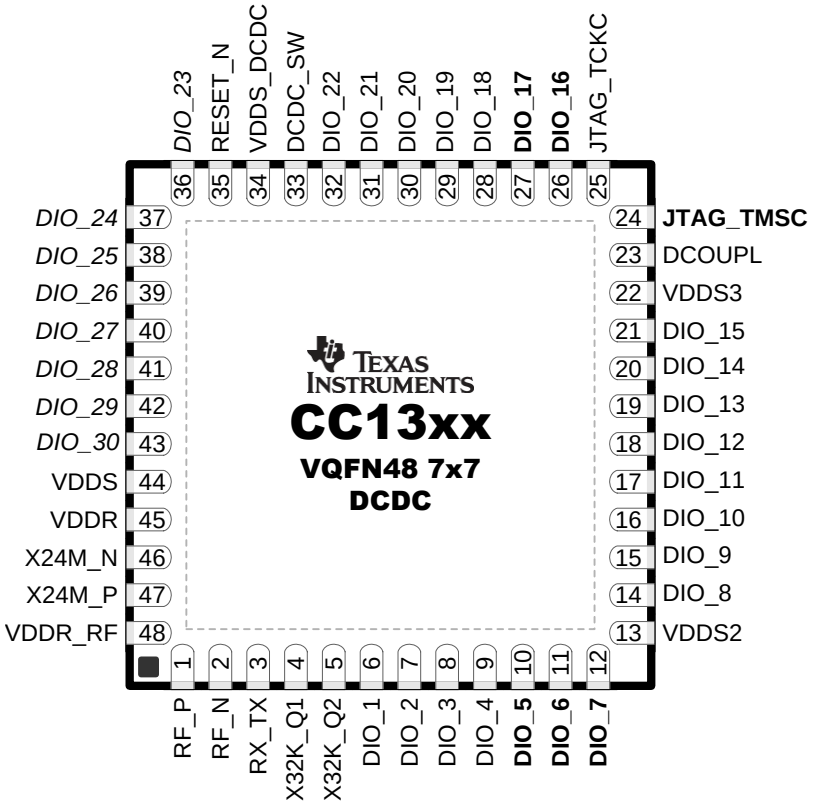
4.4 Signal Descriptions – RHB Package

Table 4-2. Signal Descriptions – RHB Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	17	Power	Output from internal DC-DC (1)
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling (2)
DIO_0	6	Digital I/O	GPIO, Sensor Controller
DIO_1	7	Digital I/O	GPIO, Sensor Controller
DIO_2	8	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_3	9	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_4	10	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_5	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_6	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_7	20	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_8	21	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_9	22	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_10	23	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_11	24	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_12	25	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_13	26	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_14	27	Digital/Analog I/O	GPIO, Sensor Controller, Analog
EGP	—	Power	Ground – Exposed Ground Pad
JTAG_TMSC	13	Digital I/O	JTAG TMSC, High drive capability
JTAG_TCKC	14	Digital I/O	JTAG TCKC
RESET_N	19	Digital input	Reset, active-low. No internal pullup
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
VDDR	29	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC (3) (2)
VDDR_RF	32	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC (4) (2)
VDDS	28	Power	1.8-V to 3.8-V main chip supply (1)
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply (1)
VDDS_DCDC	18	Power	1.8-V to 3.8-V DC-DC supply
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2

(1) See Section 8.2, technical reference manual for more details.
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.5 Pin Diagram – RGZ Package



Note: I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

Figure 4-3. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch

4.6 Signal Descriptions – RGZ Package

Table 4-3. Signal Descriptions – RGZ Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	33	Power	Output from internal DC-DC(1)
DCOUPL	23	Power	1.27-V regulated digital-supply (decoupling capacitor)(2)
DIO_1	6	Digital I/O	GPIO, Sensor Controller
DIO_2	7	Digital I/O	GPIO, Sensor Controller
DIO_3	8	Digital I/O	GPIO, Sensor Controller
DIO_4	9	Digital I/O	GPIO, Sensor Controller
DIO_5	10	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_6	11	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_7	12	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO

(1) See technical reference manual listed in *Documentation Support* for more details.
(2) Do not supply external circuitry from this pin.

Table 4-3. Signal Descriptions – RGZ Package (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, High drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, High drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_24	37	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_25	38	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_26	39	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_27	40	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_28	41	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_29	42	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_30	43	Digital/Analog I/O	GPIO, Sensor Controller, Analog
EGP	—	Power	Ground – Exposed Ground Pad
JTAG_TMSC	24	Digital I/O	JTAG TMSC, High drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCKC
RESET_N	35	Digital input	Reset, active-low. No internal pullup
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
VDDR	45	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC (3) (2)
VDDR_RF	48	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC (4) (2)
VDDS	44	Power	1.8-V to 3.8-V main chip supply (1)
VDDS2	13	Power	1.8-V to 3.8-V DIO supply (1)
VDDS3	22	Power	1.8-V to 3.8-V DIO supply (1)
VDDS_DCDC	34	Power	1.8-V to 3.8-V DC-DC supply
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2

(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
VDDS(3)	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin(4)		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input RF level			10	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VDDS, unless otherwise noted.
(3) VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIO.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	All pins	±3500	V
		Charged device model (CDM), per JESD22-C101(2)	All pins	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Ambient temperature		–40	85	°C
Operating supply voltage (VDDS)	For operation in battery-powered and 3.3-V systems (internal DC-DC can be used to minimize power consumption)	1.8	3.8	V
Rising supply voltage slew rate		0	100	mV/µs
Falling supply voltage slew rate		0	20	mV/µs
Falling supply voltage slew rate, with low-power flash setting(1)			3	mV/µs
Positive temperature gradient in standby(2)	No limitation for negative temperature gradient, or outside standby mode		5	°C/s

(1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.
(2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see Section 5.10.3.4).

5.4 Power Consumption Summary

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.6 V with DC-DC enabled, unless otherwise noted. Using boost mode (increasing VDDR up to 1.95 V), will increase currents below by 15% (does not apply to TX 14-dBm setting where this current is already included).

PARAMETER		TEST CONDITIONS	TYP	UNIT
I_{core}	Core current consumption	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	100	nA
		Shutdown. No clocks running, no retention	185	
		Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF	0.6	µA
		Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF	0.7	
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF	1.6	
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF	1.7	
		Idle. Supply Systems and RAM powered.	570	
		Active. MCU running CoreMark at 48 MHz	1.2 mA + 25.5 µA/MHz	
		Active. MCU running CoreMark at 48 MHz	2.5	mA
		Active. MCU running CoreMark at 24 MHz	1.9	
		Radio RX	5.5	mA
		Radio TX, 10-dBm output power	12.9	
		Radio TX, boost mode (VDDR = 1.95 V), 14-dBm output power	22.6	
PERIPHERAL CURRENT CONSUMPTION(1)(2)(3)				
I_{peri}	Peripheral power domain	Delta current with domain enabled	20	µA
	Serial power domain	Delta current with domain enabled	13	
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	237	
	µDMA	Delta current with clock enabled, module idle	130	
	Timers	Delta current with clock enabled, module idle	113	
	I^2C	Delta current with clock enabled, module idle	12	
	I^2S	Delta current with clock enabled, module idle	36	
	SSI	Delta current with clock enabled, module idle	93	
	UART	Delta current with clock enabled, module idle	164	

(1) Adds to core current I_{core} for each peripheral unit activated.
(2) I_{peri} is not supported in standby or shutdown modes.
(3) Measured at 3.0 V.

5.5 RF Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands(1)	(300)		(348)	MHz
	(400)		(435)	
	(470)		(510)	
	(779)		(787)	
	863		930	

(1) For more information, refer to *CC1310 SimpleLink Wireless MCU Silicon Errata* (SWRZ062).

5.6 Receive (RX) Parameters

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are done at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data rate			50		kbps
Data rate offset tolerance, IEEE 802.15.4g PHY	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-3}		1400		ppm
Data rate step size			1.5		bps
Digital channel filter programmable bandwidth	Using VCO divide by 5 setting	40		4000	kHz
Receiver sensitivity, 50 kbps	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2} 868 MHz and 915 MHZ		–110		dBm
Receiver saturation	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		10		dBm
Selectivity, ±200 kHz, 50 kbps	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		43, 45		dB
Selectivity, ±400 kHz, 50 kbps	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		48, 52		dB
Blocking ±1 MHz, 50 kbps	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		59, 62		dB
Blocking ±2 MHz, 50 kbps	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		64, 65		dB
Blocking ±5 MHz, 50 kbps	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		67, 68		dB
Blocking ±10 MHz, 50 kbps	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		75, 76		dB
Spurious emissions 1 GHz to 13 GHz (VCO leakage at 3.5 GHz) and 30 MHz to 1 GHz	Radiated emissions measured according to ETSI EN 300 220		–70		dBm
Image rejection (image compensation enabled)	Wanted signal 3-dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		44		dB
RSSI dynamic range	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode). Starting from the sensitivity limit. This is the range that will give an accuracy of ±2		95		dB
RSSI accuracy	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX BW (same modulation format as IEEE 802.15.4g mandatory mode)		±2		dB
Receiver sensitivity, long-range mode 625 bps	10 ksps, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX BW , BER = 10^{-2}		–124		dBm
Selectivity, ±100 kHz, long-range mode 625 bps	Wanted signal 3-dB above sensitivity limit. 10 ksps, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX BW , BER = 10^{-2}		52, 52		dB

Receive (RX) Parameters *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are done at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±200 kHz, long-range mode 625 bps	Wanted signal 3-dB above sensitivity limit. 10 ksps, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX BW , BER = 10^{-2}		61, 61		dB
Blocking ±1 MHz, long-range mode 625 bps	Wanted signal 3-dB above sensitivity limit. 10 ksps, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX BW , BER = 10^{-2}		73, 75		dB
Blocking ±2 MHz, long-range mode 625 bps	Wanted signal 3-dB above sensitivity limit. 10 ksps, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX BW , BER = 10^{-2}		78, 79		dB
Blocking ±10 MHz, long-range mode 625 bps	Wanted signal 3-dB above sensitivity limit. 10 ksps, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX BW , BER = 10^{-2}		89, 90		dB

5.7 Transmit (TX) Parameters

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are done at the antenna input with a combined RX and TX path.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Max output power, boost mode		VDDR = 1.95 V Min VDDS for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Max output power		868 MHz and 915 MHz		12		dBm
Output power programmable range				24		dB
Output power variation		Tested at +10-dBm setting		±0.7		dB
Output power variation, boost bode		+14 dBm		±0.5		dB
Spurious emissions (excluding harmonics)(1)	30 MHz to 1 GHz	Transmitting +14 dBm ETSI restricted bands		<–59		dBm
		Transmitting +14 dBm ETSI outside restricted bands		<–51		dBm
	1 GHz to 12.75 GHz	Transmitting +14 dBm measured in 1-MHz bandwidth (ETSI)		<–37		dBm
Harmonics	Second harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–52, –55		dBm
	Third harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–58, –55		dBm
	Fourth harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–56, –56		dBm

(1) Suitable for systems targeting compliance with EN 300 220, EN 54-25, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

Transmit (TX) Parameters *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are done at the antenna input with a combined RX and TX path.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions out-of-band, 915 MHz (1)	30 MHz–88 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–66		dBm
	88 MHz–216 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–65		dBm
	216 MHz–960 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–65		dBm
	960 MHz–2390 MHz and above 2483.5 MHz (within FCC restricted band)	Transmitting +14 dBm, conducted		<–55		dBm
	1 GHz–12.75 GHz (outside FCC restricted bands)	Transmitting +14 dBm, conducted		<–43		dBm
Spurious emissions out-of-band, 920.6 MHz (1)	Below 710 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–50		dBm
	710–900 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–63		dBm
	900–915 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–61		dBm
	930–1000 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–60		dBm
	1000–1215 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–58		dBm
	Above 1215 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–39		dBm

5.8 PLL Parameters

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868-MHz band	±100-kHz offset, VCO divide by 5		–95		dBc/Hz
	±200-kHz offset, VCO divide by 5		–105		dBc/Hz
	±400-kHz offset, VCO divide by 5		–113		dBc/Hz
	±1000-kHz offset, VCO divide by 5		–121		dBc/Hz
	±2000-kHz offset, VCO divide by 5		–129		dBc/Hz
	±10000 kHz offset, VCO divide by 5		–140		dBc/Hz
Phase noise in the 915-MHz band	±100-kHz offset, VCO divide by 5		–97		dBc/Hz
	±200-kHz offset, VCO divide by 5		–106		dBc/Hz
	±400-kHz offset, VCO divide by 5		–114		dBc/Hz
	±1000-kHz offset, VCO divide by 5		–123		dBc/Hz
	±2000-kHz offset, VCO divide by 5		–131		dBc/Hz
	±10000-kHz offset, VCO divide by 5		–141		dBc/Hz

5.9 Thermal Characteristics

THERMAL METRIC[1]		CC1310 RGZ (VQFN) 48 PINS	UNIT[2]
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) °C/W = degrees Celsius per watt.

5.10 Timing and Switching Characteristics

5.10.1 Reset Timing

	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

5.10.2 Switching Characteristics: Wakeup and Timing

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted. The times listed here do not include RTOS overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Idle → Active			14		µs
MCU, Standby → Active			174		µs
MCU, Shutdown → Active			1097		µs

5.10.3 Clock Specifications

5.10.3.1 24-MHz Crystal Oscillator (XOSC_HF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	MIN	TYP	MAX	UNIT
Crystal frequency		24		MHz
ESR equivalent series resistance		20	60	Ω
L_M Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)		$< 1.6 \times 10^{-24} / C^2_L$		H
C_L Crystal load capacitance	5		9	pF
Start-up time(2)		150		µs

(1) Probing or otherwise stopping the Crystal while the DC-DC converter is enabled may cause permanent damage to the device.
(2) The crystal start-up time is low because it is "kick-started" by using the RCOSC_HF oscillator (temperature and aging compensated) that is running at the same frequency.

5.10.3.2 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
ESR Equivalent series resistance		30	100	kΩ
Crystal load capacitance (C_L)	6		12	pF

(1) Probing or otherwise stopping the crystal while the DC-DC converter is enabled may cause permanent damage to the device.

5.10.3.3 48-MHz RC Oscillator (RCOSC_HF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1%		
Calibrated frequency accuracy(1)		±0.25%		
Start-up time		5		µs

(1) Accuracy relatively to the calibration source (XOSC_HF).

5.10.3.4 32-kHz RC Oscillator (RCOSC_LF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.768		kHz
Temperature coefficient		50		ppm/°C

5.10.4 Flash Memory Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported flash erase cycles before failure		100			k Cycles
Flash page or sector erase current	Average delta current		12.6		mA
Flash page or sector erase time(1)			8		ms
Flash page or sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash write time(1)	4 bytes at a time		8		µs

(1) This number is dependent on Flash aging and increases over time and erase cycles.

5.10.5 ADC Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, DC-DC disabled. Input voltage scaling enabled, unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V_{DDS}	V
	Resolution			12		Bits
	Sample rate				200	ksamples/s
	Offset	Internal 4.3-V equivalent reference(2)		2.1		LSB
	Gain error	Internal 4.3-V equivalent reference(2)		–0.14		LSB
DNL(3)	Differential nonlinearity			>–1		LSB
INL(4)	Integral nonlinearity			±2		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		10.0		Bits
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		10.2		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		–65		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		–72		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 kspksamples/ss, 300-Hz input tone		–75		
SINAD and SNDR	Signal-to-noise and distortion ratio	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		62		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		63		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		69		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		74		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		75		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		75		
	Conversion time	Including sampling time		5		µs
	Current consumption	Internal 4.3-V equivalent reference(2)		0.66		mA
	Current consumption	VDDS as reference		0.75		mA
	Reference voltage	Internal 4.3-V equivalent reference, voltage scaling enabled (2)		4.3		V
	Reference voltage	Internal 4.3-V equivalent reference, voltage scaling disabled (2)		1.44		V
	Reference voltage	VDDS as reference, voltage scaling disabled		VDDS / 2.82		V
	Reference voltage	VDDS as reference , voltage scaling enabled		VDDS		V
	Input Impedance	Capacitive input, Input impedance is depending on sampling time and can be increased by increasing sampling time		>1		MΩ

(1) Using IEEE Std 1241™ 2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V. Applied voltage must be within Absolute Maximum Ratings (Section 5.1) at all times.
(3) No missing codes. Positive DNL typically varies from 0.3 to 1.7, depending on the device (see Figure 5-7).
(4) For a typical example, see Figure 5-6.

5.10.6 Temperature Sensor

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		–40		85	°C
Accuracy			±5		°C
Supply voltage coefficient(1)			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

5.10.7 Battery Monitor

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V
Accuracy			13		mV

5.10.8 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
External reference voltage		0		V_{DDS}	V
Internal reference voltage	DCOUPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from –10 mV to 10 mV		0.72		µs
Current consumption when enabled(1)			8.6		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.10.9 Low-Power Clocked Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32.8		kHz
Internal reference voltage, VDDS / 2			1.49 – 1.51		V
Internal reference voltage, VDDS / 3			1.01 – 1.03		V
Internal reference voltage, VDDS / 4			0.78 – 0.79		V
Internal reference voltage, DCOUPL / 1			1.25 – 1.28		V
Internal reference voltage, DCOUPL / 2			0.63 – 0.65		V
Internal reference voltage, DCOUPL / 3			0.42 – 0.44		V
Internal reference voltage, DCOUPL / 4			0.33 – 0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from –50 mV to 50 mV		1		clock-cycle
Current consumption when enabled			362		nA

5.10.10 Programmable Current Source

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25 to 20		µA
Resolution			0.25		µA
Current consumption(1)	Including current source at maximum programmable output		23		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.10.11 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8 V					
GPIO VOH at 8-mA load	IOCURR = 2, high drive GPIOs only	1.32	1.54		V
GPIO VOL at 8-mA load	IOCURR = 2, high drive GPIOs only		0.26	0.32	V
GPIO VOH at 4-mA load	IOCURR = 1	1.32	1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		71.7		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		21.1		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.33		V
T_A = 25°C, V_{DDS} = 3.0 V					
GPIO VOH at 8-mA load	IOCURR = 2, high drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR = 2, high drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR = 1		2.72		V
GPIO VOL at 4-mA load	IOCURR = 1		0.28		V
T_A = 25°C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		277		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		113		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.54		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.4		V
VIH	Lowest GPIO input voltage reliably interpreted as a *High*			0.8	VDDS(1)
VIL	Highest GPIO input voltage reliably interpreted as a *Low*	0.2			VDDS(1)

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in Section 8.2 for more details.

5.10.12 Synchronous Serial Interface (SSI) Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	system clocks
S2(1)	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3(1)	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams Figure 5-1, Figure 5-2, and Figure 5-3.

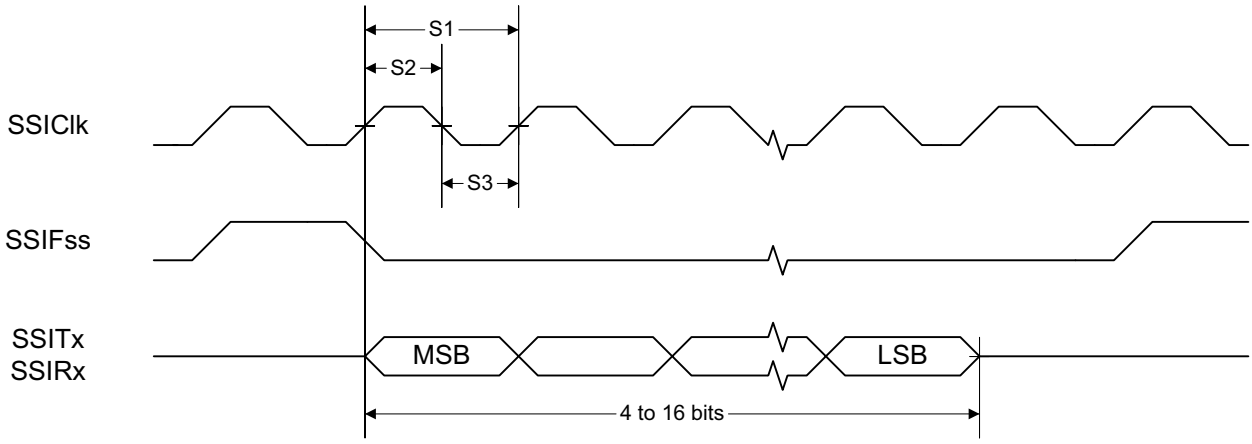


Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

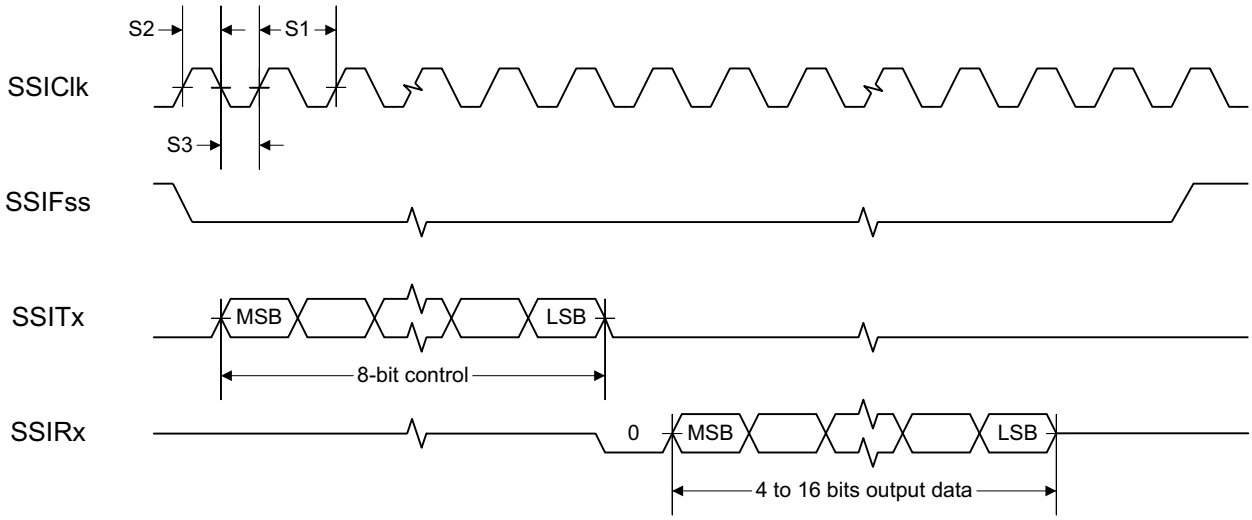


Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

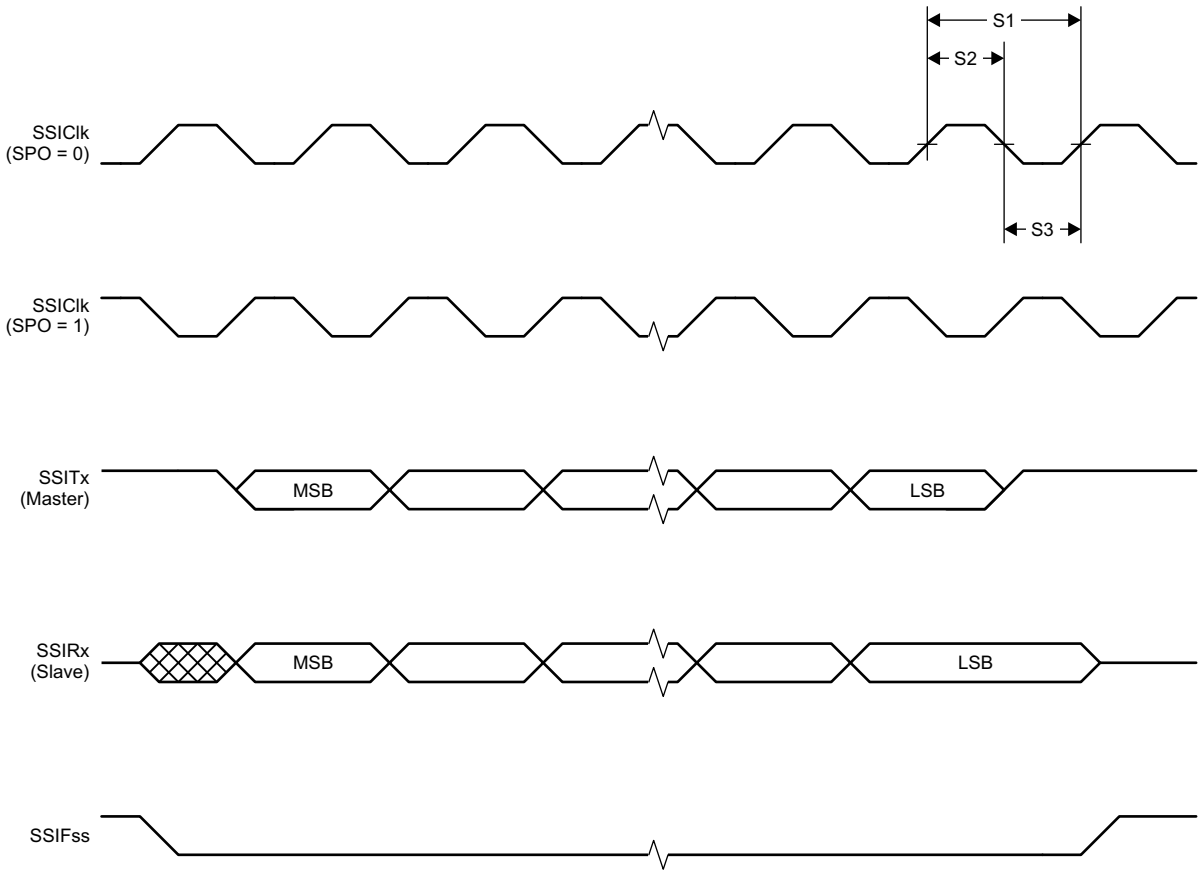


Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.11 Typical Characteristics

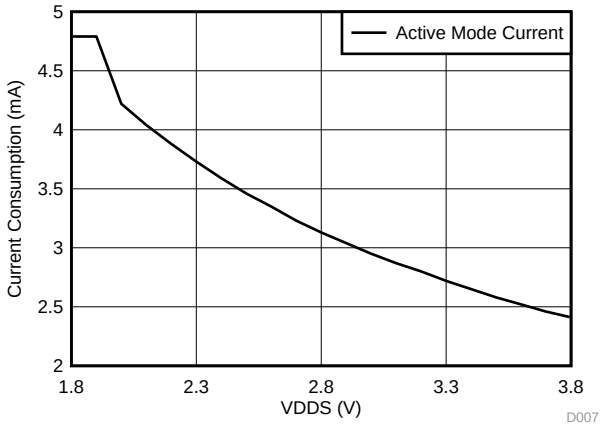


Figure 5-4. Active Mode (MCU) Current Consumption vs Supply Voltage (VDDS)

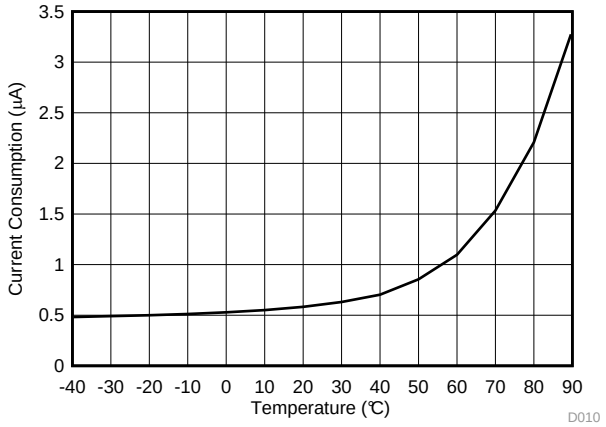


Figure 5-5. Standby MCU Current Consumption, 32-kHz Clock, RAM and MCU Retention

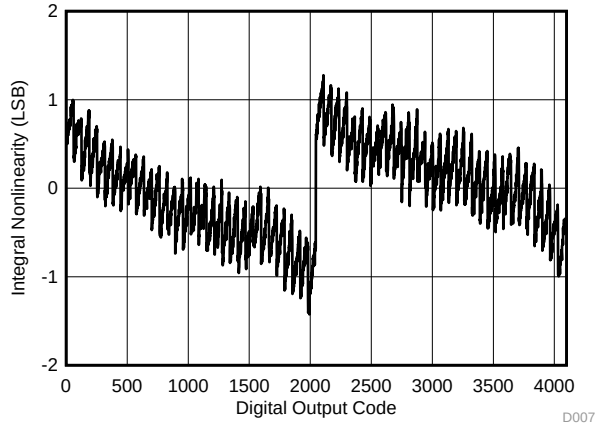


Figure 5-6. SoC ADC, Integral Nonlinearity vs Digital Output Code

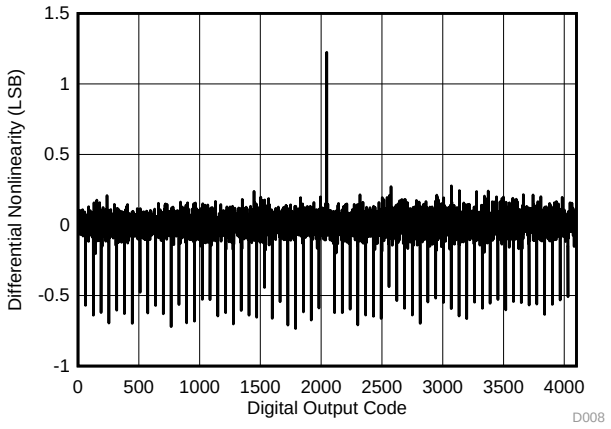


Figure 5-7. SoC ADC, Differential Nonlinearity vs Digital Output Code

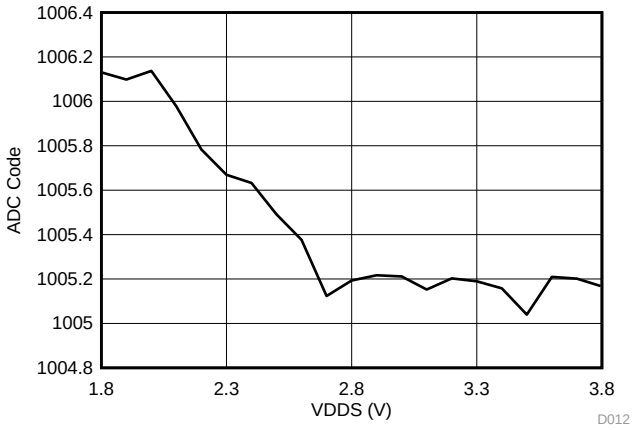


Figure 5-8. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

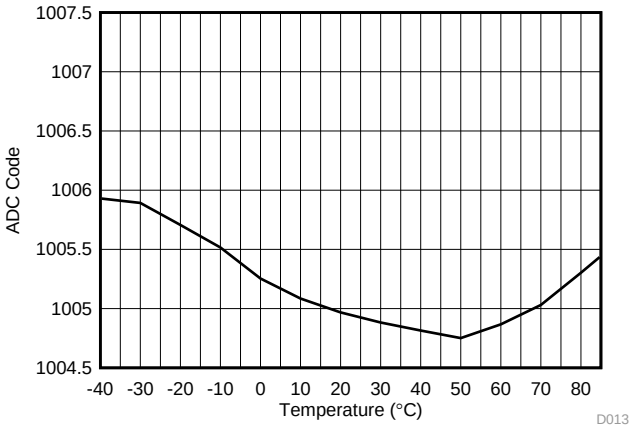


Figure 5-9. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)

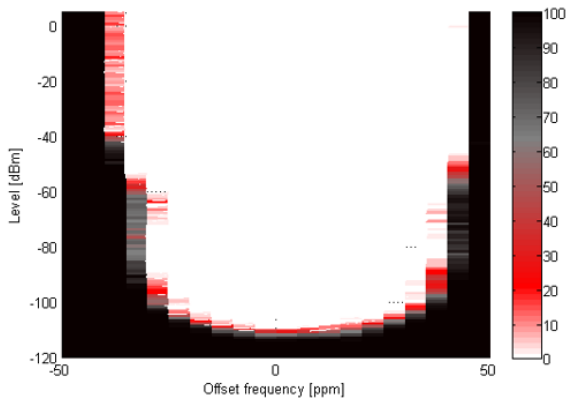


Figure 5-10. RX, (50-kbps) Packet Error Rate (PER) vs Input RF Level vs Frequency Offset, 868 MHz

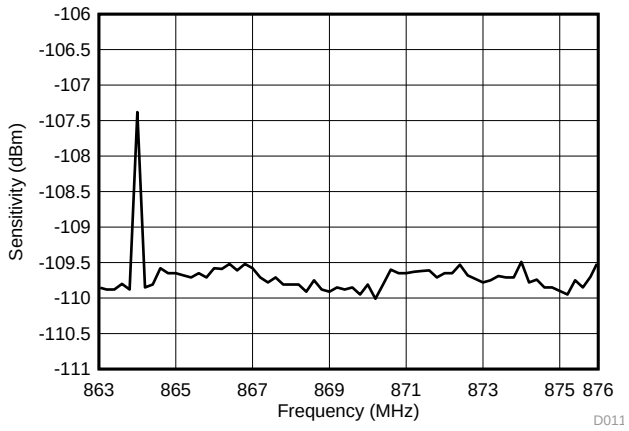


Figure 5-11. RX (50-kbps) Sensitivity vs Frequency

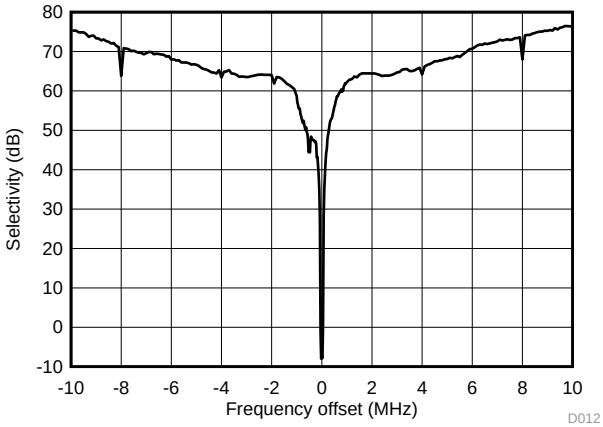


Figure 5-12. RX (50-kbps) Selectivity 868 MHz

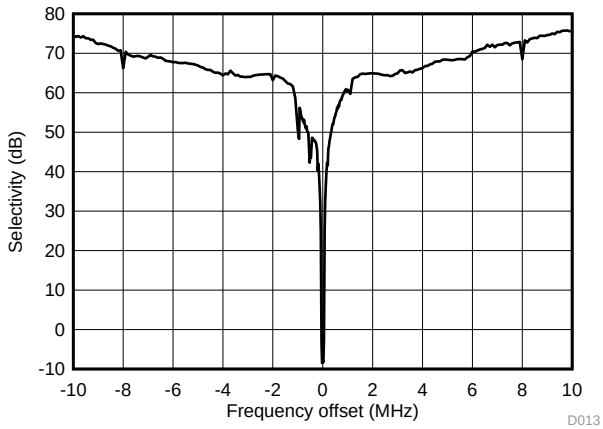


Figure 5-13. RX (50-kbps) Selectivity 915 MHz

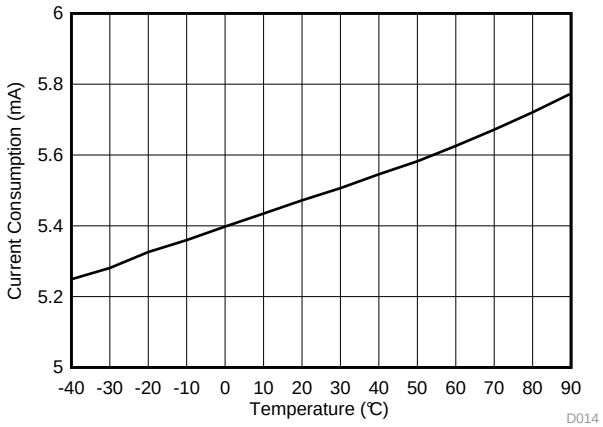


Figure 5-14. RX (50-kbps) Current Consumption vs Temperature 868 MHz

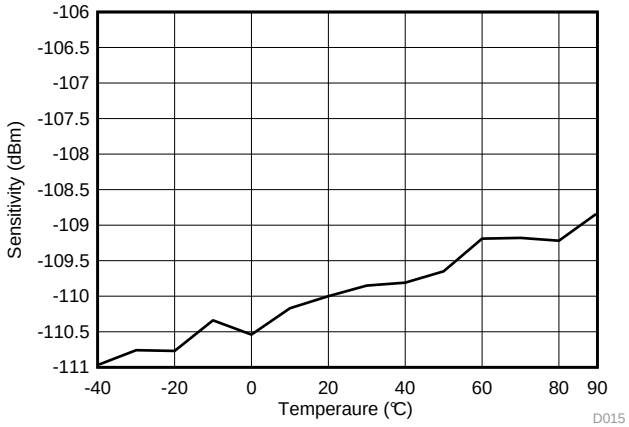


Figure 5-15. RX (50-kbps) Sensitivity vs Temperature 868 MHz

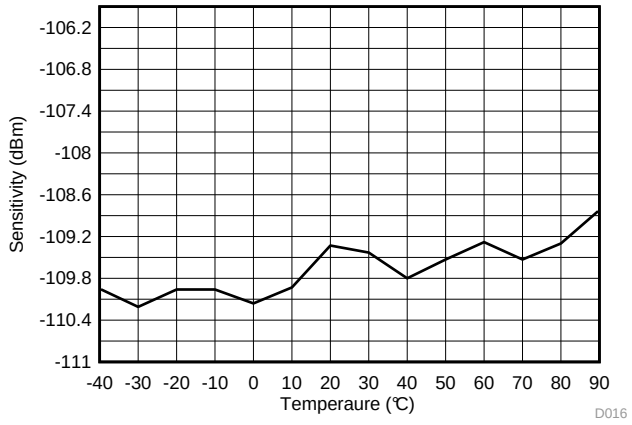


Figure 5-16. RX (50-kbps) Sensitivity vs Temperature 915 MHz

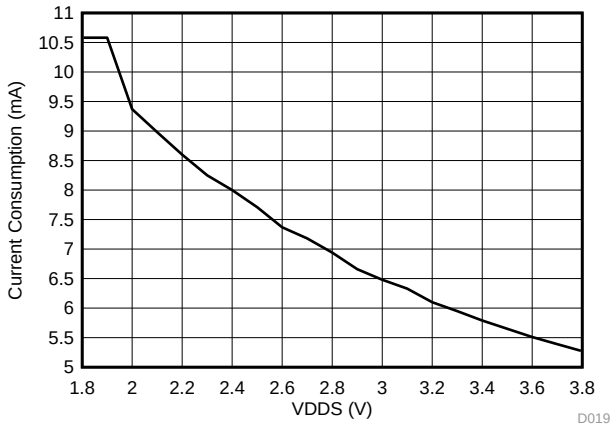


Figure 5-17. RX (50-kbps) Current Consumption vs Supply Voltage 915 MHz

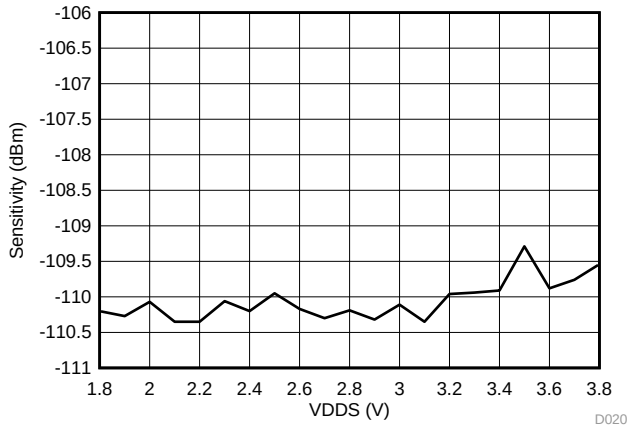
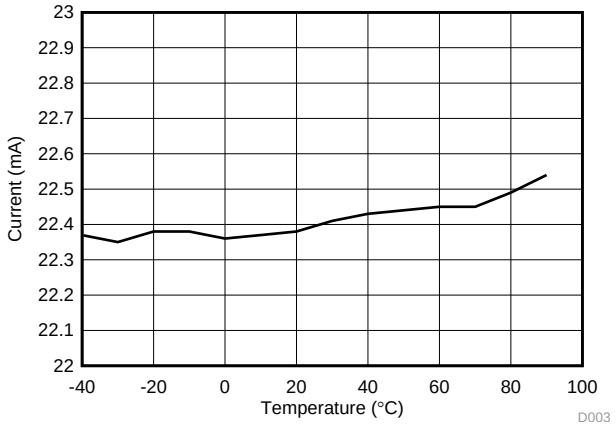


Figure 5-18. RX (50-kbps) Sensitivity vs Supply Voltage 868 MHz



DCDC On, 3.6 V

Figure 5-19. TX Current Consumption With Maximum Output Power vs Temperature 868 MHz

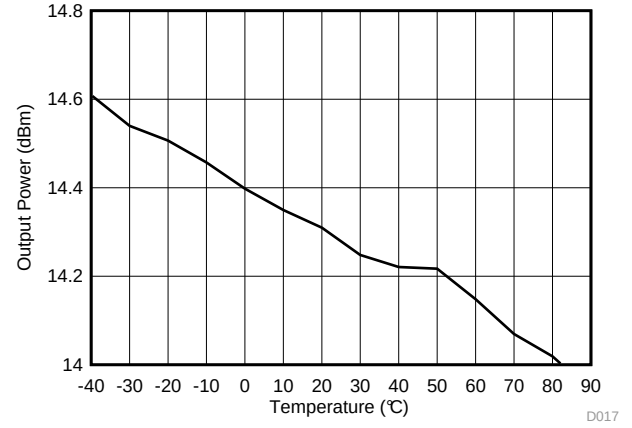


Figure 5-20. TX Maximum Output vs Temperature 868 MHz

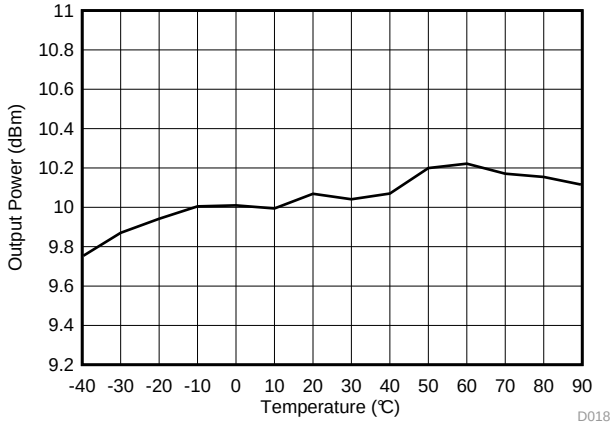


Figure 5-21. TX 10-dBm Output Power vs Temperature 868 MHz

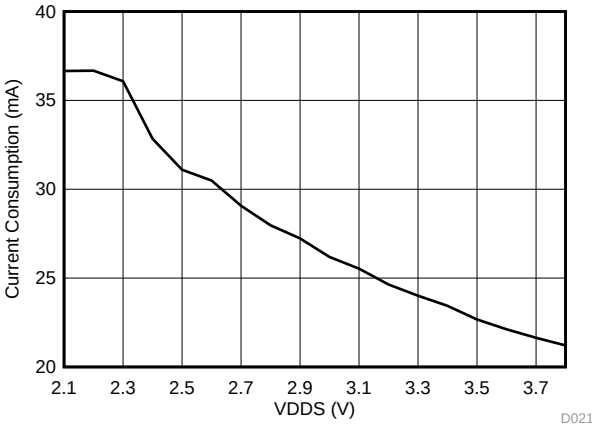


Figure 5-22. TX Current Consumption Maximum Output Power vs Supply Voltage 868 MHz

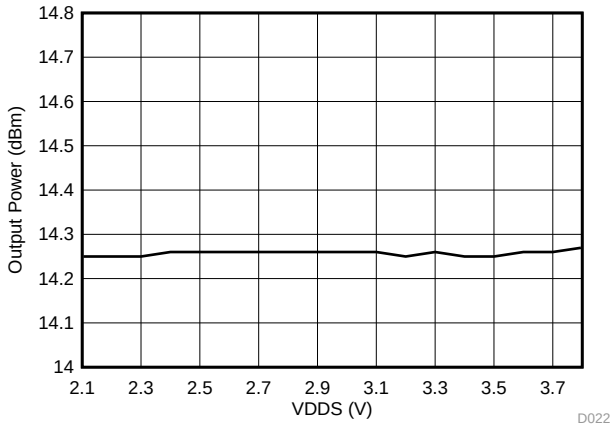


Figure 5-23. TX Maximum Output Power vs Supply Voltage 915 MHz

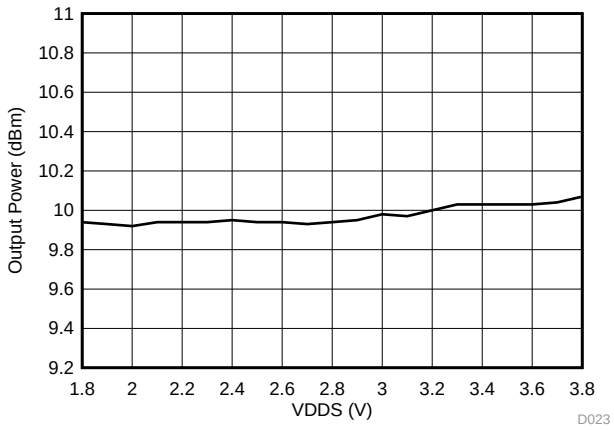


Figure 5-24. TX 10-dBm Output Power vs Supply Voltage 868 MHz

6 Detailed Description

6.1 Overview

Section 1.4 shows a block diagram of the core modules of the CC13xx product family.

6.2 Main CPU

The SimpleLink CC1310 Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

CM3 features include the following:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultralow power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.3 RF Core

The RF core is a highly flexible and capable radio system that interfaces the analog RF and base-band circuits, handles data to and from the system side, and assembles the information bits in a given packet structure.

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU and leaving more resources for the user application. The RF core offers a high-level, command-based API to the main CPU.

The RF core supports a wide range of modulation formats, frequency bands, and accelerator features, which include the following (not all of the features have been characterized yet, see *CC1310 SimpleLink Wireless MCU Silicon Errata*, SWRZ062, for more information):

- Wide range of data rates:
  - From 625 bps (offering long range and high robustness) to as high as 4 Mbps
- Wide range of modulation formats:
  - Multilevel (G)FSK and MSK
  - On-Off Keying (OOK) with optimized shaping to minimize adjacent channel leakage
  - Coding-gain support for long range
- Dedicated packet handling accelerators:
  - Forward error correction
  - Data whitening
  - 802.15.4g mode-switch support
  - Automatic CRC
- Automatic listen-before-talk (LBT) and clear channel assist (CCA)
- Digital RSSI
- Highly configurable channel filtering, supporting channel spacing schemes from 40 kHz to 4 MHz
- High degree of flexibility, offering a future-proof solution

The RF core interfaces a highly flexible radio, with a high-performance synthesizer that can support a wide range of frequency bands.

6.4 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the main CM3 CPU.

A PC-based development tool called Sensor Controller Studio is used to write, test and debug code for Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller Typical use cases may be (but are not limited to) the following:

- Analog sensors using integrated ADC
- Digital sensors using GPIOs with bit-banged I^2C or SPI
- Capacitive sensing
- Waveform generation
- Pulse counting
- Key scan
- Quadrature decoder for polling rotation sensors

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions.
- The ADC is a 12-bit, 200 ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The analog modules can be connected to up to eight different GPIOs

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1. GPIOs Connected to the Sensor Controller(1)

ANALOG CAPABLE	7 × 7 RGZ DIO NUMBER	5 × 5 RHB DIO NUMBER	4 × 4 RSM DIO NUMBER
Y	30	14	
Y	29	13	
Y	28	12	
Y	27	11	9
Y	26	9	8
Y	25	10	7
Y	24	8	6
Y	23	7	5
N	7	4	2
N	6	3	1
N	5	2	0
N	4	1	
N	3	0	
N	2		
N	1		
N	0		

(1) Depending on the package size, up to 15 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules.

6.5 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) is split into two 4-KB blocks and two 6-KB blocks and can be used for both storage of data and execution of code. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed, embedded TI RTOS kernel and Driverlib. It also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.7 Power Management

To minimize power consumption, the CC1310 supports a number of power modes and power management features (see Table 6-2).

Table 6-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.2 mA + 25.5 µA/MHz	570 µA	0.6 µA	185 nA	0.1 µA
Wake-up Time to CPU Active(1)	–	14 µs	174 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on Pin Edge	Available	Available	Available	Available	Off
Wake-up on Reset Pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled(2)	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead
(2) The Brown Out Detector is disabled between recharge periods in STANDBY. Lowering the supply voltage below the BOD threshold between two recharge periods while in STANDBY may cause the BOD to lock the device upon wake-up until a Reset/POR releases it. To avoid this, it is recommended that STANDBY mode is avoided if there is a risk that the supply voltage (VDDS) may drop below the specified operating voltage range. For the same reason, it is also good practice to ensure that a power cycling operation, such as a battery replacement, triggers a Power-on-reset by ensuring that the VDDS decoupling network is fully depleted before applying supply voltage again (for example, inserting new batteries).

In active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 6-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In standby mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU. This means that the main CPU does not have to wake up, for example to execute an ADC sample or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the Sensor Controller and to choose which peripherals are controlled and which conditions wake up the main CPU.

6.8 Clock Systems

The CC1310 supports two external and two internal clock sources.

A 24-MHz external crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32.768-kHz crystal is optional. The low-speed crystal oscillator is designed for use with a 32.768-kHz watch-type crystal.

The internal high-speed RC oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed RC oscillator (32-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in *Section 4*.

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments' synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver and transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps.

Timer 0 is a general-purpose timer module (GPTM) that provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers, or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I^2S interface is used to handle digital audio see the *CC13xx, CC26xx SimpleLink™ Wireless MCU* Technical Reference Manual (SWCU117) for more information.

The I^2C interface is used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both I^2C master and I^2C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the CM3 CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except for in shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and provide a battery status indication as well as a coarse temperature measure.

6.10 System Architecture

Depending on the product configuration, CC1310 can function as a wireless network processor (WNP – an IC running the wireless protocol stack, with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the ARM CM3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Few external components are required for the operation of the CC1310 device. Figure 7-1 shows a typical application circuit.

The board layout greatly influences the RF performance of the CC1310 device.

On the Texas Instruments CC1310EM-7XD-7793, the optimal differential impedance seen from the RF pins into the balun and filter and antenna is 44 +j15.

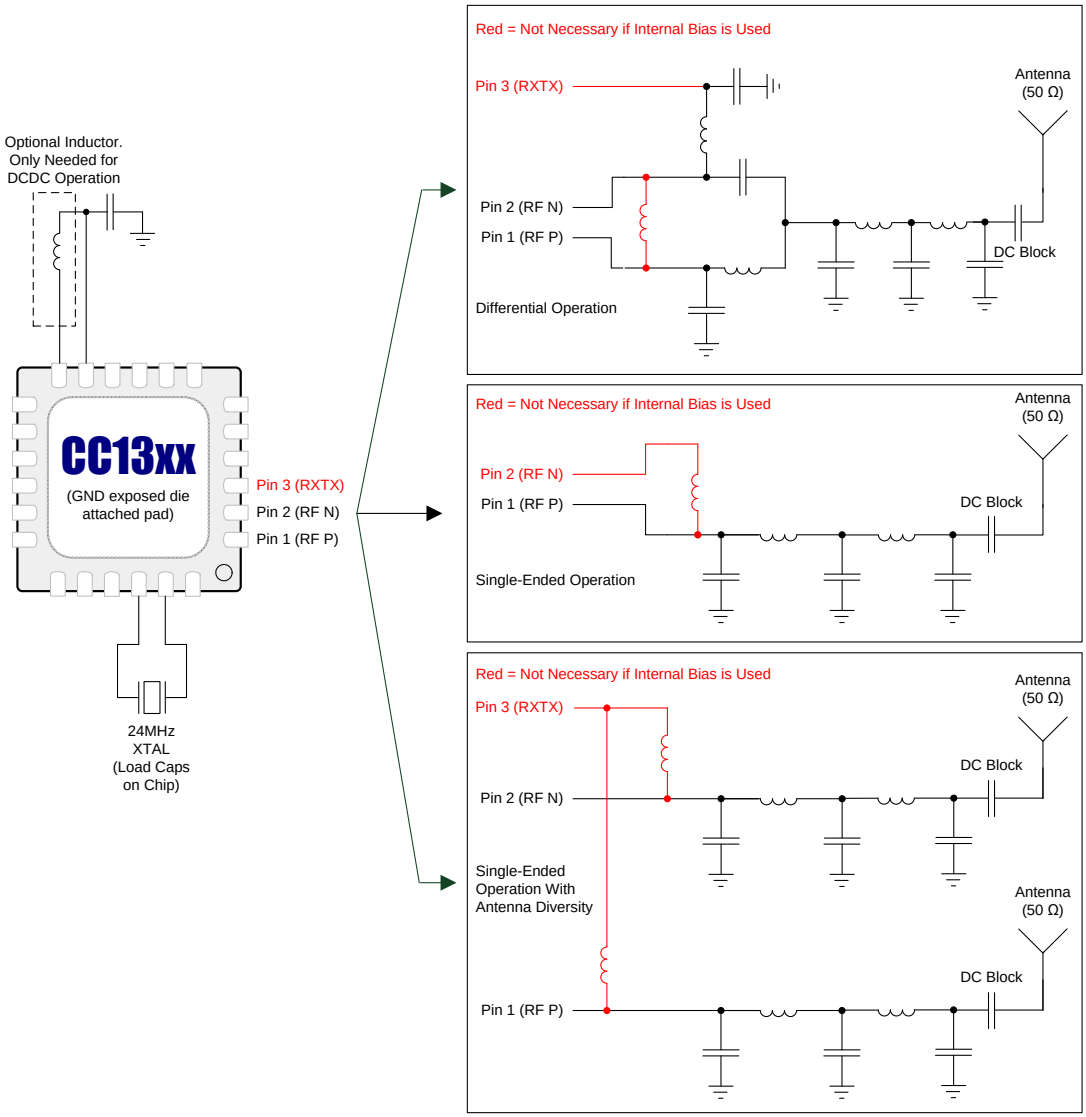


Figure 7-1 does not show decoupling capacitors for power pins. For a complete reference design, see the product folder on www.ti.com.

Figure 7-1. Differential Reference Design

7.1 TI Design

Humidity and Temp Sensor Node for Sub-1GHz Star Networks Enabling 10+ Year Coin Cell Battery Life

This TI Design uses Texas Instruments' nano-power system timer, boost converter, SimpleLink ultralow power Sub-1-GHz wireless microcontroller (MCU) platform, and humidity sensing technologies to demonstrate an ultralow power method to duty-cycle sensor end nodes leading to extremely long battery life. The TI Design includes techniques for system design, detailed test results, and information to get the design up and running quickly.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of the CC1310 device applications:

Software Tools:

SmartRF Studio 7:

SmartRF Studio is a PC application that helps designers of radio systems to easily evaluate the RF-IC at an early stage in the design process.

- Test functions for sending and receiving radio packets, continuous wave transmit and receive
- Evaluate RF performance on custom boards by wiring it to a supported evaluation board or debugger
- Can also be used without any hardware, but then only to generate, edit and export radio configuration settings
- Can be used in combination with several development kits for Texas Instruments' CCxxxx RF-ICs

Sensor Controller Studio:

Sensor Controller Studio provides a development environment for the CC13xx Sensor Controller. The Sensor Controller is a proprietary, power-optimized CPU in the CC13xx, which can perform simple background tasks autonomously and independent of the System CPU state.

- Allows for Sensor Controller task algorithms to be implemented using a C-like programming language
- Outputs a Sensor Controller Interface driver, which incorporates the generated Sensor Controller machine code and associated definitions
- Allows for rapid development by using the integrated Sensor Controller task testing and debugging functionality. This allows for live visualization of sensor data and algorithm verification.

IDEs and Compilers:

Code Composer Studio:

- Integrated development environment with project management tools and editor
- Code Composer Studio (CCS) 6.1 and later has built-in support for the CC13xx device family
- Best support for XDS debuggers; XDS100v3, XDS110 and XDS200
- High integration with TI-RTOS with support for TI-RTOS Object View

IAR Embedded Workbench for ARM

- Integrated development environment with project management tools and editor
- IAR EWARM 7.30.3 and later has built-in support for the CC13xx device family
- Broad debugger support, supporting XDS100v3, XDS200, IAR I-Jet and Segger J-Link
- Integrated development environment with project management tools and editor
- RTOS plugin available for TI-RTOS

For a complete listing of development-support tools for the CC1310 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.2 Reference Designs

Humidity and Temp Sensor Node for Sub-1GHz Star Networks Enabling 10+ Year Coin Cell Battery Life (TIDA-00484)

8.1.3 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, CC1310 is in production; therefore, no prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC1310* devices in the *RGZ (7-mm × 7-mm)* package types, see the *Package Option Addendum* of this document, the TI website (www.ti.com), or contact your TI sales representative.

8.2 Documentation Support

The following documents describe the CC1310. Copies of these documents are available on the Internet at www.ti.com.

- *CC13xx, CC26xx SimpleLink™ Wireless MCU* Technical Reference Manual (SWCU117)
- *CC26xx/CC13xx Power Management Software Developer's Reference Guide* (SWRS486)
- *Using GCC/GDB With SimpleLink™ CC26xx/CC13xx* Application Report (SWRA446)

8.2.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.2.2 Texas Instruments Low-Power RF Website

Texas Instruments' Low-Power RF website has all the latest products, application and design notes, FAQ section, news and events updates. Go to www.ti.com/lprf.

8.2.3 Low-Power RF Online Community

- Forums, videos, and blogs
- RF design help
- E2E interaction

Join at: www.ti.com/lprf-forum.

8.2.4 Texas Instruments Low-Power RF Developer Network

Texas Instruments has launched an extensive network of low-power RF development partners to help customers speed up their application development. The network consists of recommended companies, RF consultants, and independent design houses that provide a series of hardware module products and design services, including:

- RF circuit, low-power RF, and ZigBee® design services
- Low-power RF and ZigBee module solutions and development tools
- RF certification services and RF circuit manufacturing

For help with modules, engineering services or development tools:

Search the Low-Power RF Developer Network to find a suitable partner. www.ti.com/lprfnetwork

8.2.5 Low-Power RF eNewsletter

The Low-Power RF eNewsletter is up-to-date on new products, news releases, developers' news, and other news and events associated with low-power RF products from TI. The Low-Power RF eNewsletter articles include links to get more online information.

Sign up at: www.ti.com/lprfnewsletter

8.3 Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. The selection includes RF transceivers, RF transmitters, RF front ends, and Systems-on-Chips as well as various software solutions for the sub-1-GHz and 2.4-GHz frequency bands.

In addition, Texas Instruments provides a large selection of support collateral such as development tools, technical documentation, reference designs, application expertise, customer support, third-party and university programs.

Other than providing technical support forums, videos, and blogs, the Low-Power RF E2E Online Community also presents the opportunity to interact with engineers from all over the world.

With a broad selection of product solutions, end-application possibilities, and a range of technical support, Texas Instruments offers the broadest low-power RF portfolio.

8.4 Trademarks

IAR Embedded Workbench is a registered trademark of IAR Systems AB.
SimpleLink, SmartRF, Code Composer Studio, E2E are trademarks of Texas Instruments.
ARM7 is a trademark of ARM Limited (or its subsidiaries).
ARM, Cortex, ARM Thumb are registered trademarks of ARM Limited (or its subsidiaries).
ULPBench is a trademark of Embedded Microprocessor Benchmark Consortium.
CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.
IEEE Std 1241 is a trademark of Institute of Electrical and Electronics Engineers, Incorporated.
ZigBee is a registered trademark of Zigbee Alliance.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical Packaging and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1310F128RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F32RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F64RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1310F64RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

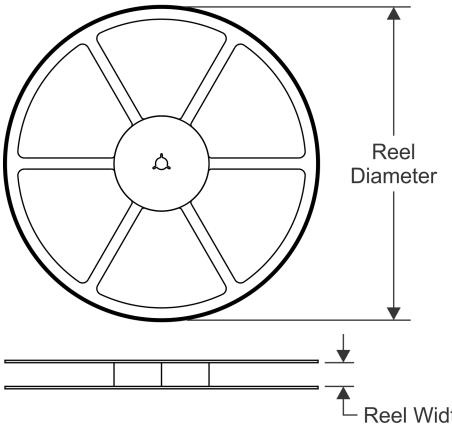
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

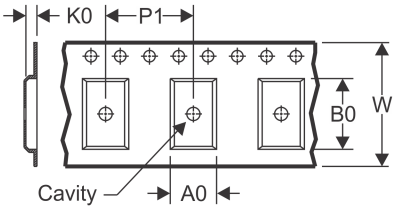
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

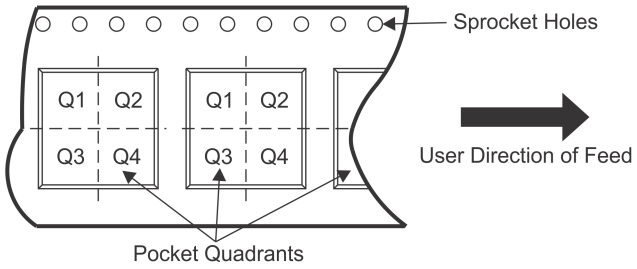


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

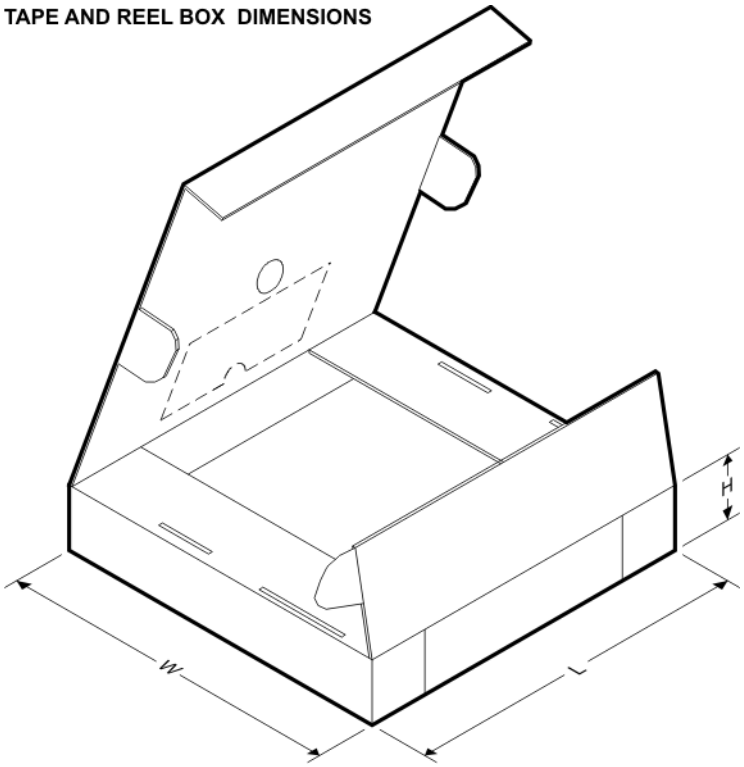
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1310F128RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F128RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F128RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F128RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F128RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F128RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F32RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F32RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F32RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F32RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F32RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F64RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F64RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F64RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F64RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F64RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F64RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

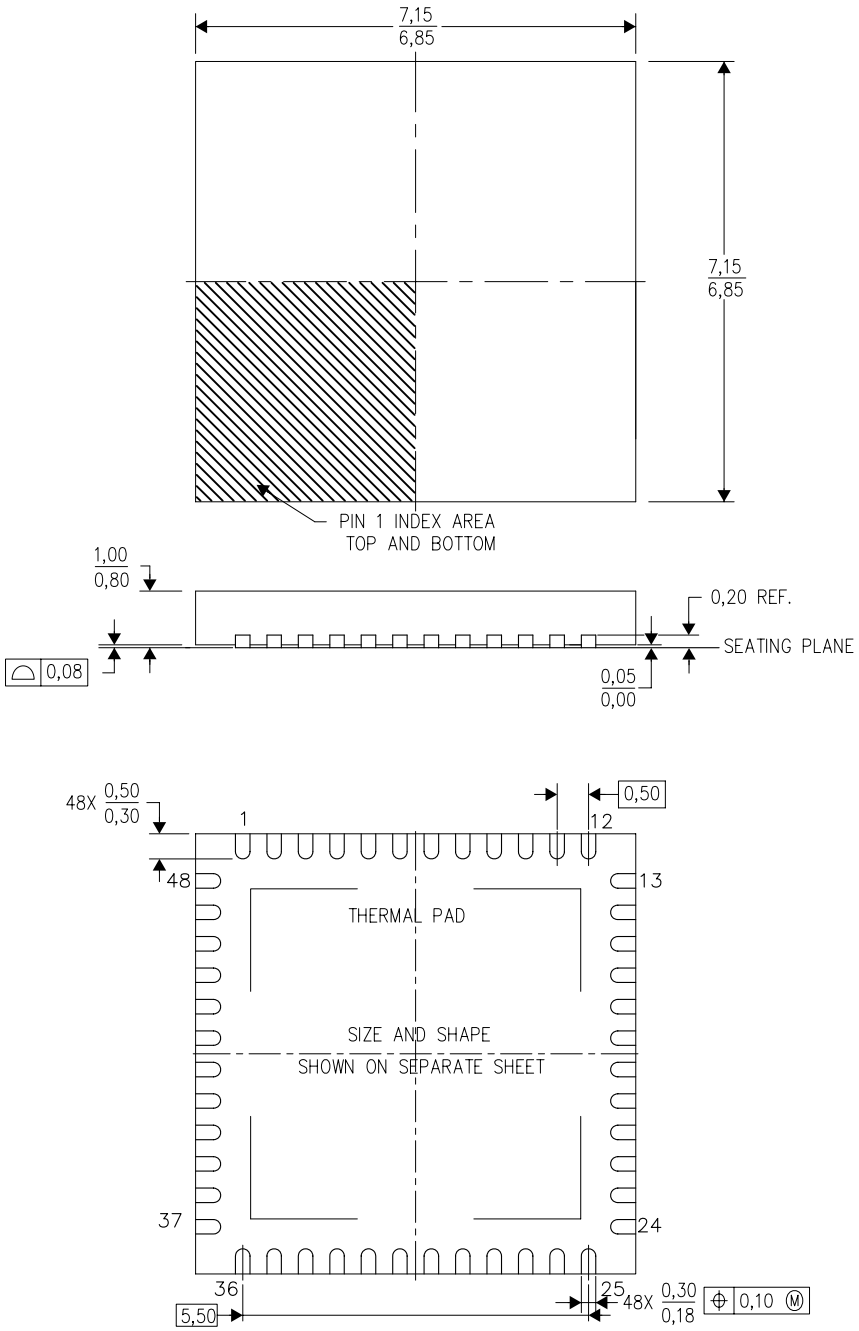
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1310F128RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC1310F128RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1310F128RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1310F128RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1310F128RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
CC1310F128RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
CC1310F32RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC1310F32RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1310F32RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1310F32RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1310F32RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
CC1310F64RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC1310F64RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1310F64RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1310F64RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1310F64RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
CC1310F64RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

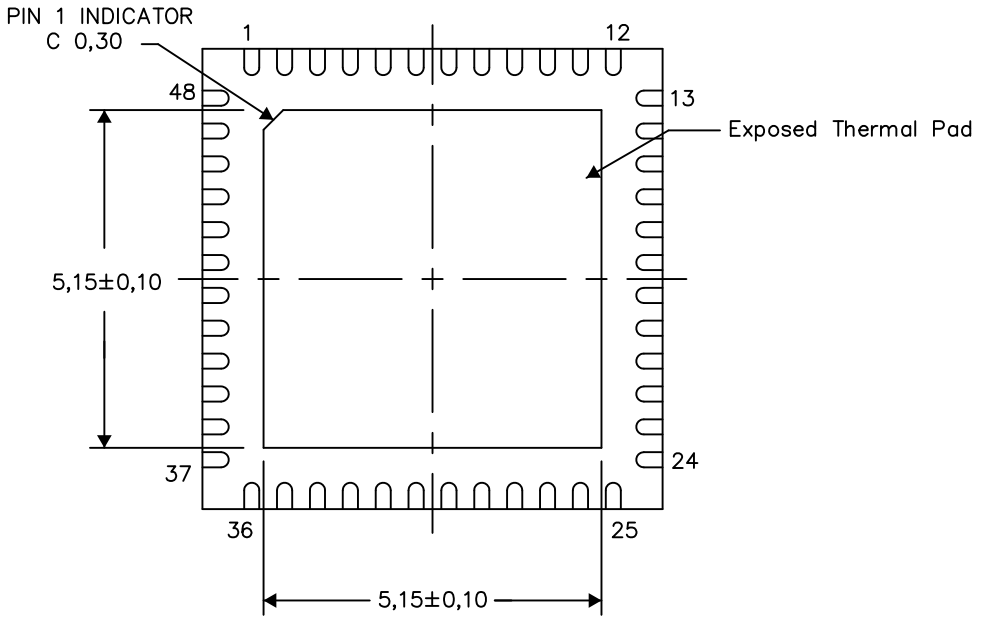
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



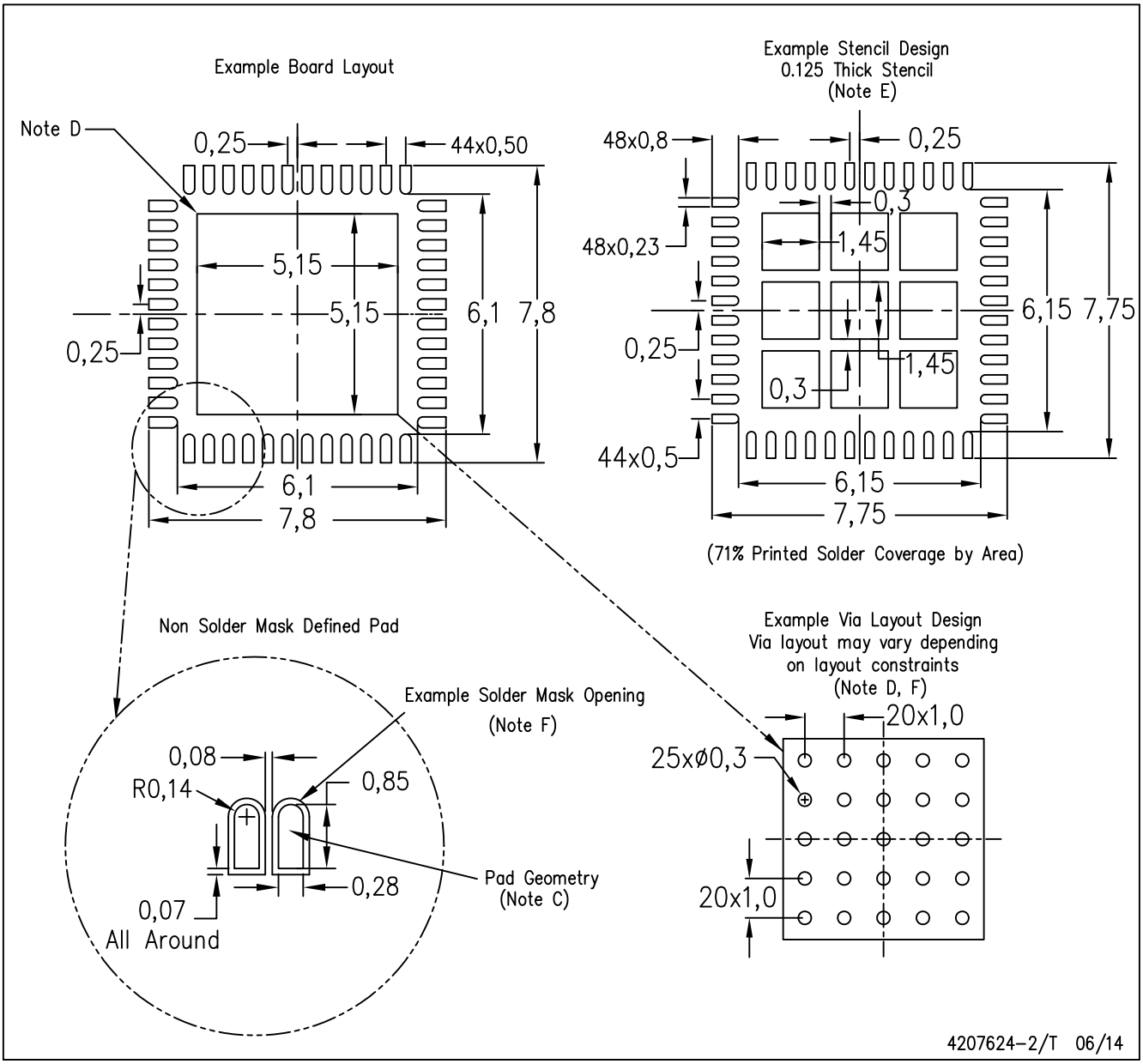
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/Z 03/15

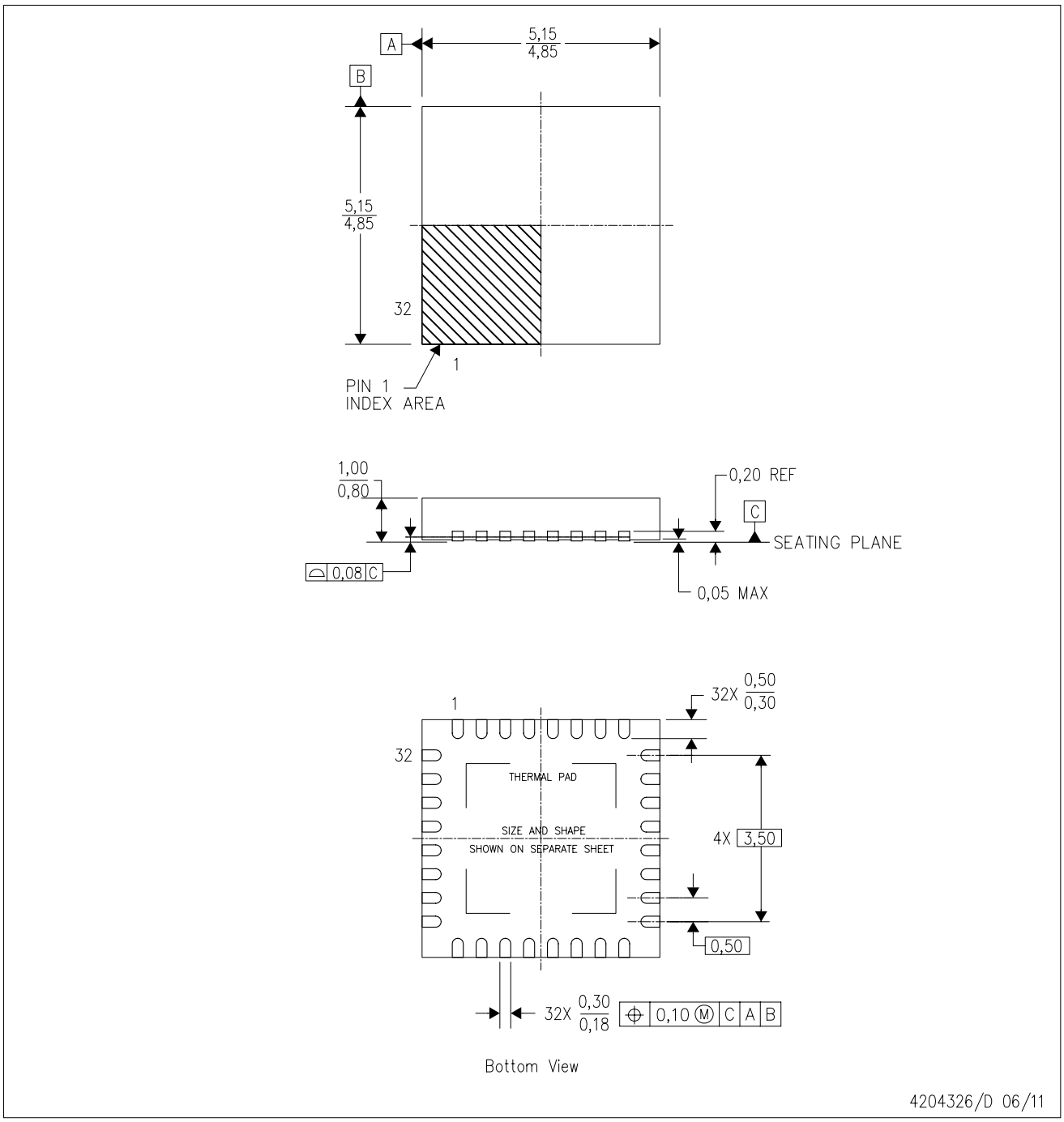
NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

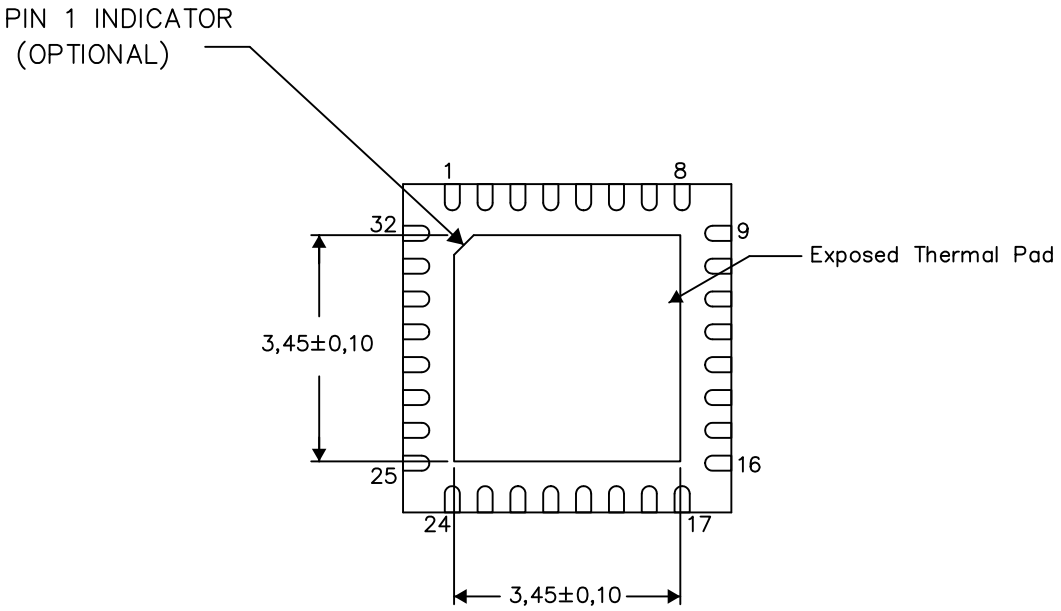
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



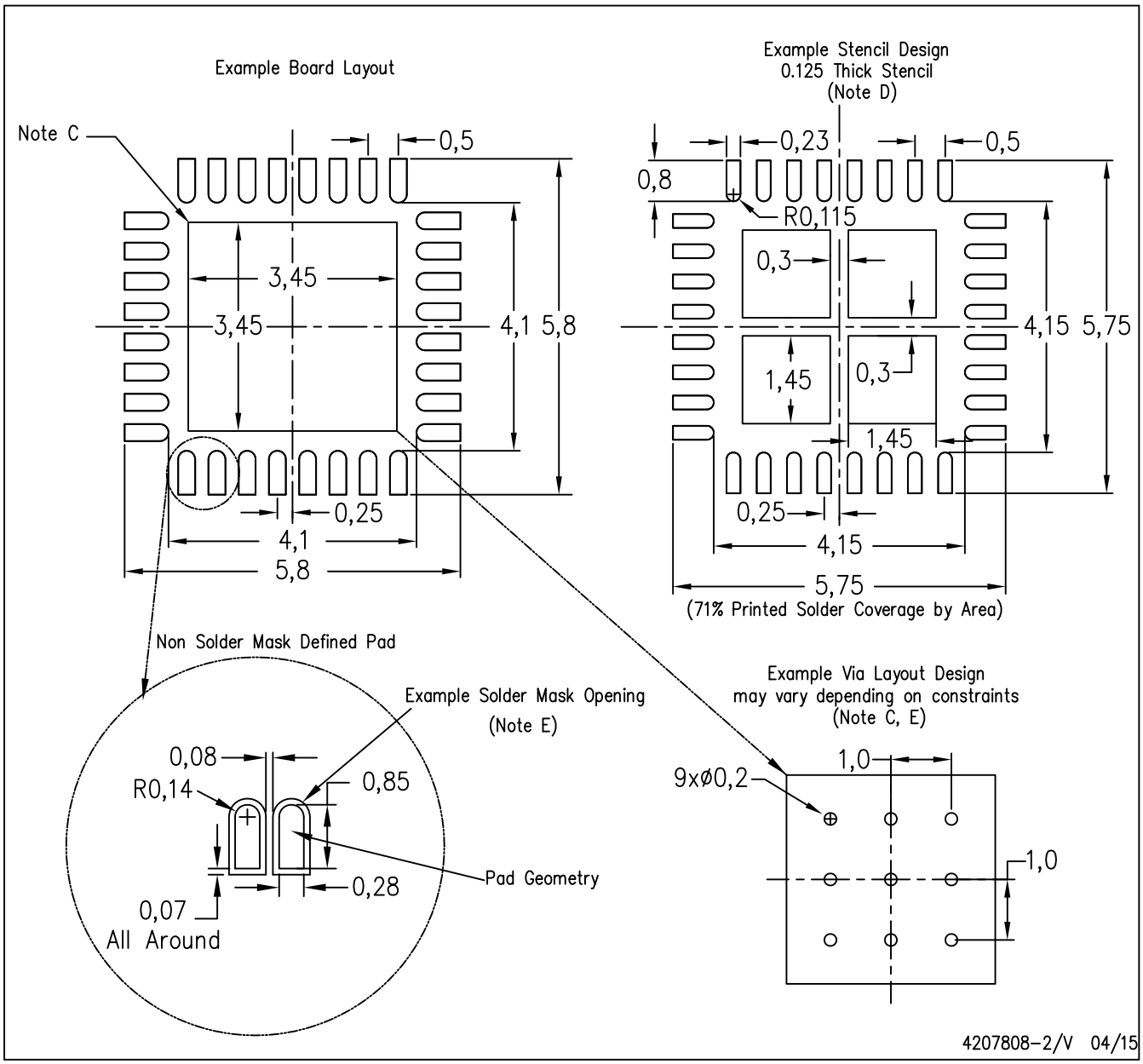
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

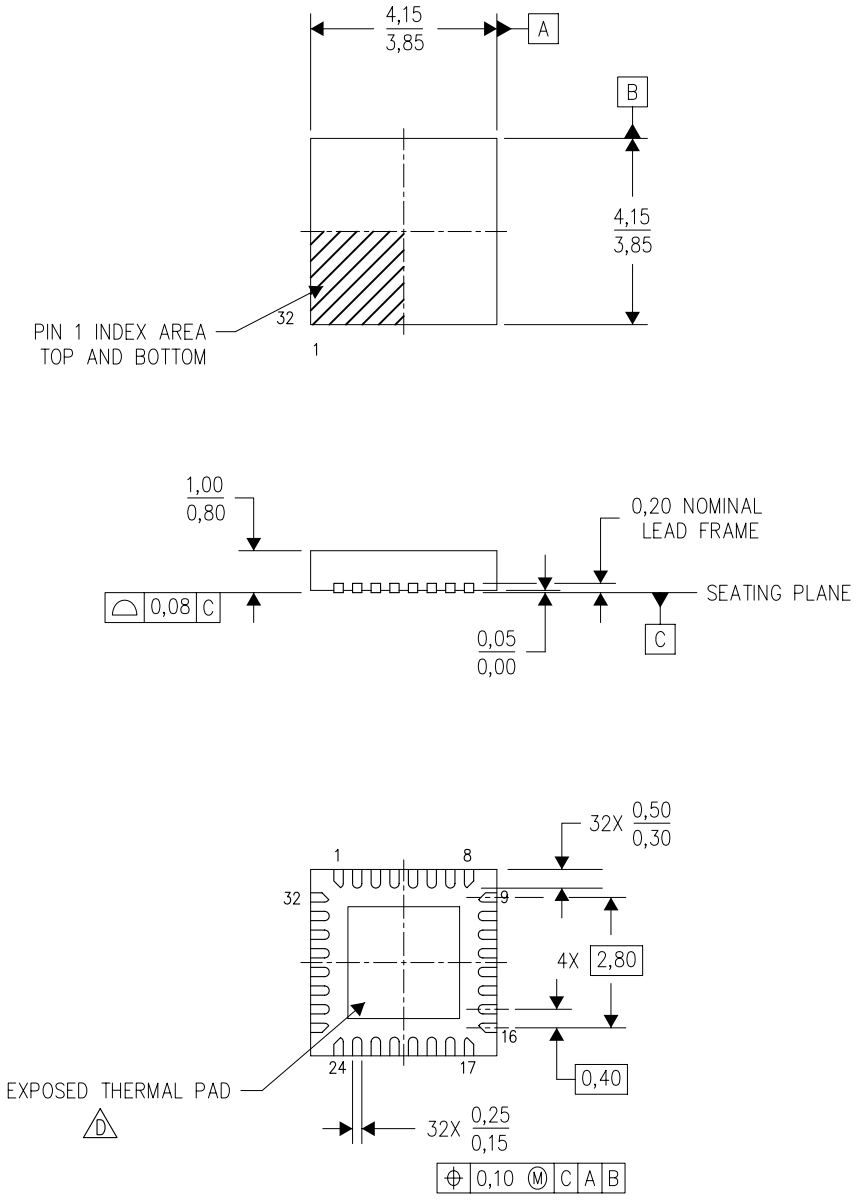
NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

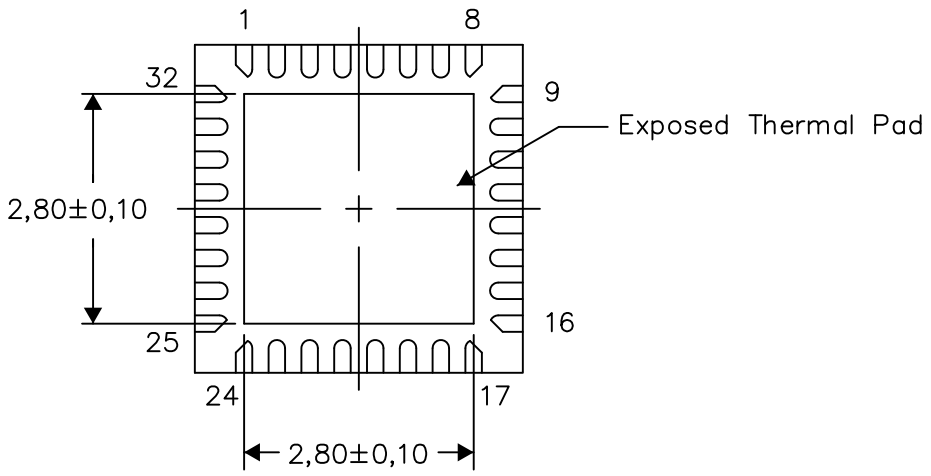
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



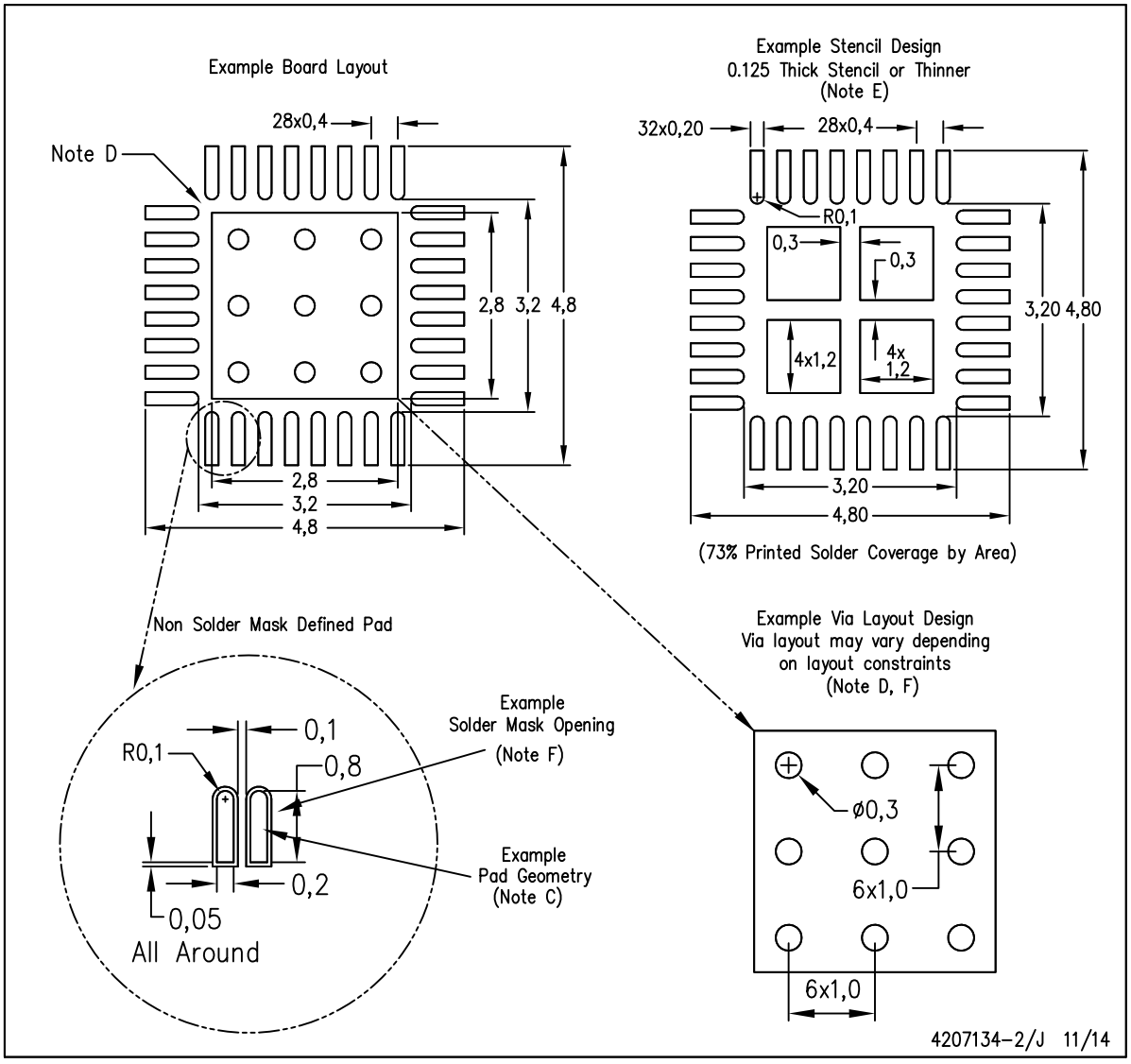
Bottom View

Exposed Thermal Pad Dimensions

4207868–2/I 07/14

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



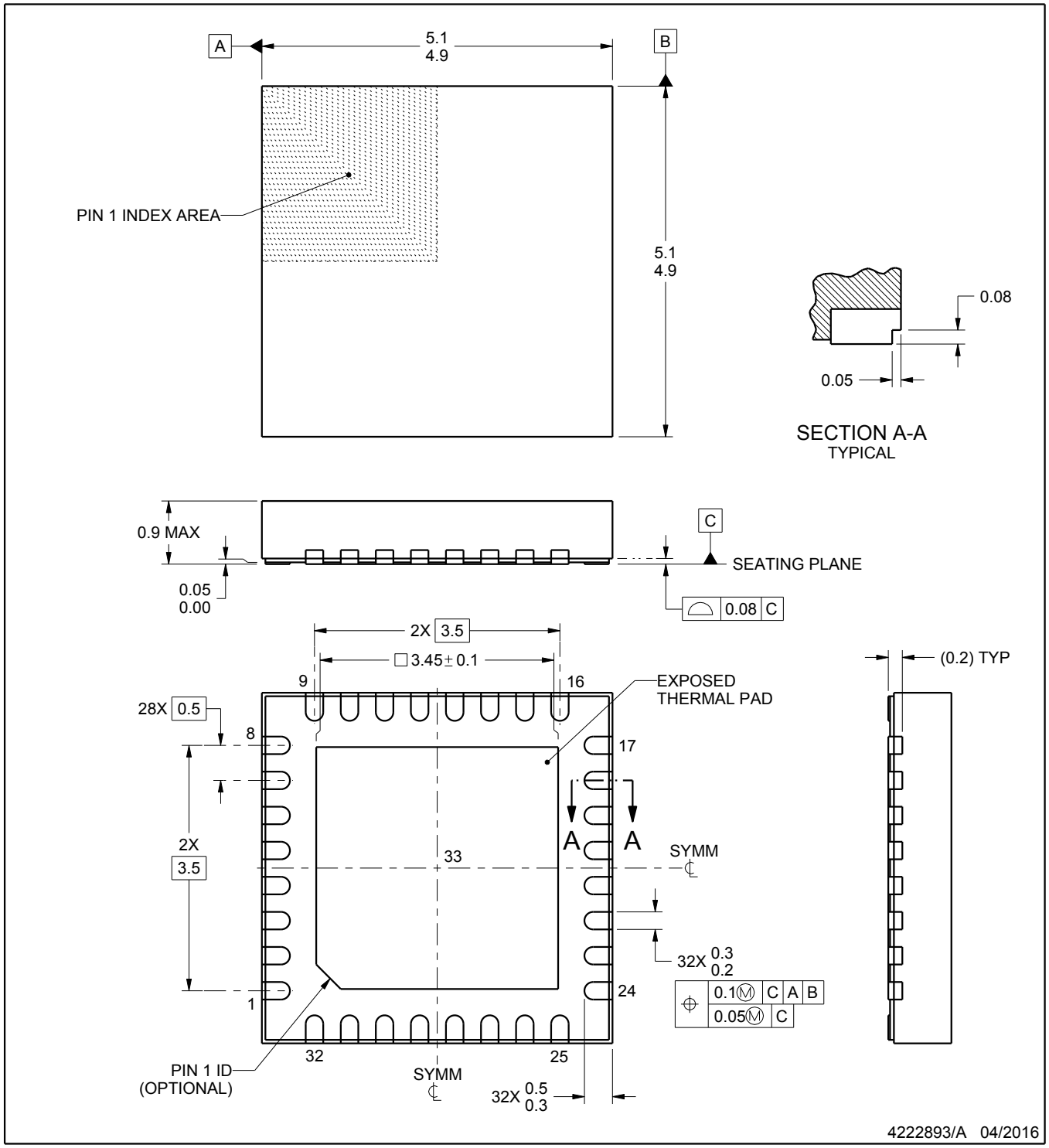
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGE OUTLINE

RHB0032N

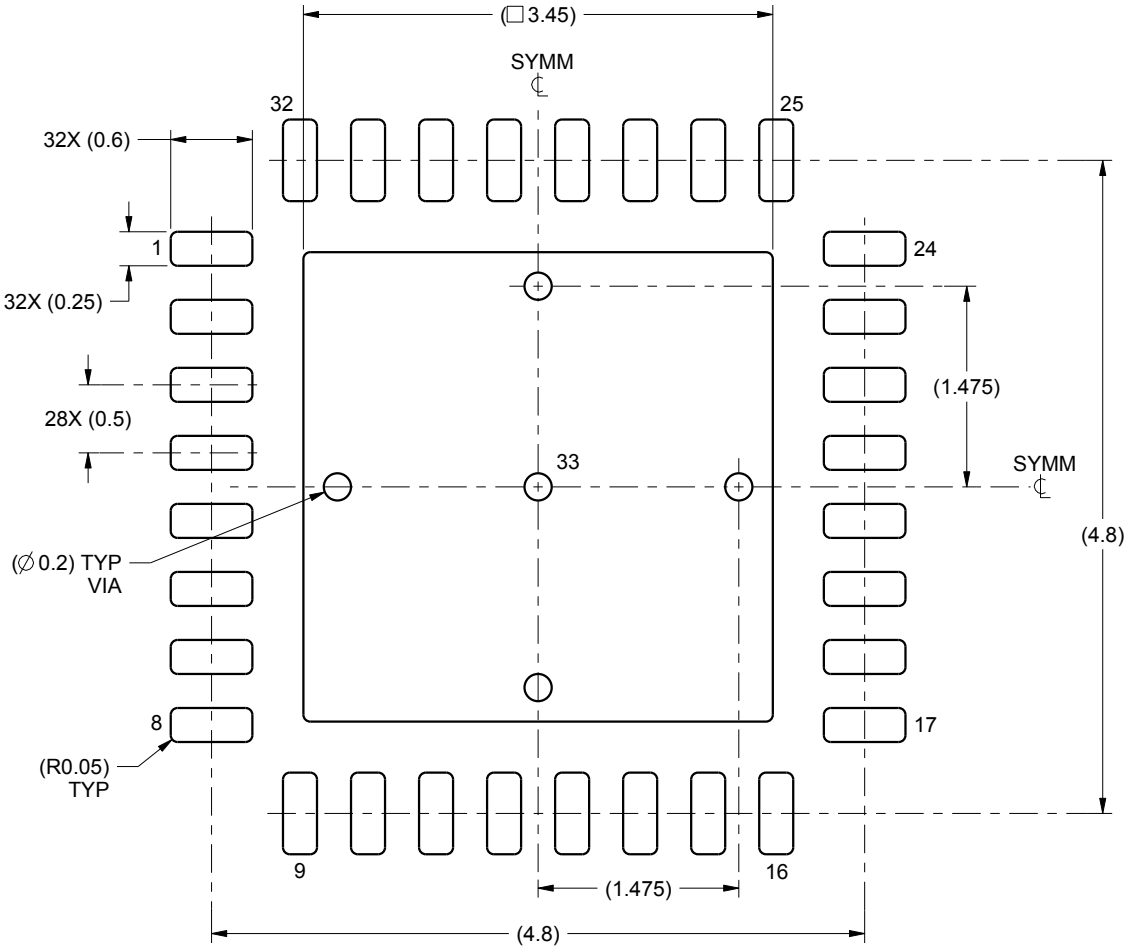
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

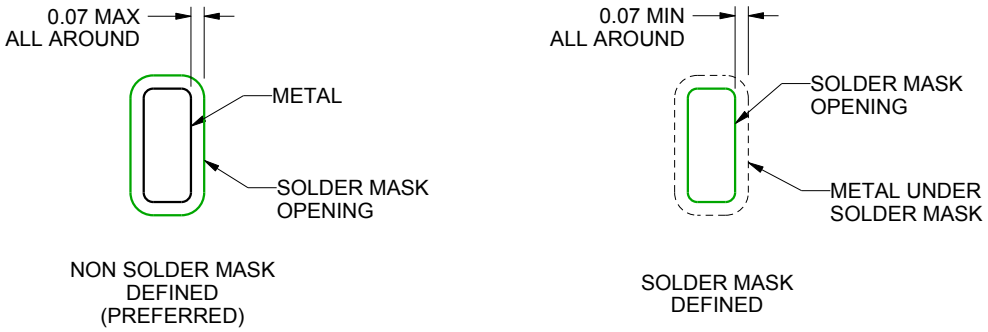


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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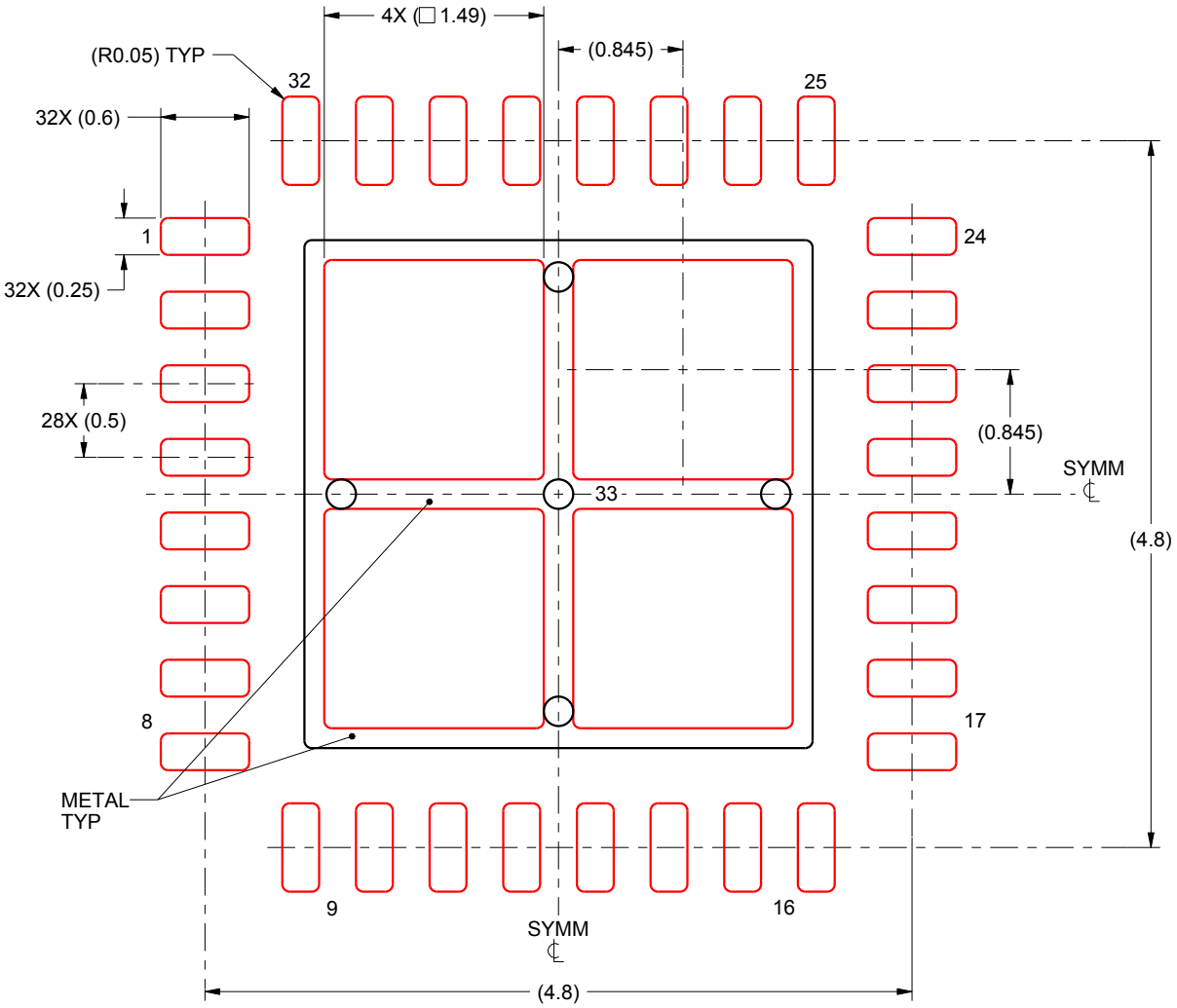
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

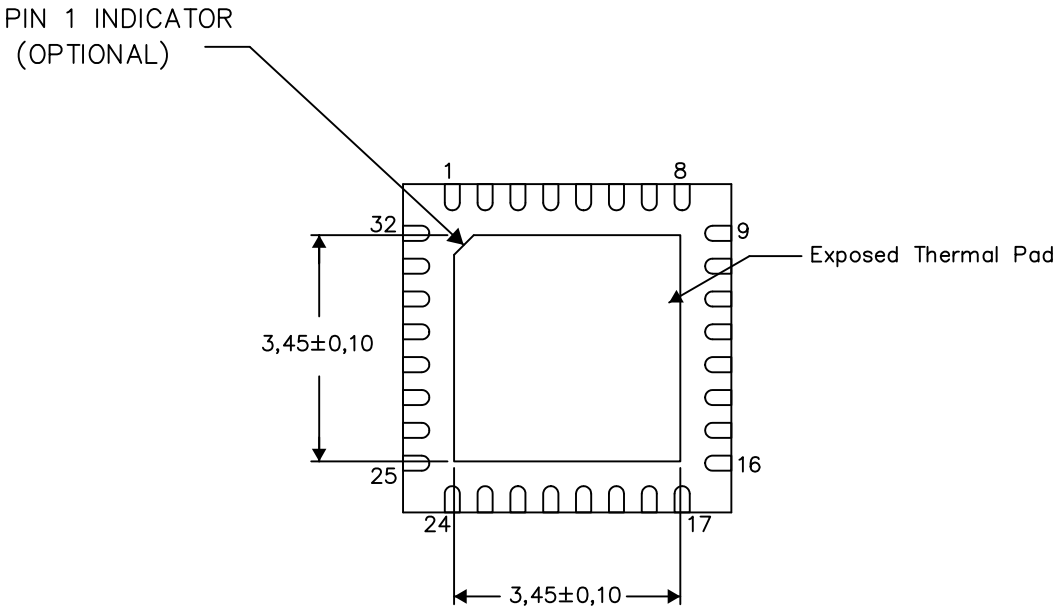
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



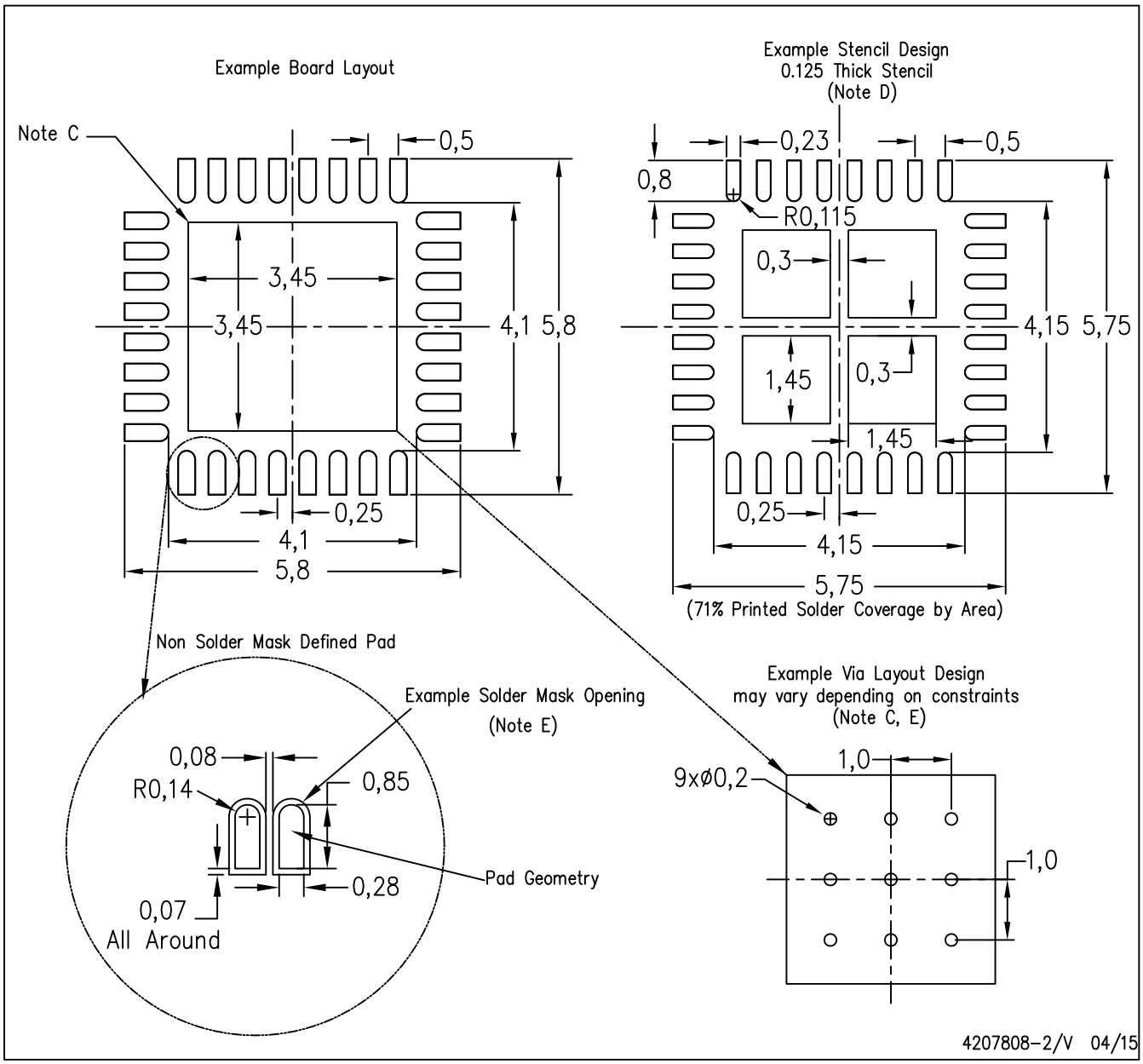
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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- Консультации по применению компонента;
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- Техническая поддержка проекта;
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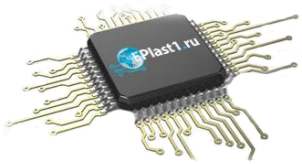

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