Features

- Fully Integrated Fractional-N PLL
- ASK and Closed Loop FSK Modulation
- Output Power Up to +12.5dBm from 300MHz to 450MHz
- Current Consumption is Scaled by Output Power Programming
- Fast Crystal Oscillator Start-up Time of Typically 200µs
- Low Current Consumption of Typically 7.3mA at 5.5dBm
- Only One 13.0000MHz Crystal for 314.1MHz to 329.5MHz and 424.5MHz to 439.9MHz Operation
- Single Ended RF Power Amplifier Output
- Many Software Programmable Options Using SPI
  - Output Power from –0.5dBm to +12.5dBm
  - RF Frequency from 300MHz to 450MHz with Different Crystals
  - FSK Deviation with 396Hz Resolution
  - CLK Output Frequency 3.25MHz or 1.625MHz
- Data Rate Up to 40kbit/s (Manchester)
- 4KV HBM ESD Protection Including XTO
- Operating Temperature Range of –40°C to +125°C
- Supply Voltage Range of 1.9V to 3.6V
- TSSOP10 Package

Benefits

- Robust Crystal Oscillator with Fast Start Up and High Reliability
- Lower Inventory Costs and Reduced Part Number Proliferation
- Longer Battery Lifetime
- Supports Multi-channel Operation
- Wide Tolerance Crystal Possible with PLL Software Compensation

1. Description

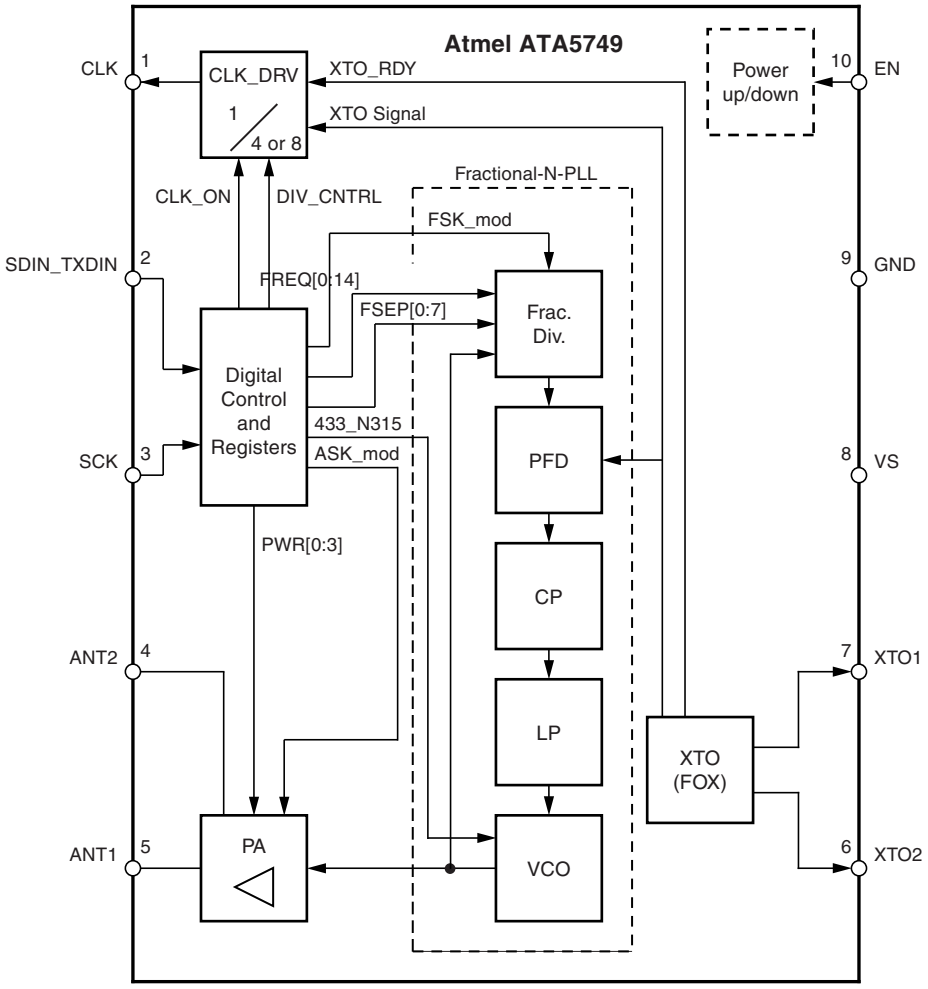
The Atmel® ATA5749 is a fractional-N-PLL transmitter IC for 300MHz to 450MHz operation and is especially targeted for Tire Pressure Sensor Gauges, Remote Keyless Entry, and Passive Entry and other automotive applications. It operates at data rates up to 40kbit/s Manchester for ASK and FSK with a typical 5.5dBm output power at 7.3mA. Transmitter parameters such as output power, output frequency, FSK deviation, and current consumption can be programmed using the SPI interface. This fully integrated PLL transmitter IC simplifies RF board design and results in very low material costs.

Fractional-N PLL Transmitter IC

Atmel ATA5749
Atmel ATA5749C

9128H–RKE–08/11

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. TSSOP10 Package Pinout

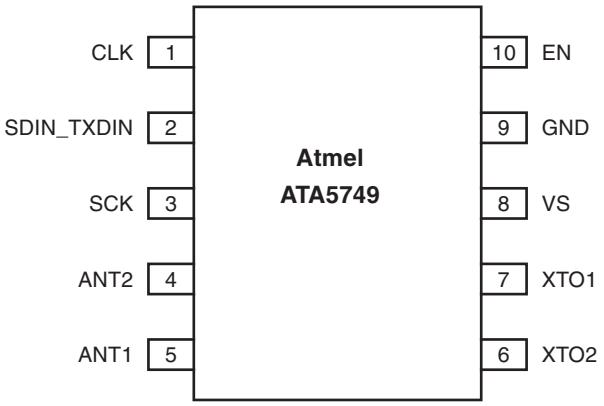


Table 2-1. Pin Description

Pin	Symbol	Function
1	CLK	CLK output
2	SDIN_TXDIN	Serial bus data input and TX data input
3	SCK	Serial bus clock input
4	ANT2	Antenna interface
5	ANT1	Antenna interface
6	XTO2	Crystal/C_{LOAD2} connection
7	XTO1	Crystal/C_{LOAD1} connection
8	VS	Supply input
9	GND	Supply GND
10	EN	Enable input

3. Functional Description

3.1 Fractional-N PLL

The Atmel® ATA5749 block diagram is shown in Figure 1-1 on page 2. The operation of the PLL is determined by the contents of a 32-bit configuration register. The 15-bit value FREQ is used with the 1-bit 434_N315 flag to determine the RF carrier frequency. This results in a user-selectable frequency step size of 793Hz (with 13.000MHz crystal). With this level of resolution, it is possible to compensate for crystal tolerance by adjusting the value of FREQ accordingly. This enables the use of lower cost crystals without compromising final accuracy. In addition, software programming of RF carrier frequency allows this device to be used in some multi-channel applications.

Modulation type is selected with the 1-bit ASK_NFSK flag. FSK modulation is achieved by modifying the divider block in the feedback loop. The benefit to this approach is that performance-reducing RF spurs (common in applications that create FSK by “pulling” the load capacitance in the crystal oscillator circuit) are completely eliminated. The 8-bit value FSEP establishes the FSK frequency deviation. It is possible to obtain FSK frequency deviations from ±396Hz to ±101kHz in steps of ±396Hz.

The PLL lock time is 1280/(external crystal frequency) and amounts to 98.46µs when using a 13.0000MHz crystal. When added to the crystal oscillator start-up time, a very fast time-to-transmit is possible (typically 300µs). This feature extends battery life in applications like Tire Pressure Monitoring Systems, where the message length is often shorter than 10ms and the time “wasted” during start-up and settling time becomes more significant.

3.2 Selecting the RF Carrier Frequency

The fractional divider can be programmed to generate an RF output frequency f_{RF} according to the formulas shown in Table 3-1. Note that in the case of $f_{RF\ ASK}$, the FSEP/2 value is rounded down to the next integer value if FSEP is an odd number.

Table 3-1. RF Output Parameter Formulas

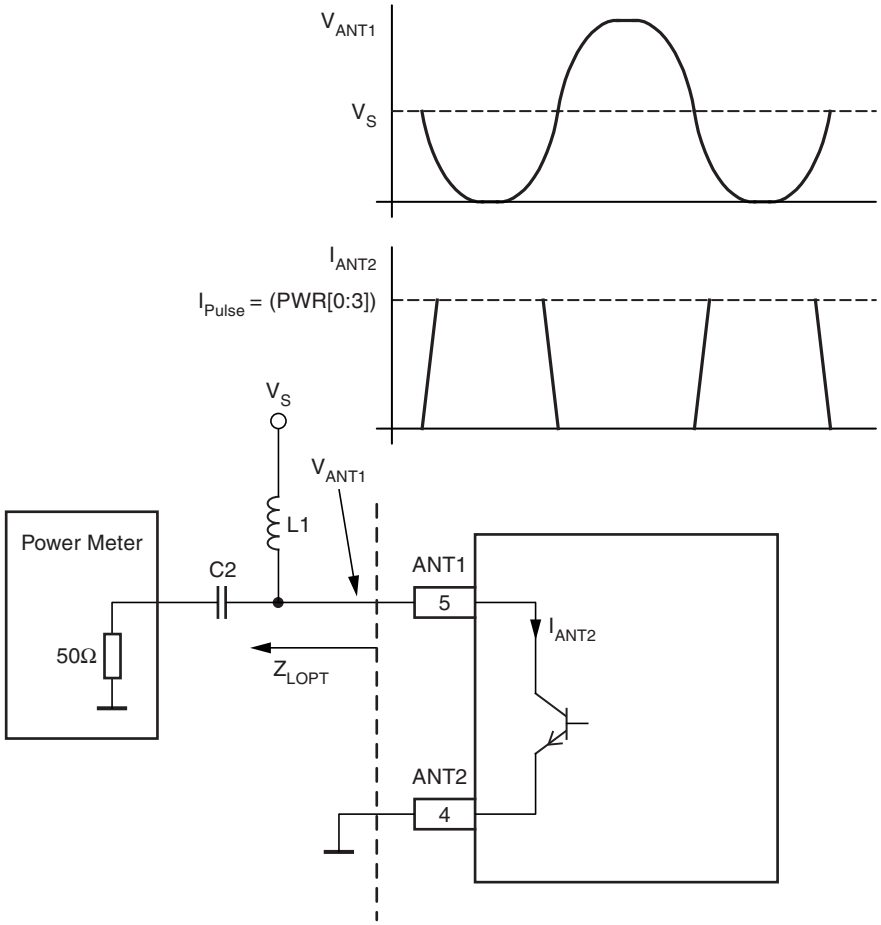
RF Output Parameter	S434_N315 = LOW	S434_N315 = HIGH
$f_{RF_FSK_LOW}$	$(24 + (FREQ + 0.5)/16384) \times f_{XTO}$	$(32.5 + (FREQ + 0.5)/16384) \times f_{XTO}$
$f_{RF_FSK_HIGH}$	$(24 + (FREQ + FSEP + 0.5)/16384) \times f_{XTO}$	$(32.5 + (FREQ + FSEP + 0.5)/16384) \times f_{XTO}$
$f_{DEV__FSK}$	$FSEP/32768 \times f_{XTO}$	$FSEP/32768 \times f_{XTO}$
$f_{RF\ ASK}$	$(24 + (FREQ + FSEP/2 + 0.5)/16384) \times f_{XTO}$	$(32.5 + (FREQ + FSEP/2 + 0.5)/16384) \times f_{XTO}$

FSEP can take on the values of 1 to 255. Using a 13.000MHz crystal, the range of frequency deviation f_{DEV_FSK} is programmable from ±396Hz to ±101.16kHz in steps of ±396Hz. For example, with FSEP = 100 the output frequency is FSK modulated with f_{DEV_FSK} = ±39.6kHz.

FREQ can take values in the range of values 2500 and 22000. Using a 13.0000MHz crystal, the output frequency f_{RF} can be programmed to 315MHz by setting FREQ[0:14] = 3730, FSEP[0:7] = 100 and S434_N315 = 0. By setting FREQ[0:14] = 14342, FSEP[0:7] = 100 and S434_N315 = 1, 433.92MHz can be realized.

The PA is enabled when the PLL is locked and the configuration register programming is completed. Upon enabling PA at FSK-mode, the RF output power will be switched on. At ASK mode, the input signal must be additionally set high for RF at output pins. The output power is user programmable from –0.5dBm to +12.5dBm in steps of approximately 1dB. Changing the output power requirements, you also modify the current consumption. This gives the user the option to optimize system performance (RF link budget versus battery life). The PA is implemented as a Class-C amplifier, which uses an open-collector output to deliver a current pulse that is nearly independent from supply voltage and temperature. The working principle is shown in Figure 3-1.

Figure 3-1. Class C Power Amplifier Output



The peak value of this current pulse I_{Pulse} is calibrated during Atmel® ATA5749 production to about ±20%, which corresponds to about 1.5dB variation in output power for a given power setting under typical conditions. The actual value of I_{Pulse} can be programmed with the 4-bit value in PWR. This allows the user to scale both the output power and current consumption to optimal levels.

ASK modulation is achieved by using the SDIN_TXDIN signal where a HIGH on this pin corresponds to RF carrier “ON” and a LOW corresponds to RF “OFF”. FSK uses the same signal path but HIGH switch on the upper FSK-frequency.

3.3 Crystal Oscillator

The crystal oscillator (XTO) is an amplitude-regulated Pierce oscillator. It has fixed function and is not programmable. The oscillator is enabled when the EN is “set”. After the oscillator’s output amplitude reaches an acceptable level, the XTO_RDY flag is “set”. The CLK-pin becomes active if CLK_ON is set. The PLL receives its reference frequency.

Typically, this process takes about 200µs when using a small sized crystal with a motional capacitance of 4fF. This start-up time strongly depends on the motional capacitance of the crystal and is lower with higher motional capacitance.

The high negative starting impedance of $R_{XTO12_START} > 1500\Omega$ is important to minimize the failure rate due to the “sleeping crystal” phenomena (more common among very small sized 3.2mm $\times$ 2.5mm crystals).

3.4 Clock Driver

The clock driver block shown in Figure 1-1 on page 2 is programmed using the CLK_ONLY, CLK_ON, and DIV_CNTRL bits in the configuration register. When CLK_ONLY is “clear”, normal operation is selected and the fractional-N PLL is operating. When CLK_ON is “set”, the CLK output is enabled. The crystal clock divider ratio can be set to divide by four when DIV_CNTRL is “set” and divide by eight when DIV_CNTRL is “clear”. With a 13.0000MHz crystal, this yields an output of 3.25MHz or 1.625MHz, respectively. When CLK_ON is “clear”, no clock is available at CLK and the transmitter has less current consumption.

The CLK signal can be used to clock a microcontroller. It is CMOS compatible and can drive up to 20pF of load capacitance at 1.625MHz and up to 10pF at 3.25MHz. When the device is in power-down mode, the CLK output stays low. Upon power up, CLK output remains low until the amplitude detector of the crystal oscillator detects sufficient amplitude and XTO_RDY and CLK_ON are “set”. After this takes place, CLK output becomes active. The CLK output is synchronized with the XTO_RDY signal so that the first period of the CLK output is always a full period (no CLK output spike at activation).

To lower overall current consumption, it is possible to power down the entire chip except for the crystal oscillator block. This can be achieved when the CLK_ONLY is “set”.

4. Application

4.1 Typical Application

Figure 4-1. Typical Application Circuit

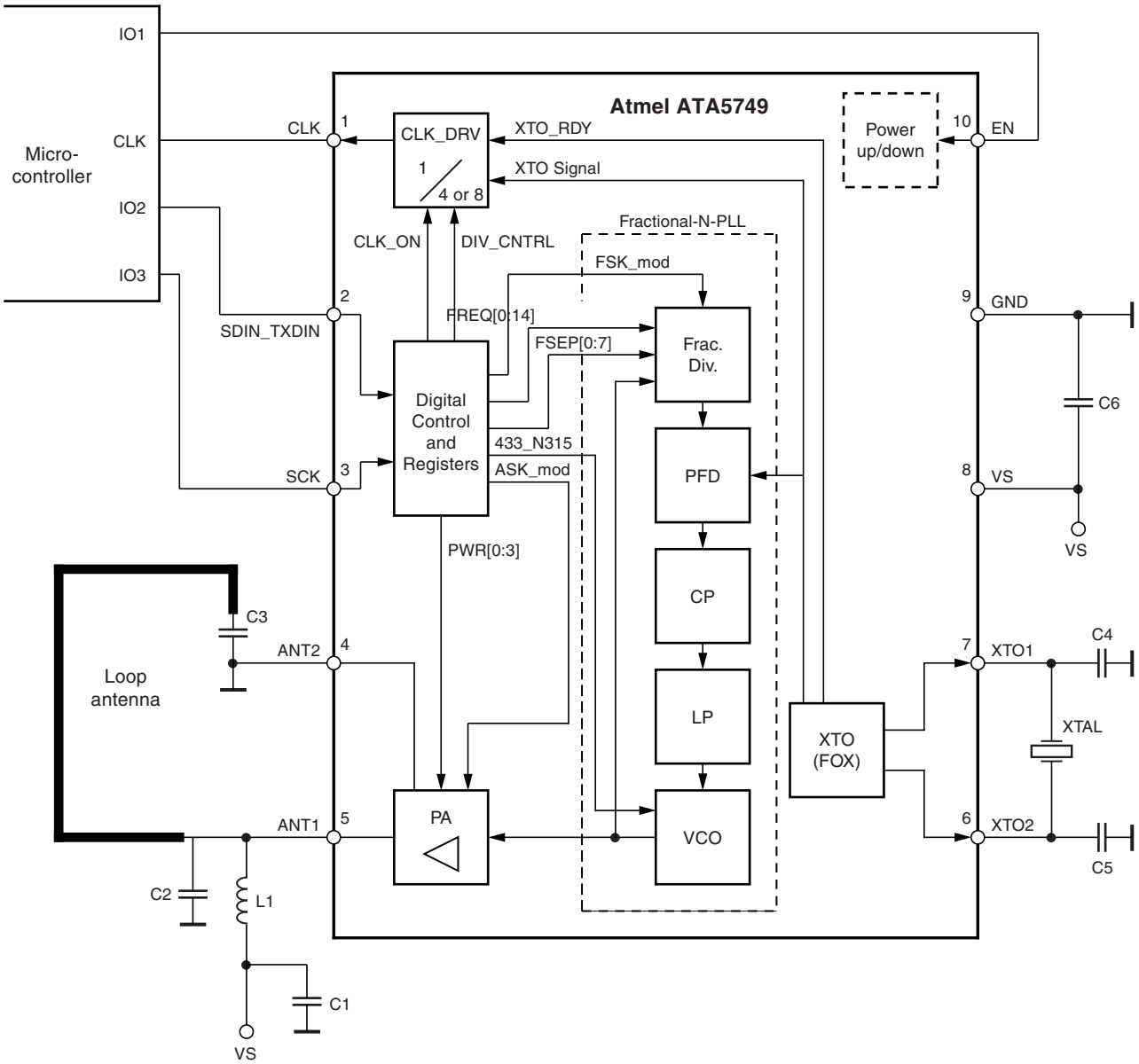


Figure 4-1 shows the typical application circuit. For C6, the supply-voltage blocking capacitor, value of 68nF X7R is recommended. C2 and C3 are NPO capacitors used to match the loop antenna impedance to the power amplifier optimum load impedance. They are based on the PCB trace antenna and are ≤20pF NPO capacitors. C1 (typically 1nF X7R) is needed for the supply blocking of the PA. In combination with L1 (200nH to 300nH), they prevent the power amplifier from coupling to the supply voltage and disturbing PLL operation. They should be placed close to pin 5. L1 also provides a low resistive path to V_S to deliver the DC current to ANT1.

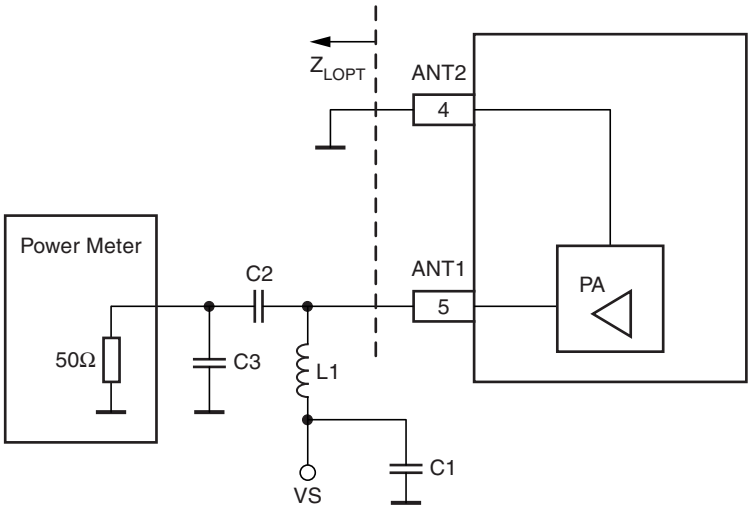
The PCB loop antenna should not exceed a trace width of 1.5mm otherwise the Q-factor of the loop antenna is too high. C4 and C5 should be selected so that the XTO runs on the load resonance frequency of the crystal. A crystal with a load capacitance of 9pF is recommended for proper start-up behavior and low current consumption. When determining values for C4 and C5, a parasitic capacitance of 3pF should be included. With value of 15pF for C4 and C5, an effective load capacitance of 9pF can be achieved, e.g., 9pF = (15pF + 3pF)/2. The supply V_S is typically delivered from a single Li-Cell.

4.1.1 Antenna Impedance Matching

The maximum output power is achieved by using load impedances according to Table 4-1 on page 9 and Table 4-2 on page 9 and the output power. The load impedance Z_{LOPT} is defined as the impedance seen from the Atmel® ATA5749 ANT1, ANT2 into the matching network. This is not the output impedance of the IC but essentially the peak voltage divided by the peak current with some additional parasitic effects (Cpar). Table 4-1 on page 9 and Table 4-2 on page 9 do not contain information pertaining to C3 in Figure 4-2, which is an option for better matching at low power steps.

Figure 4-2 is the circuit that was used to obtain the typical output power measurements in Figure 4-3 on page 10 and typical current consumption in Figure 4-4 on page 10. Table 4-1 and Table 4-2 on page 9 provide recommended values and performance info at various output power levels. For reference, Z_{LOPT} is defined as the impedance seen from the Atmel ATA5749 ANT1, ANT2 into the matching network.

Figure 4-2. Output Power Measurement Circuit



The used parts at Table 4-1 and Table 4-2 are:

Inductors: high Q COILCRAFT 0805CS; Capacitors: AVX ACCU-P 0402

Table 4-1. Measured PA Matching at 315MHz (CLK_ON = “LOW”) at Typ. Samples

PWR Register	Desired Power (dBm)	L1 (nH)	C2 (pF)	C3 [1] (pF)	R_{LOPT} (Ω)	Z_{LOPT} (Ω)	Cpar (pF)	Actual Power (dBm)
3	–0.5	110	1.2	1.6	2950	110 + 540j	0.9	–0.37
4	1.0	100	1.5	---	1940	150 + 520j	0.9	1.12
5	2.5	100	1.5	---	1550	190 + 520j	0.9	2.11
6	3.5	100	1.5	---	1250	220 + 480j	0.9	3.23
7	4.5	82	1.8	---	1000	240 + 430j	0.9	4.38
8	5.5	82	2.2	---	730	280 + 360j	0.9	5.42
9	6.5	68	2.7	---	580	290 + 300j	0.9	7.14
10	7.5	68	2.7	---	460	290 + 290j	0.9	8.22
11	8.5	68	3.3	---	350	280 + 225j	0.9	8.63
12	9.5	56	3.6	---	320	250 + 150j	0.9	9.79
13	10.5	47	4.7	---	250	215 + 85j	0.9	10.52
14	11.5	47	5.6	---	190	180 + 50j	0.9	11.67
15	12.5	47	5.6	---	160	160 + 45j	0.9	13

Note: 1. Leave capacitor out at row without value

Table 4-2. Measured PA Matching at 433.92MHz (CLK_ON = “LOW”) at Typ. Samples

PWR Register	Desired Power (dBm)	L1 (nH)	C2 (pF)	C3 [1] (pF)	R_{LOPT} (Ω)	Z_{LOPT} (Ω)	Cpar (pF)	Actual Power (dBm)
3	–0.5	68	0,9	1.5	2800	60 + 400j	0.9	–0.62
4	1.0	56	2.7 + 2.2	---	1850	90 + 390j	0.9	1.3
5	2.5	56	1.2	---	1450	110 + 380j	0.9	2.73
6	3.5	47	1.8	5.6	1150	130 + 370j	0.9	3.03
7	4.5	47	1.6	---	950	150 + 350j	0.9	4.63
8	5.5	47	1.8	---	680	180 + 300j	0.9	6.18
9	6.5	43	2.2	1	560	200 + 270j	0.9	6.66
10	7.5	36	2.4	---	450	210 + 230j	0.9	7.91
11	8.5	33	3	---	340	200 + 170j	0.9	8.68
12	9.5	36	2.7	---	310	195 + 150j	0.9	9.8
13	10.5	36	3.6	---	230	175 + 100j	0.9	10.49
14	11.5	27	4.7	---	180	150 + 70j	0.9	11.6
15	12.5	27	4.7	---	150	130 + 50j	0.9	12.5

Note: 1. Leave capacitor out at row without value

Figure 4-3. Typical Measured Output Power

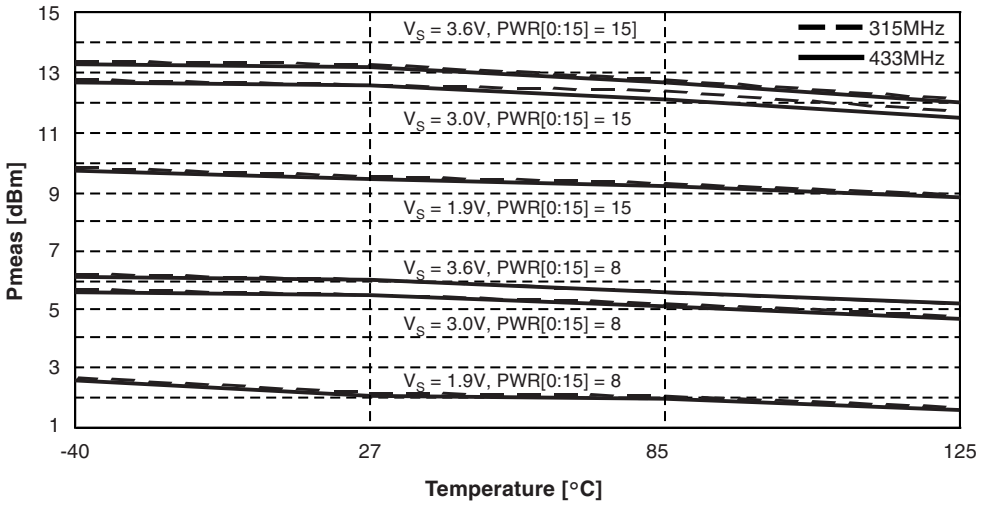
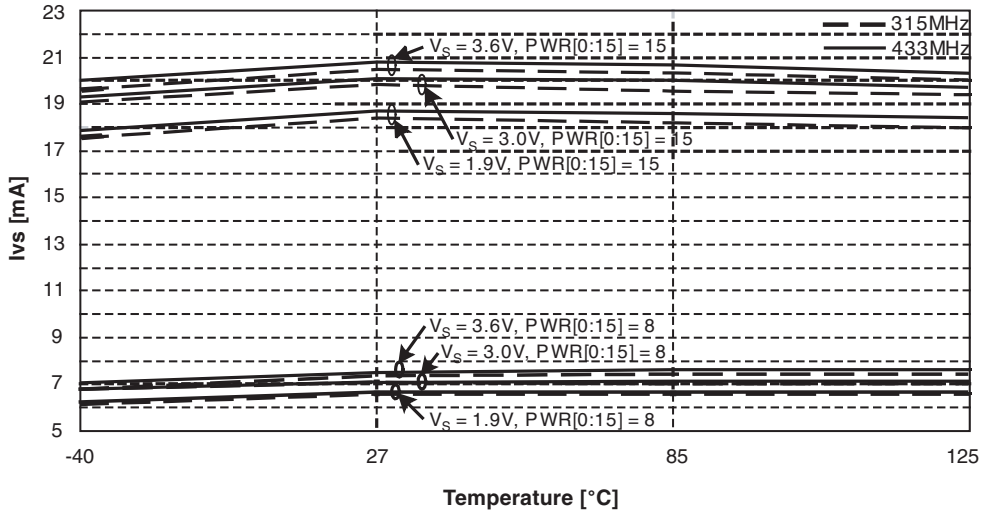


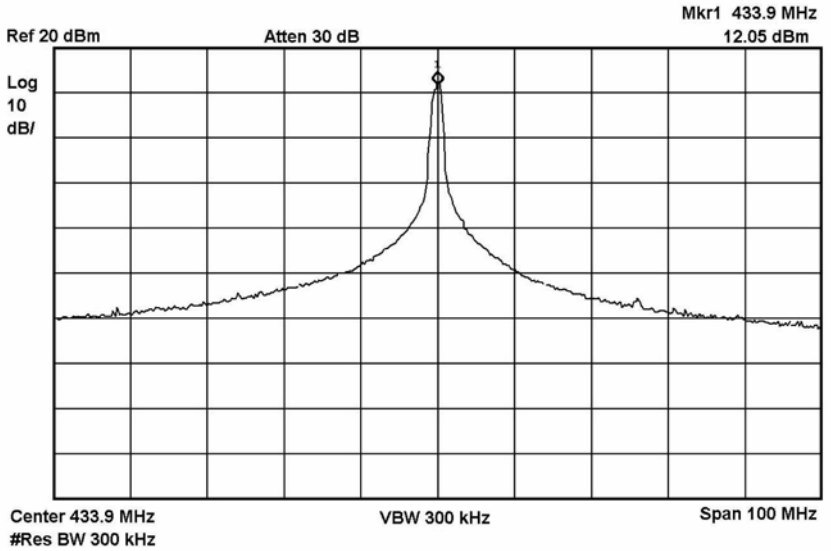
Figure 4-4. Typical Current Consumption I at Port VS



5. Pulling of Frequency due to ASK Modulation (PA Switching)

The switching effect on VCO frequency in ASK Mode is very low if a correct PCB layout and decoupling is used. Therefore, power ramping is not needed to achieve a clean spectrum (see Figure 5-1).

Figure 5-1. Typical RF Spectrum of 40kHz ASK Modulation at Pout = 12.5dBm



6. Configuration Register

6.1 General Description

The user must program all 32 bits of the configuration register upon power up (EN = HIGH) or whenever changes to operating parameters are desired. The configuration register bit assignments and descriptions can be found in Table 6-1 and Table 6-2.

Table 6-1. Organization of the Control Register

MSB															
31 CLK_ ONLY	30 S434_ N315	29 FREQ [14]	28 FREQ [13]	27 FREQ [12]	26 FREQ [11]	25 FREQ [10]	24 FREQ [9]	23 FREQ [8]	22 FREQ [7]	21 FREQ [6]	20 FREQ [5]	19 FREQ [4]	18 FREQ [3]	17 FREQ [2]	16 FREQ [1]
		Frequency Adjust = FREQ[0..14] FREQ[0] + 2 × FREQ[1] + 4 × FREQ[2] + ... + FREQ[14] × 16384 = 0..32767													

LSB															
15 FREQ [0]	14 FSEP [7]	13 FSEP [6]	12 FSEP [5]	11 FSEP [4]	10 FSEP [3]	9 FSEP [2]	8 FSEP [1]	7 FSEP [0]	6 DIV_ CNTRL	5 PWR [3]	4 PWR [2]	3 PWR [1]	2 PWR [0]	1 ASK_ NFSK	0 CLK_ ON
	FSK Shift = FSEP[0..7] FSEP[0] + ... + FSEP[7] × 128 = 0..255									Output Power = PWR[0..3] PWR[0] + .. + PWR[3] × 8 = 0..15					

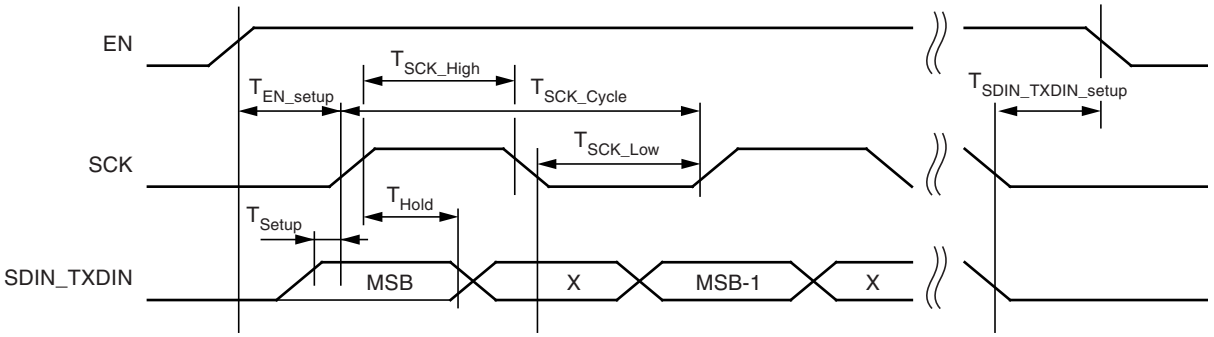
Table 6-2. Control Register Functional Descriptions

Name	Bit No.	Size	Remarks
CLK_ONLY	31	1	Activates/deactivates CLK_ONLY Mode Low = Normal Mode High = Clock Only Mode (Figure 4-1 on page 7)
S434_N315	30	1	VCO band selection High = 367MHz to 450MHz Low = 300MHz to 368MHz
FREQ[0:14]	15 ... 29	15	PLL frequency adjust See Table 6-1 for formula
FSEP[0:7]	7 ... 14	8	FSK deviation adjust See Table 6-1 for formula
DIV_CNTRL	6	1	CLK output divider ratio Low = $f_{XTO}/8$ High = $f_{XTO}/4$
PWR[0:3]	2 ... 5	4	PA output power adjustment See Table 4-1 and Table 4-2 on page 9
ASK_NFSK	1	1	Modulation type Low = FSK High = ASK
CLK_ON	0	1	CLK_DRV port control HIGH = CLK port is ON LOW = CLK port is OFF

6.2 Programming

The configuration register is programmed serially using the SPI bus, starting with the MSB. It consists of the Enable line (EN), the Data line (SDIN_TXDIN), and the SPI-Bus Clock (SCK). The SDIN_TXDIN data is loaded on the positive edge of the SCK. The contents of the configuration register become programmed on the negative SCK edge of the last bit (LSB) of the programming sequence. The timing of this bus is shown in Figure 6-1. Note that the maximum usable clock speed on the SPI bus is limited to 2MHz.

Figure 6-1. SPI Bus Timing



At the conclusion of the 32 bit programming sequence, the SDIN_TXDIN line becomes the modulation input for the RF transmitter. After programming is complete, the SCK signal has no effect on the device. To disable the transmitter and enter the OFF Mode, EN and SDIN_TXDIN must be returned to the LOW state. For clarity, several additional timing diagrams are included. Figure 6-2 shows the situation when the programming terminates faster then the XTO is ready.

Figure 6-2. Timing Diagram if Register Programming is Faster than ΔT_{XTO}

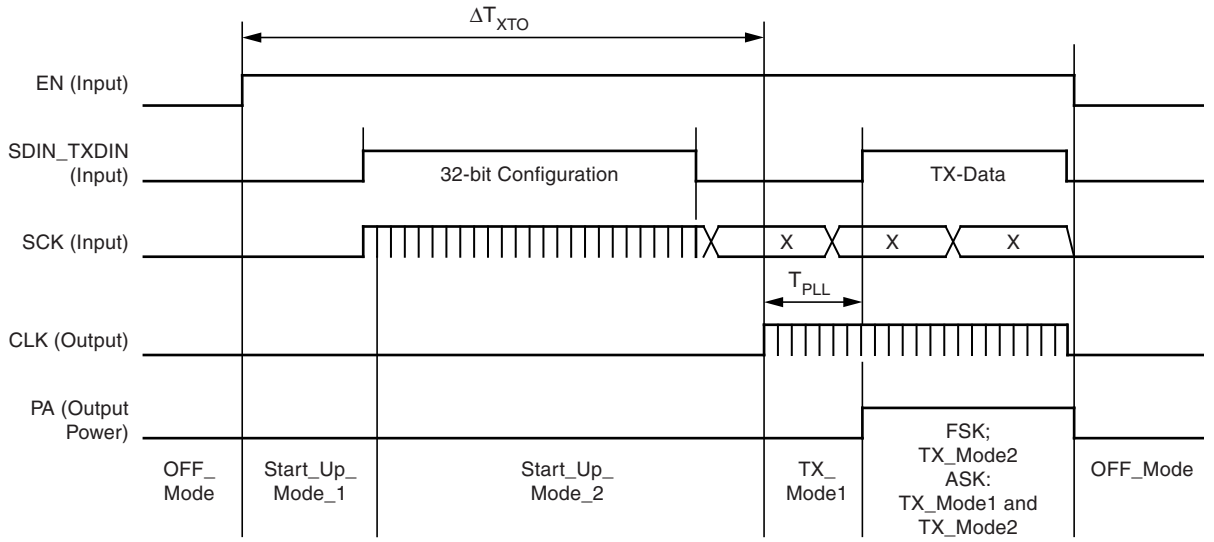
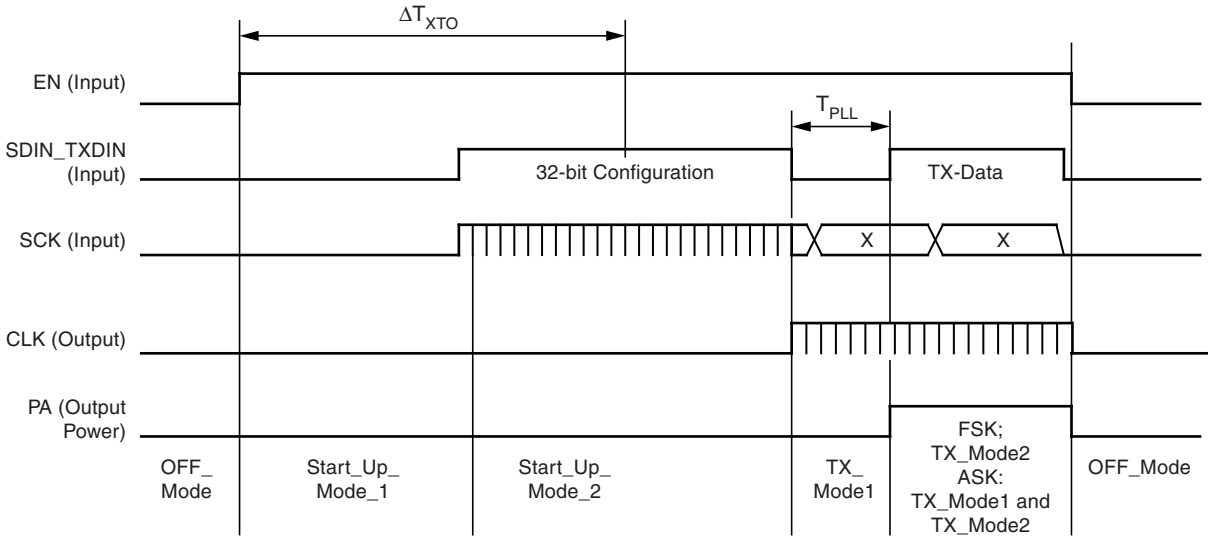


Figure 6-3 shows the combination with slow programming and a faster ramp up of XTO. A diagram of the operating modes is shown in Figure 6-5 on page 16 and a description of which circuit blocks are active is provided in Table 6-3 on page 15. This also contains the information needed for the calculation of consumed charge for one operation cycle.

Figure 6-3. Timing Diagram if Programming is Slower than T_{XTO}



6.3 Reprogramming without Stopping the Crystal Oscillator

After the configuration register is programmed and RF data transmission is completed, the OFF mode is normally entered. This stops the crystal oscillator and PLL. If it is desirable to modify the contents of the configuration register without entering the OFF mode, the Reset_Register_Mode can be used. To enter the Reset_Register_Mode, the SDIN_TXDIN must be asserted HIGH while the EN is asserted LOW for at least 10µs Reset_min time. This state is shown in Figure 6-4 on page 15, State Diagram of Operating Modes. In Reset_Register_Mode, the PA and fractional PLL remain OFF but the XTO remains active. This state must stay for minimum 10µs. At the next step you must rise first EN and SDIN_TXDIN 10µs delayed. While in this mode, the 32 bit configuration register data can be sent on the SPI bus as shown in Figure 6-2 on page 13. After data transmission, the device can be switched back to OFF_Mode by asserting EN, SCK, and SDIN_TXDIN to a LOW state. An example of programming from the Reset_Register_Mode is shown in Figure 6-4 on page 15.

Figure 6-4. Timing Diagram when using Reset_Register_Mode

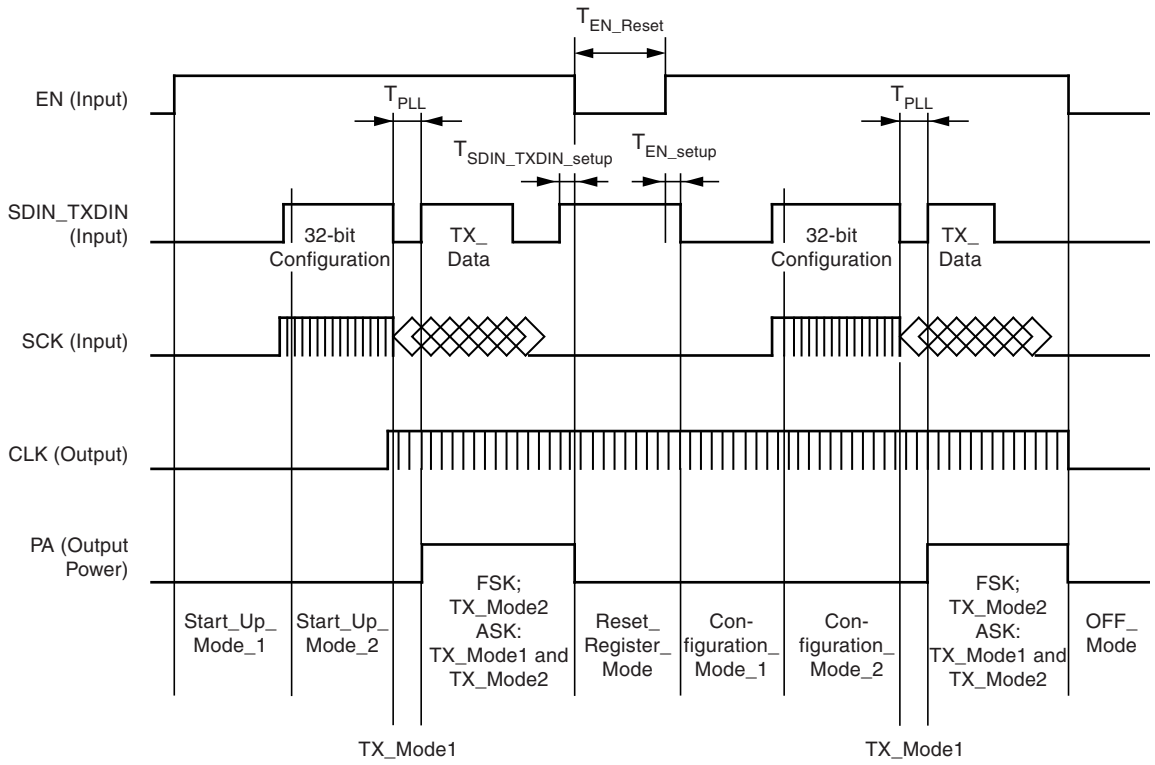
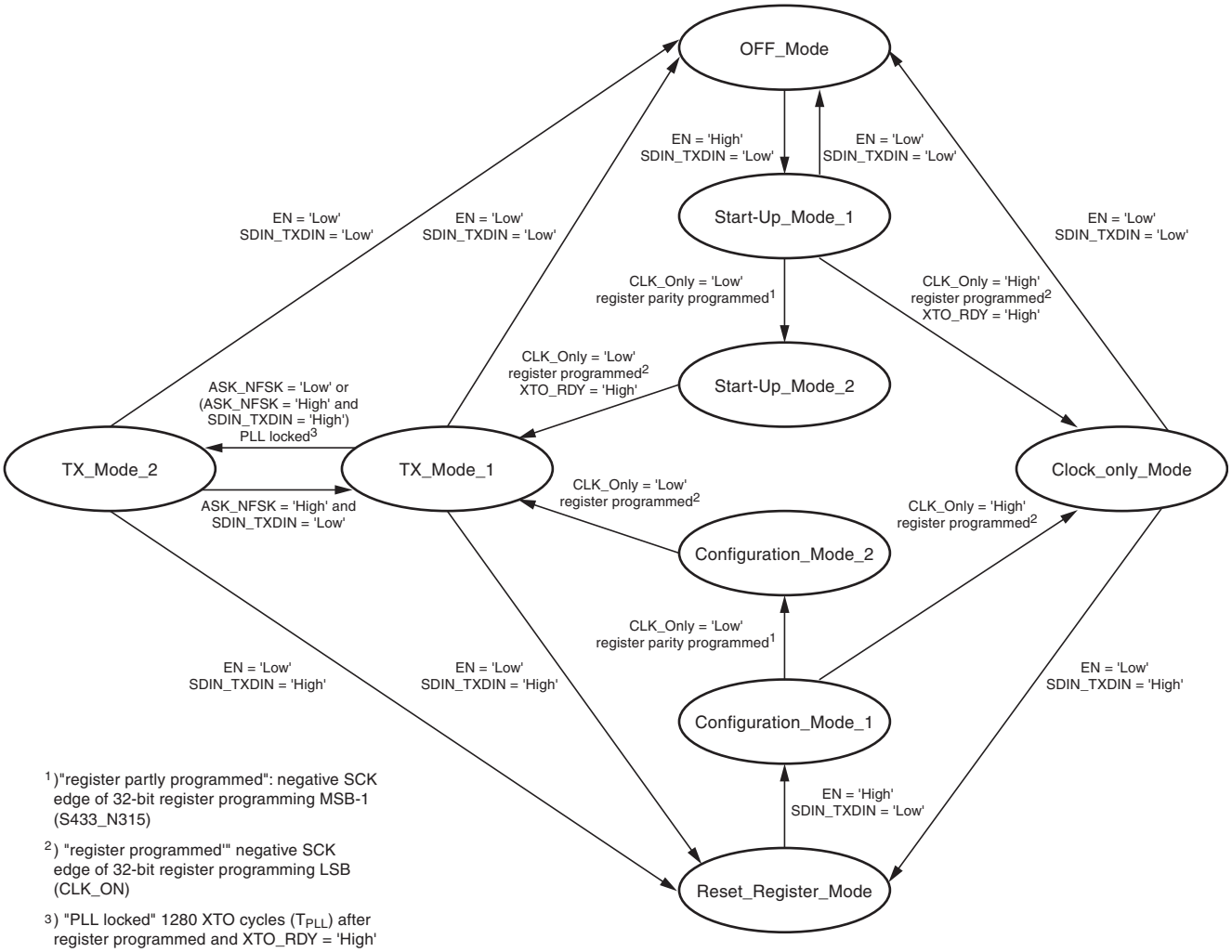


Table 6-3. Active Circuits as a Function of Operating Mode

Operating Mode	Active Circuit Blocks
OFF_Mode	-none-
Start_Up_Mode_1	Power up/down; XTO; digital control
Start_Up_Mode_2	Power up/down; XTO; digital control; fractional-N-PLL
TX_Mode1	Power up/down; XTO; digital control; fractional-N-PLL; CLK_DRV(1)
TX_Mode2	Power up/down; XTO; digital control; fractional-N-PLL; CLK_DRV(1); PA
Clock_Only_Mode	Power up/down; XTO; digital control; CLK_DRV(1)
Reset_Register_Mode	Power up/down; XTO; digital control; CLK_DRV(1)
Configuration_Mode_1	Power up/down; XTO; digital control; CLK_DRV(1)
Configuration_Mode_2	Power up/down; XTO; digital control; CLK_DRV(1); fractional-N-PLL

Note: 1. Only if activated with CLK_ON = HIGH

Figure 6-5. State Diagram of Operating Modes



1)"register partly programmed": negative SCK edge of 32-bit register programming MSB-1 (S433_N315)

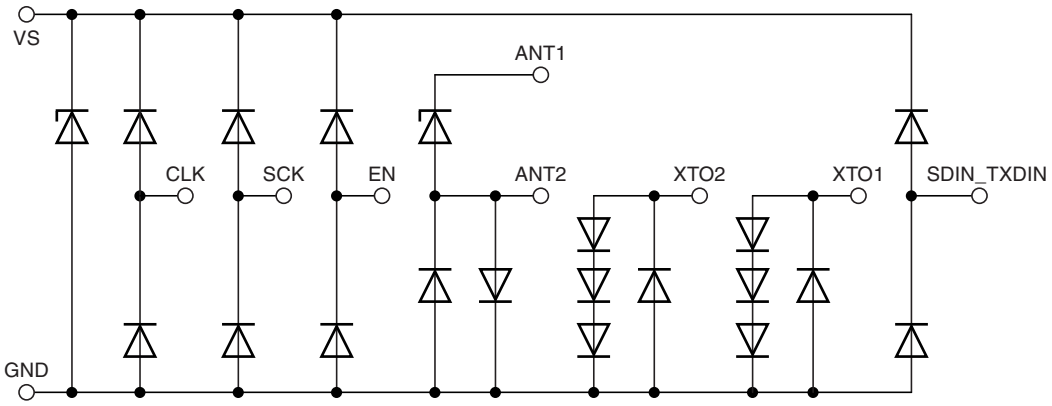
2) "register programmed'" negative SCK edge of 32-bit register programming LSB (CLK_ON)

3) "PLL locked" 1280 XTO cycles (T_{PLL}) after register programmed and XTO_RDY = 'High'

To transition from one state to another, only the conditions next to the transition arrows must be fulfilled. No additional settings are required.

7. ESD Protection Circuit

Figure 7-1. ESD Protection Circuit



8. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S	–0.3	+4.0	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	+125	°C
Ambient temperature	Tamb1	–40	+125	°C
Ambient temperature in power-down mode for 30 minutes without damage with $V_S \leq 3.2V$, $V_{ENABLE} < 0.25V$ or ENABLE is open, $V_{ASK} < 0.25V$, $V_{FSK} < 0.25V$	Tamb2		175	°C
ESD (Human Body Model ESD S5.1) every pin excluding pin 5 (ANT1)	HBM	–4	+4	kV
ESD (Human Body Model ESD S5.1) for pin 5 (ANT1)	HBM	–2	+2	kV
ESD (Machine Model JEDEC A115A) every pin excluding pin 5 (ANT1)	MM	–200	+200	V
ESD (Machine Model JEDEC A115A) for pin 5 (ANT1)	MM	–150	+150	V
ESD – STM 5.3.1-1999 every pin	CDM		750	V

9. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance, junction ambient	R_{thJA}	170	K/W

10. Electrical Characteristics

V_S = 1.9V to 3.6V T_{amb} = –40°C to +125°C, CLK_ON = “High”; DIV_CNTRL = “Low”, CLOAD_CLK = 10pF. f_{XTO} = 13.0000MHz, f_{CLK} = 1.625MHz unless otherwise specified. If crystal parameters are important values correspond to a crystal with C_M = 4.0fF, C_0 = 1.5pF, C_{LOAD} = 9pF and $R_M \leq 170\Omega$. Typical values are given at V_S = 3.0V and T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current Consumption**								
1.1	Supply current, OFF_Mode	V(SDIN_TXDIN,SCK,EN) = Low $T_{amb} \leq$ +25°C $T_{amb} \leq$ +85°C $T_{amb} \leq$ +125°C	5, 8	$I_{S_Off_Mode}$		1 20 265	100 350 7,000	nA nA nA	A
1.2	Supply current, TX_Mode1	$V_S \leq$ 3.0V	5, 8	$I_{S_TX_Mode1}$		3.6	4.75	mA	B
1.3	Supply current, TX_Mode2	$V_S \leq$ 3.0V PWR[0:3] = 8 (5.5dBm)	5, 8	$I_{S_TX_Mode2}$		7.3	8.8	mA	B
1.4	Supply current, CLK_Only_Mode	$V_S \leq$ 3.0V	5, 8	$I_{S_CLK_Only_Mode}$		480	680	µA	B
1.5	Supply current reduction, Clock Driver off	$V_S \leq$ 3.0V CLK_ON = “Low” $I_S = I_{S_any_Mode} + \Delta I_{CLKoff1}$ (can be applied to all modes except Off_Mode, add Typ. to Typ. and Max. to Max. values)	5, 8	$\Delta I_{CLKoff1}$		–250	–300	µA	B
1.6	Supply current increase, Clock Driver higher frequency	$V_S \leq$ 3.0V DIV_CNTRL = “High” f_{CLK} = 3.24MHz $I_S = I_{S_any_Mode} + \Delta I_{CLKhigh}$ (can be applied to all modes except Off_Mode add Typ. to Typ. and Max. to Max. values)	5, 8	$\Delta I_{CLKhigh}$		150	190	µA	B
1.7	Reset_Register_Mode / Configuration_Mode_1	$V_S \leq$ 3.0V	5, 8	$I_{S_Reset_Register_Mode}$ / $I_{S_Configuration_Mode_1}$			680	µA	B
1.8	Configuration_Mode_2 / Start_Up_Mode_2	$V_S \leq$ 3.0V	5, 8	$I_{S_Configuration_Mode_2}$ / $I_{S_Start_Up_Mode_2}$			4.75	mA	B
1.9	Start_Up_Mode_1	$V_S \leq$ 3.0V	5, 8	$I_{S_Start_Up_Mode_1}$			350	µA	B
2	**Power Amplifier (PA)**								
2.1	Output power 1, TX_Mode2	V_S = 3.0V, T_{amb} = 25°C PWR[0:3] = 4 $Z_{LOAD} = Z_{LOPT}$ according to Table 4-1 on page 9 and Table 4-2 on page 9	(5)	P_{OUT_1}	–1.0	+1.0	+3.0	dBm	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: (Pin Number) in brackets mean they are measured matched to 50Ω according to Figure 4-2 on page 8 with component values and optimum load impedances according to Table 4-1 and Table 4-2 on page 9

10. Electrical Characteristics (Continued)

V_S = 1.9V to 3.6V T_{amb} = –40°C to +125°C, CLK_ON = “High”; DIV_CNTRL = “Low”, CLOAD_CLK = 10pF. f_{XTO} = 13.0000MHz, f_{CLK} = 1.625MHz unless otherwise specified. If crystal parameters are important values correspond to a crystal with C_M = 4.0fF, C_0 = 1.5pF, C_{LOAD} = 9pF and $R_M \leq 170\Omega$ Typical values are given at V_S = 3.0V and T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.2	Supply current 1, TX_Mode2	V_S = 3.0V PWR[0:3] = 4	5, 8	I_{S_P1}		5.4	6.7	mA	B
		V_S = 3.6V PWR[0:3] = 4	5, 8	I_{S_P1}			7.0	mA	A
2.3	Output power 2, TX_Mode2	V_S = 3.0V, T_{amb} = 25°C PWR[0:3] = 8 $Z_{LOAD} = Z_{LOPT}$ according to Table 4-1 on page 9 and Table 4-2 on page 9	(5)	P_{OUT_2}	4.0	5.5	7.0	dBm	A
2.4	Supply current 2, TX_Mode2	V_S = 3.0V, PWR[0:3] = 8 [typ. 5.5dBm; see 2.3]	5, 8	I_{S_P2}		7.3	8.8	mA	B
		V_S = 3.6V, PWR[0:3] = 8 [typ. 5.5dBm; see 2.3]	5, 8	I_{S_P2}			9.1	mA	A
2.5	Output power 3, TX_Mode2	V_S = 3.0V, T_{amb} = 25°C PWR[0:3] = 15 $Z_{LOAD} = Z_{LOPT}$ according to Table 4-1 on page 9 and Table 4-2 on page 9	(5)	P_{OUT_3}	11.0	12.5	14.0	dBm	B
2.6	Supply current 3, TX_Mode2	V_S = 3.0V PWR[0:3] = 15	5, 8	I_{S_P3}		20.2	23.5	mA	A
		V_S = 3.6V PWR[0:3] = 15	5, 8	I_{S_P3}			24.5	mA	A
2.7	Output Power Variation for full temperature and supply voltage range	T_{amb} = –40°C to +125°C V_S = 1.9V to 3.6V Pout = $P_{OUT_x} + \Delta P_{OUT}$ (can be applied to all power levels)	(5)	ΔP_{OUT}	–4.0		+1.5	dB	B
3	**Crystal Oscillator (XTO)**								
3.1	Maximum series resistance R_M of XTAL after start-up	C_0 < 2.0pF	6, 7	R_{M_MAX}			170	Ω	D
3.2	Motional capacitance of XTAL	Recommended values	6, 7	C_M	2	4.0	15	fF	D
3.3	Stabilized Amplitude XTAL	C_0 < 2.0pF C_M = 4.0fF R_M = 20Ω C_{LOAD} = 9pF V(XTO2) – V(XTO1) V(XTO1)	6, 7	 Vpp_{XTO21} Vpp_{XTO1}		 640 320		mVpp	A
3.4	Pulling of f_{XTO} versus temperature and supply change	1.0 < C_0 < 2.0pF R_M < 170Ω C_{LOAD} = 9pF 4fF < C_M < 10fF C_M < 15fF	6, 7	Δf_{RF}	–3 –5		+3 +5	ppm	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: (Pin Number) in brackets mean they are measured matched to 50Ω according to Figure 4-2 on page 8 with component values and optimum load impedances according to Table 4-1 and Table 4-2 on page 9

10. Electrical Characteristics (Continued)

V_S = 1.9V to 3.6V T_{amb} = –40°C to +125°C, CLK_ON = “High”; DIV_CNTRL = “Low”, CLOAD_CLK = 10pF. f_{XTO} = 13.0000MHz, f_{CLK} = 1.625MHz unless otherwise specified. If crystal parameters are important values correspond to a crystal with C_M = 4.0fF, C_0 = 1.5pF, C_{LOAD} = 9pF and $R_M \leq 170\Omega$. Typical values are given at V_S = 3.0V and T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	DC voltage after XTAL amplitude stable	V(XTO2) – V(XTO1) XTO running	6, 7	V_{DC_XTO}		40		mV	C
3.6	Negative real part of XTO impedance at begin of start-up	This value is important for crystal oscillator start-up behavior C_0 < 2.0pF, 8pF < C_{LOAD} < 10pF F_{XTAL} = 13.000MHz 11.0MHz < F_{XTAL} < 14.8MHz	6, 7	R_{XTO12_START}	–1,500 –1,300	–2,200		Ω	B
3.7	External Capacitors C4, C5	Recommended values for proper start-up and low current consumption Quality NPO $C_{LOAD} = (C_4 + C_{XTO1}) \times (C_5 + C_{XTO2}) / (C_4 + C_5 + C_{XTO1} + C_{XTO2})$ C_{Load_nom} = 9pF (inc. PCB)	6, 7	C_4 C_5	–5%	15	+5%	pF	D
3.8	Pin Capacitance XTO1 and XTO2	The PCB Capacitance of about 1pF has to be added	6, 7	C_{XTO1} C_{XTO2}	–15% –15%	2 2	+15% +15%	pF	C
3.9	Crystal oscillator start-up time	Time between EN = “High” and XTO_RDY = “High” C_0 < 2.0pF, 4fF < C_M < 15fF C_0 < 2.0pF, 2fF < C_M < 15fF R_M < 170Ω 11.0MHz < F_{XTAL} < 14.8MHz	6, 7, 1	ΔT_{XTO}		0.20 0.32	0.3 0.5	ms	B
3.10	Maximum shunt capacitance C_0 of XTAL	Required for stable operation of XTO, C_{Load} > 7. 5pF	6, 7	C_{0_MAX}		1.5	3.0	pF	D
3.11	Oscillator frequency XTO	433.92MHz and 315MHz other frequencies	6, 7	f_{XTO}	11.0	13.0000	14.8	MHz	C
4	**Fractional-N-PLL**								
4.1	Frequency range of RF frequency	S434_N315 = “LOW” S434_N315 = “HIGH”	5	f_{RF}	300 367		368 450	MHz	A
4.2	Locking time of the PLL	Time between XTO_RDY= “High” and Register programmed till PLL is locked f_{XTO} = 13.0000MHz other f_{XTO}	1, 5	ΔT_{PLL}			98.46 $\left(1280/f_{XTO}\right)$	µs	B
4.3	PLL loop bandwidth	Unity gain loop frequency of synthesizer	5	f_{Loop_PLL}	140	280	380	kHz	B
4.4	In Loop phase noise PLL	25kHz distance to carrier	5	L_{PLL}		–83	–76	dBc/Hz	A
4.5	Out of Loop Phase noise (VCO)	At 1MHz At 36MHz	5	L_{at1M} L_{at36M}		–91 –122	–84 –115	dBc/Hz dBc/Hz	A C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: (Pin Number) in brackets mean they are measured matched to 50Ω according to Figure 4-2 on page 8 with component values and optimum load impedances according to Table 4-1 and Table 4-2 on page 9

10. Electrical Characteristics (Continued)

V_S = 1.9V to 3.6V T_{amb} = –40°C to +125°C, CLK_ON = “High”; DIV_CNTRL = “Low”, CLOAD_CLK = 10pF. f_{XTO} = 13.0000MHz, f_{CLK} = 1.625MHz unless otherwise specified. If crystal parameters are important values correspond to a crystal with C_M = 4.0fF, C_0 = 1.5pF, C_{LOAD} = 9pF and $R_M \leq 170\Omega$ Typical values are given at V_S = 3.0V and T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.6	FSK modulation frequency	Duty cycle of the modulation signal = 50%, (this corresponds to 40kBit/s Manchester coding and 80kBit/s NRZ coding)	2, 5	F_{MOD_FSK}	0		40	kHz	B
4.7	ASK modulation frequency	Duty cycle of the modulation signal = 50%, (this corresponds to 40kBit/s Manchester coding and 80kBit/s NRZ coding)	2, 5	F_{MOD_ASK}	0		40	kHz	B
4.8	Spurious emission	At $f_{RF} \pm f_{XTO}$ / 8 At $f_{RF} \pm f_{XTO}$ / 4 At $f_{RF} \pm f_{XTO}$	5	Spur		–47 –47 –60		dBc	B
4.9	Spurious emission	DIV_CNTRL = “High” At $f_{RF} \pm f_{XTO}$ / 4 At $f_{RF} \pm f_{XTO}$	5	Spur		–47 –58		dBc	B
4.10	Spurious emission	CLK_ON = “Low” At $f_0 \pm f_{XTO}$	5	Spur		–60		dBc	B
4.11	Fractional Spurious	ASK_NFSK = “High” TX_Mode_2 FREQ[0:14] = 3730, FSEP[0:7] = 101 S434_N315 = “Low” f_{RF} ±3.00MHz f_{RF} ±6.00MHz FREQ[0:14] = 14342, FSEP[0:7] = 101 S434_N315 = “High” f_{RF} ±3.159MHz f_{RF} ± 9.840MHz	5	Spur		–50 –50 –50 –50		dBc	B
4.12	FSK frequency deviation	f_{XTO} = 13.0000MHz other f_{XTO} see Table 3-1 on page 4	5	f_{dev}	±0.396 $\left(f_{XTO}/32768\right)$		±101.16 $\left(f_{XTO}/128.5\right)$	kHz	A
4.13	Frequency resolution	f_{XTO} = 13.0000MHz other f_{XTO}		Δf_{PLL}		793 $\left(f_{XTO}/16384\right)$		Hz	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: (Pin Number) in brackets mean they are measured matched to 50Ω according to Figure 4-2 on page 8 with component values and optimum load impedances according to Table 4-1 and Table 4-2 on page 9

11. Timing Characteristics (Atmel ATA5749)

V_S = 1.9V to 3.6V, T_{amb} = –40°C to +125°C. Typical values are given at V_S = 3.0V and T_{amb} = 25°C. All parameters are referred to GND (pin 9). Parameters where crystal relevant parameters are important correspond to a crystal with C_M = 4.0fF, C_0 = 1.5pF, C_{LOAD} = 9pF and $R_M \leq 170\Omega$ unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	EN set-up time to rising edge of SCK		1, 10	T_{EN_setup}	10			µs	C
1.2	SDIN_TXDIN set-up time to falling edge of EN		2, 10	$T_{SDIN_TXDIN_setup}$	125			ns	C
1.3	SDIN_TXDIN set-up time to rising edge of SCK		2, 3	T_{Setup}	10			ns	C
1.4	SDIN_TXDIN hold time from rising edge of SCK		2, 3	T_{Hold}	10			ns	C
1.5	SCK Cycle time		3	T_{SCK_Cycle}	500			ns	C
1.6	SCK high time period		3	T_{SCK_High}	200			ns	C
1.7	SCK low time period		3	T_{SCK_Low}	200			ns	C
1.8	EN low time period with SDIN_TXDIN = “High” for register reset		2, 10	T_{EN_Reset}	10			us	C
1.9	Clock output frequency (CMOS microcontroller compatible)	f_{XTO} = 13.000MHz DIV_CNTRL = “High” ($f_{CLK} = f_{XTO} / 4$) DIV_CNTRL = “Low” ($f_{CLK} = f_{XTO} / 8$)	1	f_{CLK}		3.25 1.625		MHz	A
1.10	Clock output minimum “High” and “Low” time	Cload ≤ 20pF, DIV_CNTRL = “Low” ($f_{clk} = f_{XTO} / 8$) “High” = 0.8 × V_S, “Low” = 0.2 × V_S, f_{CLK} < 1.625MHz	1	T_{CLKLH}	125	220		ns	A
1.11	Clock output minimum “High” and “Low” time	Cload ≤ 10pF, DIV_CNTRL = “High” ($f_{clk} = f_{XTO} / 4$) “High” = 0.8 × V_S, “Low” = 0.2 × V_S, f_{CLK} < 3.25MHz	1	T_{CLKLH}	62.5	110		ns	A
1.12	Clock output minimum “High” and “Low” time	Cload ≤ 20pF, DIV_CNTRL = “Low” ($f_{clk} = f_{XTO} / 8$) “High” = 0.8 × V_S, “Low” = 0.2 × V_S, f_{CLK} < 1.85MHz	1	T_{CLKLH}	125	180		ns	C
1.13	Clock output minimum “High” and “Low” time	Cload ≤ 10pF, DIV_CNTRL = “High” ($f_{clk} = f_{XTO} / 4$) “High” = 0.8 × V_S, “Low” = 0.2 × V_S, f_{CLK} < 3.7MHz	1	T_{CLKLH}	62.6	90		ns	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

12. Digital Port Characteristics

V_S = 1.9V to 3.6V, T_{amb} = 40°C to +125°C unless otherwise specified. Typical values are given at V_S = 3.0V and T_{amb} = 25°C, all inputs are Schmitt trigger interfaces.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	SDIN_TXDIN	“Low” level input voltage “High” level input voltage Internal pull-down resistor		V_{Il} V_{ih} R_{PDN}	0 V_S – 0.25 160	 250	0.25 V_S 380	V V kΩ	A
1.2	SCK	“Low” level input voltage “High” level input voltage Internal pull-down resistor		V_{Il} V_{ih} R_{PDN}	0 V_S – 0.25 160	 250	0.25 V_S 380	V V kΩ	A
1.3	EN input	“Low” level input voltage “High” level input voltage Internal pull-down resistor		V_{Il} V_{ih} R_{PDN}	0 V_S – 0.25 160	 250	0.23 V_S 380	V V kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

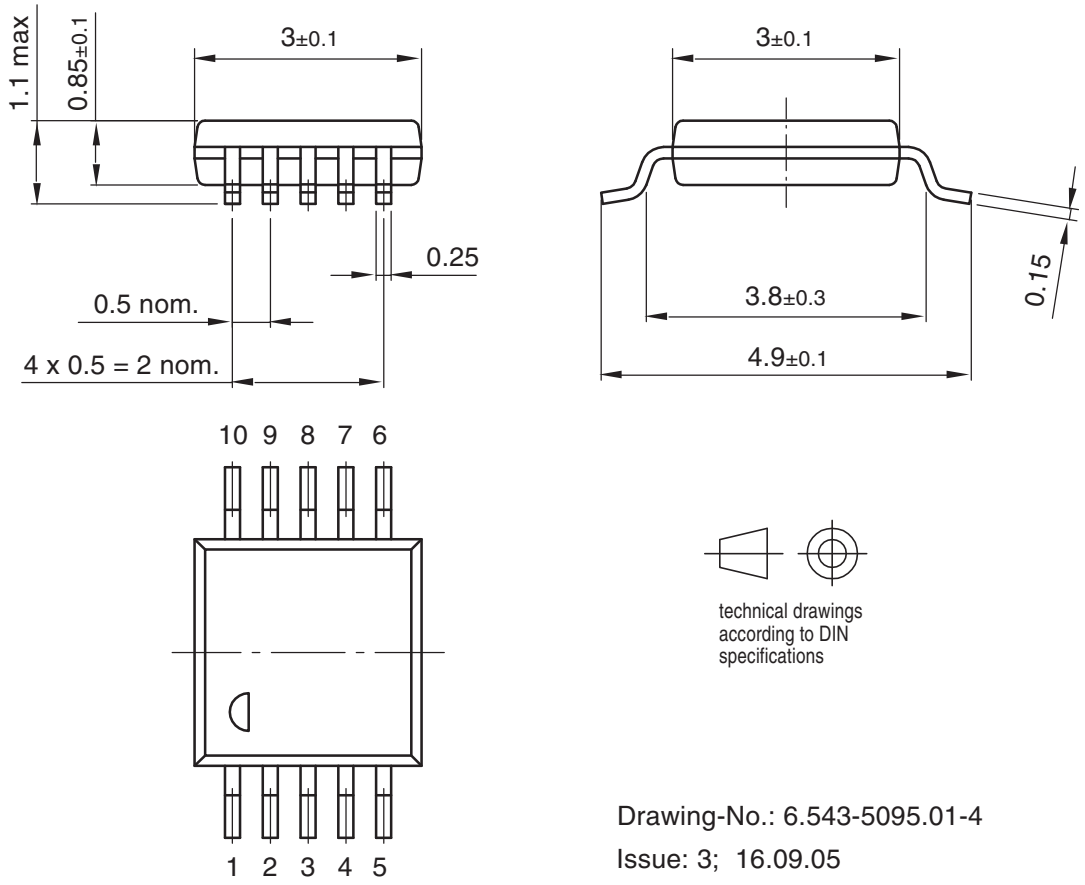
13. Ordering Information

Extended Type Number	Package	Remarks
ATA5749-6DQY	TSSOP10	-
ATA5749C-6DQY	TSSOP10	-

14. Package Information

Package: TSSOP 10
(acc. to JEDEC Standard MO-187)

Dimensions in mm
Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5095.01-4
Issue: 3; 16.09.05

15. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9128H-RKE-08/11	• Section 13 “Ordering Information” on page 24 changed
9128G-RKE-03/11	• ATA5749C on page 1 added • Section 13 “Ordering Information” on page 24 changed
9128F-RKE-09/10	• Page 9: Table 4-1 changed • Page 9: Table 4-2 changed
9128E-RKE-09/10	• El. Char. table: rows 1.2, 1.3, 1.4, 1.7, 1.8, 1.9, 2.1, 2.2, 2.4, 2.5 changed • Dig. Port Char. table: row 1.3 changed • Ordering table changed
9128D-RKE-01/09	• Features on page 1 changed • Section 8 “Absolute Maximum Ratings” on page 17 changed
9128C-RKE-10/08	• Features on page 1 changed • Section 8 “Absolute Maximum Ratings” on page 17 changed • Section 12 “Digital Port Characteristics” on page 23 changed
9128B-RKE-08/08	• Put datasheet in the newest template • Features on page 1 changed • Section 1 “Description” on page 1 changed • Figure 1-1 “Block Diagram” on page 2 changed • Section 3.1 “Fractional-N PLL” on page 4 changed • Section 3.4 “Clock Driver” on page 6 changed • Figure 4-1 “Typical Application Circuit” on page 7 changed • Figure 4-2 “Output Power Measurement Circuit” on page 8 changed • Section 10 “Electrical Characteristics” numbers 4.2, 4.12 and 4.13 on pages 20 to 21 changed

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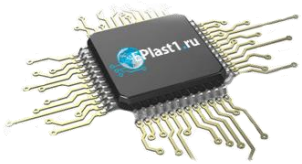
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