MLX75023 Time-of-Flight Sensor Array

Product Datasheet

Features & Benefits

- 1/3” optical Time-of-Flight sensor (optical area = 4.8 x 3.6 mm^2)
- QVGA resolution, 320 x 240 pixels
- 15 x 15 µm DepthSense® pixels
- Demodulation frequency up to 40 MHz
- Two dual channel analog outputs
- < 600 raw correlation frames per second (typ. settings : 25 MS/s, Tint = 130 µs)
- Typical system background light robustness according to Table 1
- Integrated optical filter (>80% transmission in range 800-900nm)
- Ambient operating temperature ranges of -20 +85°C and -40 +105°C
- Wafer level glass BGA package (Dimensions : 6.6 x 5.5 x 0.6 mm)
- AEC-Q100 qualification available!

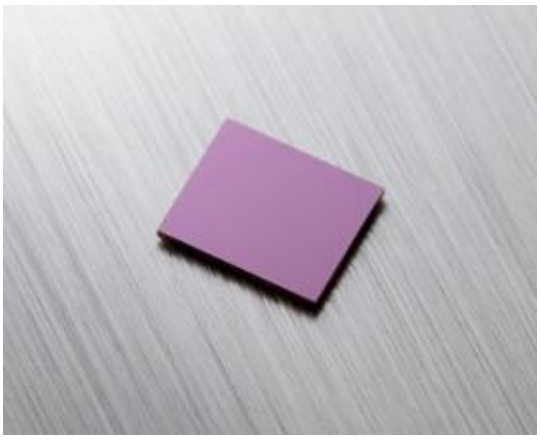

Figure 1: MLX75023

Description

MLX75023 is a fully integrated optical time-of-flight (TOF) camera sensor. Potential use cases include gesture recognition, automotive driver monitoring, surveillance & people counting, robot vision & more. The sensor features 320 x 240 (QVGA) time-of-flight pixels based on DepthSense® pixel technology. This unique design allows up to 120 klux background light rejection in typical application conditions. The sensor features high-speed analog signal outputs which enable a raw frame rate of up to 600 frames per second. The sensor offers maximum compatibility with MLX75123, Melexis’ dedicated TOF companion chip. Combined with a modulated light source, a system is capable of measuring distance and reflectivity at full resolution. The sensor is available in automotive and industrial grades, both in a small glass BGA wafer level package form factor which offers many integration possibilities.

Illumination	Modulation Frequency	QVGA Mode	QQVGA Binning Mode
LED	20 MHz	> 40 klux	> 120 klux
Laser	20 MHz	> 60 klux	> 120 klux

Table 1: Typical TOF system background light robustness

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1. Datasheet Change Log

Version	Date	Changes
1.1 - 1.13	2014-2016	Internal release(s)
1.14	17.1.2017	Document updated to the new Melexis template Added industrial product variant with code S Add chief ray angle and bad pixel count limit and definition Added test row and test column specifications Updated electrical specifications Other miscellaneous, minor improvements
1.15	18.4.2018	BAB-00x variants recommended for new designs in section 2 Renamed CRA to max. light acceptance angle in section 6.7 Added relative sensitivity in function of incident light angle graph in section 6.7 Updated ArrayBias description in section 6.5 Added Package Marking Information section 9.2
1.16	09.01.2019	Updated disclaimer Removed BAA-00x variants. Parts only available to selected customers. Added pixel (0, 0) location in Figure 12 Updated Table 13 Added external quantum efficiency parameter, replacing responsivity & fill factor Updated typical full well capacity to 240 ke- Added conversion gain parameter Removed pixel capacitance parameter Added Figure 5, typical demodulation contrast
1.17	18.06.2019	Corrected document reference links
1.18	08.11.2019	Added note about cover tape lifetime.

Table 2: Change log

2. Ordering Information

Product	Temperature Code	Package	Option Code	Packing Form
MLX75023	R	TF	BAB-000	TR
MLX75023	R	TF	BAB-001	TR
MLX75023	S	TF	BAB-000	TR
MLX75023	S	TF	BAB-001	TR

Table 3: Product ordering code(s)

Legend:

Temperature Code (see section 11)	R : -40°C to 105°C S : -20°C to 85°C
Package Code	TF : Glass BGA Package, 44pins
Option Code	BAB-000 : without covertape BAB-001 : with cover tape[1] (see section 9.1)
Packing Form	TR : Tray
Ordering Example	MLX75023RTF-BAB-001-TR

Table 4: Option code(s)

[1] The properties of the covertape are guaranteed for one year after shipping date considering the devices are stored in appropriate conditions according the device MSL rating.

3. Application System Architecture

A complete TOF system or camera module typically includes the following main components :

- MLX75123 + MLX75023 TOF chipset
- A synchronized high bandwidth near infrared (NIR) active illumination source (LED or laser)
- Beam shaping optics for the light distribution
- A receiving sensor lens, optimized for maximum NIR transmittance
- A microprocessor with parallel video input port, to calculate and process the data

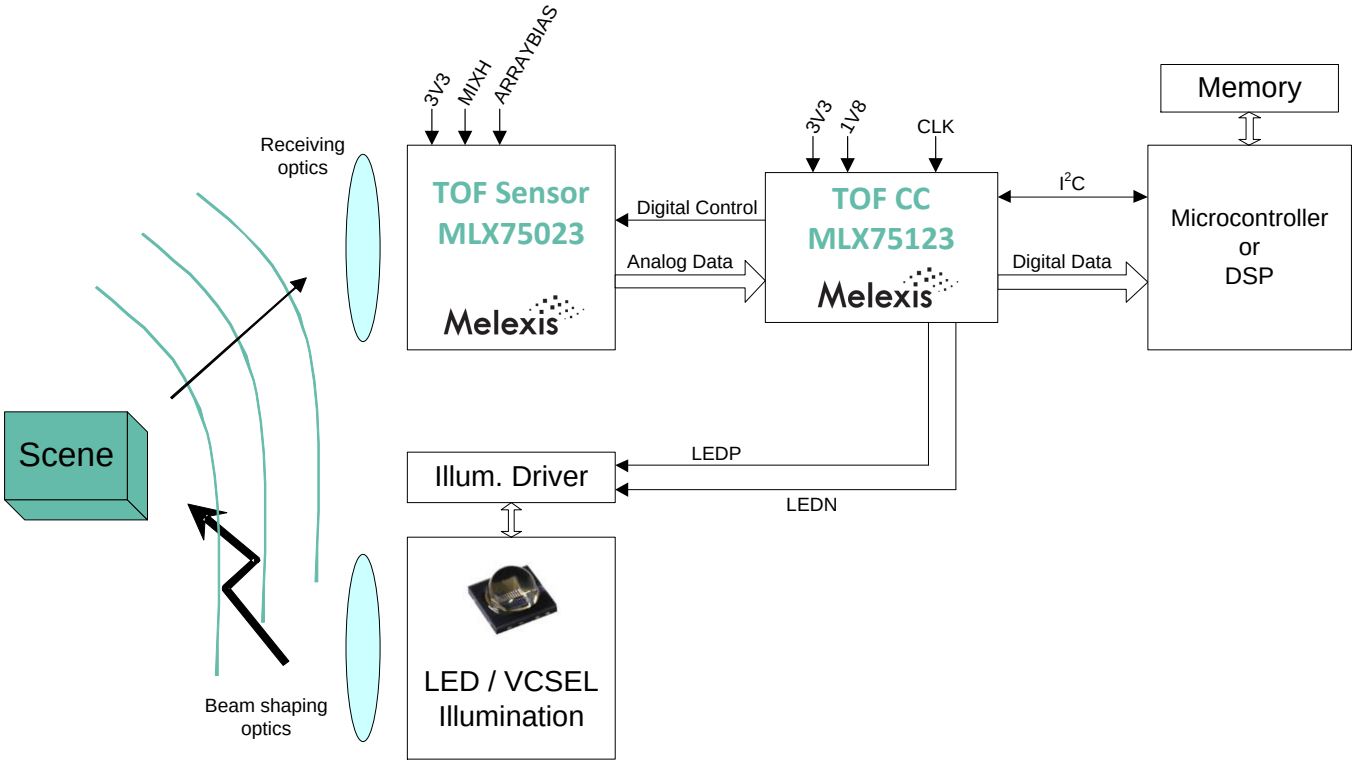

Figure 2: System architecture

4. Pinout Description

Designator	Pin #	Function	Domain
ROW[7] ROW[6] ROW[5] ROW[4] ROW[3] ROW[2] ROW[1] ROW[0]	1 2 3 4 5 6 7 8	Dynamic Digital Input	3V3
LATCH_ENABLE	9	Dynamic Digital Input	3V3
GND	10	Ground	GND
OUT3	11	Analog Output	
OUT2	12	Analog Output	
PIXELBIAS	13	Voltage Bias	GND
OUT0	14	Analog Output	
GND	15	Ground	GND
OUT1	16	Analog Output	
ARRAYBIAS	17	Voltage Bias	ARRAYBIAS
AVDD	18	Analog Supply	3V3
PIXELFLUSH	19	Dynamic Digital Input	3V3
CORE_RESET	20	Dynamic Digital Input	3V3
PIXELVDD	21	Pixel Supply	3V3
AVDD	22	Analog Supply	3V3
COLUMN[7] COLUMN[6] COLUMN[5] COLUMN[4] COLUMN[3] COLUMN[2] COLUMN[1] COLUMN[0]	23 24 25 26 27 28 29 30	Dynamic Digital Input	3V3
SHUTTER	31	Dynamic Digital Input	3V3
GND	32	Ground	GND
DVDD	33	Digital Supply	3V3
DMIX[1] DMIX[0]	34 35	Dynamic Digital Input	3V3
GND	36	TOF Ground	GND
MIXH	37	TOF Supply	VMIX
MIXH	38	TOF Supply	VMIX
GND	39	TOF Ground	GND
GND	40	TOF Ground	GND
MIXH	41	TOF Supply	VMIX
MIXH	42	TOF Supply	VMIX
GND	43	TOF Ground	GND
DVDD	44	Digital Supply	3V3

Table 5.1: MLX75023 Pinout

5. Typical Connection Diagram

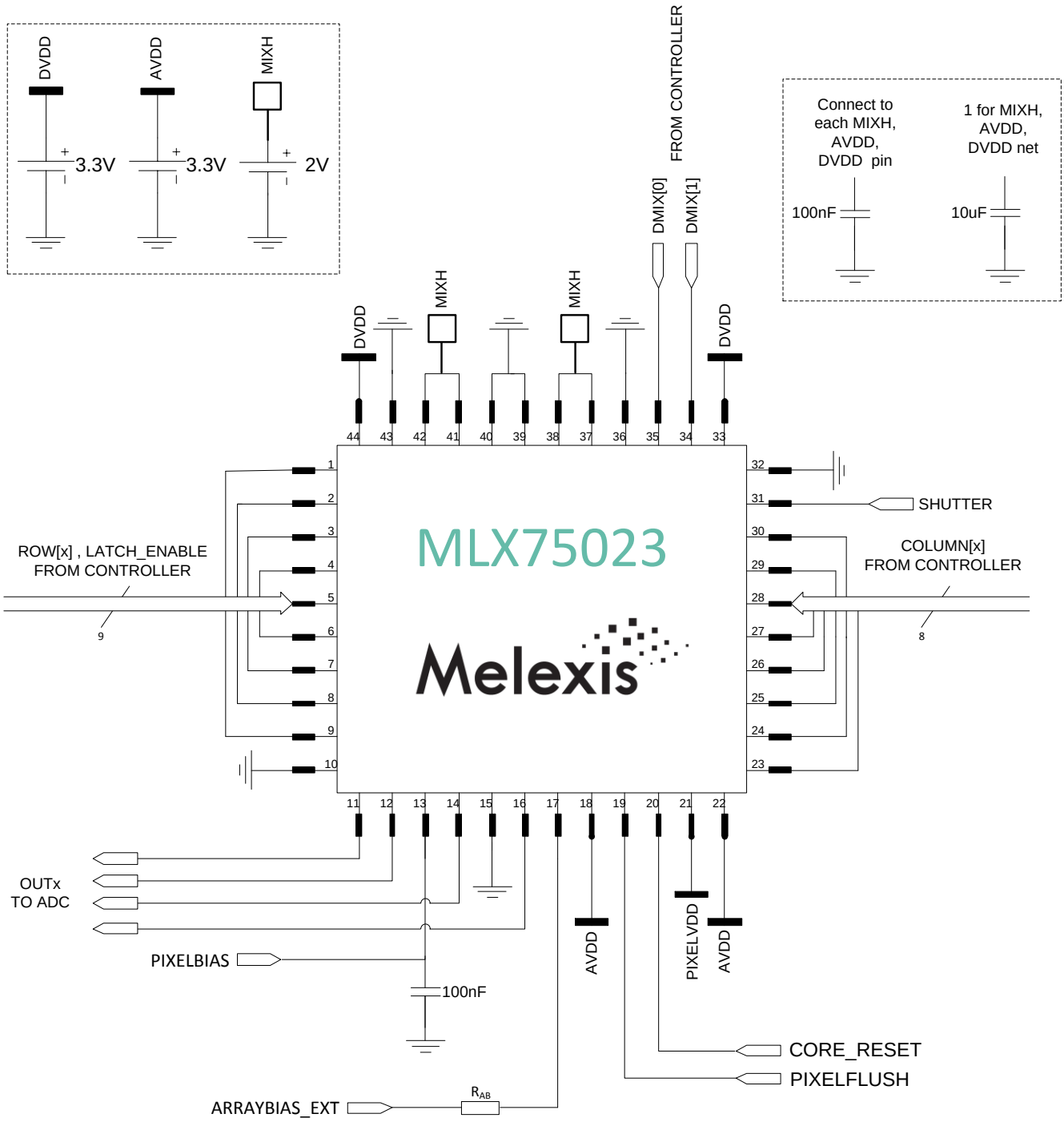

Figure 3: Typical connection diagram

6. Electrical Characteristics

6.1. Absolute Maximum Ratings[2]

Parameter	Symbol	Min.	Typ.	Max.	Unit
3V3 supply voltage range	$V_{DD_33_x}$	-0.3	3.3	3.6	V
3V3 DC input voltage		-0.3		V_{DD_33} + 0.3	V
3V3 DC input current	I_{N33}		60		µA
MIXH input voltage	V_{MIXH}	-0.3		2.5	V
MIXH DC input current	I_{MIXH}			2	A
Storage temperature	T_{stg}	-50		125	°C
Power dissipation (dc equiv.) [1]	P_{tot}			0.4	W
Junction temperature	T_{jnt}			125	°C

Table 6: Absolute maximum ratings[2]

[1] The maximum power dissipation depends on the ambient-to-silicon thermal resistance. The sensor package, connected to a PCB by its solder balls (standard mounting) has a thermal resistance of 50 K/W. Under these conditions, the maximum power dissipation is 0.4 watt. With improved thermal connection of the sensor backside to the PCB, the thermal resistance can typically decrease by factor 2 or more (depending on the thermally conductive material and the contacting process), thereby allowing a correspondingly higher power dissipation.

[2] Absolute maximum ratings must not be exceeded to prevent permanent damage to the device.
The device is not guaranteed to be functional while applying the absolute maximum stress.

6.2. Electrical Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
AVDD supply voltage	V_{AVDD}	3.0	3.3	3.6	V
AVDD supply current	I_{AVDD}		40		mA
DVDD supply voltage	V_{DVDD}	3.0	3.3	3.6	V
DVDD current (idle)	I_{DVDD_IDLE}		0.5		mA
DVDD supply current (100% MIX activity, 60MHz fmix)	I_{DVDD_IDLE}		70		mA
PIXELVDD supply voltage	$V_{PIXELVDD}$	3.2	3.3	3.6	V
PIXELVDD supply current	$I_{PIXELVDDD}$		4		mA
ARRAYBIAS supply voltage	$V_{ArrayBias}$	-15	-3	0	V
Peak ARRAYBIAS current	$I_{ArrayBias}$		15	100	mA
PIXELBIAS voltage	$V_{PixelBias}$		0		V
PIXELBIAS current	$I_{PixelBias}$		50		uA
Operating temperature (ambient)	T_A	-40		105	°C
MIXH supply voltage	V_{MIXH}	1.0	1.5	2.5	V
MIXH supply current (100% MIX activity, VMIXH = 1.5V, T_a = -40°C)	$I_{MIXH@1.5V}$		1400	1900	mA
MIXH supply current (100% MIX activity, VMIXH = 1.5V, T_a = 25°C)	$I_{MIXH@1.5V}$		1200	1900	mA
MIXH supply current (100% MIX activity, VMIXH = 1.5V, T_a = 105°C)	$I_{MIXH@1.5V}$		1050	1900	mA
MIXH supply current (100% MIX activity, VMIXH = 2V, T_a = -40°C)	$I_{MIXH@2V}$		1735	2000	mA
MIXH supply current (100% MIX activity, VMIXH = 2V, T_a = 35°C)	$I_{MIXH@2V}$		1398	2000	mA

Table 7: Electrical operation conditions

6.3. Digital IO Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	2.5		V_{DD_33} + 0.3	V
Input low voltage	V_{IL}			0.8	V
Input current (pull-down R)	$I_{DINDOWN}$		65		µA
Input current (pull-up R)	I_{DINUP}		65		µA
Input pin capacitance			1		pF

Table 8: Digital IO characteristics

6.4. Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Column addressing frequency	f_{COL}	10	25	50 [1]	MHz
Row addressing frequency	f_{ROW}			1	MHz
Pixel address to analog output valid	t_{VAL}	40			Ns
OUTx output swing	$RANGE_{OUT}$		0.9		V
OUTx output voltage		0.2		1.9	V
OUTx load capacitance				15	pF
DMIX frequency	f_{MIX}		20	40	MHz

Table 9: Dynamic characteristics

[1] Column addressing above 25 MHz can create image artefacts due to settling errors.
These errors can be avoided with an alternative, but more complicated, timing diagram than explained in section 7.1

6.5. ArrayBias

ARRAYBIAS requires a negative current to improve the pixel demodulating efficiency. It's recommended to supply ARRAYBIAS via a series resistor (= ARRAYBIAS_EXT) to reduce the device self-heating. This is also shown in Figure 3.

Parameter	Conditions	Min.	Typ.	Max.	Unit
ARRAYBIAS voltage		-15	-3	0	V
ARRAYBIAS current	-3V, R_{AB} = 0 Ω		15	75	mA

Table 10: MLX75023xTF-BAA-00x-TR ARRAYBIAS Conditions

Parameter	Conditions	Min.	Typ.	Max.	Unit
ARRAYBIAS_EXT voltage		-5	-3.3	-3	V
ARRAYBIAS_EXT current	-3.3V, R_{AB} = 330 Ω			10	mA
R_{AB} series resistor		300	330	500	Ω

Table 11: MLX75023xTF-BAB-00x-TR[1] ARRAYBIAS_EXT & R_{AB} Conditions

Note[1]: Recommended for new designs

6.6. Sensor Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal resolution	h		320		pixels
Vertical resolution	v		240		pixels
Pixel pitch	pp		15		µm
CAPD architecture			Two-tap differential		

Table 12: Sensor physical characteristics

6.7. Optical & TOF Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
External Quantum Efficiency[2] @850 nm	EQE_{850}	7.7%	9.7%		%
AC contrast @ 15 MHz	C_{AC_15MHz}	80	89		%
Single tap full well capacity			240		ke^-
Pixel conversion gain	C_GAIN		3.9		uV/e-
Noise floor	η_e		100		e^-
max. light acceptance angle				35	°
Bad pixel count[1]				28	px

Table 13: Optical & TOF characteristics

[1] A bad pixel is defined as a pixel with a demodulation contrast <80% or a low responsivity compared to other pixels.
[2] The external quantum efficiency is calculated as $FF.R.E_{ph}/e.$, where *FF* is pixel fill factor, *R* is responsivity in A/W, E_{ph} is photon energy in Joule and *e* is a unit charge in Coulomb.

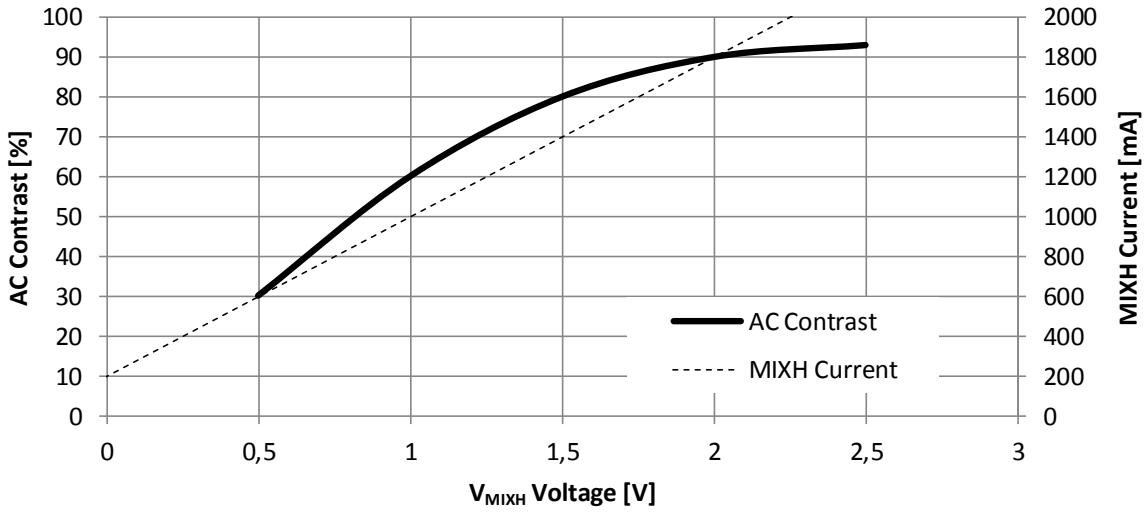

Figure 4: Typical AC demodulation contrast at 15 MHz & the estimated max. MIXH current in function of VMIXH voltage with 0V ARRAYBIAS and 0V PIXELBIAS

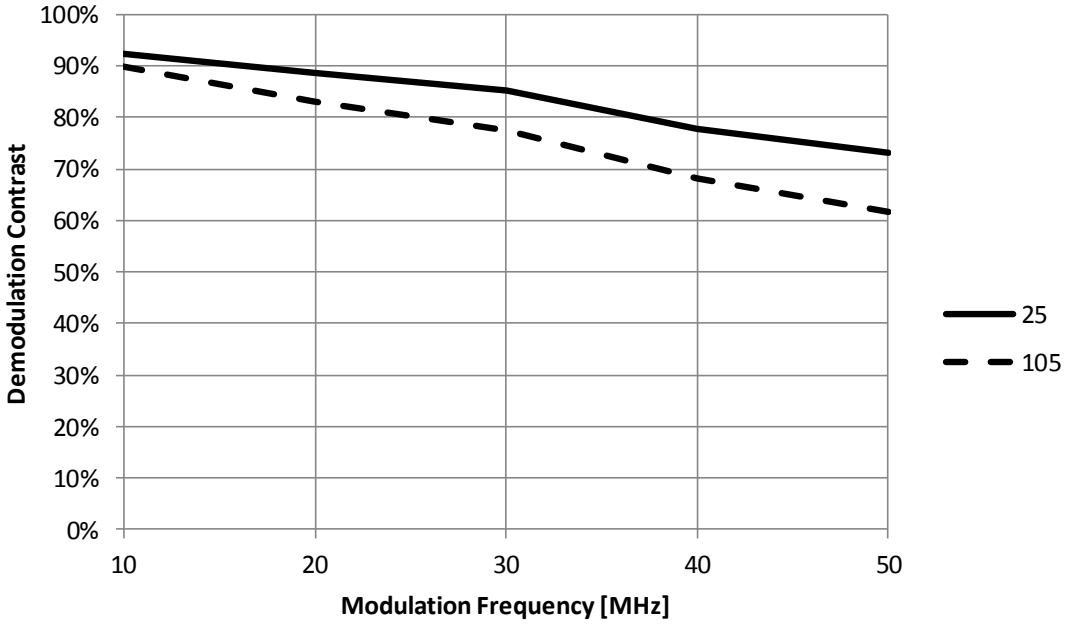

Figure 5: Typical AC demodulation contrast versus modulation frequency
at T_a 25°C and 105°C, 1.5V VMIXH, 0V PIXELBIAS, -3.3V ARRAYBIAS_EXT, 330 Ohm R_{AB}

Due to the pixel layer stack design, incident light rays under an angle might generate a minor shadow on the sensitive pixel area and as a consequence will result in lower pixel sensitivity. The effect is visualized in the figure below and can be minimized on application level with optical lens design.

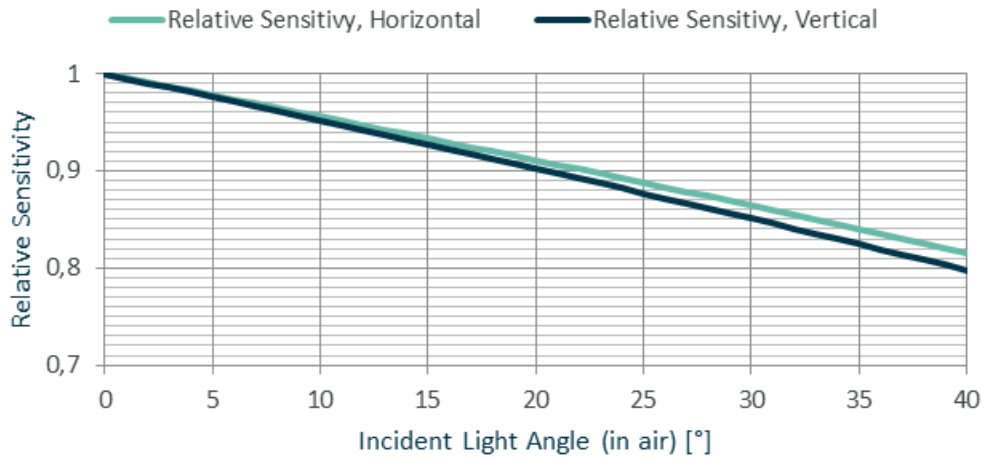

Figure 6: Typical pixel sensitivity as a function of incident light angle, relative to normal incidence.

7. Interface

7.1. Timing Diagram

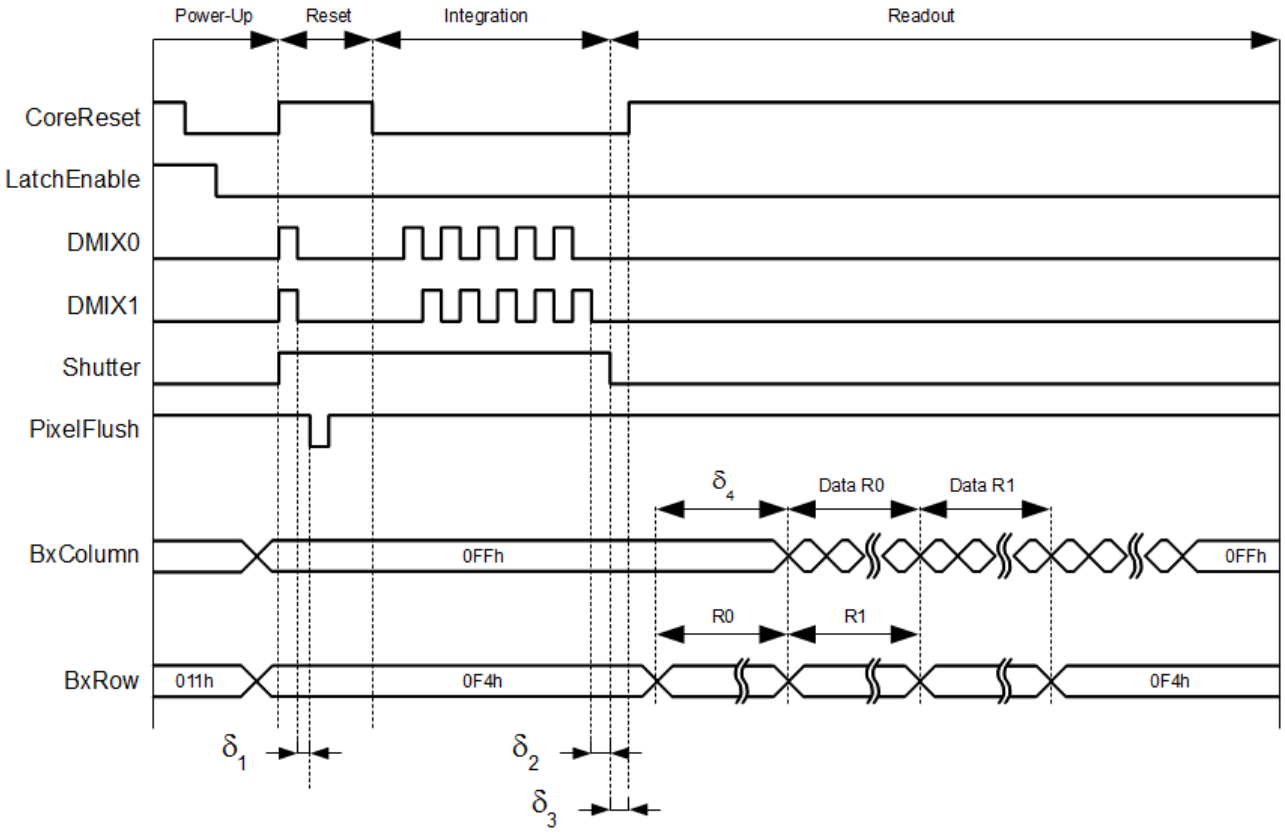

Figure 7: Global shutter timing δ1 ≥ 0.1us, δ2 ≥ 0.1us, δ3 ≥ 1us, δ4 ≥ 1us.
Each cycle consists of a reset phase, an integration phase and a read-out phase.

7.1.1. Power Up

The power up phase should last at least for 10us after the supply reached the nominal value, after which the internal latches can be programmed. To initiate normal operating mode, a code of 0x11 should be applied to the ROW[X] bus at the falling edge of the LATCH_ENABLE signal (for details see Section 7.2).

7.1.2. Reset

The reset is organized in 3 steps. CORE_RESET is HIGH during all three steps.
The electronic shutter should be opened by setting SHUTTER to HIGH.

- Step 1 : Substrate flush
  During step 1 mix signals DMIXx are pulled HIGH for at least 100 ns.
  The step ends by pulling DMIXx terminal LOW.

- Step 2 : Pixel flush
  The second phase implements a flushed reset by switching PIXELFLUSH low during the first 5 us of CORE_RESET HIGH.

- Step 3 : Reset
  The 3rd phase of the reset period lasts another 5 us, where the PIXELFLUSH is asserted.
  During the 2nd and 3rd phase of the reset, DMIXx states should be LOW.

7.1.3. Integration

After the reset cycle, the integration cycle is started. The electronic shutter should be kept open (keep SHUTTER HIGH). The mix signals DMIX0/1 are alternated using the Time-of-Flight modulation pattern. When the integration is completed, the mix signals DMIX0/1 should be again put in idle state LOW. The electronic shutter can be closed by setting SHUTTER to LOW.

7.1.4. Read-out

Reading out the sensor is done by toggling both Row and Column address. Both addresses have 8 bit width.
The Row binary word is directly mapped to the row number. The column binary word is toggled from 00h to 09Fh (0 to 159).

When row 0 is addressed the data from the pixels in row 0 is stored on a column-level memory Mem0.
After this, row 1 is addressed and the data from the pixels in row 1 is stored in a second column-level memory Mem1. Simultaneously, after row 0 to row 1 transition, the data from row 0 previously stored in Mem0 can be read at the outputs OUT0 to OUT3 by selecting the columns sequentially. The Mem0-Mem1 shadow buffer switching is controlled by the B0_ROW signal; when reading out the matrix the B0_ROW signal must change its state every row.

When selecting column 0, OUT0 and OUT3 offer the data from pixel 0, while OUT1 and OUT2 offer the data from pixel 8. As such, the data is read out in blocks of 8. (Pixel 0 is located in the bottom right corner as indicated in the mechanical dimensions drawing of Section 9.1)
When selecting column 1, OUT0/3 offer the data from pixel 1, while OUT1/2 offer the data from pixel 9.
When selecting column 8, OUT0/3 offer the data from pixel 16, while OUT1/2 offer the data from pixel 24.
As such when selecting column N, the data at
OUT0/3 is coming from pixel (N MOD 8) + 16*FLOOR(N/8)
OUT1/2 is coming from pixel (N MOD 8) + 16*FLOOR(N/8) + 8

Parameter	OUT0/3 : Pixel #	OUT1/2 : Pixel #
0	0	8
1	1	9
…	…	…
6	6	14
7	7	15
8	16	24
9	17	25
…	…	…
15	23	31
16	32	40
17	33	41
…	..	…

Table 14: Read-out table

7.2. Device Control

LATCH_ENABLE allows to program latches which control the general behaviour of the circuitry.
During latch enable the B0-7_ROW inputs are the latch inputs.

LATCH_ENABLE = 1	Name	Function	Configuration	Typical Value
B0_Row	PUP	Power-up of bandgap and bias	1 = Power-up 0 = Power-down	1
B1_Row	coltest_i	Multiplexes the 4 test columns on the 4 last columns of the array	1 = Testcolumns active 0 = Testcolumns inactive	0
B4_Row	PDN_sw	Power-down of output amplifiers	1 = Power-up 0 = Power-down	1

Table 15: System control

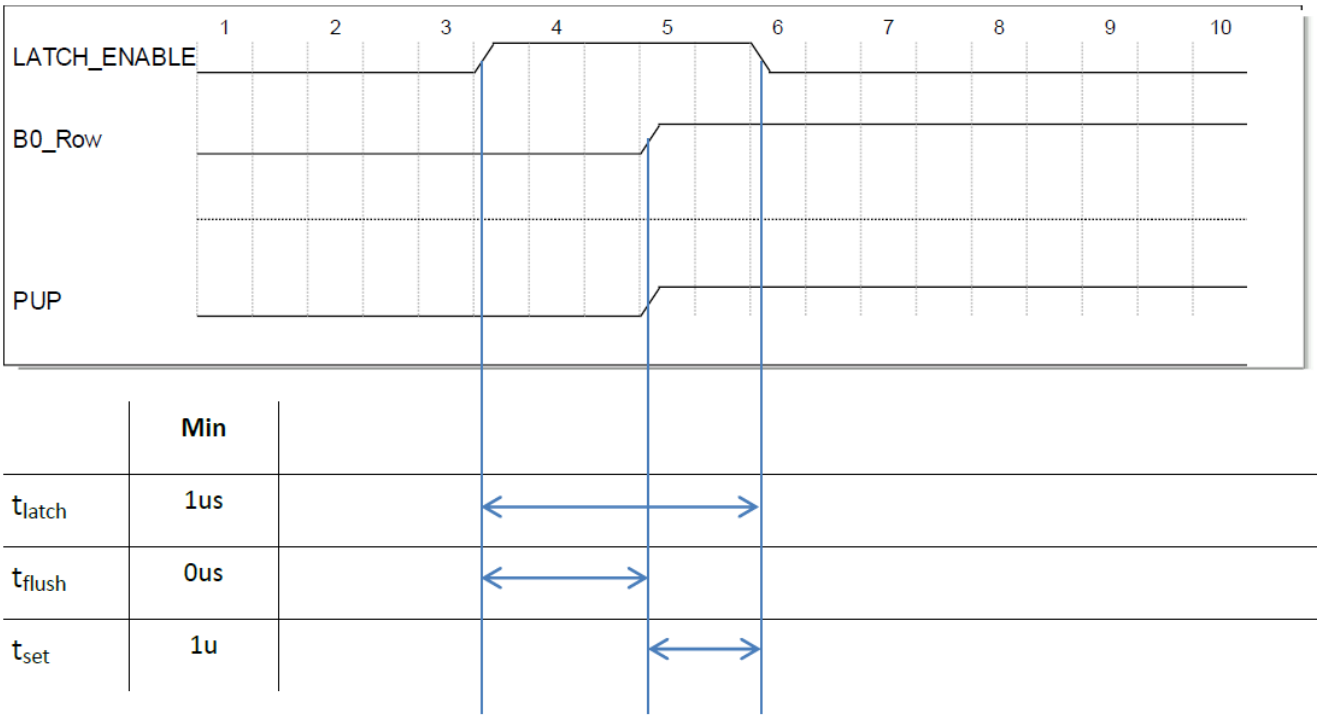

Figure 8: Device control

7.3. Test Column Specification

MLX75023 has built in test columns (four) that can be used to debug the analog to digital conversion as described in section 7.2. The test columns can be enabled by reprogramming the LATCH_ENABLE at sensor startup. The test columns contain a chess pattern with min. & max. values as shown in Figure 9 :

Figure 9: Raw tap A phase0 image of a hand with enabled test columns

RowNo. ROW[7:0]	Col 316 Tap A	Col 317 Tap A	Col 318 Tap A	Col 319 Tap A	Col 316 Tap B	Col 317 Tap B	Col 318 Tap B	Col 319 Tap B
0	ROW[7]	ROW[5]	ROW[3]	ROW[1]	ROW[6]	ROW[4]	ROW[2]	ROW[0]
1	ROW[7]	ROW[5]	ROW[3]	ROW[1]	ROW[6]	ROW[4]	ROW[2]	ROW[0]
…	…	…	…	…	…	…	…	…
239	ROW[7]	ROW[5]	ROW[3]	ROW[1]	ROW[6]	ROW[4]	ROW[2]	ROW[0]
240	ROW[7]	ROW[5]	ROW[3]	ROW[1]	ROW[6]	ROW[4]	ROW[2]	ROW[0]

Table 16: Test column description

7.4. Test Row Specification

On top of the four test columns as described in section 7.3 MLX75023 also has eight test rows. They have a similar chess pattern and can be used to debug the system. The test rows are always enabled and can be read-out and addressed like any other pixel row.

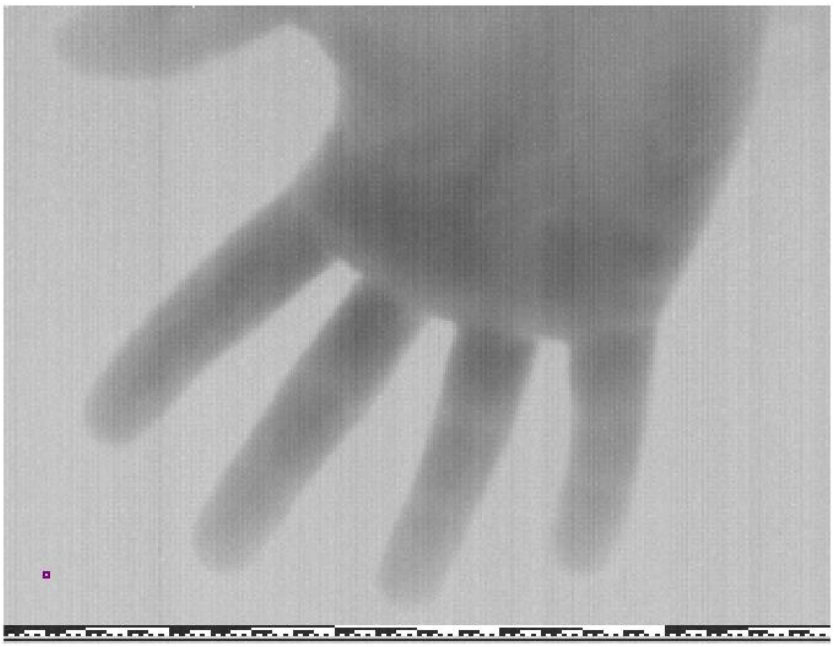

Figure 10: Raw tap A phase180 image of a hand with the test rows enabled

RowNo.		Col 0 (dec 0)	Col 1 (dec 1)	…	Col 255 (dec 255)	Col 256 (dec 0)	Col 257 (dec 1)	…	Col319 (dec 63)
240	Tap A	COL[7]	COL[7]	…	COL[7]	COL[7]	COL[7]	…	COL[7]
241	Tap A	COL[5]	COL[5]	…	COL[5]	COL[5]	COL[5]	…	COL[5]
242	Tap A	COL[3]	COL[3]	…	COL[3]	COL[3]	COL[3]	…	COL[3]
243	Tap A	COL[1]	COL[1]	…	COL[1]	COL[1]	COL[1]	…	COL[1]
240	Tap B	COL[6]	COL[6]	…	COL[6]	COL[6]	COL[6]	…	COL[6]
241	Tap B	COL[4]	COL[4]	…	COL[4]	COL[4]	COL[4]	…	COL[4]
242	Tap B	COL[2]	COL[2]	…	COL[2]	COL[2]	COL[2]	…	COL[2]
243	Tap B	COL[0]	COL[0]	…	COL[0]	COL[0]	COL[0]	…	COL[0]

Table 17: Test row description

8. Noise Considerations

The noise limitation of the MLX75023 under high background illumination is typically the shot noise coming from the DC background light. Under low background light conditions the lowest theoretical noise floor is the thermal noise coming from the in-pixel reset switch, this noise is also known as kT/C ("kT over C") noise. The reset kT/C noise is the minimum achievable noise level under low light conditions if the sample and hold (S/H) signal ("Shutter") is not used.

If the system designer implements the default timing as shown in Figure 7.1 the thermal noise of the in-pixel sample and hold switch also contributes to the pixel's noise floor.

The typical pixel noise RMS values are given below:

Pixel noise floor (reset kT/C noise):	340uV
Pixel noise floor in shutter mode (reset and S/H kT/C noise):	410uV
Pixel shot noise (@ 0.9V total signal):	2mV

The noise of the data acquisition system should be lower than the pixel's intrinsic noise.

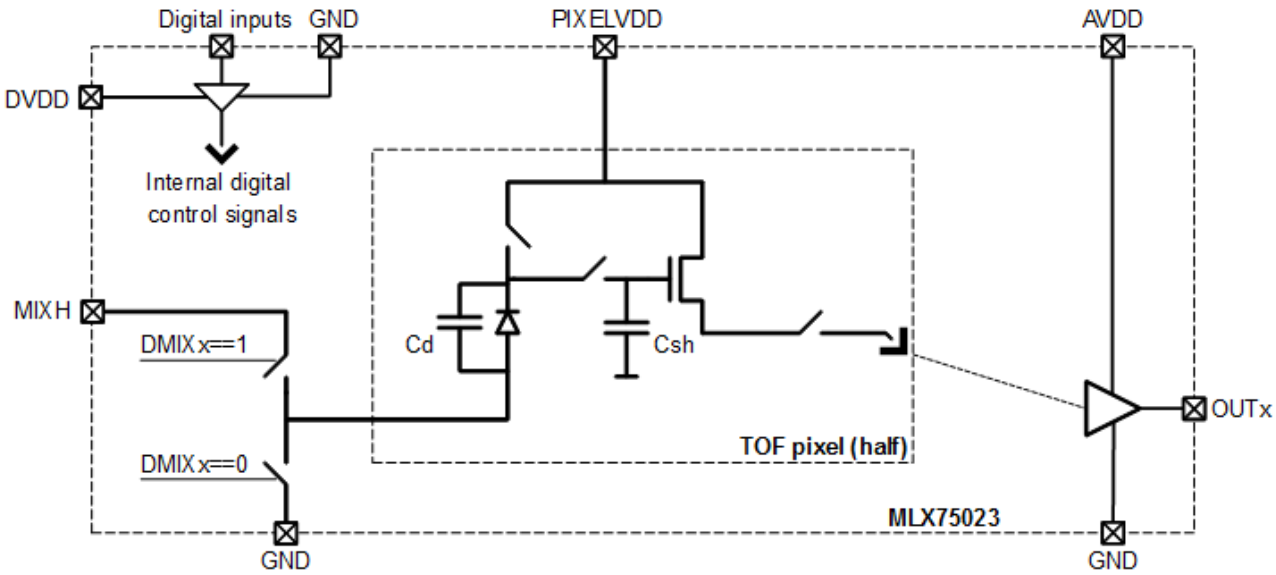

Figure 11: Electrical model of one phase output of the pseudo differential TOF pixel

The architecture of MLX75023 comprises pseudo differential signal paths for the pixel output counter-phase signals, it is highly recommended to implement a simultaneous sampling of OUT0/OUT3 and OUT1/OUT2 signals to reduce the common mode noise coupling from the chip power supply and biases (PIXELBIAS). The supply voltage ripple (AVDD, DVDD) and PIXELBIAS voltage ripple during the CORE_RESET signal falling edge, SHUTTER signal falling edge and data sampling time instants should not exceed ~10 times the pixel noise. It is also recommended that separate, decoupled supply routing of AVDD and PIXELVDD is implemented. AVDD and DVDD could share the same supply routing.

If MLX75023 is operated in a single ended mode it is important to guarantee that the voltage ripple of the PIXELVDD supply is lower than pixel noise.

To avoid noise coupling from the MIXH supply the DMIX[0] and DMIX[1] signals should be in '00' state during the falling edge of the CORE_RESET and SHUTTER signals and also during the pixel array readout. To avoid noise coupling from ARRAYBIAS or PIXELBIAS pins, these pins should not be left floating (see Section 5).

It is recommended to short all the grounds of MLX75023 to the ground plane and use this ground potential as the ground reference for the analog to digital conversion.

To reduce common mode noise coupling to the analog sensor output pairs (OUT0, OUT3), (OUT1, OUT2), it is recommended to layout the output pair traces like for a differential signal. In this way, any common mode noise coupling to the traces can be cancelled afterwards in the digital domain.

9. Package

9.1. Mechanical Dimensions & Cover Tape Specifications

To avoid dust accumulation, scratches or other sources of damage during component storage, logistics or the assembly process(es) we offer product variants that include a plastic cover tape to protect the sensitive area of the sensor. See section 2 for more detailed ordering information.

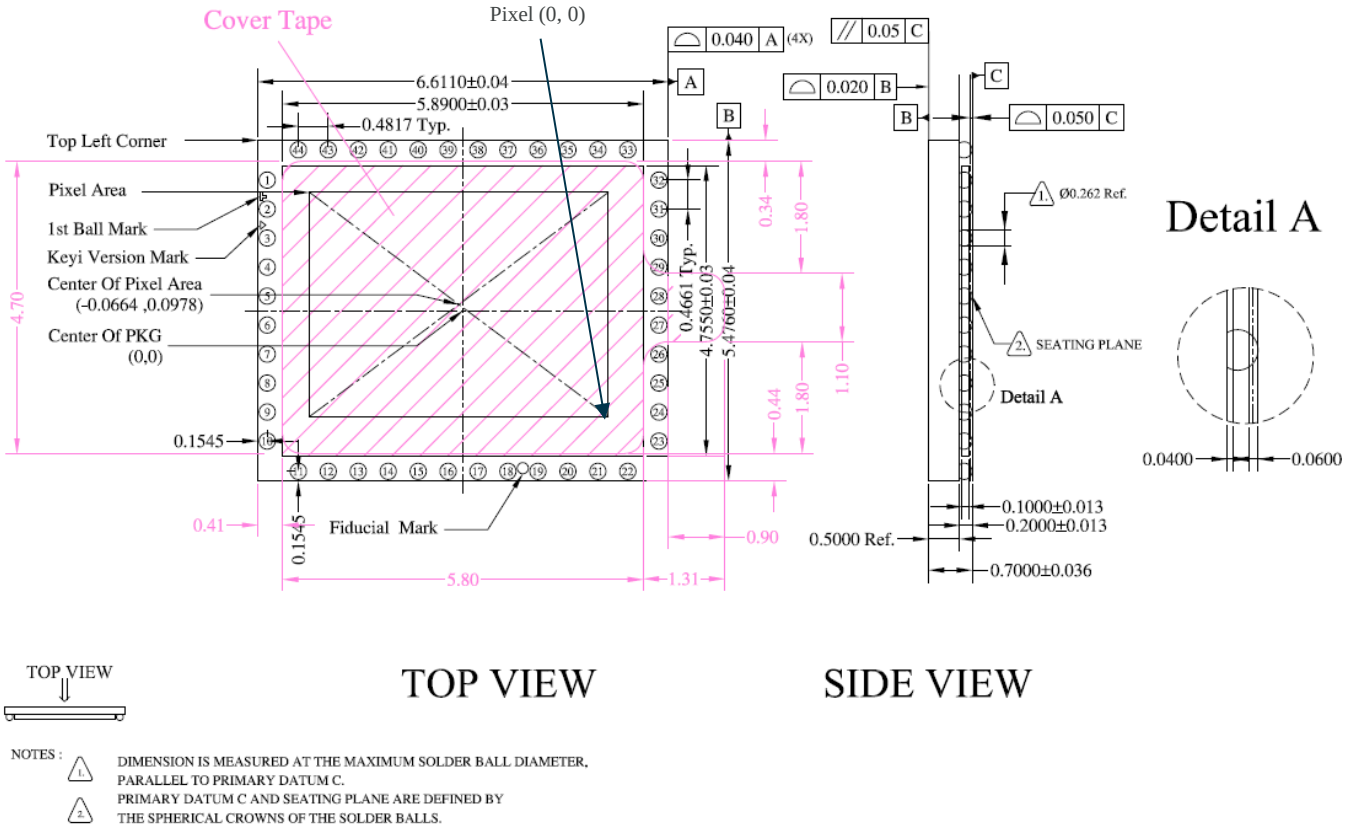

Figure 12: Mechanical & cover tape dimensions

9.2. Package Marking

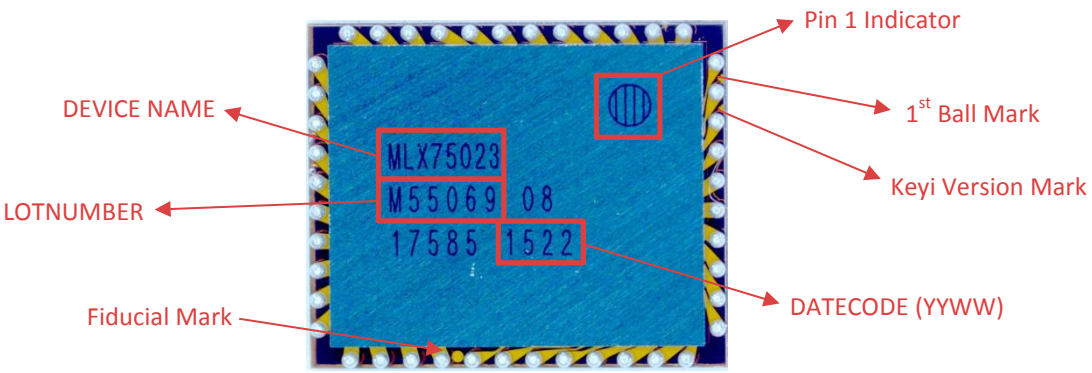

Figure 13: Contrast Enhanced Picture of Sensor Backside

9.3. Thermal Resistance

The package has an ambient-to-silicon thermal resistance of 50 K/W when the device is connected to the PCB by its solder balls (standard BGA mounting). The thermal resistance can be decreased by applying a thermal connection between the PCB and the sensor backside, e.g. by an underfill material.

Good performances can be achieved with e.g. Fischer WLPF, but also Lord ME-525 is a similar alternative.[1]
Underfill materials with an even higher thermal conductivity are also available in the market.

This process is highly recommended when operating under severe applications requirements.
It is also advised to work with a capillary underfill process. When applying underfill with a needle, specific care should be taken not to touch the sensor die with the needle, as non-repairable damage to the sensor die (e.g. die crack) may incur.

[1] Melexis cannot take any responsibility related to the use and performance of products from 3rd party suppliers.

9.4. Optical Filter

Specifications	
Glass side	Top side
T_Stop	< 0.1% average transmittance
T_Pass	>80% transmittance [800nm – 900nm]
50% transmittance cross-overs	775 nm; 925 nm
AOI	0 to 35 degrees

Table 18: Bandpass filter characteristics

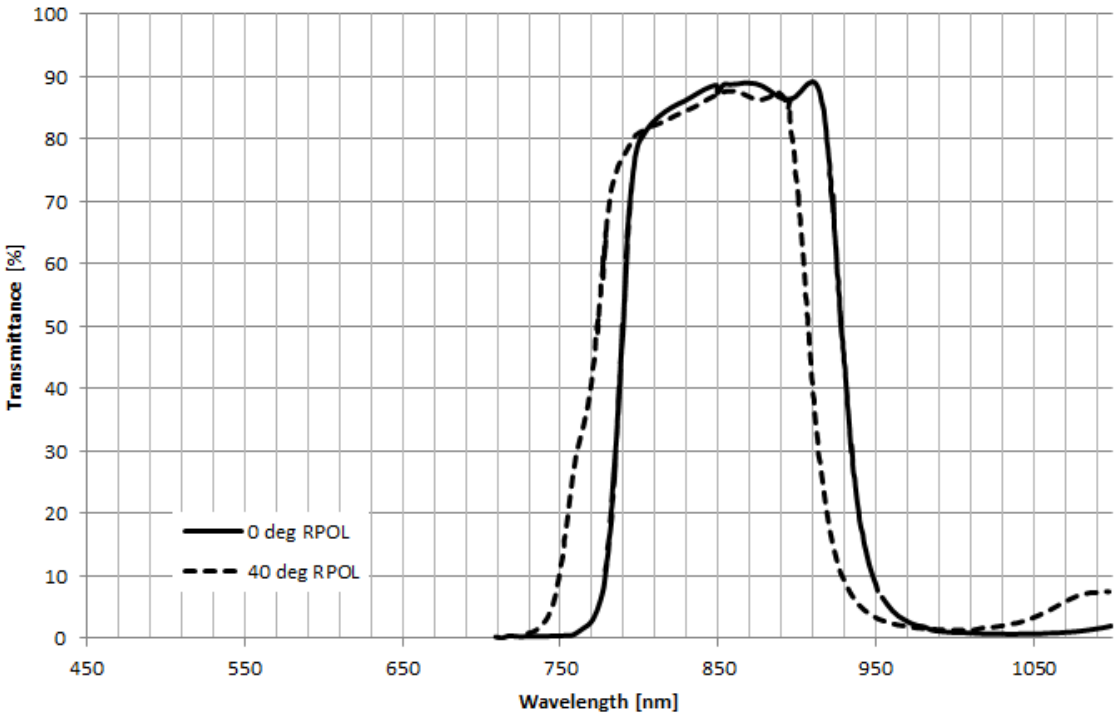

Figure 14: Bandpass filter spectral response for 0° and 40° angle of incidence (AOI)

9.5. Shipping & Handling

For proper shipment, the sensor device should be placed in a dedicated tray (see Figure 15) or a waffle pack container in case of sample quantities. The sensor device needs to be very carefully handled when being transported without the container, to avoid contamination of the glass, glass chipping, damage to the solder balls or damage to the sensor die. It is strongly recommended to avoid any manual contact and only if necessary, manually pick and place the device with plastic tweezers, holding the sides of the glass.

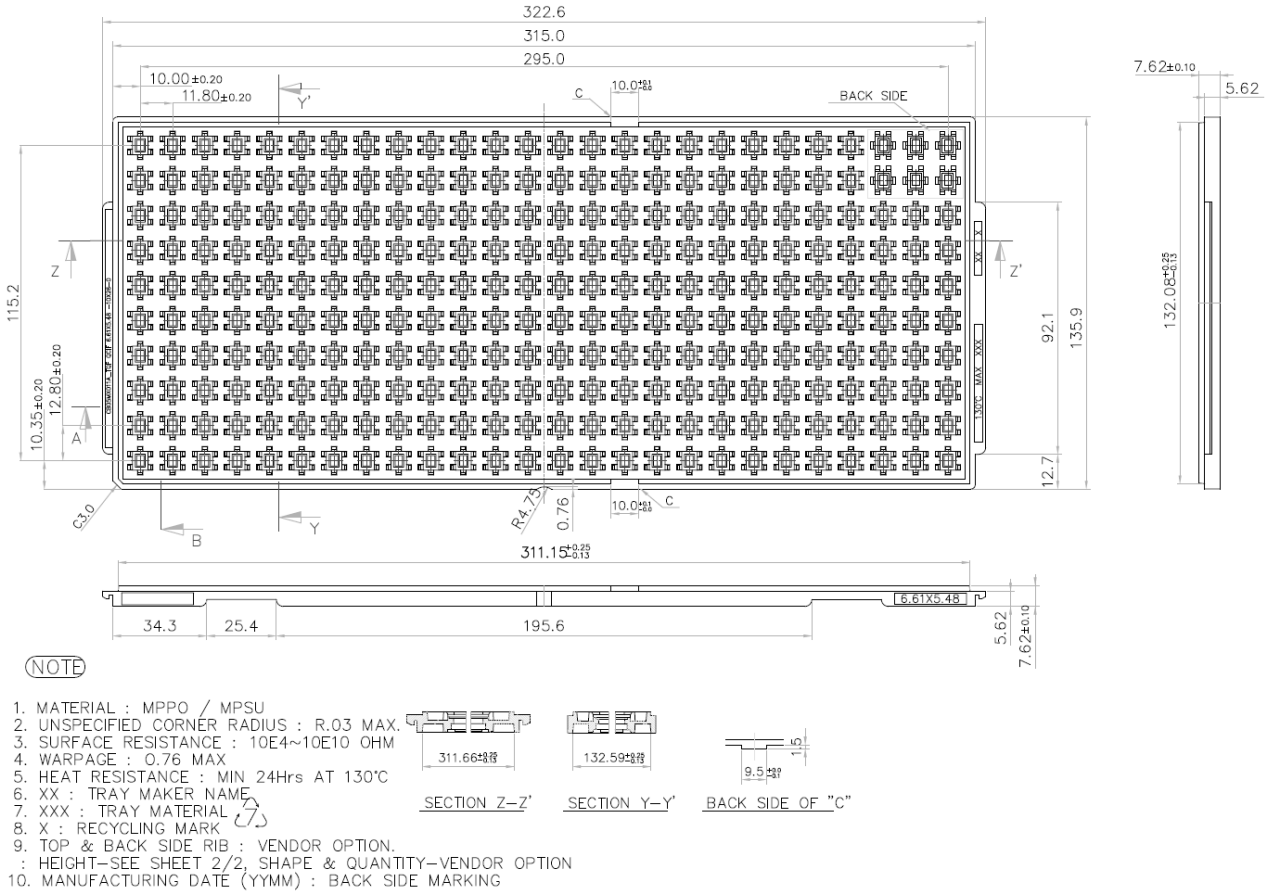

Figure 15: Production tray drawing (dimensions in mm)

9.6. PCB Footprint Recommendation

It's recommended to use NSMD (Non Solder Mask Defined) type of pads on the PCB. In order to prevent touching of the solder balls to the sensor after reflow, it's also recommended to shift the solder ball pads 50 um outward from the package position, as illustrated in Figure 16 and Figure 17.

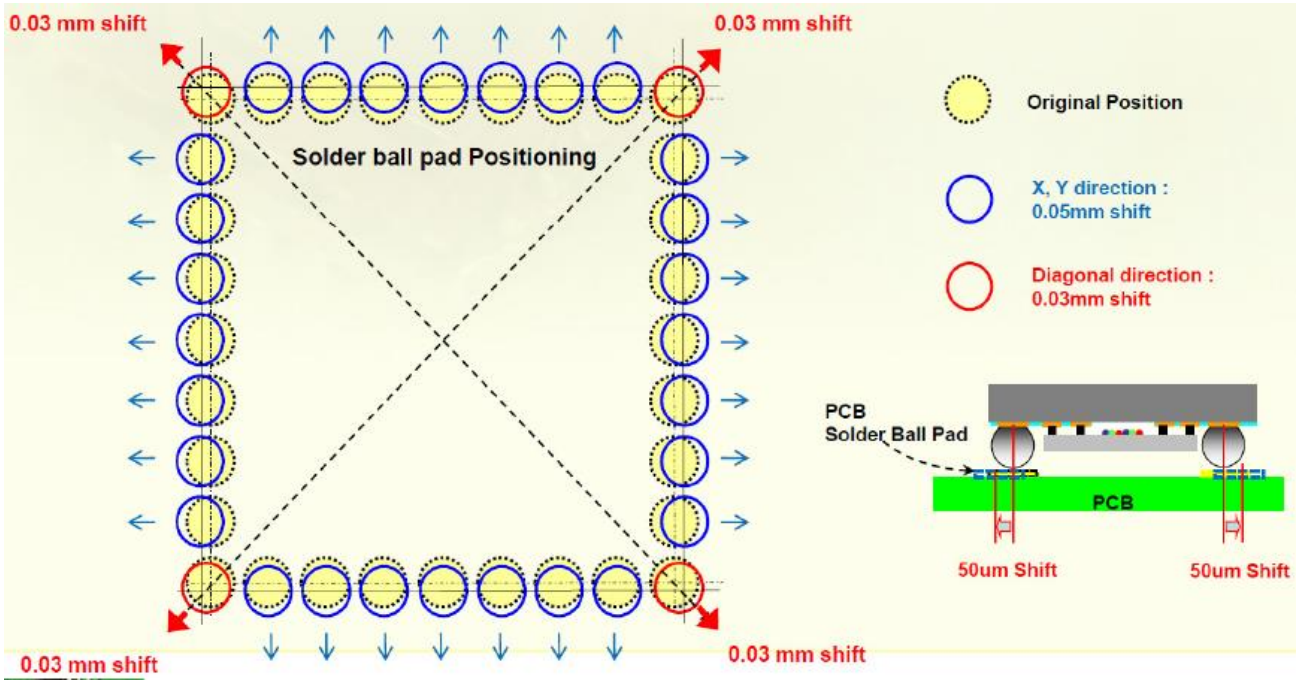

Figure 16: Recommended solder ball pad shift

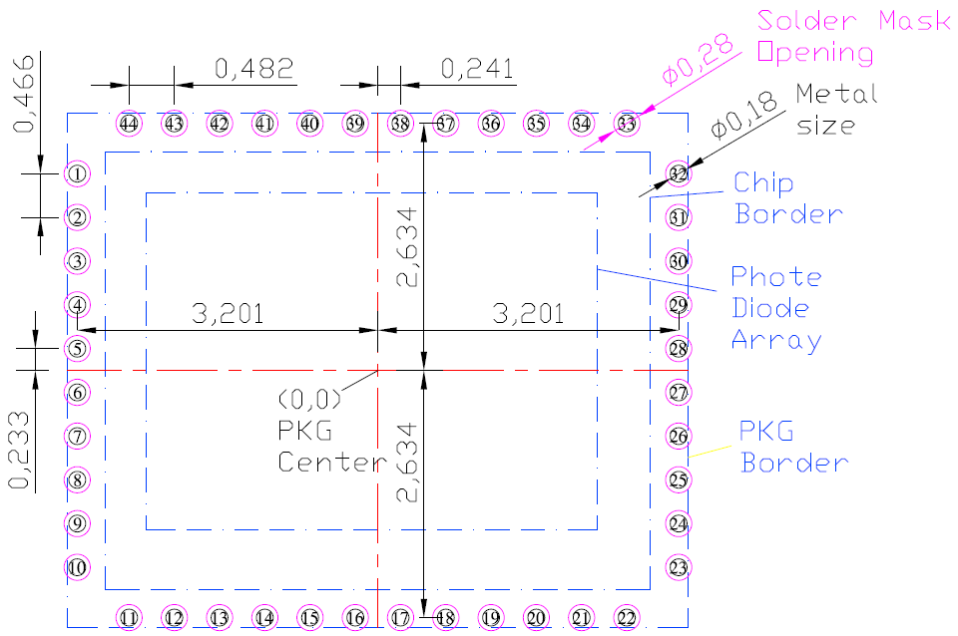

Figure 17: Recommended PCB land pattern (dimenions in mm)

9.7. PCB Trace Layout Recommendation

It is mandatory to route the traces connected to the solder balls outside of the solder ball perimeter (see Figure 18, left). In case that traces should be routed inside of the solder ball perimeter, the trace angle should be greater than 45 deg (see Figure 18, right). It is recommended to use NSMD (none solder mask defined) type of pads.

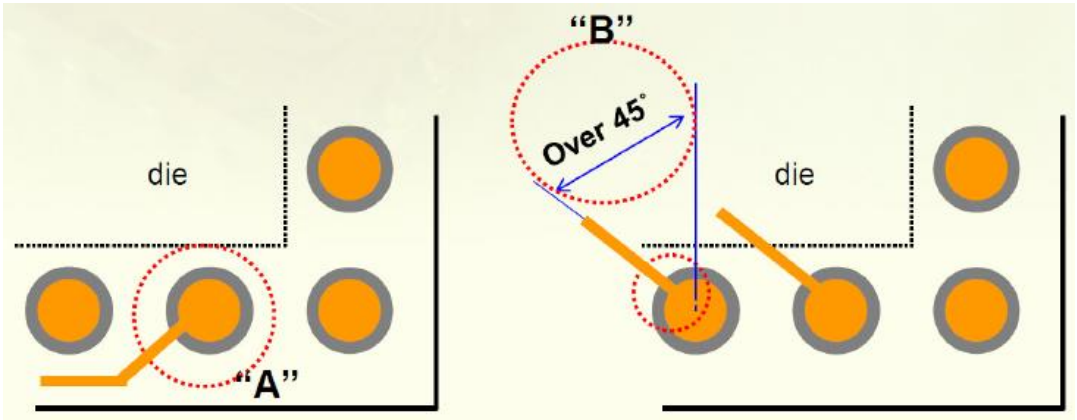

Figure 18: Recommended trace layout

9.8. Sensor Reflow Profile

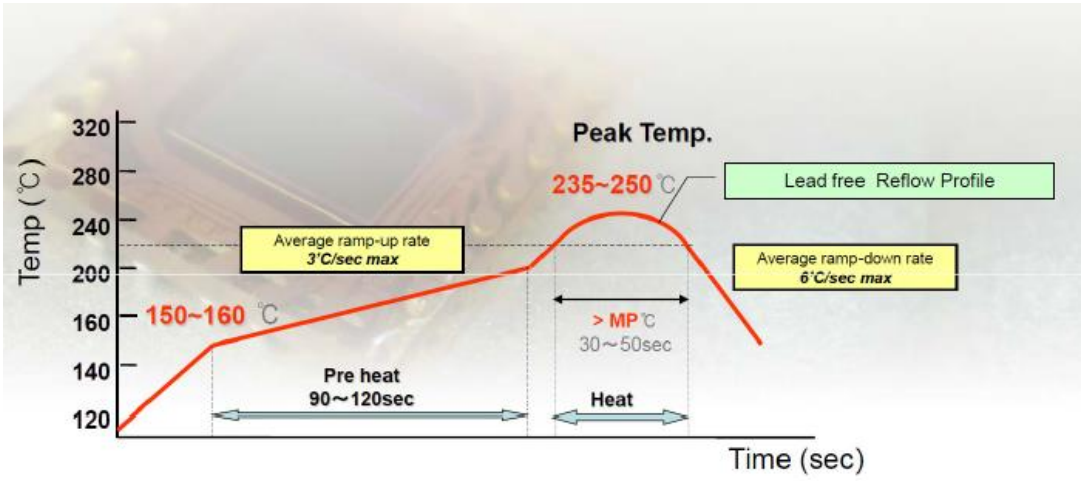

Figure 19: Recommended reflow profile

10. Depth & Confidence Calculation

10.1. Correlation Measurement

A depth and confidence measurement can be realized by a sequence of 4 correlation measurements, followed by a digital processing step. In one implementation, a single correlation measurement is realized by synchronous demodulation of the light signal of the active illumination source: during the integration time T_{int}, the active illumination source should be turned on while the TOF pixel responsivity and the light signal are amplitude modulated at a frequency f_{MIX}. Between the illumination source and the TOF pixel modulation signal, a fixed phase delay $\phi \in \{0, 180, 90, 270\}$ degrees should be applied per correlation measurement. After each integration time, the light source should be switched off to cool down for a time $T_{cooldown}$. During this cool down time, there is a time T_{read} to read out the TOF pixel correlation values S_ϕ. In an N-tap TOF pixel design, multiple correlations $S_{k,\phi}$, where $k \in 1..N$ can be measured in parallel.

Figure 20 shows the sequence of 4 correlation measurements and the synchronization between the pixel and active illumination timings.

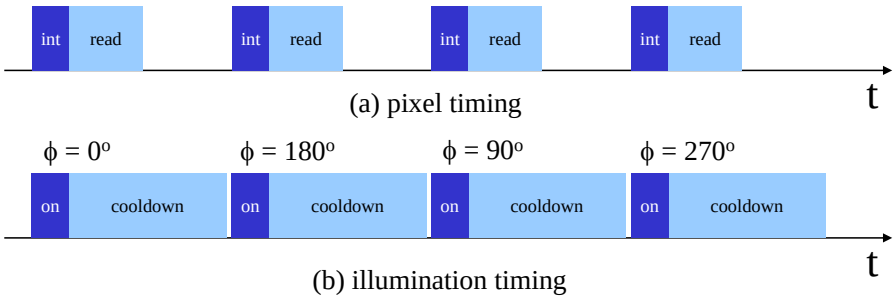

Figure 20: Pixel and illumination timing sequence(s)

The MLX75023 features a two-tap TOF pixel design. One tap measures the in-phase correlation, while the other tap measures the counter phase correlation. Following the described sequence, there will be 8 correlation values available per depth measurement sequence, per pixel: $S_{k,\phi}$ where $k \in \{0,1\}$ denotes the in-phase and counter phase correlation respectively, and $\phi \in \{0, 180, 90, 270\}$.

The MLX75023 features two dual-ended outputs. The dual ended output terminal pairs are (OUT0, OUT3) and (OUT1, OUT2). During readout of the sensor, each dual ended pair will output the voltages of a two-tap pixel. Each output pair can be assigned to readout one half of the pixel array as explained in Section 7.1.4. For columns 0 … 7, 16 … 23, … :

$$OUT_0 \rightarrow S_{0,\phi}$$
$$OUT_3 \rightarrow S_{1,\phi}$$

For columns 8 … 15, 24 … 33, … :

$$OUT_1 \rightarrow S_{1,\phi}$$
$$OUT_2 \rightarrow S_{0,\phi}$$

The MLX75023 features digital mix input terminals DMIX0 (pin 35) and DMIX1 (pin 34). During the integration time T_{int}, the modulation reference signal should be applied differentially to these terminals. During the remainder of the time, the timing requirements as detailed in Section 7.1 should be followed.

10.2. Active Illumination

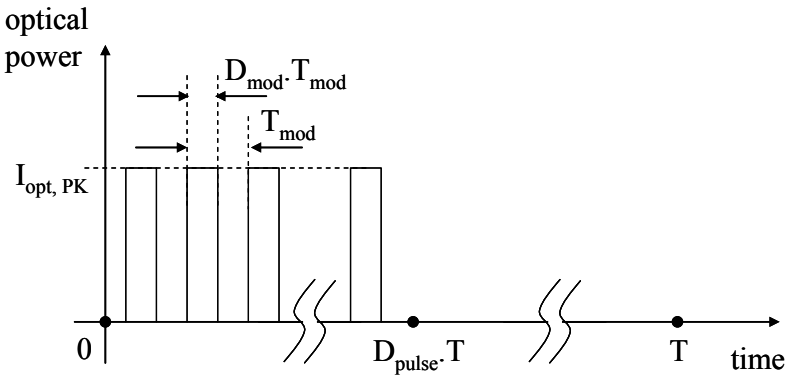

Figure 21: Active illumination waveform

A typical active illumination waveform is shown in Figure 21. The waveform consists of two parts: during the first, a pulse train of active illumination is emitted and during the second, no active light is emitted. During this time, the active light source can cool down and the pixel values can be read out.

The symbols in the graph have the following meaning:

- T is the time between consecutive measurements
- D_{pulse} is the ratio between the time that active pulses should be emitted and the total time of the measurement
- T_{mod} is the duration of each active pulse
- D_{mod} is the ratio between the duration of an active pulse and the time between consecutive pulses
- $I_{opt,PK}$ is the peak optical power or intensity level of the active pulse

The average optical power or intensity $I_{opt,AVG}$ can be calculated as

$$I_{opt,AVG} = I_{opt,PK} * D_{mod} * D_{pulse}$$

The average duty cycle $D_{mod} * D_{pulse}$ should be chosen such that the active illumination can operate reliably i.e. does not exceed its critical temperature, while aiming for maximum peak power $I_{opt,PK}$ to achieve the best measurement SNR in high ambient light conditions.

Referring to Section 10.1, we note that:

- the integration time T_{int} equals $D_{pulse} * T$
- the cool down time $T_{cooldown}$ equals $(1 - D_{pulse}) * T$
- the modulation frequency f_{MIX} equals $1/T_{mod}$
- the modulation duty cycle D_{mod} equals 50% in case of square wave or sine modulation

10.3. Depth and Confidence Calculation

The depth data per pixel in degrees can be calculated by following formula

$$\phi = \begin{cases} 90 * (1 - x) & \text{if } y < 0 \\ 90 * (3 + x) & \text{if } y \geq 0 \end{cases}$$

Where x, y are average quadrature values calculated as

$$x = \frac{X_0}{2N_0} - \frac{X_1}{2N_1}$$
$$y = \frac{Y_0}{2N_0} - \frac{Y_1}{2N_1}$$

Where X_0, Y_0, N_0 and X_1, Y_1, N_1 are the quadrature and norm values measured by the first and second pixel tap, respectively. They can be calculated from the correlation values by following formula:

$$X_k = S_{k,0} - S_{k,180}$$
$$Y_k = S_{k,270} - S_{k,90}$$
$$N_k = |X_k| + |Y_k|$$

Where $k \in \{0,1\}$ is the pixel tap index. A good measure of the depth value confidence is the total norm $N_0 + N_1$.

11. Reliability

MLX75023RTF is qualified according to AEC-Q-100-002 (-40 - 105°C) and following ESD classification:

- ESD HBM - Class H1C acc. to AEC - Q100-002-Rev.D
- ESD CDM - Class C4A acc. to AEC - Q100-011-Rev.C1

11.1. Board Level Reliability

In order to meet the board level reliability requirements it is highly recommended to use low CTE (coefficient of thermal expansion) PCB substrate material, like FR-5, in combination with an underfill material (like explained in section 9.3) to match the CTE of the glass package (3.8 ppm/K).

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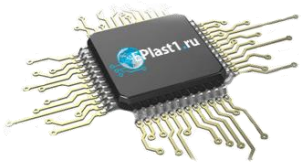

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